MH88625
DID/OPS SLIC
Preliminary Information

DS5167 ISSUE 7 August 1999

Ordering Information

MH88625 40 Pin SIL Package

0°C to 70°C

Features

- Programmable gain, network balance and impedance
- Transformerless 2-4wire conversion
- Constant current with constant voltage fallback for long loop capability
- Pin compatible with MH88632 and MH88628.
- Unbalance detection (Tip, Ring ground sensing)
- Auto ring trip
- On-Hook transmission (ANI) capability
- Compatible with requirements of CCITT, DOC/ FCC and CSA/ULs
- Excellent power dissipation (SIL vertical mounting)
- 12/16kHz meter pulse injection control
- Solid State TIP/RING reversals

Applications

- On/Off Premise PBX Line Cards
- DID (Direct Inward Dial) Line Cards
- Central Office Line Cards

Description

The Zarlink MH88625 SLIC provides all of the functions required to interface 2-wire off premise subscriber loops to a serial TDM, PCM, switching network of a modern PBX. The MH88625 is manufactured using thick-film hybrid technology which offers high voltage capability, reliability and high density resulting in significant printed circuit board area savings. A complete line card can be implemented with very few external components.

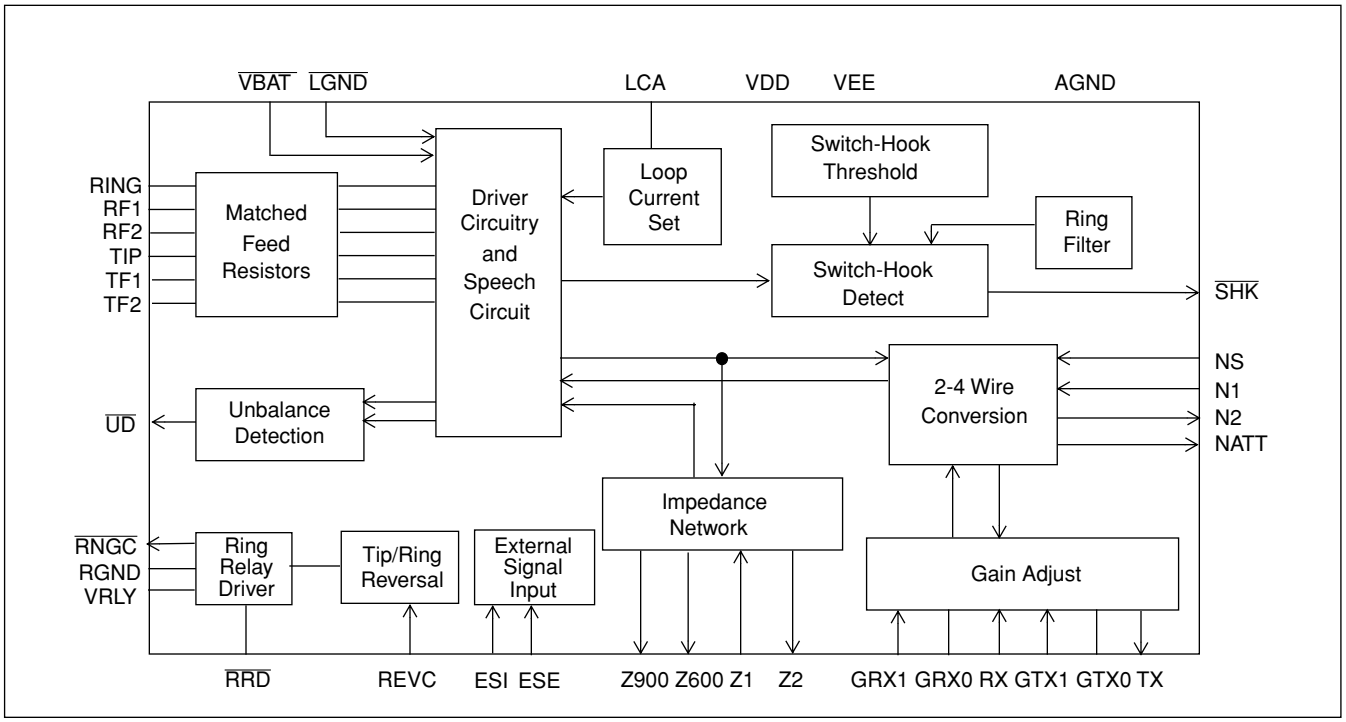


Figure 1 - Functional Block Diagram

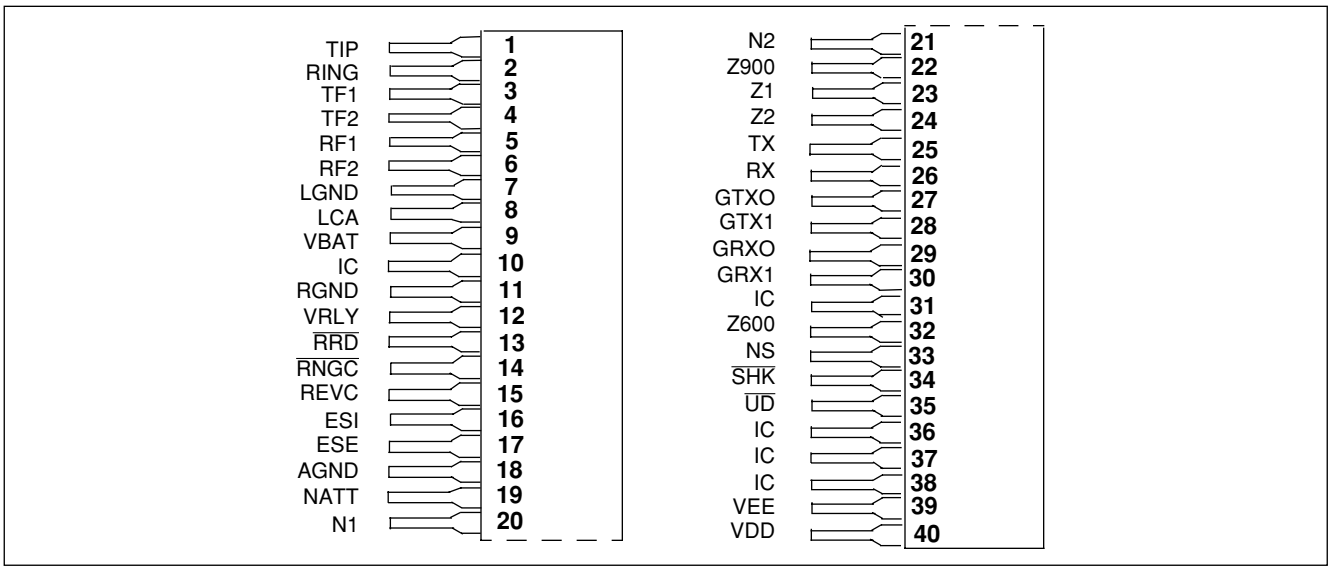


Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	TIP	**Tip Lead.** Connects to the “Tip” lead of subscriber line.
2	RING	**Ring Lead**. Connects to the "Ring" lead of the subscriber line.
3	TF1	**Tip Feed 1.** Access point for balanced ringing. Normally connects to TF2.
4	TF2	**Tip Feed 2.** Access point for balanced ringing. Normally connects to TF1.
5	RF1	**Ring Feed 1.** Access point for balanced ringing. Normally connects to RF2.
6	$\overline{RF2}$	**Ring Feed 2.** Access point for balanced ringing. Normally connects to RF1.
7	$\overline{LGND}$	**Battery Ground**. V_{BAT} return path. Connected to system’s energy dumping ground.
8	LCA	**Current Limit Set (Input).** The current limit is set by connecting an external resistor to ground. For 30mA default current, this pin is tied to GND
9	VBAT	**Battery Voltage**. Typically -48Vdc is applied to this pin.
10	IC	**Internal Connection**. This pin is internally connected and must be left open.
11	RGND	**Relay Driver Ground Connection.**
12	VRLY	**Relay Supply Voltage Connection**.
13	$\overline{RRD}$	**Ring Relay Drive (Output).** Connects to ring relay coil.
14	$\overline{RNGC}$	**Ring Relay control (Input).** A logic low enables the Ring Relay Drive ($\overline{RRD}$) output which activates the Ring Relay. The internal auto ring trip circuitry de-activates the relay drive output upon detection of switch-hook.
15	REVC	**Reversal Control (Input).** A logic high reverse the internal Tip and Ring connections.
16	ESI	**External Signal Input.** 12/16kHz meter pulse input.
17	ESE	**External Signal Enable.** 12/16kHz meter pulse enable.
18	AGND	**Analog Ground.** V_{DD} and V_{EE} return path.
19	NATT	**Network Balance AT+T Node.** Connects to N1 for a network balance impedance of AT&T compromise (350Ω + 1kΩ // 210nF); the device’s input impedance must be set to 600Ω. This node is active only when NS is at logic high. This node should be left open circuit when not used.

Pin Description (continued)

Pin #	Name	Description
20	N1	**Network Balance Node 1 (Input).** 0.1 times the impedance between pins N1 and N2 must match the device's input impedance, while 0.1 times the impedance between pins N1 and AGND is the device's network balance impedance. This node is active only when NS is at logic high. This node may be terminated when not used (i.e., NS at logic low).
21	N2	**Network Balance Node 2 (Output).** See N1 for description.
22	Z900	**Line Impedance 900Ω Node.** Connects to Z1 for a line impedance of 900Ω. This node should be left open circuit when not used.
23	Z1	**Line Impedance Node 1 (Input)**. 0.1 times the times the impedance between pins Z1 and Z2 is the device's line impedance. This node must always be connected.
24	Z2	**Line Impedance Node 2 (Output).** 0.1 times the times the impedance between pins Z1 and Z2 is the device's line impedance. This node should be left open circuit when not used.
25	TX	**Transmit (output)**. 4-Wire (AGND) referenced audio output.
26	RX	**Receive (Input)**. 4-Wire (AGND) referenced audio input.
27	GTXO	**Transmit Gain Node 0**. Connects to GTX1 for 0dB transmit gain.
28	GTX1	**Transmit Gain Node 1**. Connects to a resistor to AGND for transmit gain adjustment.
29	GRXO	**Receive Gain Node 0.** Connects to GRX1 for 0dB gain.
30	GRX1	**Receive Gain Node 1.** Connects to a resistor to AGND to receive gain adjustment.
31	IC	**Internal Connection.** This pin is internally connected and must be left open.
32	Z600	**Line Impedance 600Ω Node (Output).** Connects to Z1 for a line impedance of 600Ω. This pin should be left open circuit when not used.
33	NS	**Network Balance Setting (Input.** The logic level at NS selects the network balance impedance. A logic 0 enables an internal balance equivalent to the input impedance (Zin). While a logic 1 enables an external balance 0.1 times the impedance between pins N1 and AGND balanced to 0.1 times the impedance between pins N1 and N2. The impedance between N1 and N2 must be equivalent to 10 times the input impedance (Zin).
34	$\overline{\text{SHK}}$	**Off-Hook Indication (Output).** A logic low output indicates when the subscriber equipment has gone Off-Hook.
35	$\overline{\text{UD}}$	**Unbalance Detect (Output).** A log IC low output indicates when the DC current flow in the Tip and Ring leads is unbalanced, indicating that the subscriber equipment has grounded the Ring lead.
36,37 38	IC	**Internal Connection.** These pins are internally connected and must be left open
39	V_{EE}	**Negative Supply Voltage.** -5V dc.
40	V_{DD}	**Positive Supply Voltage.** +5V dc.

Functional Description

The SLIC uses a transformerless electronic 2-wire to 4-wire conversion which can be connected to a Codec to interface the 2 wire subscriber loops to a time division multiplexed (TDM) pulse code modulated (PCM) digital switching network. For analog applications, the Tx and Rx of the 2-4 wire converter can be connected directly to an analog crosspoint switch such as the MT8816. Powering of the line is provided through precision battery feed resistors. The MH88625 also contains control, signalling and status circuitry which combines to provide a complete functional solution which simplifies the manufacture of line cards. This circuitry is illustrated in the functional block diagram in Figure 1. The MH88625 is designed to be pin compatible with Zarlink's MH88632 and MH88628. This allows a common PCB design with common gain, input impedance and network balance.

Approvals

FCC part 68, CCITT, DOC CS-03, UL 1950, IEC950, CAN/CSA 22.2 No.225-M90 and ANSI/EIA/TIA-464-A are system level safety standards and performance requirements. As a component of a system, the MH88625 is designed to comply with the applicable requirements of these specifications

Battery Feed

The loop current for the subscriber equipment is sourced through a pair of matched 200Ω resistors connected to the Tip and Ring. The two wire loop is biased such that the Ring lead is 2V above VBat (typically -46V) and the Tip lead is 2V below LPGD (typically -2V) during constant voltage, constant current mode.

The SLIC is designed for a nominal battery voltage of -48Vdc and can provide the maximum loop current of 45mA under the condition.

The MH88625 is designed to operate down to a minimum of 16mA DC, with a battery voltage of -44V. The Tip and Ring output drivers can operate within 2V of VBat and LGND rails. This permits a maximum loop range of 2300Ω

Loop Current Setting

The MH88625 SLIC provides a constant current with constant voltage fallback. This design feature provides for long loop capability regardless of the constant current setting. Refer to Graph 1.

The LCA (Loop Current Adjust) pin is an input to an internal resistor divider network which generates a bias voltage. The loop current is proportional to this voltage. The loop current can be set between 20 and 45mA by various connections to the LCA pin as illustrated in Graph 2 and Figure 8. The loop current during a fault condition will be limited to a safe level. Primary over-current protection is inherent in the current limiting feature of the 200Ω battery feed resistors. Refer to Graph 1.

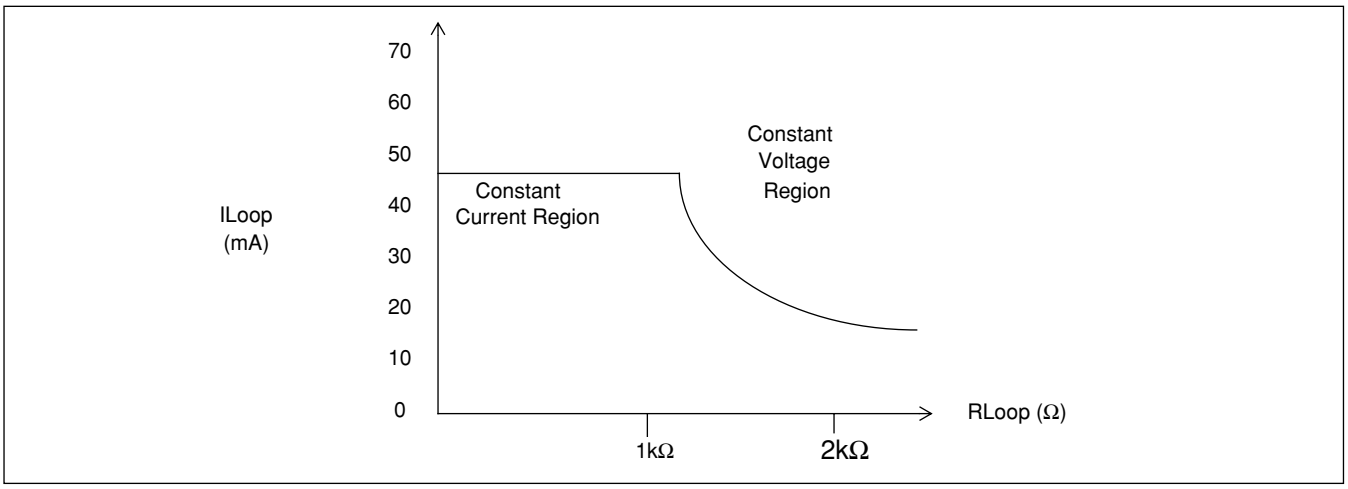
Receive and Transmit Audio Path

The audio signal of the 2-wire side is sensed differentially across the external 200Ω feed resistors and is passed on to a second differential amplifier stage in the 2W/4W conversion block. This block sets the transmit gain on the 4-wire side and cancels signals originating from the receive input before outputting the signal.

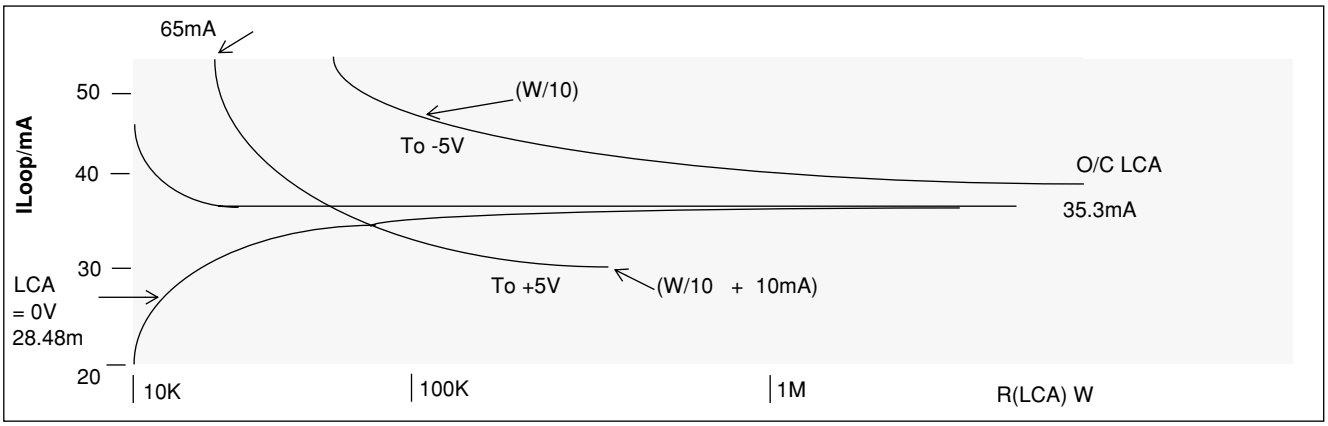
Programmable Transmit and Receive Gain

Transmit Gain (Tip-Ring to Tx) and Receive Gain (Rx to Tip-Ring) are programmed by connecting external resistors (RRX and RRT) from GRXI to AGND and from GTX1 to AGND as indicated in Figure 3 and Tables 1 and 2. The programmable gain range is from -12dB to +6dB; this wide range will accommodate almost any loss plan. Alternatively, the default Receive Gain of 0dB and Transmit Gain of 0dB can be obtained by connecting GRX0 to GRX1 and GTX0 to GTX1. In addition, a Receive gain of +6dB and Transmit Gain of +6dB can be obtained by not connecting resistors RRX and RTX. For correct gain programming, the MH88625's Tip-Ring impedance (Zin) must match the line termination impedance.

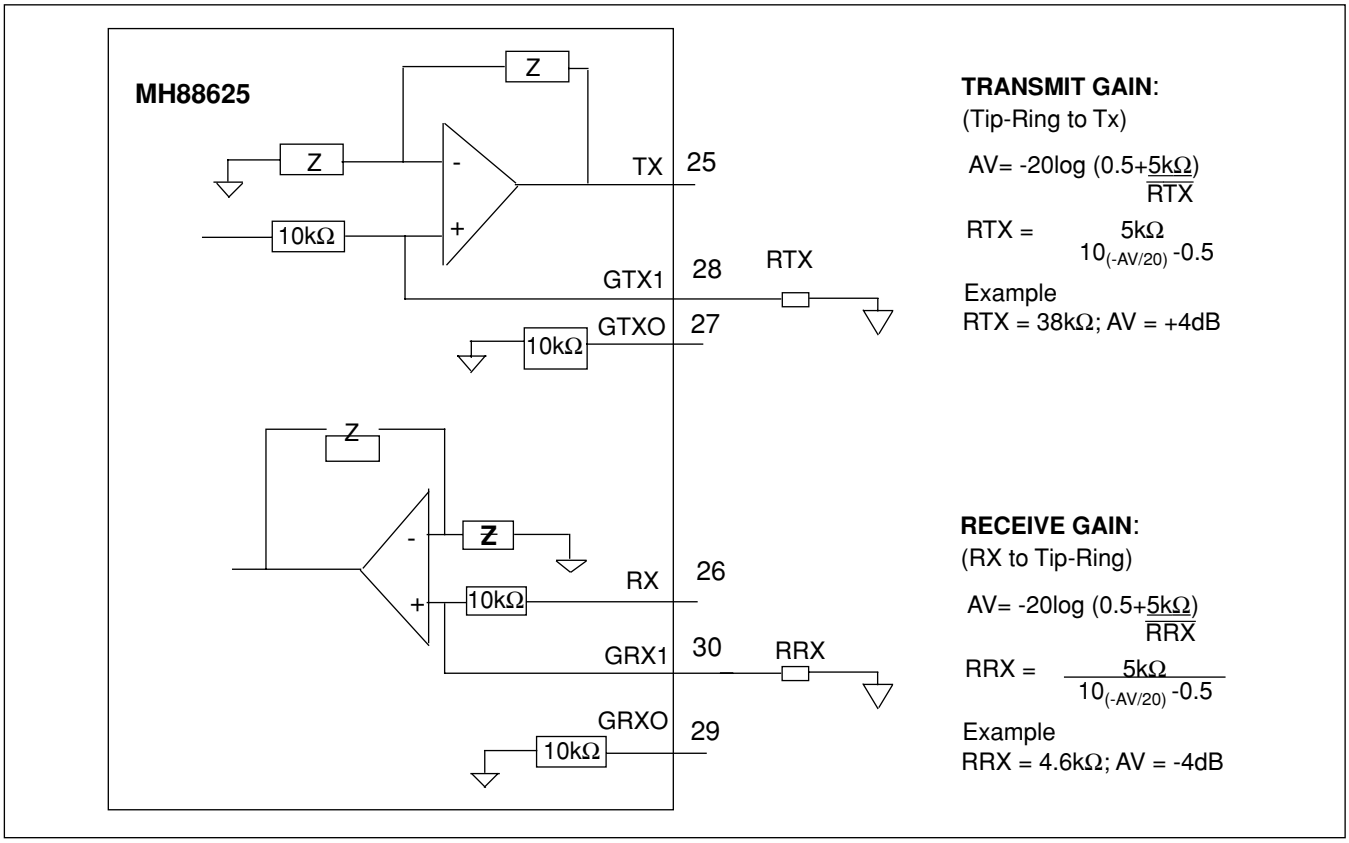
For optimum performance, resistor RRX should be physically located as close as possible to the GRX1 input pin, and resistor RTX should be physically located as close as possible to the GTX1 input pin.



Graph 1 - Iloop/Rloop Characteristics



Graph 2 - Loop Current Setting



TRANSMIT GAIN:
(Tip-Ring to Tx)

$$AV = -20\log\left(0.5+\frac{5k\Omega}{RTX}\right)$$

$$RTX = \frac{5k\Omega}{10_{(-AV/20)} - 0.5}$$

Example
RTX = 38kΩ; AV = +4dB

RECEIVE GAIN:
(RX to Tip-Ring)

$$AV = -20\log\left(0.5+\frac{5k\Omega}{RRX}\right)$$

$$RRX = \frac{5k\Omega}{10_{(-AV/20)} - 0.5}$$

Example
RRX = 4.6kΩ; AV = -4dB

Figure 3 - Gain Programming with External Components

Two wire Port Termination Impedance

The AC termination impedance of 600 or 900Ω, of the 2W port, is set using active feedback paths to give the desired relationship between the line voltage and the line current. The loop current is sensed differentially across the two feed resistors and converted to a single ended signal. This signal is fed back to the Tip/Ring driver circuitry such that impedance in the feedback path gets reflected to the two wire port. The MH88625's Tip-Ring impedance (Zin) can be set to 600Ω, 900Ω or to a user selectable value. Thus, Zin can be set to any international requirement. The connection to Z1 determines the input impedance. With Z1 connected to Z600, the line impedance is set to 600Ω. With Z1 connected to Z900, the line impedance is set to 900Ω. A user defined impedance can be selected which is 0.1 times the impedance between Z1 and Z2. For example, with 2200Ω in series with 11.5nF in parallel with 8200Ω, all between Z1 and Z2, the devices line impedance will be 220Ω in series with 115nF in parallel with 820Ω. See Table 3 and Figures 4 and 5.

Network Balance

Transhybrid loss is maximized when the line termination impedance and SLIC network balance are matched. The MH88625's network balance impedance set can be set to Zin, AT&T (350Ω + 1kΩ //210nF) or to a user selectable value. Thus, the network balance impedance can be set to any international requirement, A logic level control input NS selects the balance mode. With NS at logic low, an internal network balance impedance is matched to the line impedance (Zin). With NS at logic high, a user defined network balance impedance is selected which is 0.1 times the impedance between N1 and AGND. For example, with 2200Ω in series with 11.5nF in parallel with 8200Ω, all between N1 and AGND, and NS at logic high, the devices network balance impedance is 220Ω in series with 115nF in parallel with 820Ω; the impedance between N1 and N2 must be equivalent to 10 times the input impedance (Zin). In addition, with NS at logic high, an AT&T network balance impedance can be selected by connecting NATT to N1; in this case, no additional network is required between N1 and N2. See Table 4 and Figure 6.

12/16kHz Meter Pulse

The MH88625 provides control of an external signal path to the driver. A 12/16kHz continuous signal can be applied to the ESI pin. Control of the ESE input allows the metering signal to be transmitted to the line.

Unbalanced Detection

The Unbalanced Detect ($\overline{UD}$) pin goes low when the DC current through the two battery feed resistors is unbalanced eg., when the average DC current into the Ring lead exceeds the current flow out of the Tip lead (indicating that the Ring lead has been grounded).

When the SLIC is interfaced to ground start subscriber equipment during the idle state, the $\overline{UD}$ output is monitored for indication of the subscribers Ring Ground signal. The maximum loop current supplied by the feed circuitry under this condition is limited.

Longitudinal Balance

The longitudinal balance specifies the degree of common mode rejection in the 2 to 4 wire direction. Precision laser trimming of internal resistors in the hybrid ensures good overall longitudinal balance.

The interface circuitry can operate in the presence of induced longitudinal currents of up to 40mA at 60Hz.

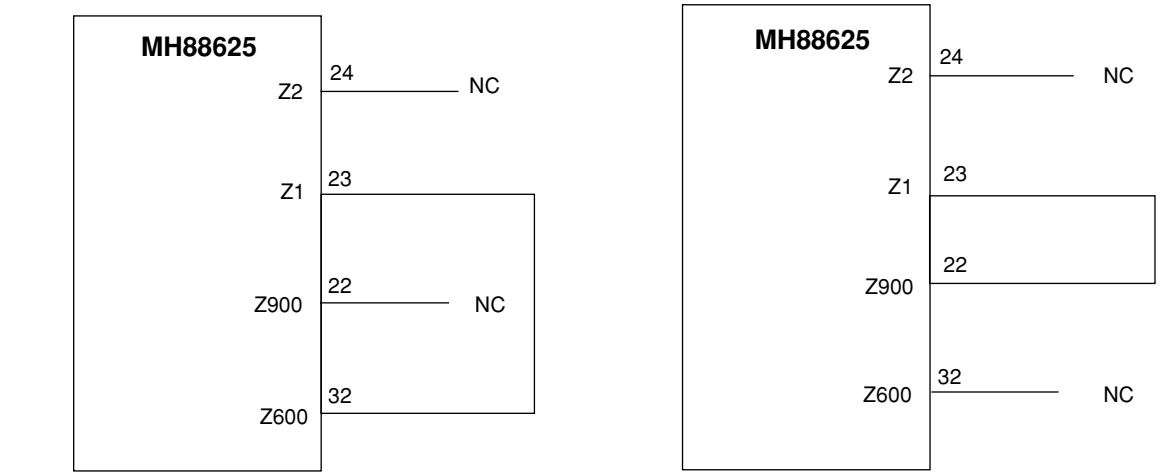
Off-Hook and Dial Pulse Detection

The $\overline{SHK}$ pin goes low when the DC-loop current exceeds a specified level. The threshold level is internally set by the bias voltage of the switch-hook detect circuitry.

Dial pulse can be detected by monitoring the interruption rate at the $\overline{SHK}$ pin. These dial pulseswould be debounced by the system's software.

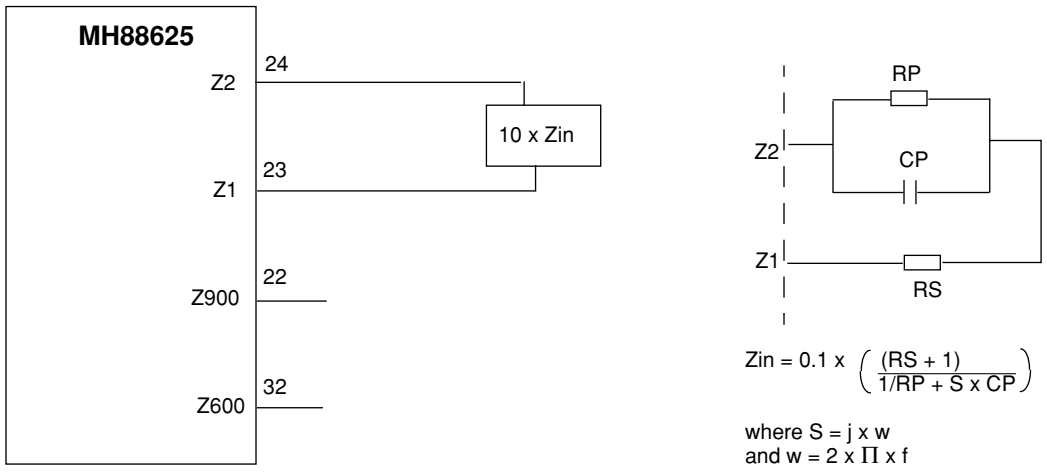
Ring Trip Detection

The interface permits detection of an Off-Hook condition during the ringing. If the subscriber set goes Off-Hook when the ringing signal has been applied, the DC loop current flow will be detected within approximately 100msecs and the $\overline{SHK}$ output will go low. The ring relay is automatically disabled by the internal hardware.



Note: Make connection between Z1 and other points as short as possible

Figure 4 - Input Impedance (Zin) Settings with Zin equal to 600 or 900Ω

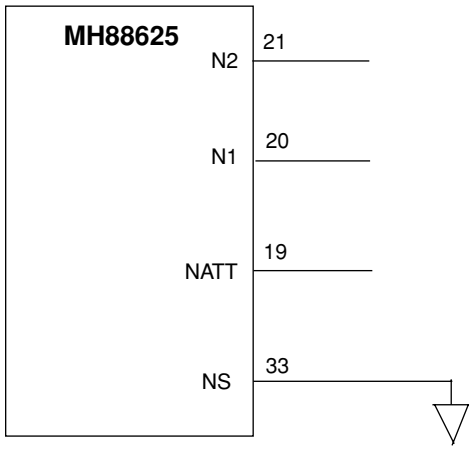


Notes:
1) The 10xZin network must be set to 10 x the desired input impedance (Zin).
2) The network balance must be set to the desired network balance. See section on network balance.
3) Make connection between Z1 and component as short as possible.

Example:

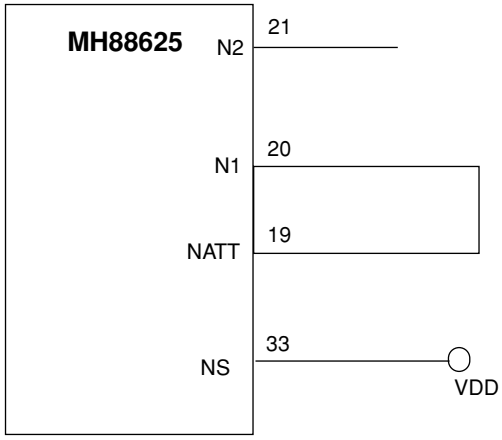
If RS = 2200Ω, RP = 8200Ω, CP= 11.5nF
Then the input impedance (Zin) is 220Ω in series with 820Ω in parallel with 115nF.

Figure 5 - Input Impedance (Zin) Settings with Zin <u>not</u> equal to 600 to 900Ω



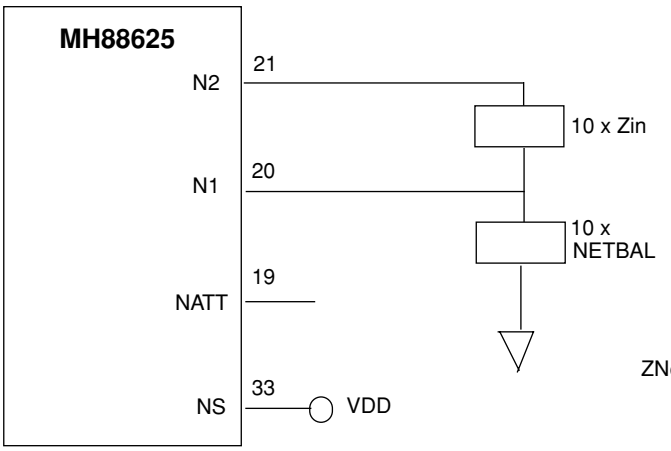
Network balance is set to the input Impedance (Zin)

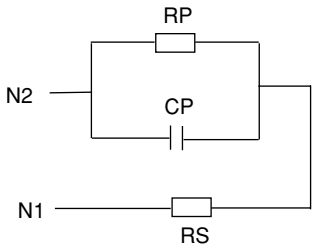
Note: Make connection between Z1 and other points as short as possible



Network balance is set to the AT&T compromise network (350Ω + 1000Ω // 210nF) impedance. The input impedance must be set to 600W.

Figure 6 - Network Balance Setting with NETBAL equal to Zin or AT&T





$$ZNetbal = 0.1 \times \left(\frac{(RS + 1)}{1/RP + S \times CP} \right)$$

where S = j x w
and w = 2 x Π x f

Notes:

1) The 10xZin network must be set to 10 x the desired input impedance (Zin).
2) The network balance must be set to the desired network balance. See section on network balance.
3) Make connection between Z1 and component as short as possible.

Example:

If RS = 2200Ω, RP = 8200Ω, CP= 11.5nF
Then the input impedance (ZNetbal) is 220Ω in series with 820Ω in parallel with 115nF.

Figure 7 - Network Balance Setting with NETBAL <u>not</u> equal to ZNetbal or AT&T

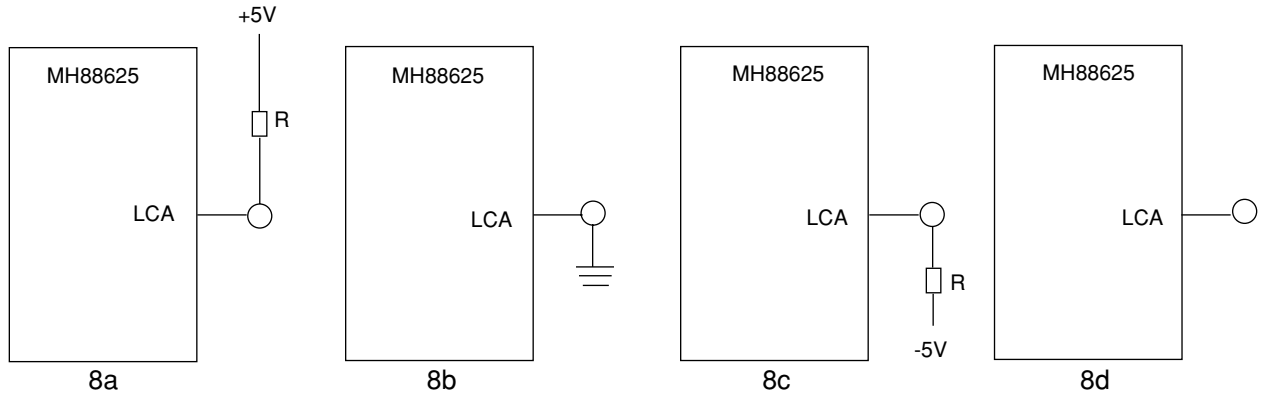


Figure 8 - Loop Current Setting (See Graph 2)

Transmit Gain (dB)	RTX Resistor Value (Ω)	Notes
+6.0	No Resistor	
+4.0	38.3k	Results in 0dB overall gain when used with Zarlink A-law codec (i.e. MT8965)
+3.7	32.4k	Results in 0dB overall gain when used with Zarlink μ-law codec (i.e. MT8964)
0.0	GTX0 to GTX1	
-3.0	5.49k	
-6.0	3.32k	
-12.0	1.43k	

Table 1 - Transmit Gain Programming

Note 1: See Figures 3 and 4 for additional details.
Note 2: Overall gain refers to the receive path of PCM to 2-wire, and transmit path of 2-wire to PCM.

Receive Gain (dB)	RRX Resistor Value (Ω)	Notes
+6.0	No Resistor	
0.0	GRX0 to GRX1	
-3.0	5.49k	
-3.7	4.87k	Results in 0dB overall gain when used with Zarlink A-law codec (i.e. MT8965)
-4.0	4.64k	Results in 0dB overall gain when used with Zarlink μ-law codec (i.e. MT8964)
-6.0	3.32k	
-12.0	1.43k	

Table 2 - Receive Gain Programming

Note 1: See Figures 3 and 4 for additional details.
Note 2: Overall gain refers to the receive path of PCM to 2-wire, and transmit path of 2-wire to PCM.

Z2	Z1	Z600	Z900	Resulting input impedance (Zin)
NA	Connect Z1 to Z600		NA	600Ω
NA	Connect Z1 to Z900	NA	Connect Z1 to Z900	900Ω
Connect network from Z1 to Z2		NA	NA	0.1 x impedance between Z1 & Z2

Table 3 - Input Impedance Settings

Note 1: NA indicates high impedance (10kΩ) connection to this pin does not effect the resulting network balance.
Note 2: See Figure 4 & 5 for Applications Circuits

NS (Input)	N2	N1	NATT	Resulting input impedance (Zin)
Low	NA	NA	NA	Equivalent to Zin
High	NA	Connect N1 to NATT		AT&T compromise (350Ω + 1kΩ // 210nF) Zin must be 600Ω
High	Connect network from N1 to AGND equivalent to 10 x NETBAL. Connect network from N1 to N2 equivalent to 10 x Zin.		NA	0.1 x impedance between N1 & N2

Table 4 - Network Balance Settings

Note 1: NA indicates high impedance (10kΩ) connection to this pin does not effect the resulting network balance.
Note 2:Low indicates Logic Low.
Note 3: See Figures 6 and 7 for Application Circuit.

DTMF

DTMF tones may be transmitted and received at the 4-wire port.

DID Operation

For DID operation, the Tip and Ring reversal is controlled by the REVC pin. A logic level one causes Tip and Ring to be reversed. This can be controlled by a Zarlink Codec (MT896X) system drive output. (refer to Figure 9b)

High Voltage capability

Inherent in the thick-film process is the ability of the substrate to handle high voltage. The standard Zarlink thick-film process provides dielectric strengths of greater than 1000VAC or 1500VDC. The thick-film process allows easy integration of surface mount components such as the high voltage bi-polar power transistor line drivers. This allows for simplier, less elaborate and less expensive protection circuitry required to handle high voltage transients and fault conditions caused by lightning, induced voltages and power line crossings.

On-Hook Transmission

The MH88625 provides for on-hook transmission which supports features such as Automatic Numbers Identification (ANI). The ANI information is a FSK signal originating from and sent by the C.O. during the off period of the ringing voltage being sent to the subscribers set decodes the FSK signal and displays the calling party's number.

Loop Length

The MH88625 can accommodate loop length of up to 2300Ω minimum (including the subscriber equipment). This corresponds to approximately 8km using 26AWG twisted pair or 15km using 24AWG twisted pair.

OPS Operation

As shown in the application diagram, Figure 9a, the ringing voltage, typically 90Vrms 20Hz biased at V_{BAT}, is applied to the subscriber line through an external relay K1. Enabling of the relay is performed by applying a logic low level to the relay driver control input, RGNDC. Figure 9c, shows how balanced ringing can be accommodated if required.

Central Office Operation

The MH88625 can be configured for ground start C.O. applications with the addition of Q1, D1 and K2, as shown in Figure 9c. Ground start requires control of the Tip lead to remove battery ground from subscriber loop. For loop start applications, control of the Tip lead is not required.

C.O's perform Tip/Ring reversals to indicate that a toll call has been dialled. The Tip/Ring reversal can indicate a toll diversion signal.

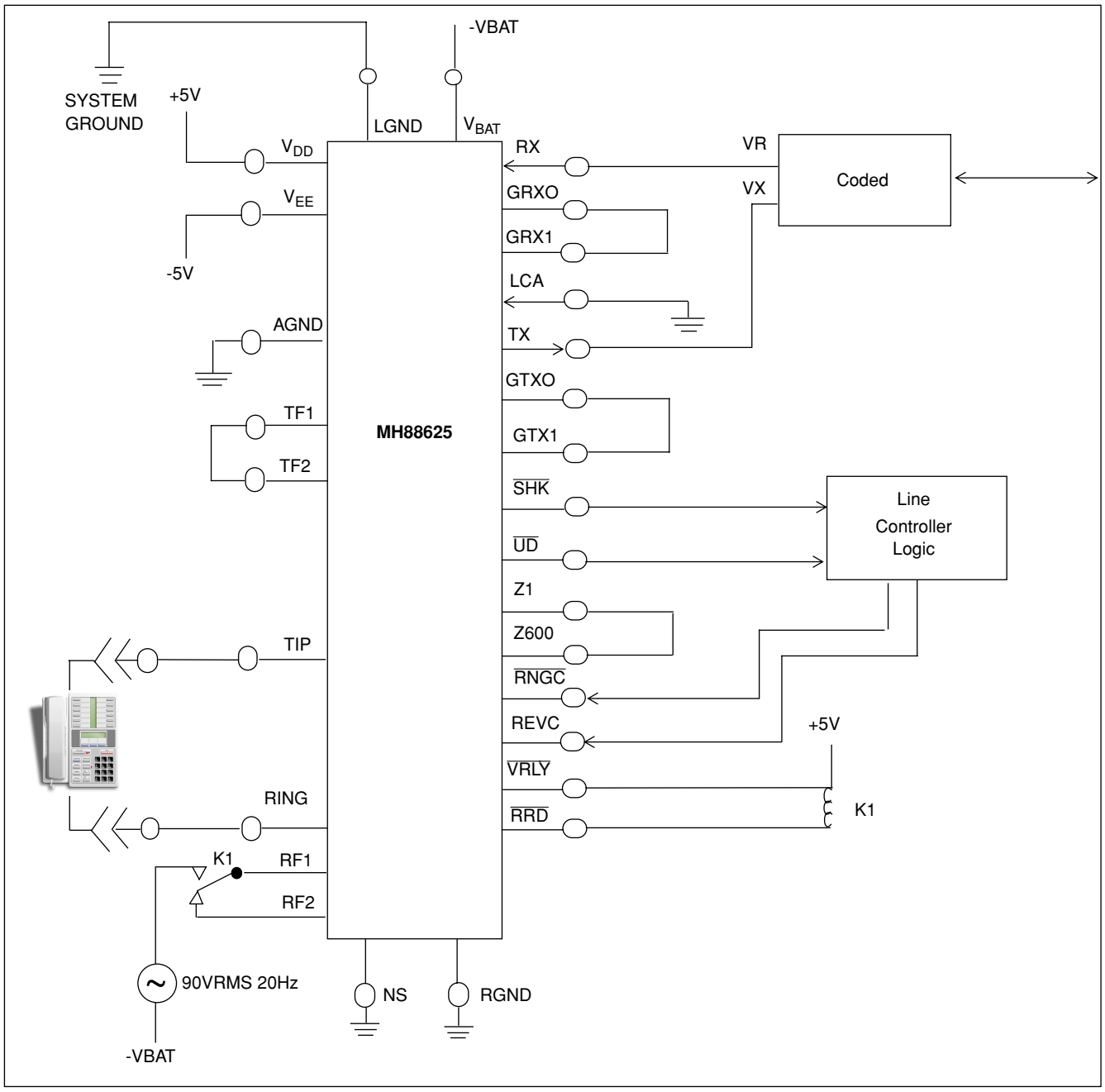


Figure 9a - OPS SLIC Configuration Applications Circuit - Normal Ringing

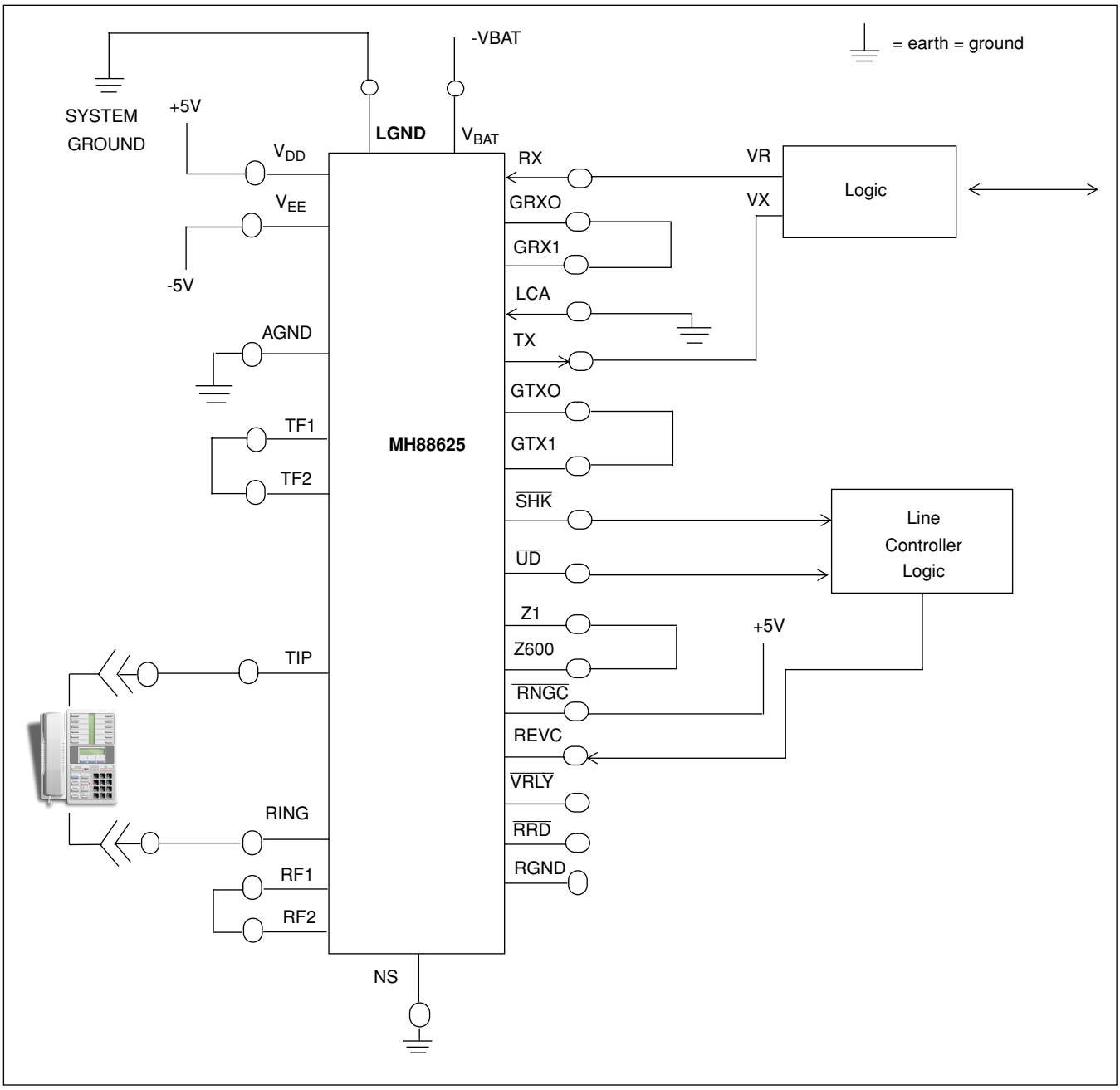


Figure 9b - DID SLIC Configuration Applications Circuit

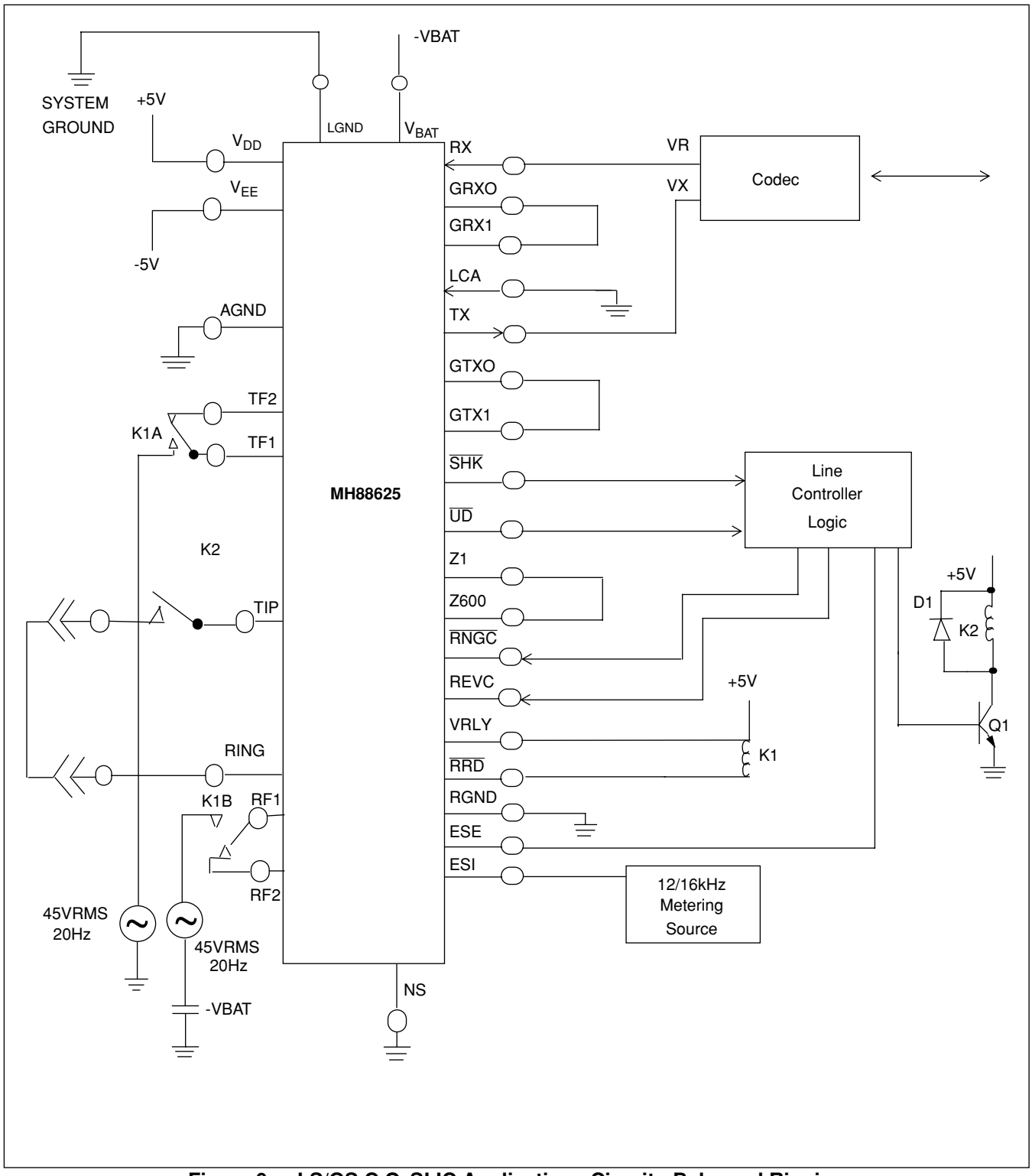
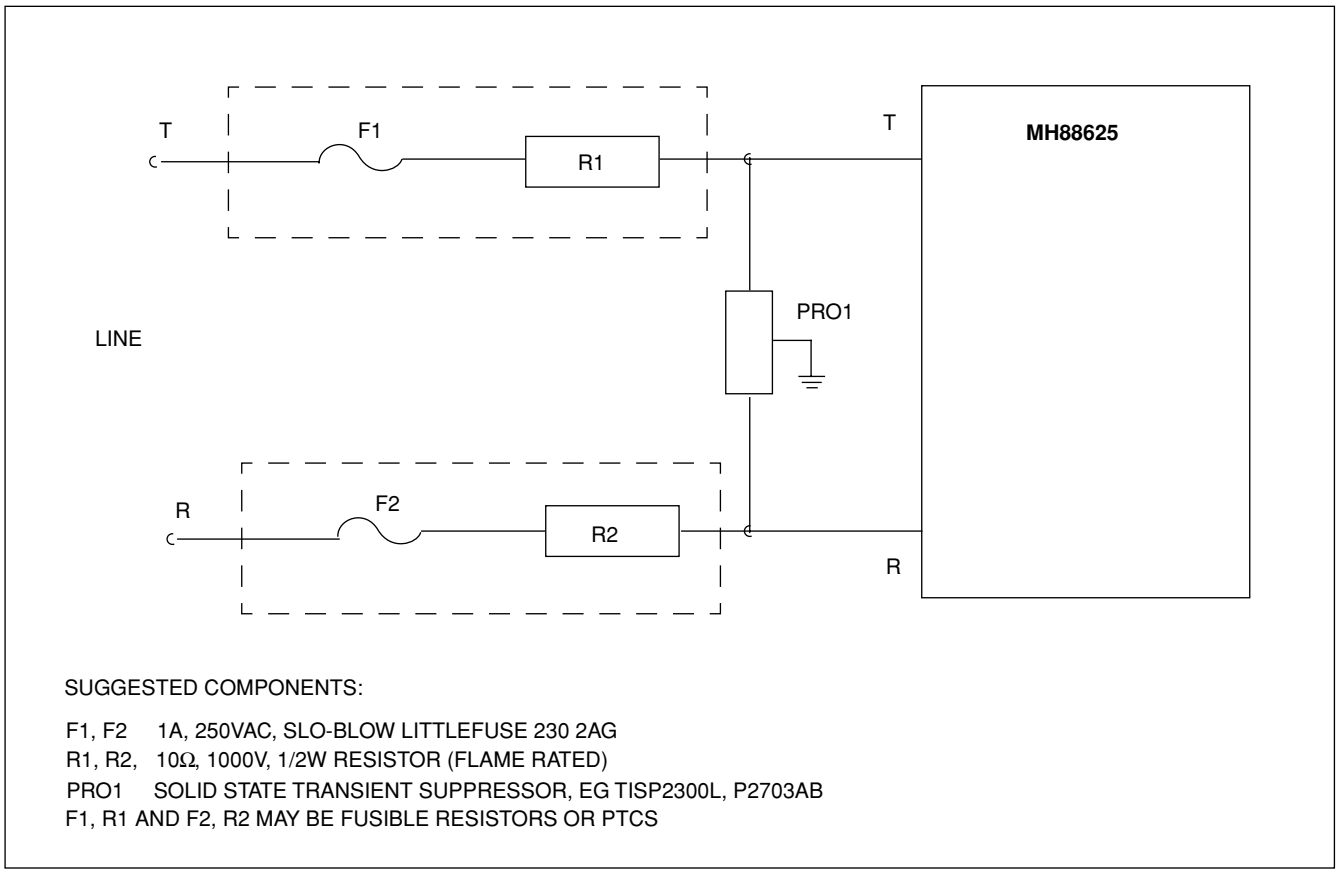


Figure 9c - LS/GS C.O. SLIC Applications Circuit - Balanced Ringing



SUGGESTED COMPONENTS:

F1, F2 1A, 250VAC, SLO-BLOW LITTLEFUSE 230 2AG
R1, R2, 10Ω, 1000V, 1/2W RESISTOR (FLAME RATED)
PRO1 SOLID STATE TRANSIENT SUPPRESSOR, EG TISP2300L, P2703AB
F1, R1 AND F2, R2 MAY BE FUSIBLE RESISTORS OR PTCS

Figure 9d - Suggested Protection Circuit

Absolute Maximum Ratings

	Parameter	Sym	Min	Max	Units	Comments
1	Supply Voltage	V_{Bat} V_{DD} $-V_{EE}$	+0.3 -0.3 +0.3	65 6 6	V V V	With respect LGND
2	Storage Temperature	T_S	-40	+125	°C	

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

	Parameter	Sym	Min	Typ*	Max	Units	Comments
1	Supply Voltage	V_{Bat} V_{DD} V_{EE}	-44 4.75 -4.75	-48 +5.0 -5.0	-60 5.25 -5.25	V V V	
2	Operating Temperature	T_{OP}	20	0	70	°C	

* Typical figures are at 25° C with nominal ± 5V supplies for design aid only.

DC Electrical Characteristics

		Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1		Operating Loop Current	I_{Loop} I_{Loop}	 16		45	mA mA	R_{Loop}=0Ω 2300Ω VBat =-48V
		Var in loop current from nominal	I_{Loop}	26	30	34	mA	R_{Loop}=0Ω, LCA -GND
2		Operating Currents	I_{Bat} I_{Bat} I_{DD} I_{EE}		32 2 25 25		mA mA mA mA	R_{Loop} =0 (off Hook), LCA=GND R_{Loop} = open (On-Hook) On-hook or Off-Hook On-Hook or Off-Hook
3		Power Dissipation	PD_O PD_1		2 300		W mW	Active Standby/Idle
4	$\overline{SHK}$ $\overline{UD}$	Low Level Output Voltage High Level Output	V_{OL} V_{OH}	 3.7		0.5	V V	I_{OL} = 400µA I_{OH}= 40µA
5	ESE NS	Low Level Input Voltage High Level Input Voltage	V_{IL} V_{IH}	 2.4		0.8	V V	
6	ESE NS	High Level Input Current Low Level Input Current	I_{IH} I_{IL}			20 20	µA µA	V_{IH}=5.0V V_{IL}=0.0V

‡ DC Electrical Characteristics are over recommended operating conditions unless otherwise stated.
* Typical figures are at 25° C with nominal ±5V supplies and are for design aid only.

AC Electrical Characteristics

	Characteristics	Sym	Min	Typ*	Max	Units	Test Conditions
1	TX Gain			0		dB	externally adjustable
2	RX Gain			0		dB	externally adjustable
3	Ringing Capability			5		REN	
4	On-Hook Transmission Signal Input Level Gain			 6	2.0	 V_{rms} dB	 VBat=-48V T-R load = 10kΩ min.
5	External Signal Output Level		1.75		2.25	V_{rms}	VBat= -48V, T-R load= 200Ω LCA=0V, Zo-600Ω, Gain=0dB
6	SHK Rise Time Fall time	t_R t_F		1 1		ms ms	Dial Pulse Detection
7	2-Wire Termination Impedance			600/ 900		Ω	 Selectable or user defined
8	Off-Hook Detect Threshold			10		mA	
9	2-Wire Return Loss		20 20 20			dB dB dB	300 to 500Hz 500 to 2500Hz 2500 to 3400Hz
10	Longitudinal Balance Longitundinal to Metallic Metallic to Longitudinal		 58 53			 dB dB	 200-1000Hz 3400Hz
11	Longitudinal Current Capability				40	mA	20mA per lead
12	Idle channel Noise Rx to T-R T-R to Tx	N_{CR} N_{CX}		8 12		 dBrnC dBrnC	
13	Transhybrid Loss	THL	22	40		dB	200-3400Hz
14	Unbalanced Detect Threshold	I_{UB}		10		mA	
15	Analog Signal Overload Level At Tip and Ring				4	dBm	T-R=600Ω, VBat=-48V
16	Ringing Signal Voltage				90	Vrms	
17	Ringing Frequency		17		68	Hz	
18	Ring Trip Delay			100		ms	
19	Absolute Gain, Variation			±0.1		dB	0dB at T-R, 1kHz, Z_O = 600Ω
20	Relative Gain, reference to 1kHz			±0.0 5		dB	300-3400Hz Z_O = 600Ω
21	Power supply Rejection Ratio V_{Bat} V_{DD} V_{EE}	PSR R		 24 24 24		dB	1kHz, 100mVpp

* Typical figure are at 25°C with nominal ±5V supplies and are for design aid only.
‡ AC Electrical Characteristics are over recommended operating conditions unless otherwise stated.

Notes: Impedance set by external network of 600Ω or 900Ω default.
External network for test purposes consists of 2200Ω + 8200Ω // 11.5nF between pins Z1 and Z2, the equivalent Zin has 1/10th the impedance and is equivalent o 220Ω+820Ω // 115nF
Test condition uses a Zin value of 600Ω, 900Ω and the above external network.
Test conditions use a transmit and receive gain set to 0dB default and a Zin value of 600Ω unless otherwise stated.
"Ref" indicates reference impedance which is equivalent to the termination impedance.
"Net" indicates network balance impedance
Refer to Table 1, 2 for TX, RX gain adjustment.

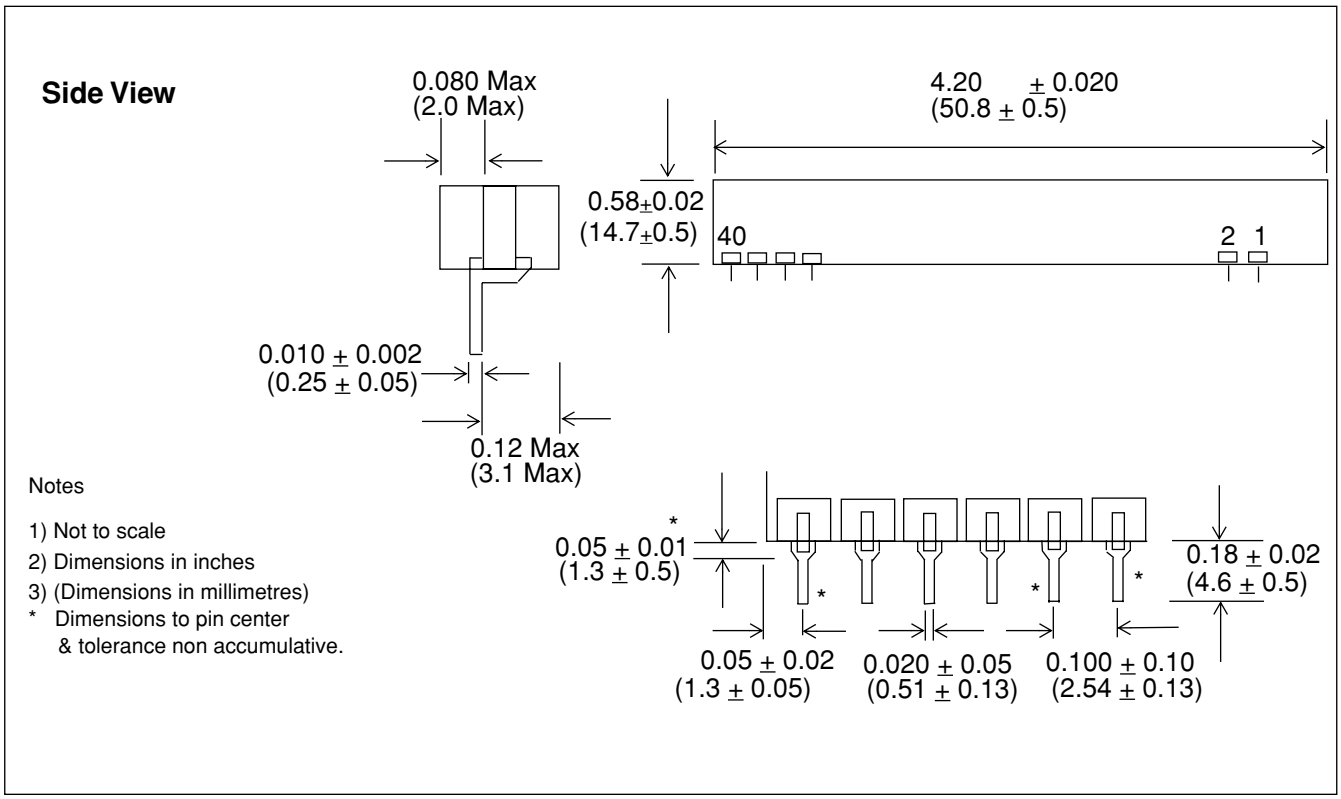


Figure 10 - Mechanical Data



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