



YSS902

AC3D

Dolby Digital (AC-3) / Pro Logic decoder + Sub DSP

■ INTRODUCTION

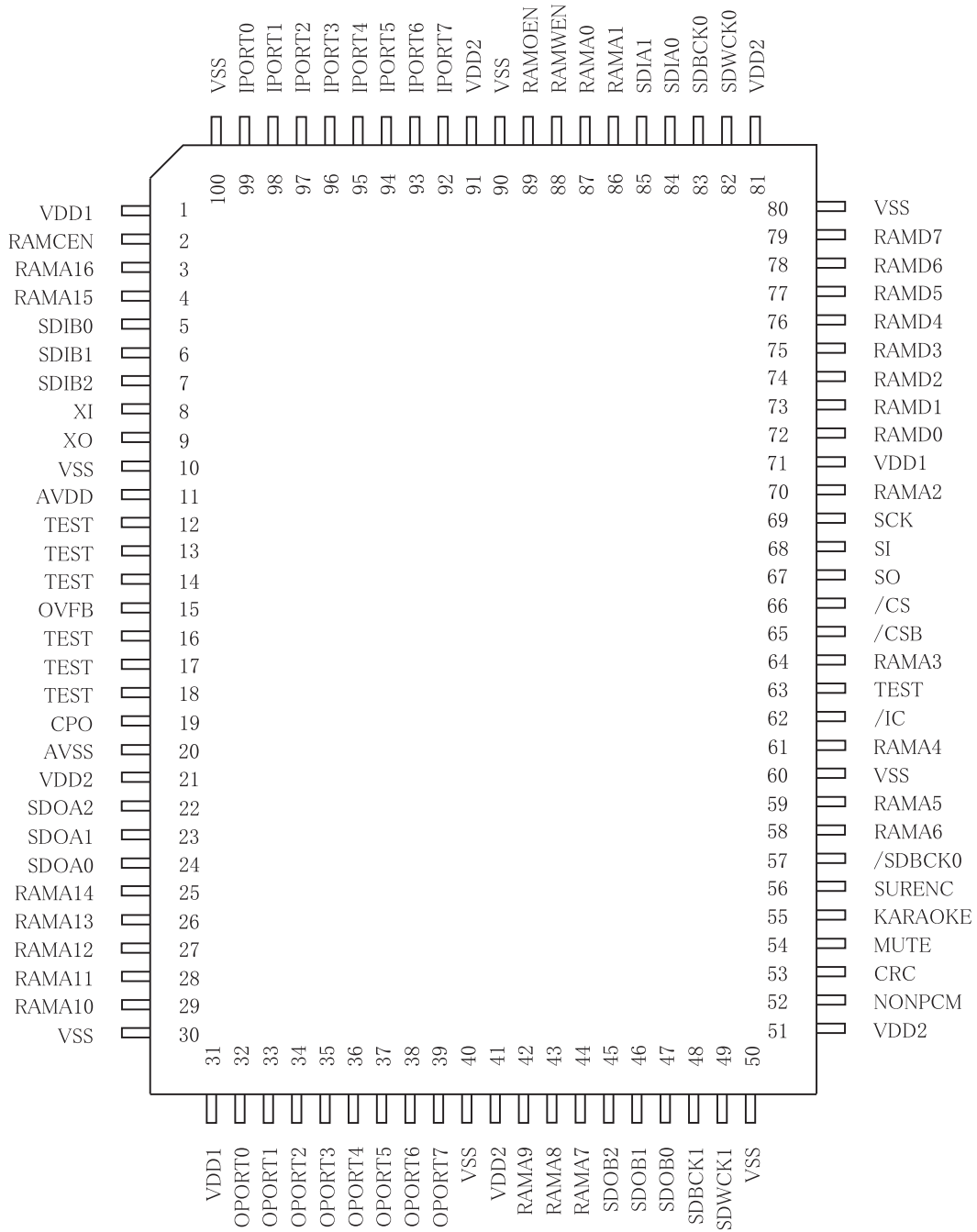
The YSS902 is one chip LSI consisting of two built-in DSP's ; Dolby Digital (AC-3) / Pro Logic (Main DSP) and a sound processing DSP (Sub DSP). Sub DSP is capable of realizing various sound fields, such as virtual surround, by down-loading the program and coefficient.

■ FEATURERS

- Dolby Digital 5.1 channel full decode.
- 24 bit DSP. (Group-A Dolby Digital decoder)
- No external memory is required. (Memory for center and surround channel delay is included)
- Possible to decode multi-language encoded data. (possible to decode based on data-stream-number)
- AC-3 karaoke mode.
- Original compression mode as well as four compression modes recommended by Dolby.
- Dolby Digital decoding latency is fixed to two audio blocks (512 samples).
- Included de-emphasis filter.
- Pro Logic decoding for Dolby Digital 2 channels decoded signal as well as ordinary PCM.
- High performance 25 MIPS programmable DSP suitable for a variety of sound field processing such as original surround, filtering, virtual surround etc.
- Up to 1.36 second delay time is capable when used with an external 1Mbit SRAM. (at fs= 48 kHz)
- Reads Dolby Digital decode information through the microprocessor interface.
- Provide total sixteen I/O ports.
- Possible to connect most of SPDIF receivers, A/D and D/A converters, by setting I/O data interface format.
- Has a built-in PLL oscillation circuit to generates its own operating clock.
- Internal operating clock is 25MHz.
- Supply Voltage: 3.3v for core logic. 5v for I/Os.
- Power saving mode.
- Si-gate CMOS process.
- 100 QFP.(YSS902-F)

Note: "AC-3" and "Pro Logic" are registered trademarks of Dolby Laboratories Licensing Corporation.
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■ PIN CONFIGURATION



< 100QFP TOP VIEW >

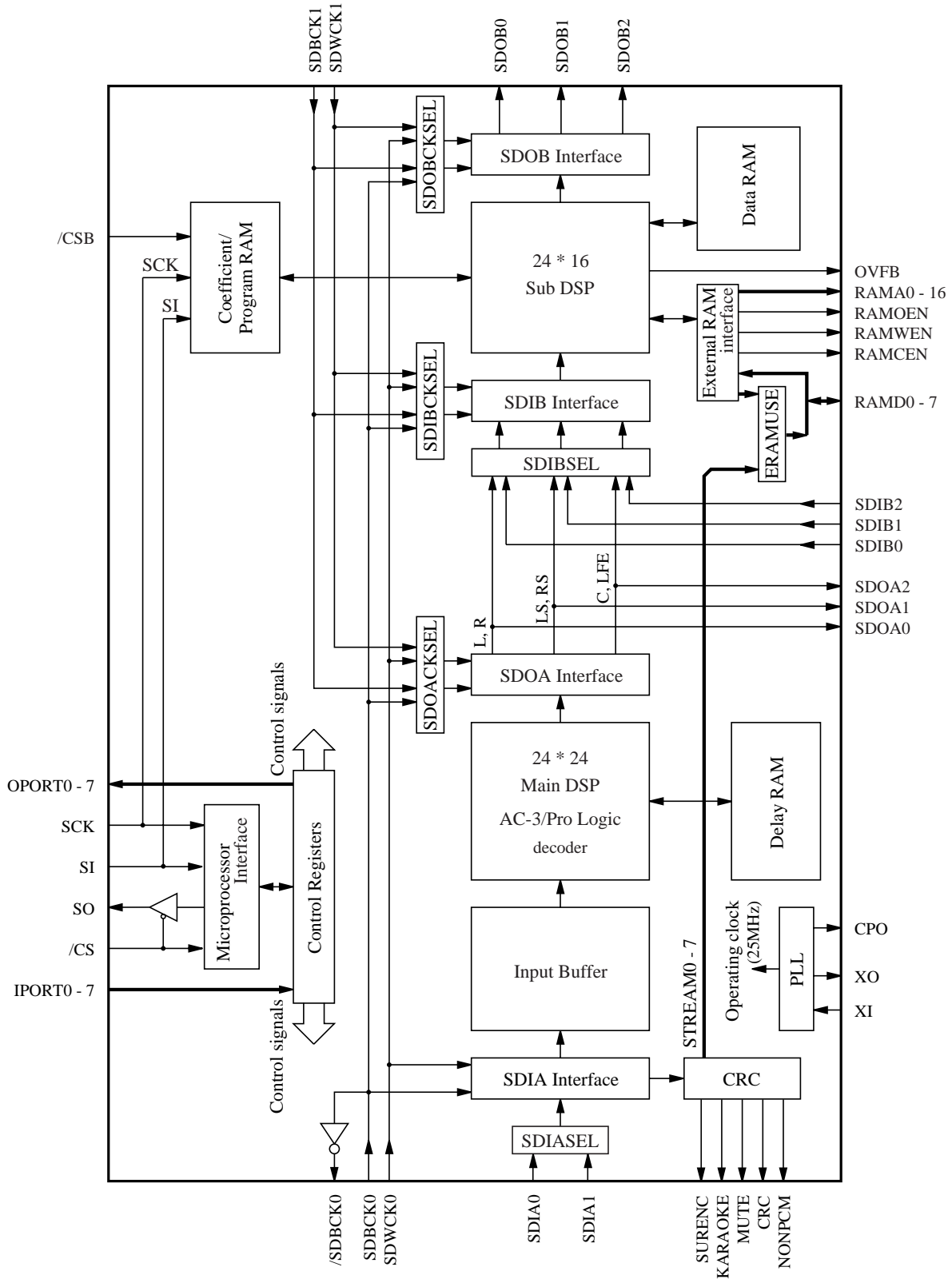
■ PIN FUNCTION

| No. | Name | I/O | FUNCTION |
|-----|---------|-----|---|
| 1 | VDD1 | - | +5V power supply (for I/Os) |
| 2 | RAMCEN | O | External SRAM interface /CE |
| 3 | RAMA16 | O | External SRAM interface address 16 |
| 4 | RAMA15 | O | External SRAM interface address 15 |
| 5 | SDIB0 | I+ | PCM input 0 to Sub DSP |
| 6 | SDIB1 | I+ | PCM input 1 to Sub DSP |
| 7 | SDIB2 | I+ | PCM input 2 to Sub DSP |
| 8 | XI | I | Crystal oscillator connection (6.125MHz - 50.0MHz) |
| 9 | XO | O | Crystal oscillator connection |
| 10 | VSS | - | Ground |
| 11 | AVDD | - | +3.3 V power supply (for PLL circuit) |
| 12 | TEST | | Test terminal (to be open in normal use) |
| 13 | TEST | | Test terminal (to be open in normal use) |
| 14 | TEST | | Test terminal (to be open in normal use) |
| 15 | OVFB | O | Detection of overflow at Sub DSP |
| 16 | TEST | | Test terminal (to be open in normal use) |
| 17 | TEST | | Test terminal (to be open in normal use) |
| 18 | TEST | | Test terminal (to be open in normal use) |
| 19 | CPO | A | Output terminal for PLL, to be connected to ground through the external analog filter circuit |
| 20 | AVSS | - | Ground (for PLL circuit) |
| 21 | VDD2 | - | +3.3 V power supply (for core logic) |
| 22 | SDOA2 | O | PCM output from Main DSP (C, LFE) |
| 23 | SDOA1 | O | PCM output from Main DSP (LS, RS) |
| 24 | SDOA0 | O | PCM output from Main DSP (L, R) |
| 25 | RAMA14 | O | External SRAM interface address 14 |
| 26 | RAMA13 | O | External SRAM interface address 13 |
| 27 | RAMA12 | O | External SRAM interface address 12 |
| 28 | RAMA11 | O | External SRAM interface address 11 |
| 29 | RAMA10 | O | External SRAM interface address 10 |
| 30 | VSS | - | Ground |
| 31 | VDD1 | - | +5V power supply (for I/Os) |
| 32 | OPORT0 | O | Output port for general purpose |
| 33 | OPORT1 | O | Output port for general purpose |
| 34 | OPORT2 | O | Output port for general purpose |
| 35 | OPORT3 | O | Output port for general purpose |
| 36 | OPORT4 | O | Output port for general purpose |
| 37 | OPORT5 | O | Output port for general purpose |
| 38 | OPORT6 | O | Output port for general purpose |
| 39 | OPORT7 | O | Output port for general purpose |
| 40 | VSS | - | Ground |
| 41 | VDD2 | - | +3.3 V power supply (for core logic) |
| 42 | RAMA9 | O | External SRAM interface address 9 |
| 43 | RAMA8 | O | External SRAM interface address 8 |
| 44 | RAMA7 | O | External SRAM interface address 7 |
| 45 | SDOB2 | O | PCM output from Sub DSP |
| 46 | SDOB1 | O | PCM output from Sub DSP |
| 47 | SDOB0 | O | PCM output from Sub DSP |
| 48 | SDBCK1 | I+ | Bit clock input for SDOA, SDIB, SDOB |
| 49 | SDWCK1 | I+ | Word clock input for SDOA, SDIB, SDOB |
| 50 | VSS | - | Ground |
| 51 | VDD2 | - | +3.3 V power supply (for core logic) |
| 52 | NONPCM | O | Detection of non-PCM data |
| 53 | CRC | O | Detection of CRC error |
| 54 | MUTE | O | Detection of auto mute |
| 55 | KARAOKE | O | Detection of AC-3 karaoke data |

| No. | Name | I/O | FUNCTION |
|-----|---------|-------|--|
| 56 | SURENC | O | Detection of AC-3 2/0 mode Dolby surround encoded input |
| 57 | /SDBCK0 | O | Inverted SDBCK0 clock output (refer to Block diagram) |
| 58 | RAMA6 | O | External SRAM interface address 6 |
| 59 | RAMA5 | O | External SRAM interface address 5 |
| 60 | VSS | - | Ground |
| 61 | RAMA4 | O | External SRAM interface address 4 |
| 62 | /IC | Is | Initial clear |
| 63 | TEST | | Test terminal (to be open in normal use) |
| 64 | RAMA3 | O | External SRAM interface address 3 |
| 65 | /CSB | Is+ | Sub DSP Chip select |
| 66 | /CS | Is | Microprocessor interface Chip select input |
| 67 | SO | Ot | Microprocessor interface Serial data output |
| 68 | SI | Is | Microprocessor interface / Sub DSP Serial data input |
| 69 | SCK | Is | Microprocessor interface / Sub DSP clock input |
| 70 | RAMA2 | O | External SRAM interface address 2 |
| 71 | VDD1 | - | +5V power supply (for I/Os) |
| 72 | RAMD0 | I+/ O | External SRAM interface data (STREAM0 output when External SRAM is not in use) |
| 73 | RAMD1 | I+/ O | External SRAM interface data (STREAM1 output when External SRAM is not in use) |
| 74 | RAMD2 | I+/ O | External SRAM interface data (STREAM2 output when External SRAM is not in use) |
| 75 | RAMD3 | I+/ O | External SRAM interface data (STREAM3 output when External SRAM is not in use) |
| 76 | RAMD4 | I+/ O | External SRAM interface data (STREAM4 output when External SRAM is not in use) |
| 77 | RAMD5 | I+/ O | External SRAM interface data (STREAM5 output when External SRAM is not in use) |
| 78 | RAMD6 | I+/ O | External SRAM interface data (STREAM6 output when External SRAM is not in use) |
| 79 | RAMD7 | I+/ O | External SRAM interface data (STREAM7 output when External SRAM is not in use) |
| 80 | VSS | - | Ground |
| 81 | VDD2 | - | +3.3 V power supply (for core logic) |
| 82 | SDWCK0 | I | Word clock input for SDIA, SDOA, SDIB, SDOB |
| 83 | SDBCK0 | I | Bit clock input for SDIA, SDOA, SDIB, SDOB |
| 84 | SDIA0 | I | AC-3 bitstream (or PCM) data input for Main DSP |
| 85 | SDIA1 | I | AC-3 bitstream (or PCM) data input for Main DSP |
| 86 | RAMA1 | O | External SRAM interface address 1 |
| 87 | RAMA0 | O | External SRAM interface address 0 |
| 88 | RAMWEN | O | External SRAM interface /WE |
| 89 | RAMOEN | O | External SRAM interface /OE |
| 90 | VSS | - | Ground |
| 91 | VDD2 | - | +3.3 V power supply (for core logic) |
| 92 | IPORT7 | I+ | Input port for general purpose |
| 93 | IPORT6 | I+ | Input port for general purpose |
| 94 | IPORT5 | I+ | Input port for general purpose |
| 95 | IPORT4 | I+ | Input port for general purpose |
| 96 | IPORT3 | I+ | Input port for general purpose |
| 97 | IPORT2 | I+ | Input port for general purpose |
| 98 | IPORT1 | I+ | Input port for general purpose |
| 99 | IPORT0 | I+ | Input port for general purpose |
| 100 | VSS | - | Ground |

NOTE) Is: Schmidt trigger input terminal
I+: Input terminal with a pull-up resistor
O: Digital output terminal
Ot: Tri-state digital output terminal
A: Analog terminal

■ BLOCK DIAGRAM



■ FUNCTION DESCRIPTION

The YSS902 consist of Main DSP section where AC-3/Pro Logic decoding is executed and Sub DSP section where various sound field effects are added. Please refer to “BLOCK DIAGRAM” section.

Sub DSP is a 6 ch input / 6 ch output programmable DSP exclusively for the sound field processing. It can apply such effects as virtual surround, echo and equalizing. In addition, with an SRAM up to 1Mbit connected, it can produce reverberation for one second or longer. By using this function, it is possible to simulate various sound fields such as a hall or a church.

* If adopting some technology owned by another company is desired for use in Sub DSP section, note that a separate contract may be required between the owner of that technology and the user with respect to adoption of the technology.

1. Clocks XI, XO, CPO

The crystal oscillation circuit is formed by using XI and XO terminals. Oscillation frequency 50MHz is divided by 2 internally to provide the operating clock signals of 25MHz.

Clock signals should be obtained through self oscillation by using XI and XO terminals, or external clock signals should be fed through the XI terminal.

This LSI operates in a PLL oscillation mode as well. When the PLL oscillation mode is selected and an external clock signal whose frequency is lower than 49MHz is fed through the XI terminal and multiplied, connect an external analog filter between CPO terminal and Ground.

2. Data Interface SDIA0, SDIA1, SDOA0-2, SDIB0-2, SDOB0-2, SDWCK0, SDBCK0, SDWCK1, SDBCK1, /SDBCK0

Main DSP section

AC-3 bitstream or PCM data should be fed from SDIA0 or SDIA1 terminal. These signals are processed by AC-3 / Pro Logic decoding procedure in Main DSP section and then transmitted to Sub DSP section as well as outputted through SDOA0-2 terminals.

Sub DSP section

In Sub DSP section, various types of processing can be applied to the PCM data decoded in Main DSP section or inputted through SDIB0-2 terminals. Then, processed signals are outputted from each of SDOB0-2 terminals.

Following parameters can be selected by changing the control register setting.

- Selection of Main DSP input signal (SDIA0, SDIA1)
- Selection of Sub DSP input signal (Main DSP output, SDIB0-2 input)
- Polarity of bit clock and word clock
- Format and bit count of input/output data

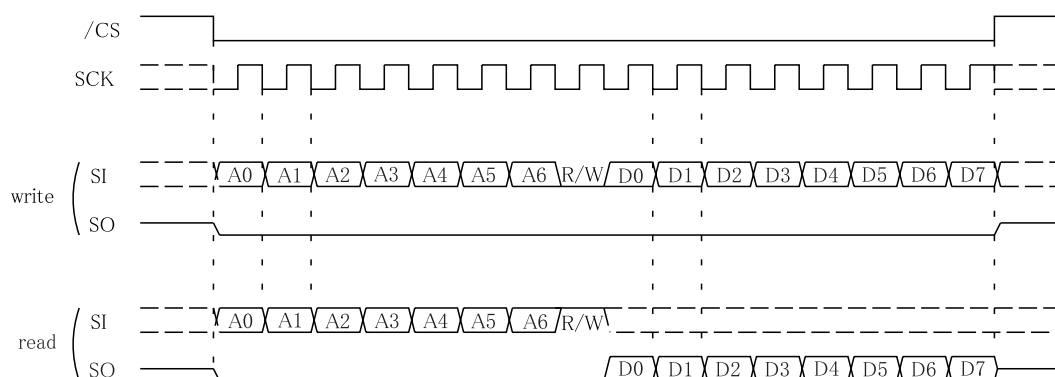
For more information on the format of the input/output data, please refer to “Serial Data Interface” section.

3. Microprocessor Interface /CS, /CSB, SCK, SI, SO

The control registers can be read/written via the serial microprocessor interface by using /CS, SCK, SI, and SO terminals.

Please refer to the following format diagram for the details of read/write timing.

Format diagram for read/write timing



When /CS=1, the SO output becomes high-impedance.

* Be sure to set /CSB to "1" when making an access to the control register.

The sound field processing program used for Sub DSP is down-loaded by using the /CSB, SCK, and SI terminals. Please refer to Application manual for the details of Sub DSP.

4. External Interface RAMA0-16, RAMD0-7, RAMCEN, RAMOEN, RAMWEN

An external SRAM can be connected to Sub DSP.

5. General purpose I/O ports OPORT0-7, IPORT0-7

OPORT0-7 terminals are output ports for general purpose. Data written on the register (address 0x04) are outputted from these terminals.

IPORT0-7 terminals are input ports for general purpose. Data inputted to these terminals can be read from the register (address 0x05).

6. Initial clear /IC

This LSI requires initial clear when turning on the power.

7. LSI test terminals TEST

Leave the test terminals open in normal use.

■ CONTROL REGISTER

The decoding system is controlled by reading and writing the control registers through microprocessor interface. (/CS, SCK, SI and SO)

Note : All bits are set to "0" by initial clear (/IC=0) except for PLL0(bit 4) of PLL/DSN register (0x00).

| address | Name | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | |
|---------|-------------------------|------------------------|---------|--------------|--------------|--------------|--------------|--------------|---------|--|
| 0x00 | PLL/DSN Register | PLLUSE | PLL2-0 | | | DSNIGN | DSN2 - 0 | | | |
| 0x01 | Mute Register | LMUTEN | CMUTEN | RMUTEN | RSMUTEN | LSMUTEN | LFEMUTEN | DSPMUTEN | AMOFF | |
| 0x02 | SDIA Register | SDIASEL | PDOWN | SDIAFMT1 - 0 | | SDIABIT1 - 0 | | SDIAWP | SDIABP | |
| 0x03 | SDOA Register | SDOACKSEL | | SDOAFMT1 - 0 | | SDOABIT1 - 0 | | SDOAWP | SDOABP | |
| 0x04 | OPORT Register | OPORT7 - 0 | | | | | | | | |
| 0x05 | IPORT Register | IPORT7 - 0 (Read only) | | | | | | | | |
| 0x09 | Noise Level Register | NOISELEV7 - 0 | | | | | | | | |
| 0x0A | Center Delay Register | | | | | | CDELAY2 - 0 | | | |
| 0x0B | Surround Delay Register | | | | | | SRDELAY3 - 0 | | | |
| 0x0C | Noise Register | NOISE | PN/WN | | | | | | | |
| 0x0D | FS Register | | | | | | | | FS1 - 0 | |
| 0x0E | L Volume Register | LVOL7 - 0 | | | | | | | | |
| 0x0F | C Volume Register | CVOL7 - 0 | | | | | | | | |
| 0x10 | R Volume Register | RVOL7 - 0 | | | | | | | | |
| 0x11 | LS Volume Register | LSVOL7 - 0 | | | | | | | | |
| 0x12 | RS Volume Register | RSVOL7 - 0 | | | | | | | | |
| 0x13 | LFE Volume Register | LFEVOL7 - 0 | | | | | | | | |
| 0x14 | Compression Register | EMPON | AIBON | VOLON | DITHOFF | P11OFF | DIALOFF | COMPMOD1 - 0 | | |
| 0x15 | HDYNRNG Register | HDYNRNG7 - 0 | | | | | | | | |
| 0x16 | LDYNRNG Register | LDYNRNG7 - 0 | | | | | | | | |
| 0x17 | Mode Register | AC3/PCM | PLDECON | PLSRMOD | DUALMOD1 - 0 | | OUTMOD2 - 0 | | | |
| 0x30 | COEF0-H Register | COEF0-15 - 8 | | | | | | | | |
| 0x31 | COEF0-L Register | COEF0-7 - 0 | | | | | | | | |
| 0x32 | COEF1-H Register | COEF1-15 - 8 | | | | | | | | |
| 0x33 | COEF1-L Register | COEF1-7 - 0 | | | | | | | | |
| 0x34 | SDIB Register | SDIBCKSEL | SDIBSEL | SDIBFMT1 - 0 | | SDIBBIT1 - 0 | | SDIBWP | SDIBBP | |
| 0x35 | SDOB Register | SDOBCKSEL | SDBUSE | SDOBFMT1 - 0 | | SDOBBIT1 - 0 | | SDOBWP | SDOBBP | |
| 0x36 | ERAM Register | ERAMUSE | | | | | | | | |

Note : Do not write "1" into the cross-hatched bits because they are used for testing the LSI.

The following registers of address 0x18 to 0x2F are read-only (write disabled).

| address | Name | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 | |
|---------|-----------------------|------------|-----------|------------|------------|-------|-----------|-------|-------|--|
| 0x18 | Bitstream Register 0 | fscod | | | frmsizecod | | | | | |
| 0x19 | Bitstream Register 1 | bsid | | | | | bsmod | | | |
| 0x1A | Bitstream Register 2 | acmod | | | cmixlev | | surmixlev | | lfeon | |
| 0x1B | Bitstream Register 3 | dsurmod | | copyrightb | origbs | 0 | 0 | 0 | 0 | |
| 0x1C | Bitstream Register 4 | 0 | 0 | 0 | dialnorm | | | | | |
| 0x1D | Bitstream Register 5 | 0 | 0 | 0 | dialnorm2 | | | | | |
| 0x1E | Bitstream Register 6 | audprodi | mixlevel | | | | roomtyp | | | |
| 0x1F | Bitstream Register 7 | audprodi2e | mixlevel2 | | | | roomtyp2 | | | |
| 0x20 | Bitstream Register 8 | timecod1e | 0 | timecod1 | | | | | | |
| 0x21 | Bitstream Register 9 | timecod1 | | | | | | | | |
| 0x22 | Bitstream Register 10 | timecod2e | 0 | timecod2 | | | | | | |
| 0x23 | Bitstream Register 11 | timecod2 | | | | | | | | |
| 0x24 | Bitstream Register 12 | langcode | langcod2e | compre | compr2e | 0 | 0 | 0 | 0 | |
| 0x25 | Bitstream Register 13 | langcod | | | | | | | | |

(Registermap continued)

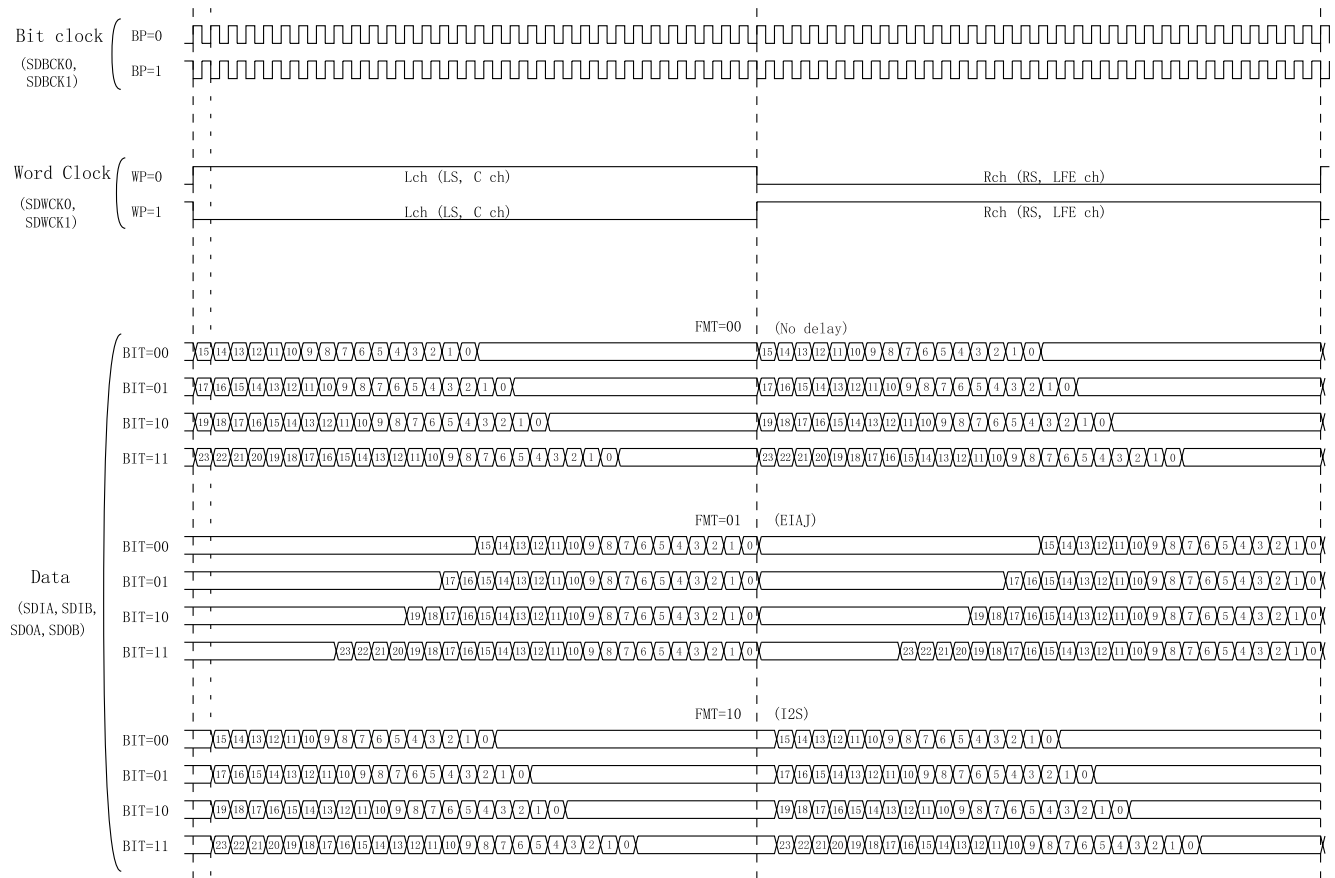
| address | Name | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---------|-----------------------|--|---------|---------|---------|---------|---------|---------|---------|
| 0x26 | Bitstream Register 14 | langcod2 | | | | | | | |
| 0x27 | Bitstream Register 15 | compr | | | | | | | |
| 0x28 | Bitstream Register 16 | compr2 | | | | | | | |
| 0x29 | Bitstream Register 17 | dynrng | | | | | | | |
| 0x2A | Bitstream Register 18 | dynrng2 | | | | | | | |
| 0x2B | (not used) | (write disable, all "0" out when read) | | | | | | | |
| 0x2C | | | | | | | | | |
| 0x2D | | | | | | | | | |
| 0x2E | Data Stream Register | STREAM7 | STREAM6 | STREAM5 | STREAM4 | STREAM3 | STREAM2 | STREAM1 | STREAM0 |
| 0x2F | Status Register | 0 | 0 | 2/0MODE | SURENC | KARAOKE | MUTE | CRC | NONPCM |

Address 0x06 to 0x08 and 0x37 to 0x7F are assigned for TEST. Never access to these registers.

Please refer to Application manual for details of Control register.

■ SERIAL DATA INTERFACE

Data timing of the serial data interface is as follows.



Please refer to Application manual for details of SDIA, SDOA, SDIB, and SDOB registers.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Unit |
|----------------------|------------------|----------------------|----------------------|------|
| Power Supply Voltage | VDD1 | V _{ss} -0.5 | V _{ss} +7.0 | V |
| | VDD2, AVDD | V _{ss} -0.5 | V _{SS} +4.6 | V |
| Input Voltage | V _I | V _{ss} -0.5 | VDD1+0.5 | V |
| Storage Temperature | T _{stg} | -50 | 125 | °C |

2. Recommended Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|-----------------------|-----------------|------|------|------|------|
| Power Supply Voltage | VDD1 | 4.75 | 5.0 | 5.25 | V |
| | VDD2, AVDD | 3.0 | 3.3 | 3.6 | V |
| Operating Temperature | T _{op} | 0 | 25 | 70 | °C |

3. DC Characteristics (Condition: Under Recommended Operating Conditions)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---------------------------|------------------|-------------------------------------|-----------------------|------|---------------------|------|
| Input Voltage H Level (1) | V _{IH1} | *1 | 0.7V _{DD1} | | | V |
| Input Voltage H Level (2) | V _{IH2} | *2 | 2.2 | | | V |
| Input Voltage L Level (1) | V _{IL1} | *1 | | | 0.2V _{DD1} | V |
| Input Voltage L Level (2) | V _{IL2} | *2 | | | 0.8 | V |
| Output Voltage H Level | V _{OH} | I _{OH} = -80 μA | V _{DD1} -1.0 | | | V |
| Output Voltage L Level | V _{OL} | I _{OL} = 1.6 mA | | | 0.4 | V |
| Input Leakage Current | I _{LI} | Terminal without a pull-up resistor | -10 | | 10 | μA |
| Pull-up Resistor | R _U | | 25 | | 100 | kΩ |
| Power Consumption | P _D | XI=50MHz, PLL not used | | 250 | 500 | mW |

*1 Applicable to XI and /IC input terminals.

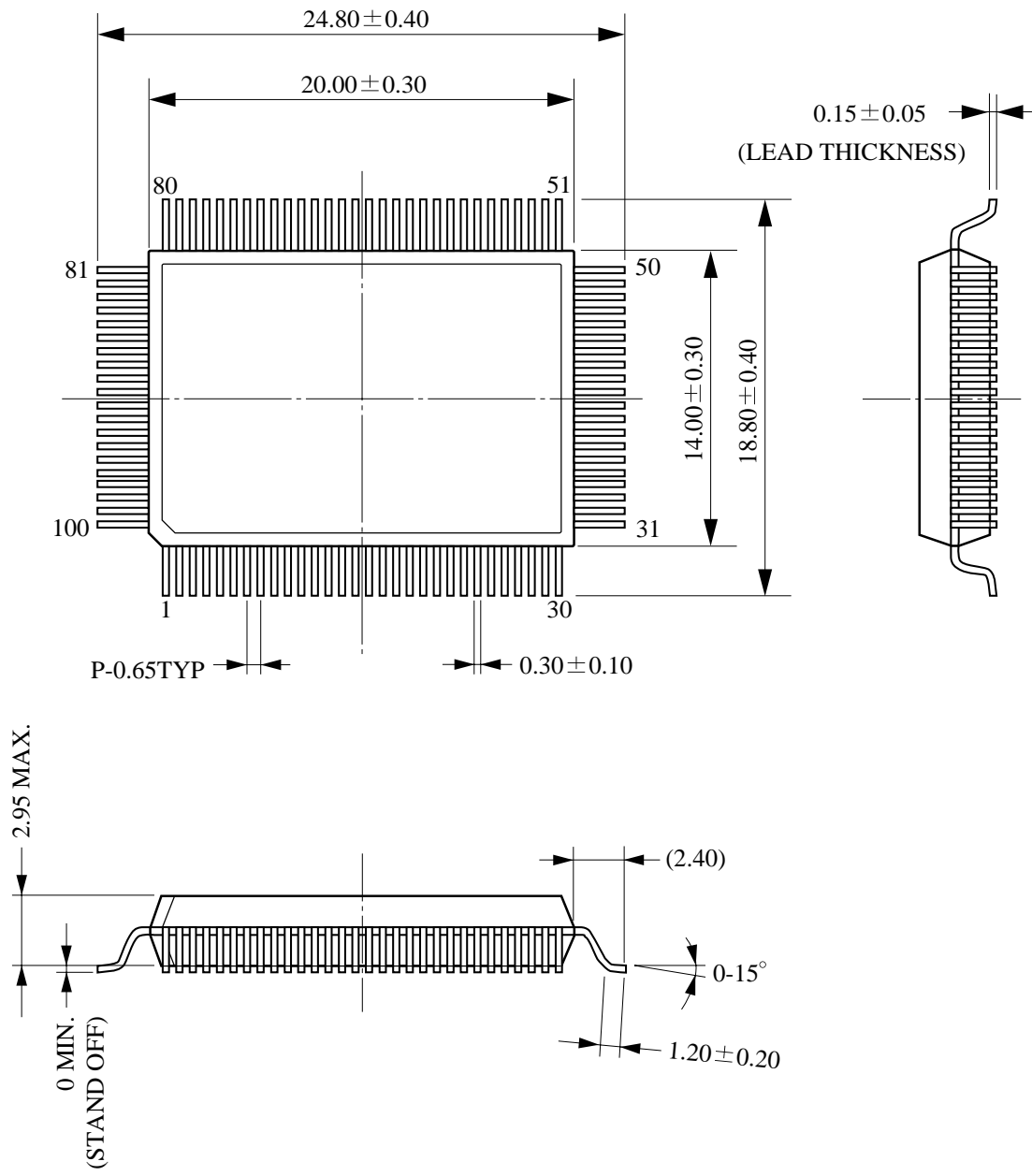
*2 Applicable to input terminals except XI and /IC terminals.

4. XI

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--------------------|-------------------|------------|-------|-----|-----|------|
| XI clock frequency | X _{in} | | 6.125 | | 50 | MHz |
| XI clock duty | X _{duty} | | 40 | 50 | 60 | % |

EXTERNAL DIMENSIONS

C-PK100FP-1



The figure in the parenthesis () should be used as a reference.
 Plastic body dimensions do not include burr of resin.
 UNIT: mm

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