Panasonic

1.1 Overview

The MN103LF series of 32-bit single-chip microcomputers have multiple types of peripheral functions. This LSI series is well suited for camera, TV, VCR, Car Audio, printer, telephone, FAX machine, air-conditioner, music instrument and other applications.

This LSI series has flexible and optimized hardware configurations and simple efficient instruction set. This LSI series incorporates an internal ROM of 1048 KB (maximum) and RAM of 76 KB (maximum), 11 external interrupts, 96 internal interrupts including non-maskable interrupt, 26 timer counters, 14 sets of serial interfaces, A/D converter, D/A converter, 2 sets of watchdog timer, DMA, CAN, and IEBus interface.

In addition, this LSI series has 5 oscillation circuits (external high frequency: 4 MHz to 20 MHz/ external low frequency:32.768 kHz/ internal high frequency: 20 MHz/ internal low frequency: 30 kHz/ PLL: frequency multiplier of high or low frequency).

The internal clock can be switched to four oscillation clock except the internal low oscillation. The internal clock is generated by dividing the oscillation clock or PLL clock. The best operation clock for the system can be selected by switching its frequency ratio by programming.

A machine cycle (minimum instruction execution time) is 25 ns (internal operating condition: 1.8 V, 40 MHz).

1.2 Product Summary

This manual describes the following model.

Series *1	Model	Pin Number	ROM Size	RAM Size *2	Sector swap *3	In-vehicle LAN	Package
MN103L32	MN103LF32R *	100 pin	1048 KB	76 KB	-	CAN/IEBus	100 pin LQFP (14 mm × 14 mm/0.5mm pitch)
	MN103LF32Q *		792 KB				
	MN103LF32N *		536 KB	40 KB			
	MN103LF32M *		408 KB	32 KB			
	MN103LF32K *		280 KB	20 KB			
	MN103LF32Z *		1048 KB	76 KB	Existence		
	MN103LF32Y *		792 KB				
	MN103LF32X *		536 KB	40 KB			
	MN103LF32W *		408 KB	32 KB			
	MN103LF32T *		280 KB	20 KB			
MN103L33	MN103LF33R *	128 pin	1048 KB	76 KB	-		128 pin LQFP (18 mm × 18 mm/0.5mm pitch)
	MN103LF33Q *		792 KB				
	MN103LF33N *		536 KB	40 KB			
	MN103LF33M *		408 KB	32 KB			
	MN103LF33K *		280 KB	20 KB			
	MN103LF33Z *		1048 KB	76 KB	Existence		
	MN103LF33Y *		792 KB				
	MN103LF33X *		536 KB	40 KB			
	MN103LF33W *		408 KB	32 KB			
	MN103LF33T *		280 KB	20 KB			
MN103L09	MN103LF09R *	144 pin	1048 KB	76 KB	-		144 pin LQFP (20 mm × 20 mm/0.5mm pitch)
	MN103LF09Q *		792 KB				
	MN103LF09N *		536 KB	40 KB			
	MN103LF09M *		408 KB	32 KB			
	MN103LF09K *		280 KB	20 KB			
	MN103LF09Z *		1048 KB	76 KB	Existence		
	MN103LF09Y *		792 KB				
	MN103LF09X *		536 KB	40 KB			
	MN103LF09W *		408 KB	32 KB			
	MN103LF09T *		280 KB	20 KB			

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Series *1	Model	Pin Number	ROM Size	RAM Size *2	Sector swap *3	In-vehicle LAN	Package
MN103L10/ MN103L13	MN103LF13R *	100 pin	1048 KB	76 KB	-	IEBus	100 pinLQFP (14 mm × 14 mm/0.5mm pitch)
	MN103LF13Q *		792 KB				
	MN103LF10R *		1048 KB	64 KB			
	MN103LF10Q *		792 KB				
	MN103LF10N *		536 KB	40 KB			
	MN103LF10M *		408 KB	32 KB			
	MN103LF10K		280 KB	20 KB			
	MN103LF13Z *		1048 KB	76 KB	Existence		
	MN103LF13Y *		792 KB				
	MN103LF10Z *		1048 KB	64 KB			
	MN103LF10Y *		792 KB				
	MN103LF10X *		536 KB	40 KB			
	MN103LF10W *		408 KB	32 KB			
	MN103LF10T *		280 KB	20 KB			
MN103L11/ MN103L14	MN103LF14R	128 pin	1048 KB	76 KB	-		128 pinLQFP (18mm × 18 mm/0.5mm pitch)
	MN103LF14Q *		792 KB				
	MN103LF11R *		1048 KB	64 KB			
	MN103LF11Q *		792 KB				
	MN103LF11N *		536 KB	40 KB			
	MN103LF11M *		408 KB	32 KB			
	MN103LF11K *		280 KB	20 KB			
	MN103LF14Z *		1048 KB	76 KB	Existence		
	MN103LF14Y *		792 KB				
	MN103LF11Z *		1048 KB	64 KB			
	MN103LF11Y *		792 KB				
	MN103LF11X *		536 KB	40 KB			
	MN103LF11W *		408 KB	32 KB			
	MN103LF11T *		280 KB	20 KB			
MN103L12/ MN103L15	MN103LF15R	144 pin	1048 KB	76 KB	-		144 pinLQFP (20mm × 20 mm/0.5mm pitch)
	MN103LF15Q *		792 KB				
	MN103LF12R *		1048 KB	64 KB			
	MN103LF12Q *		792 KB				
	MN103LF12N		536 KB	40 KB			
	MN103LF15Z *		1048 KB	76 KB	Existence		
	MN103LF15Y *		792 KB				
	MN103LF12Z *		1048 KB	64 KB			
	MN103LF12Y *		792 KB				
	MN103LF12X *		536 KB	40 KB			

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Series *1	Model	Pin Number	ROM Size	RAM Size *2	Sector swap *3	In-vehicle LAN	Package
MN103L16/ MN103L19	MN103LF19R	100 pin	1048 KB	76 KB	-	-	100 pinLQFP (14mm × 14 mm/0.5mm pitch)
	MN103LF19Q *		792 KB				
	MN103LF16R		1048 KB	64 KB			
	MN103LF16Q		792 KB				
	MN103LF16N *		536 KB	40 KB			100 pinLQFP (14mm × 14 mm/0.5mm pitch) 100 pinQFP (18mm × 18mm/0.65mm pitch)
	MN103LF16M *		408 KB	32 KB			
	MN103LF16K		280 KB	20 KB			
	MN103LF19Z *		1048 KB	76 KB	Existence		100 pinLQFP (14mm × 14 mm/0.5mm pitch)
	MN103LF19Y *		792 KB				
	MN103LF16Z *		1048 KB	64 KB			
	MN103LF16Y *		792 KB				
	MN103LF16X *		536 KB	40 KB			100 pinLQFP (14mm × 14 mm/0.5mm pitch) 100 pinQFP (18mm × 18mm/0.65mm pitch)
	MN103LF16W *		408 KB	32 KB			
	MN103LF16T *		280 KB	20 KB			
MN103L17/ MN103L20	MN103LF20R	128 pin	1048 KB	76 KB	-		128 pinLQFP (18mm × 18 mm/0.5mm pitch)
	MN103LF20Q *		792 KB				
	MN103LF17R *		1048 KB	64 KB			
	MN103LF17Q *		792 KB				
	MN103LF17N *		536 KB	40 KB			
	MN103LF17M *		408 KB	32 KB			
	MN103LF17K		280 KB	20 KB			
	MN103LF20Z *		1048 KB	76 KB	Existence		
	MN103LF20Y *		792 KB				
	MN103LF17Z *		1048 KB	64 KB			
	MN103LF17Y *		792 KB				
	MN103LF17X *		536 KB	40 KB			
	MN103LF17W *		408 KB	32 KB			
	MN103LF17T *		280 KB	20 KB			
MN103L18/ MN103L21	MN103LF21R *	144 pin	1048 KB	76 KB	-		144 pinLQFP (20mm × 20 mm/0.5mm pitch)
	MN103LF21Q *		792 KB				
	MN103LF18R *		1048 KB	64 KB			
	MN103LF18Q *		792 KB				
	MN103LF18N *		536 KB	40 KB			
	MN103LF21Z *		1048 KB	76 KB	Existence		
	MN103LF21Y *		792 KB				
	MN103LF18Z *		1048 KB	64 KB			
	MN103LF18Y *		792 KB				
	MN103LF18X *		536 KB	40 KB			

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Series *1	Model	Pin Number	ROM Size	RAM Size *2	Sector swap *3	In-vehicle LAN	Package
MN103L22/ MN103L25	MN103LF25R *	100 pin	1048 KB	76 KB	-	CAN	100 pinLQFP (14mm × 14 mm/0.5mm pitch)
	MN103LF25Q *		792 KB				
	MN103LF22R *		1048 KB	64 KB			
	MN103LF22Q *		792 KB				
	MN103LF22N		536 KB	40 KB			
	MN103LF22M *		408 KB	32 KB			
	MN103LF22K		280 KB	20 KB			
	MN103LF25Z *		1048 KB	76 KB	Existence		
	MN103LF25Y *		792 KB				
	MN103LF22Z *		1048 KB	64 KB			
	MN103LF22Y *		792 KB				
	MN103LF22X *		536 KB	40 KB			
	MN103LF22W *		408 KB	32 KB			
	MN103LF22T *		280 KB	20 KB			
MN103L23/ MN103L26	MN103LF26R *	128 pin	1048 KB	76 KB	-		128 pinLQFP (18mm × 18 mm/0.5mm pitch)
	MN103LF26Q *		792 KB				
	MN103LF23R *		1048 KB	64 KB			
	MN103LF23Q *		792 KB				
	MN103LF23N *		536 KB	40 KB			
	MN103LF23M *		408 KB	32 KB			
	MN103LF23K *		280 KB	20 KB			
	MN103LF26Z *		1048 KB	76 KB	Existence		
	MN103LF26Y *		792 KB				
	MN103LF23Z *		1048 KB	64 KB			
	MN103LF23Y *		792 KB				
	MN103LF23X *		536 KB	40 KB			
	MN103LF23W *		408 KB	32 KB			
	MN103LF23T *		280 KB	20 KB			
MN103L24/ MN103L27	MN103LF27R *	144 pin	1048 KB	76 KB	-		144 pinLQFP (20mm × 20 mm/0.5mm pitch)
	MN103LF27Q *		792 KB				
	MN103LF24R *		1048 KB	64 KB			
	MN103LF24Q *		792 KB				
	MN103LF24N *		536 KB	40 KB			
	MN103LF27Z *		1048 KB	76 KB	Existence		
	MN103LF27Y *		792 KB				
	MN103LF24Z *		1048 KB	64 KB			
	MN103LF24Y *		792 KB				
	MN103LF24X *		536 KB	40 KB			

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Series *1	Model	Pin Number	ROM Size	RAM Size *2	Sector swap *3	In-vehicle LAN	Package
MN103LB8/ MN103LC2	MN103LFC2R *	100 pin	1048KB	76KB	-	CAN/IEBus	100 pinLQFP (14mm × 14 mm/0.5mm pitch)
	MN103LFC2Q *		792KB				
	MN103LFB8N *		536KB	40KB			
	MN103LFB8M *		408KB	32KB			
	MN103LFB8K *		280KB	20KB			
	MN103LFC2Z *		1048KB	76KB	Existence		
	MN103LFC2Y *		792KB				
	MN103LFB8X *		536KB	40KB			
	MN103LFB8W *		408KB	32KB			
	MN103LFB8T *		280KB	20KB			
MN103LB9/ MN103LC3	MN103LFC3R *	128 pin	1048KB	76KB	-		128 pinLQFP (18mm × 18 mm/0.5mm pitch)
	MN103LFC3Q *		792KB				
	MN103LFB9N *		536KB	40KB			
	MN103LFB9M *		408KB	32KB			
	MN103LFB9K *		280KB	20KB			
	MN103LFC3Z *		1048KB	76KB	Existence		
	MN103LFC3Y *		792KB				
	MN103LFB9X *		536KB	40KB			
	MN103LFB9W *		408KB	32KB			
	MN103LFB9T *		280KB	20KB			
MN103L99/ MN103LC0	MN103LF99R *	144 pin	1048KB	76KB	-		144 pinLQFP (20mm × 20 mm/0.5mm pitch)
	MN103LF99Q *		792KB				
	MN103LFC0N *		536KB	40KB			
	MN103LFC0M *		408KB	32KB			
	MN103LFC0K *		280KB	20KB			
	MN103LF99Z *		1048KB	76KB	Existence		
	MN103LF99Y *		792KB				
	MN103LFC0X *		536KB	40KB			
	MN103LFC0W *		408KB	32KB			
	MN103LFC0T *		280KB	20KB			

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Series *1	Model	Pin Number	ROM Size	RAM Size *2	Sector swap *3	In-vehicle LAN	Package
MN103LA0/ MN103LA3	MN103LFA3R *	100 pin	1048KB	76KB	-	IEBus	100 pinLQFP (14mm × 14 mm/0.5mm pitch)
	MN103LFA3Q *		792KB				
	MN103LFA0R *		1048KB	64KB			
	MN103LFA0Q *		792KB				
	MN103LFA0N *		536KB	40KB			
	MN103LFA0M *		408KB	32KB			
	MN103LFA0K *		280KB	20KB			
	MN103LFA3Z *		1048KB	76KB	Existence		
	MN103LFA3Y *		792KB				
	MN103LFA0Z *		1048KB	64KB			
	MN103LFA0Y *		792KB				
	MN103LFA0X *		536KB	40KB			
	MN103LFA0W *		408KB	32KB			
	MN103LFA0T *		280KB	20KB			
MN103LA1/ MN103LA4	MN103LFA4R *	128 pin	1048KB	76KB	-		128 pinLQFP (18mm × 18 mm/0.5mm pitch)
	MN103LFA4Q *		792KB				
	MN103LFA1R *		1048KB	64KB			
	MN103LFA1Q *		792KB				
	MN103LFA1N *		536KB	40KB			
	MN103LFA1M *		408KB	32KB			
	MN103LFA1K *		280KB	20KB			
	MN103LFA4Z *		1048KB	76KB	Existence		
	MN103LFA4Y *		792KB				
	MN103LFA1Z *		1048KB	64KB			
	MN103LFA1Y *		792KB				
	MN103LFA1X *		536KB	40KB			
	MN103LFA1W *		408KB	32KB			
	MN103LFA1T *		280KB	20KB			
MN103LA2/ MN103LA5	MN103LFA5R *	144 pin	1048KB	76KB	-		144 pinLQFP (20mm × 20 mm/0.5mm pitch)
	MN103LFA5Q *		792KB				
	MN103LFA2R *		1048KB	64KB			
	MN103LFA2Q *		792KB				
	MN103LFA2N *		536KB	40KB			
	MN103LFA5Z *		1048KB	76KB	Existence		
	MN103LFA5Y *		792KB				
	MN103LFA2Z *		1048KB	64KB			
	MN103LFA2Y *		792KB				
	MN103LFA2X *		536KB	40KB			

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Series *1	Model	Pin Number	ROM Size	RAM Size *2	Sector swap *3	In-vehicle LAN	Package
MN103LA6/ MN103LA9	MN103LFA9R *	100 pin	1048KB	76KB	-	-	100 pinLQFP (14mm × 14 mm/0.5mm pitch)
	MN103LFA9Q *		792KB				
	MN103LFA6R *		1048KB	64KB			
	MN103LFA6Q *		792KB				
	MN103LFA6N *		536KB	40KB			
	MN103LFA6M *		408KB	32KB			
	MN103LFA6K *		280KB	20KB			
	MN103LFA9Z *		1048KB	76KB	Existence		
	MN103LFA9Y *		792KB				
	MN103LFA6Z *		1048KB	64KB			
	MN103LFA6Y *		792KB				
	MN103LFA6X *		536KB	40KB			
	MN103LFA6W *		408KB	32KB			
	MN103LFA6T *		280KB	20KB			
MN103LA7/ MN103LB0	MN103LFB0R *	128 pin	1048KB	76KB	-		128 pinLQFP (18mm × 18 mm/0.5mm pitch)
	MN103LFB0Q *		792KB				
	MN103LFA7R *		1048KB	64KB			
	MN103LFA7Q *		792KB				
	MN103LFA7N *		536KB	40KB			
	MN103LFA7M *		408KB	32KB			
	MN103LFA7K *		280KB	20KB			
	MN103LFB0Z *		1048KB	76KB	Existence		
	MN103LFB0Y *		792KB				
	MN103LFA7Z *		1048KB	64KB			
	MN103LFA7Y *		792KB				
	MN103LFA7X *		536KB	40KB			
	MN103LFA7W *		408KB	32KB			
	MN103LFA7T *		280KB	20KB			
MN103LA8/ MN103LB1	MN103LFB1R *	144 pin	1048KB	76KB	-		144 pinLQFP (20mm × 20 mm/0.5mm pitch)
	MN103LFB1Q *		792KB				
	MN103LFA8R *		1048KB	64KB			
	MN103LFA8Q *		792KB				
	MN103LFA8N *		536KB	40KB			
	MN103LFB1Z *		1048KB	76KB	Existence		
	MN103LFB1Y *		792KB				
	MN103LFA8Z *		1048KB	64KB			
	MN103LFA8Y *		792KB				
	MN103LFA8X *		536KB	40KB			

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Series *1	Model	Pin Number	ROM Size	RAM Size *2	Sector swap *3	In-vehicle LAN	Package
MN103LB2/ MN103LB5	MN103LFB5R *	100 pin	1048KB	76KB	-	CAN	100 pinLQFP (14mm × 14 mm/0.5mm pitch)
	MN103LFB5Q *		792KB				
	MN103LFB2R *		1048KB	64KB			
	MN103LFB2Q *		792KB				
	MN103LFB2N *		536KB	40KB			
	MN103LFB2M *		408KB	32KB			
	MN103LFB2K *		280KB	20KB			
	MN103LFB5Z *		1048KB	76KB	Existence		
	MN103LFB5Y *		792KB				
	MN103LFB2Z *		1048KB	64KB			
	MN103LFB2Y *		792KB				
	MN103LFB2X *		536KB	40KB			
	MN103LFB2W *		408KB	32KB			
	MN103LFB2T *		280KB	20KB			
MN103LB3/ MN103LB6	MN103LFB6R *	128 pin	1048KB	76KB	-		128 pinLQFP (18mm × 18 mm/0.5mm pitch)
	MN103LFB6Q *		792KB				
	MN103LFB3R *		1048KB	64KB			
	MN103LFB3Q *		792KB				
	MN103LFB3N *		536KB	40KB			
	MN103LFB3M *		408KB	32KB			
	MN103LFB3K *		280KB	20KB			
	MN103LFB6Z *		1048KB	76KB	Existence		
	MN103LFB6Y *		792KB				
	MN103LFB3Z *		1048KB	64KB			
	MN103LFB3Y *		792KB				
	MN103LFB3X *		536KB	40KB			
	MN103LFB3W *		408KB	32KB			
	MN103LFB3T *		280KB	20KB			
MN103LB4/ MN103LB7	MN103LFB7R *	144 pin	1048KB	76KB	-		144 pinLQFP (20mm × 20 mm/0.5mm pitch)
	MN103LFB7Q *		792KB				
	MN103LFB4R *		1048KB	64KB			
	MN103LFB4Q *		792KB				
	MN103LFB4N *		536KB	40KB			
	MN103LFB7Z *		1048KB	76KB	Existence		
	MN103LFB7Y *		792KB				
	MN103LFB4Z *		1048KB	64KB			
	MN103LFB4Y *		792KB				
	MN103LFB4X *		536KB	40KB			

*1 Refer to [Chapter Appendix] of LSI User's Manual.
*2 When using On-Chip Debug function, the debugger take over 500 Byte in size
*3 Refer to [Chapter Internal Flash Memory] of LSI User's Manul for details.
* Under development

There are the notes at DMA forced end that need to be applied only to MN103LF09/10/11/12/13/14/15/16/17/18/19/20/21/22/23/24/25/26/27/32/33 series. The notes do not need to apply in MN103LF99/A0/A1/A2/A3/A4/A5/A6/A7/A8/A9/B0/B1/B2/B3/B4/B5/B6/B7/B8/B9/C0/C2/C3 series. Refer to [Chapter DMA Controller] of LSI User's Manual about the notes.

1.3 Hardware Functions

CPU core

MN103L core (The instruction set is compatible MN103S series)

Memory space 4 GB (instruct/data common use)

LOAD-STORE architecture (3-stage pipeline)

Machine cycle

High-speed mode	25 ns/ 40 MHz (Max)
Low-speed mode	30.3 µs/ 33 kHz (Max)

Operation mode

NORMAL mode	(CPU clock operation, Peripheral circuit clock operation mode)
SLOW mode	(CPU clock operation, Peripheral circuit clock operation mode)
HALT mode	(CPU clock stop, Peripheral circuit clock operation mode)
STOP mode	(All clocks stop mode)

Clock oscillation circuit : 5 circuits

External high-speed oscillation (clkosc)	: Crystal oscillator/ Ceramic oscillator
	: 4 MHz to 20 MHz
External low-speed oscillation (clkx)	: Crystal oscillator/ Ceramic oscillator
	: 32.768 kHz
Internal high-speed oscillation (clkrc)	: 20 MHz
Internal low-speed oscillation (clkrcx)	: 30 kHz
PLL output (clkpll)	: 60 MHz to 120 MHz

Clock multiple circuit (PLL)

Multiplication rate:	4, 6, 8, 10, 12, 16, 20 multiplied clock of clkoscsel
	2440 to 3660 multiplied clock of clkx
Clock dividing	2, 3 divided of clkpll
PLL output dividing clock:	20 MHz to 40 MHz (clkplldiv)

Internal operation clock : 6 types

CPU clock (clkcpu)

Frequency : 40 MHz (Max)

Clock source : clkplldiv, clkosc, clkrc, clkx

Clock dividing : 1, 2, 4, 8, 16, 32, 64 divided of clock source

Peripheral bus clock (clkbus)

Frequency : 20 MHz (Max)

Clock source : clkplldiv, clkosc, clkrc, clkx

Clock dividing : 2, 4, 8, 16, 32, 64, 128 divided of clock source

(This setting is independent from the dividing clock setting of clkcpu.

Set the frequency of clkbus to less than clkcpu.)

Peripheral high-speed clock (clksp)

Frequency : 22 MHz (Max)

Clock source : clkrc, clkosc, clkplldiv

Clock dividing : 1, 2, 4, 8, 16 divided of clock source

High-speed oscillation clock (clkoscsel)

Frequency : 22 MHz (Max)

Clock source : clkrc, clkosc

Internal low-speed oscillation clock (clkrcx)

Frequency : 33 kHz (Max)

Low-speed oscillation clock (clksx)

Frequency : 33 kHz (Max)

Clock source : clkrcx, clkxsel

External bus interface

Bus area : 2 MB × 2 banks

Data bus : 8/ 16 bits

DMA Controller

Transfer area : Internal ROM space / Internal RAM space / Internal I/O area / External memory space
⇔ Internal ROM space / Internal RAM space / Internal I/O area / External memory space

Channel : 4 ch

Transfer form : 2 bus cycles transfer

Transfer requests

MN103LF09/32/33/99/B8/B9/C0/C2/C3 series: 75 types
(External interrupts:4, Timer:30, Serial I/F:33, IIC: 3,
A/D converter:1, CAN controller:1, IEBus controller:2, Software:1)

MN103LF10/11/12/13/14/15/A0/A1/A2/A3/A4/A5 series: 74 types
(External interrupts:4, Timer:30, Serial I/F:33, IIC: 3,
A/D converter:1, IEBus controller:2, Software:1)

MN103LF22/23/24/25/26/27/B2/B3/B4/B5/B6/B7 series: 73 types
(External interrupts:4, Timer:30, Serial I/F:33, IIC: 3,
A/D converter:1, CAN controller:1, Software:1)

MN103LF16/17/18/19/20/21/A6/A7/A8/A9/B0/B1 series: 72 types
(External interrupts:4, Timer:30, Serial I/F:33, IIC: 3,
A/D converter:1, Software:1)

Transfer modes: 3 modes (One word transfer / Burst transfer / Intermittent transfer)

Interrupt functions

Internal interrupts

MN103LF09/32/33/99/B8/B9/C0/C2/C3 series: 97 factors
(Timer:46, Serial I/F:22, IIC:6, Watchdog timer:1,
DMA:12, A/D converter:1, CAN controller: 1, LIN controller: 1,
IEBus controller: 4, Power Voltage Detection: 2, System error:1)

MN103LF10/11/12/13/14/15/A0/A1/A2/A3/A4/A5 series: 96 factors
(Timer:46, Serial I/F:22, IIC:6,
Watchdog timer:1, DMA:12, A/D converter:1, LIN controller: 1,
IEBus controller: 4, Power Voltage Detection: 2, System error:1)

MN103LF22/23/24/25/26/27/B2/B3/B4/B5/B6/B7 series: 93 factors
(Timer:46, Serial I/F:22, IIC:6, Watchdog timer:1,
DMA:12, A/D converter:1, CAN controller: 1, LIN controller: 1,
Power Voltage Detection: 2, System error:1)

MN103LF16/17/18/19/20/21/A6/A7/A8/A9/B0/B1 series: 92 factors
(Timer:46, Serial I/F:22, IIC:6,
Watchdog timer:1, DMA:12, A/D converter:1, LIN controller: 1,
Power Voltage Detection: 2, System error:1)

External interrupts: 11 factor
(IRQn pin(n=0 to 8) :9, NMIRQ pin(sharing pin with IRQ7 as an interrupt factors) :1,
Key input:1)

Watchdog Timer

Watchdog Timer

On detection of error, hardware reset is done inside the LSI
(Non-maskable interrupt is generated by the first watchdog time-out event, and hardware reset is done by a series of two time-out events)

Time-out cycle : CPU clock cycle × N (N = 2^{16}, 2^{18}, 2^{20}, 2^{27})

Watchdog Timer2

On detection of error, hardware reset is done inside the LSI
(Non-maskable interrupt is generated by the first watchdog time-out event, and hardware reset is done by a series of two time-out events)

Time-out cycle : Internal low-speed oscillation clock cycle × N
(N = 2^4, 2^5, 2^6, 2^7, 2^8, 2^9, 2^{10}, 2^{11}, 2^{12}, 2^{13}, 2^{14}, 2^{15})

Timer counter : 26 units

8-bit timer : 8 units

8-bit simple timer : 5 units

8-bit free-running timer : 1 unit

16-bit timer : 10 units

Motor control 16-bit timer : 1 unit

24H 8-bit timer : 1 unit

Timer 0 (8-bit timer)

Timer count (Up count), external event count, timer pulse output,
PWM output (Cycle is fixed), compare register with double buffer

Clock source : clksp, clksp/4, clksp/16, clksp/32, clksp/64, clksp/128,
clkbus/2, clkbus/4, clkbus/8, clksx, external clock

Timer 1 (8-bit timer)

Timer count (Up count), external event count, timer pulse output,
16-bit cascade connection (to timer 0), compare register with double buffer

Clock source : clksp, clksp/4, clksp/16, clksp/32, clksp/64, clksp/128,
clkbus/2, clkbus/4, clkbus/8, clksx, external clock

Timer 2 (8-bit timer)

Timer count (Up count), external event count, timer pulse output,
PWM output (Cycle is fixed), 24-bit cascade connection (to timer 0, timer 1),
compare register with double buffer

Clock source : clksp, clksp/4, clksp/16, clksp/32, clksp/64, clksp/128,
clkbus/2, clkbus/4, clkbus/8, clksx, external clock

Timer 3 (8-bit timer)

Timer count (Up count), external event count, timer pulse output,
16-bit cascade connection (to timer 2),
32-bit cascade connection (to timer 0, timer 1, timer 2),
compare register with double buffer

Clock source : clksp, clksp/4, clksp/16, clksp/32, clksp/64, clksp/128,
clkbus/2, clkbus/4, clkbus/8, clksx, external clock

Timer 4 (8-bit timer)

Timer count (Up count), external event count, timer pulse output,
PWM output (Cycle is fixed)

Clock source : clksp, clksp/4, clksp/16, clksp/32, clksp/64, clksp/128,
clkbus/2, clkbus/4, clkbus/8, clksx, external clock

Timer 20 (8-bit timer)

Timer count (Up count), external event count, timer pulse output,
PWM output (Cycle is fixed)

Clock source : clksp, clksp/4, clksp/16, clksp/32, clksp/64,
clkbus/2, clkbus/4, clksx, external clock

Timer 21 (8-bit timer)

Timer count (Up count), timer pulse output,
timer output for VFD

Clock source : clkbus/2, clkbus/4, clkbus/16, clkbus/32, clkbus/64, clkbus/128

Timer 22 (8-bit timer)

Timer count (Up count), external event count, timer pulse output,
PWM output (Cycle is fixed)

Clock source : clksp, clksp/4, clksp/16, clksp/32, clksp/64,
clkbus/2, clkbus/4, clksx, external clock

Timer 6 (8-bit free-running timer)

Clock source : clksp, clkbus, clksx, clksp/2^{12}, clksp/2^{13}, clksx/2^{12}, clksx/2^{13}

Timer 7 (16-bit timer)

Timer count (Up count), external event count, timer pulse output,
PWM output (cycle/duty continuous changeable), input capture (1 system)

Clock source : clksp, clksp/2, clksp/4, clksp/16,
clkbus/2, clkbus/4, clkbus/16, external clock

Timer 8, 9, 10, 11, 12, 13, 14, 15, 16 (16-bit timer)

Timer count (Up count, Down count), external event count, timer pulse output,
PWM output (cycle/duty continuous changeable), input capture (2 system),
2 phases encoder

Clock source : clkbus, clkbus/8, timer 0 or 1 compare match cycle, external clock

Timer M (Motor control 16-bit timer)

Timer pulse output, external event count,
complementary 3 phases PWM output (triangular wave and saw-tooth wave output,
dead time insertion),
4 phases PWM output,
output control by external interrupt (Hi-Z output or output data is fixed)

Clock source: clksp, clkbus, external clock divided by 1, 2, 4 or 16

Timer A, B, C, D, E (8-bit simple timer)

Serial transfer base clock generation

Clock source : clksp, clksp/2, clksp/4, clksp/8, clksp/16, clksp/32,
clkbus/2, clkbus/4

24H Timer

Alarm function, Interval function

Clock source : clksx, clksp (Only when CPU stop)

Serial interface : 14 channels

UART/ Clock Synchronous : 11 channels

IIC : 3 channels

Serial 0 (UART / Clock Synchronous / LIN)

- UART
  Parity check, overrun error/frame error detection,
  Transfer size can be selected from 7 to 8 bits.

- Clock Synchronous
  The communication type can be selected from 2-ware or 3-wire.
  First tansfer bit can be selected from MSB or LSB.
  Arbitrary size of 2 to 8 bits are selectable.
  Continuous transmission, continuous reception, continuous transmission/reception are available.
  Synchronous edge selection of transfer clock.
  Maximum transfer rate: 3.3 Mbps

- LIN
  Operate in conjunction with Timer 0, 7 and 8.
  Master communication.
  Synch Break field transmission, Check sum arithmetic
  Slave communication
  Wake-up reception, Synch Break field reception, Synch field reception, Check sum arithmetic
  Error detection
  Check sum error, Bit error

Clock source: Baud Rate Timer B0 output, external clock

Serial 1, 2, 3, 4, 9, 10 (UART / Clock Synchronous)

- UART
  Parity check, overrun error/frame error detection,
  Transfer size can be selected from 7 to 8 bits.

- Clock Synchronous
  The communication type can be selected from 2-ware or 3-wire.
  First tansfer bit can be selected from MSB or LSB.
  Arbitrary size of 2 to 8 bits are selectable.
  Continuous transmission, continuous reception, continuous transmission/reception are available.
  Synchronous edge selection of transfer clock.
  Maximum transfer rate: 3.3 Mbps

  Clock source: Baud Rate Timer Bn output (n=1 to 4, 9, 10), external clock

Serial 5, 6, 7, 8 (UART / Clock Synchronous)

- UART
  Parity check, overrun error/frame error detection.
  Transfer size can be selected from 7 to 8 bits.

- Clock Synchronous
  The communication type can be selected from 2-ware or 3-wire.
  (Data input from SBO pin is prohibited)
  First tansfer bit can be selected from MSB or LSB.
  Arbitrary size of 7 to 8 bits are selectable.
  (When selection size is 7 bits, first transfer bit setting is LSB only.)
  Continuous transmission, continuous reception, continuous transmission/reception are available.
  Maximum transfer rate: 3.3 Mbps

  Clock source: Output of timer A, B, C, D, E divided by 2, 16.
  External clock

IIC 0, 1, 2 (Multi master IIC)

- Multi master IIC
  100 kHz/ 400 kHz communication is supported.
  7-bit, 10-bit slave address is settable.
  General call communication mode is supported.

Clock source : Baud Rate Timer BIn output (n=0 to 2), external clock

A/D converter

Resolution : 10 bit

Channel : 16 channels

Clock source : clkbus/2, clkbus/4, clkbus/8, clkbus/16, clksx × 2

D/A converter

Resolution : 10-bit

Unit : 2 units

Auto reset

Auto reset function can be selected ON/OFF

Power supply voltage detection circuit

Detection voltage can be set 2.6 V to 4.0 V by software

Clock monitoring function

Frequency error detection of external / PLL clock

Hardware reset or non-maskable interrupt generation can be selected by program when a frequency error is detected.

LED driver :8 sets

CAN controller (MN103LF09/22/23/24/25/26/27/32/33/99/B2/B3/B4/B5/B6/B7/B8/B9/C0/C2/C3 series only)

Channels	: 1 channel CAN 2.0B specification basis
Communication method	: NRZ (Non-Return to Zero)
Transmission line	: 2-wire serial communication
Communication channel	: Max 1 Mbps
Data length	: 0 to 8 byte
Message frame	: Standard frame and extended frame are supported (Standard frame format ID: 11 bits Extended frame format ID: 29 bits)
Buffer size	: 136-bit × 32 (transmission / reception)

IEBus (MN103LF09/10/11/12/13/14/15/32/33/99/A0/A1/A2/A3/A4/A5/B8/B9/C0/C2/C3 series only)

Channels	: 2 channels
Communication mode	: Select from mode1 and mode2
Driver/receiver	: External

Port function

MN103LF09/12/15/18/21/24/27/99/A2/A5/A8/B1/B4/B7/C0 series

I/O ports	: 130 pins
CMOS I/O	: 102 pins
Combination CMOS I/O and oscillation pin	: 4 pins
Combination CMOS I/O and Analog I/O	: 16 pins
Combination CMOS I/O and LED driver	: 8 pins
Special function pin	: 5 pins
Reset input pin (NRST) (software reset is available)	: 1 pin
A/D converter reference voltage input pin (VREFH)	: 1 pin
Capacity connect pin (VOUT18)	: 1 pin
Function contol pins (NOCDMOD, ATRST)	: 2 pins
Power pins	: 9 pins
Power supply pin(VDD50)	: 3 pins
GND pins (VSS)	: 4 pins
Analog power supply pin(AVDD)	: 1 pins
Analog GND pins (AVSS)	: 1 pins

MN103LF11/14/17/20/23/26/33/A1/A4/A7/B0/B3/B6/B9/C3 series

I/O ports	: 115 pins
CMOS I/O	: 87 pins
Combination CMOS I/O and oscillation pin	: 4 pins
Combination CMOS I/O and Analog I/O	: 16 pins
Combination CMOS I/O and LED driver	: 8 pins
Special function pin	: 5 pins
Reset input pin (NRST) (software reset is available)	: 1 pin
A/D converter reference voltage input pin (VREFH)	: 1 pin
Capacity connect pin (VOUT18)	: 1 pin
Function contol pins (NOCDMOD, ATRST)	: 2 pins
Power pins	: 8 pins
Power supply pin(VDD50)	: 2 pins
GND pins (VSS)	: 4 pins
Analog power supply pin(AVDD)	: 1 pins
Analog GND pins (AVSS)	: 1 pins

MN103LF10/13/16/19/22/25/32/A0/A3/A6/A9/B2/B5/B8/C2 series

I/O ports	: 87 pins
CMOS I/O	: 59 pins
Combination CMOS I/O and oscillation pin	: 4 pins
Combination CMOS I/O and Analog I/O	: 16 pins
Combination CMOS I/O and LED driver	: 8 pins
Special function pin	: 5 pins
Reset input pin (NRST) (software reset is available)	: 1 pin
A/D converter reference voltage input pin (VREFH)	: 1 pin
Capacity connect pin (VOUT18)	: 1 pin
Function contol pins (NOCDMOD, ATRST)	: 2 pins
Power pins	: 8 pins
Power supply pin(VDD50)	: 2 pins
GND pins (VSS)	: 4 pins
Analog power supply pin(AVDD)	: 1 pins
Analog GND pins (AVSS)	: 1 pins

Package

MN103LF09/12/15/18/21/24/27/99/A2/A5/A8/B1/B4/B7/C0 series
: 144pin LQFP (20 mm × 20 mm / 0.5 mm pitch, halogen free)

MN103LF11/14/17/20/23/26/33/A1/A4/A7/B0/B3/B6/B9/C3 series
: 128pin LQFP (18 mm × 18 mm / 0.5 mm pitch, halogen free)

MN103LF10/13/16/19/22/25/32/A0/A3/A6/A9/B2/B5/B8/C2 series
: 100pin LQFP (14 mm × 14 mm / 0.5 mm pitch, halogen free)

MN103LF16N/M/K/X/W/T: 100pin QFP (18 mm × 18 mm / 0.65 mm pitch)

Panasonic's "halogen free" semiconductor products refer to the products made of molding resin and interposer which conform to the following standards.

- Bromine : 900 ppm (Maximum Concentration Value)
- Chlorine : 900 ppm (Maximum Concentration Value)
- Bromine + Chlorine : 1500 ppm (Maximum Concentration Value)

The above-mentioned standards are based on the numerical value described in IEC61249-2-21.
Antimony and its compounds are not added intentionally.

Power supply voltage

VDD50 : 2.2 V to 5.5 V

AVDD : AVDD=VDD50 (A/D converter or D/A converter is not used)
AVDD=VDD50≥2.7 V (A/D converter or D/A converter is used)

Operating temperature

-40 °C to +105 °C

1.4 Block Diagram

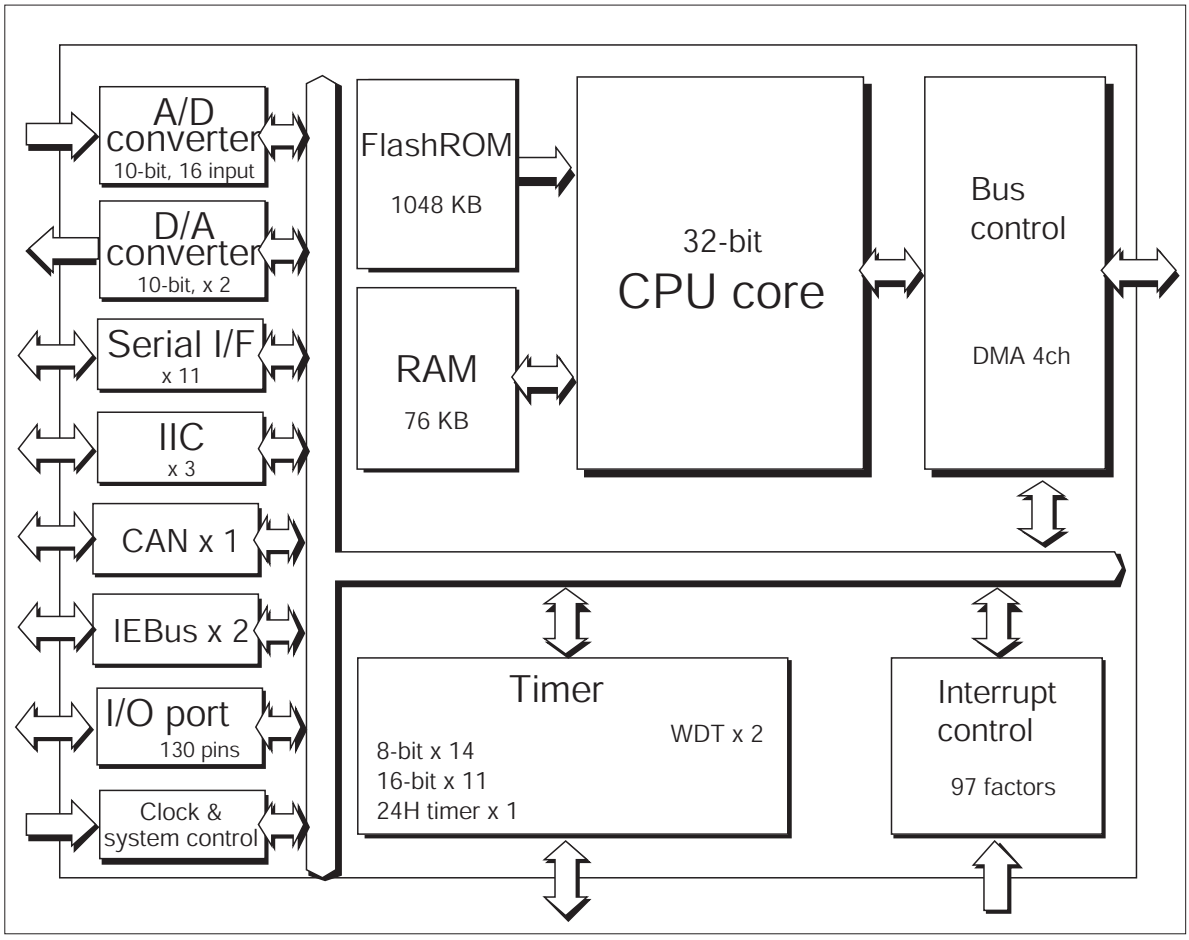

Figure:1.4.1 MN103LF09 Series Block Diagram

Functions in Figure:1.4.1 are different for each series. Refer to [1.3 Hardware Functions] for detail of each series.

1.5 Pin Specification

1.5.1 Pin Configuration

Figure:1.5.1 shows pin configuration of 144 pin version. Figure:1.5.2 shows pin configuration of 128 pin version. Figure:1.5.3 shows pin configuration of 100 pin version.
Table:1.5.1 shows pin specification of 144 pin version. Table:1.5.2 shows pin specification of 128 pin version. Table:1.5.3 shows pin specification of 100 pin version.

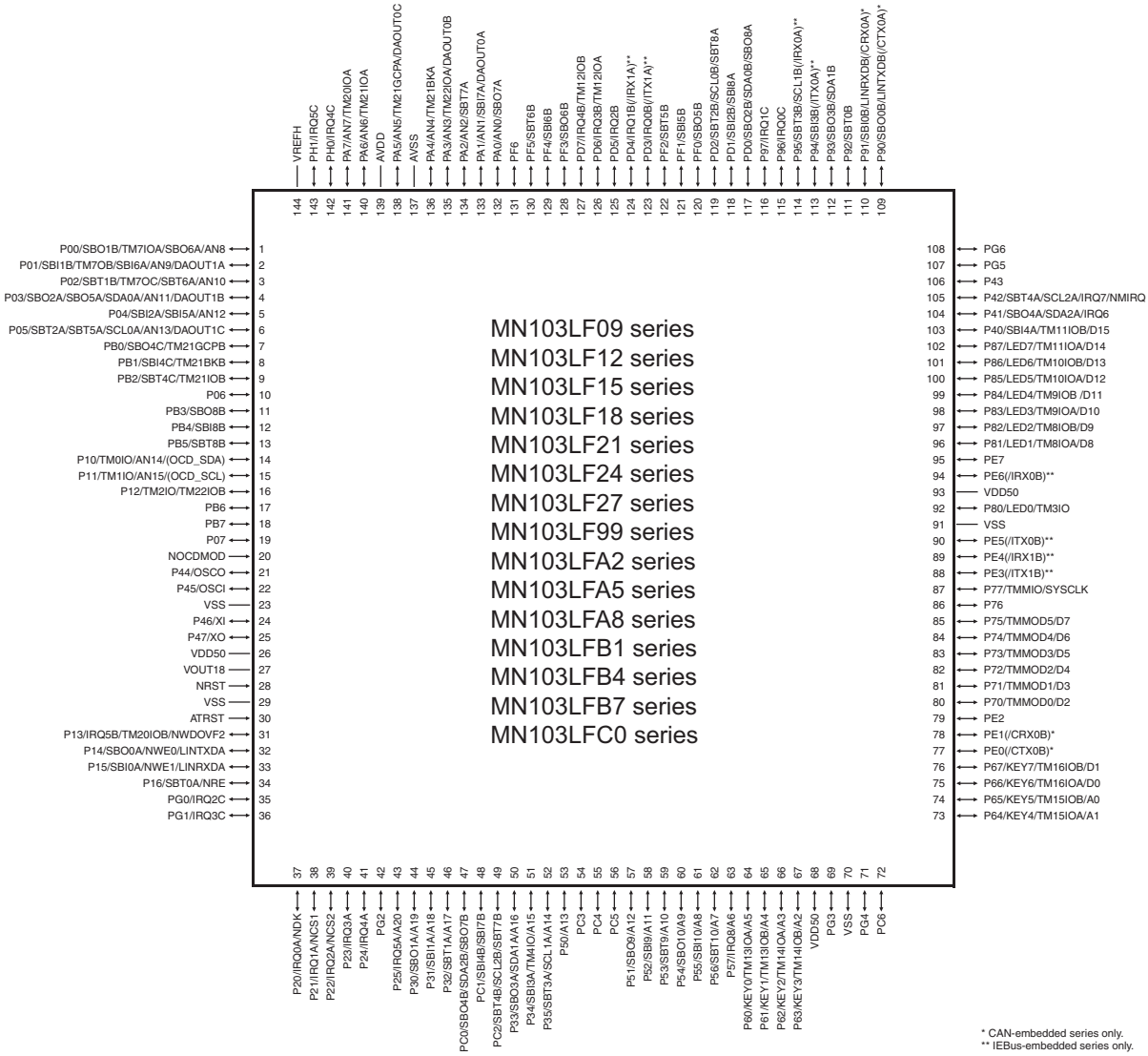

Figure:1.5.1 Pin Configuration of 144 pin Version

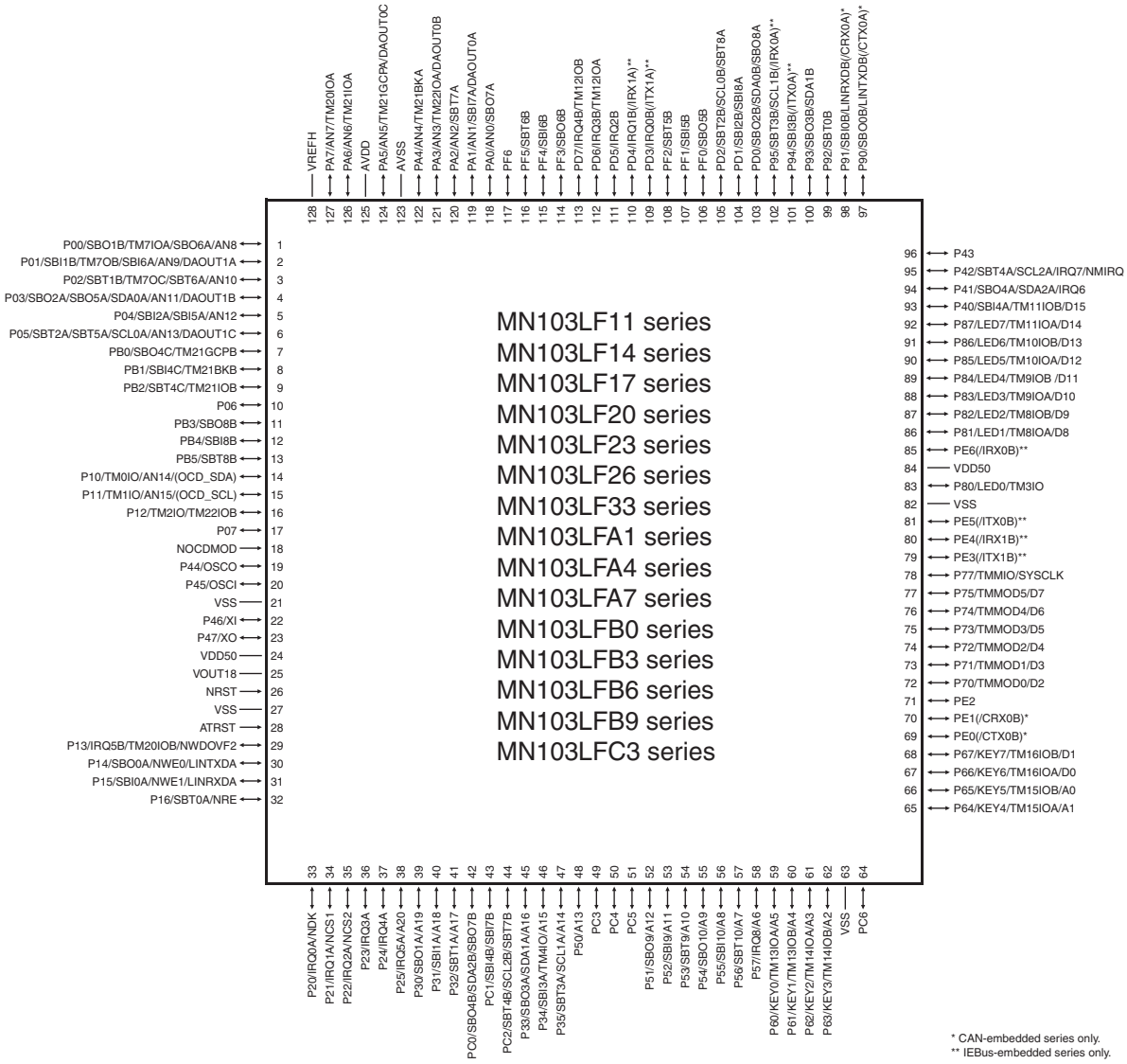

Figure:1.5.2 Pin Configuration of 128 pin Version

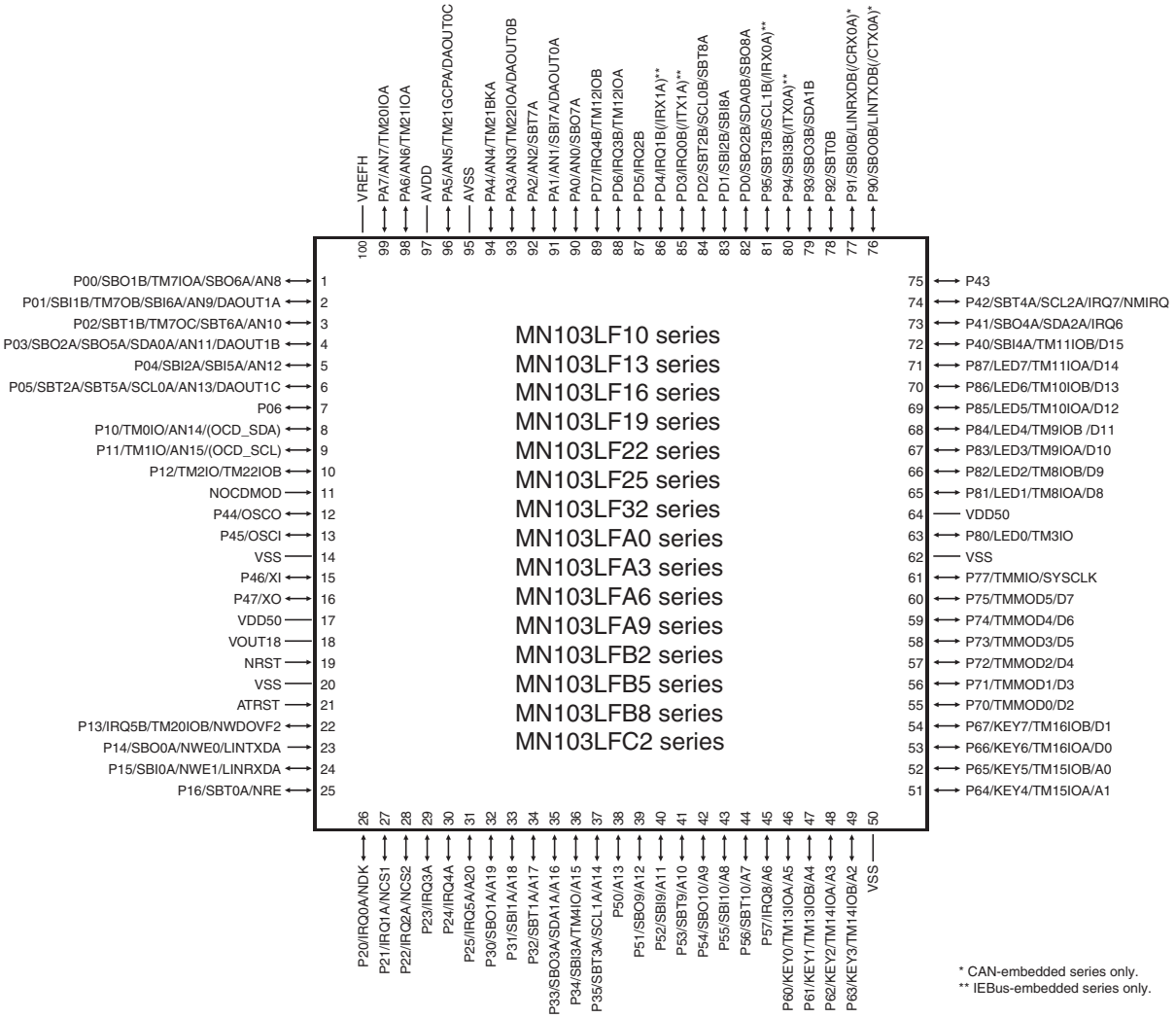

Figure:1.5.3 Pin Configuration of 100 pin Version

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Table:1.5.1 Pin Specification of 144 pin Version

Pin No.	Pin Name	Pin condition at Reset
1	P00 / SBO1B / TM7IOA / SBO6A / AN8	Hi-Z
2	P01 / SBI1B / TM7OB / SBI6A / AN9 / DAOUT1A	Hi-Z
3	P02 / SBT1B / SBT6A / TM7OC / AN10	Hi-Z
4	P03 / SBO2A / SDA0A / SBO5A / AN11/ DAOUT1B	Hi-Z
5	P04 / SBI2A / SBI5A / AN12	Hi-Z
6	P05 / SBT2A / SCL0A / SBT5A / AN13/ DAOUT1C	Hi-Z
7	PB0 / SBO4C / TM21GCPB	Hi-Z
8	PB1 / SBI4C / TM21BKB	Hi-Z
9	PB2 / SBT4C / TM21IOB	Hi-Z
10	P06	Hi-Z
11	PB3 / SBO8B	Hi-Z
12	PB4 / SBI8B	Hi-Z
13	PB5 / SBT8B	Hi-Z
14	P10 / TM0IO / AN14 / (OCD_SDA)	(*1)
15	P11 / TM1IO / AN15 / (OCD_SCL)	(*1)
16	P12 / TM2IO / TM22IOB	Hi-Z
17	PB6	Hi-Z
18	PB7	Hi-Z
19	P07	Hi-Z
20	NOCDMOD	INPUT
21	OSCO / P44	Hi-Z
22	OSCI / P45	Hi-Z
23	VSS	-
24	XI / P46	Hi-Z
25	XO / P47	Hi-Z
26	VDD50	-
27	VOUT18	-
28	NRST	INPUT
29	VSS	-
30	ATRST	INPUT
31	P13 / IRQ5B / TM20IOB / NWDOVF2	Hi-Z
32	P14 / SBO0A / NWE0/LINTXDA	Hi-Z
33	P15 / SBI0A / NWE1/LINRXDA	Hi-Z
34	P16 / SBT0A / NRE	Hi-Z
35	PG0 / IRQ2C	Hi-Z
36	PG1 / IRQ3C	Hi-Z
37	P20 / IRQ0A / NDK	Hi-Z
38	P21 / IRQ1A / NCS1	Hi-Z
39	P22 / IRQ2A / NCS2	Hi-Z
40	P23 / IRQ3A	Hi-Z
41	P24 / IRQ4A	Hi-Z
42	PG2	Hi-Z
43	P25 / IRQ5A / A20	Hi-Z
44	P30 / SBO1A / A19	Hi-Z
45	P31 / SBI1A / A18	Hi-Z
46	P32 / SBT1A / A17	Hi-Z
47	PC0 / SBO4B / SDA2B / SBO7B	Hi-Z
48	PC1 / SBI4B / SBI7B	Hi-Z
49	PC2 / SBT4B / SCL2B / SBT7B	Hi-Z
50	P33 / SBO3A / SDA1A / A16	Hi-Z
51	P34 / SBI3A / TM4IO / A15	Hi-Z
52	P35 / SBT3A / SCL1A / A14	Hi-Z
53	P50 / A13	Hi-Z
54	PC3	Hi-Z
55	PC4	Hi-Z
56	PC5	Hi-Z
57	P51 / SBO9 / A12	Hi-Z
58	P52 / SBI9 / A11	Hi-Z
59	P53 / SBT9 / A10	Hi-Z
60	P54 / SBO10 / A9	Hi-Z
61	P55 / SBI10 / A8	Hi-Z
62	P56 / SBT10 / A7	Hi-Z
63	P57 / IRQ8 / A6	Hi-Z
64	P60 / KEY0 / TM13IOA / A5	Hi-Z
65	P61 / KEY1 / TM13IOB / A4	Hi-Z
66	P62 / KEY2 / TM14IOA / A3	Hi-Z
67	P63 / KEY3 / TM14IOB / A2	Hi-Z
68	VDD50	-
69	PG3	Hi-Z
70	VSS	-
71	PG4	Hi-Z
72	PC6	Hi-Z
73	P64 / KEY4 / TM15IOA / A1	Hi-Z
74	P65 / KEY5 / TM15IOB / A0	Hi-Z
75	P66 / KEY6 / TM16IOA / D0	Hi-Z
76	P67 / KEY7 / TM16IOB / D1	Hi-Z
77	PE0 (/ CTX0B) *2	Hi-Z
78	PE1 (/ CRX0B) *2	Hi-Z
79	PE2	Hi-Z
80	P70 / TMMOD0 / D2	Hi-Z
81	P71 / TMMOD1 / D3	Hi-Z
82	P72 / TMMOD2 / D4	Hi-Z
83	P73 / TMMOD3 / D5	Hi-Z
84	P74 / TMMOD4 / D6	Hi-Z
85	P75 / TMMOD5 / D7	Hi-Z
86	P76	Hi-Z
87	P77 / TMMIO / SYSCLK	Hi-Z
88	PE3 (/ ITX1B) *3	Hi-Z
89	PE4 (/ IRX1B) *3	Hi-Z
90	PE5 (/ ITX0B) *3	Hi-Z
91	VSS	-
92	P80 / LED0 / TM3IO	Hi-Z
93	VDD50	-
94	PE6 (/ IRX0B) *3	Hi-Z
95	PE7	Hi-Z
96	P81 / LED1 / TM8IOA / D8	Hi-Z
97	P82 / LED2 / TM8IOB / D9	Hi-Z
98	P83 / LED3 / TM9IOA / D10	Hi-Z
99	P84 / LED4 / TM9IOB / D11	Hi-Z
100	P85 / LED5 / TM10IOA / D12	Hi-Z
101	P86 / LED6 / TM10IOB / D13	Hi-Z
102	P87 / LED7 / TM11IOA / D14	Hi-Z
103	P40 / SBI4A / TM11IOB / D15	Hi-Z
104	P41 / SBO4A / SDA2A / IRQ6	Hi-Z
105	P42 / SBT4A / SCL2A / IRQ7 / NMIRQ	Hi-Z
106	P43	Hi-Z
107	PG5	Hi-Z
108	PG6	Hi-Z
109	P90 / SBO0B / LINTXDB (/ CTX0A) *2	Hi-Z
110	P91 / SBI0B / LINRXDB (/ CRX0A) *2	Hi-Z
111	P92 / SBT0B	Hi-Z
112	P93 / SBO3B / SDA1B	Hi-Z
113	P94 / SBI3B (/ ITX0A) *3	Hi-Z
114	P95 / SBT3B / SCL1B (/ IRX0A) *3	Hi-Z
115	P96 / IRQ0C	Hi-Z
116	P97 / IRQ1C	Hi-Z
117	PD0 / SBO2B / SDA0B / SBO8A	Hi-Z
118	PD1 / SBI2B / SBI8A	Hi-Z
119	PD2 / SBT2B / SCL0B / SBT8A	Hi-Z
120	PF0 / SBO5B	Hi-Z
121	PF1 / SBI5B	Hi-Z
122	PF2 / SBT5B	Hi-Z
123	PD3 / IRQ0B (/ ITX1A) *3	Hi-Z
124	PD4 / IRQ1B (/ IRX1A) *3	Hi-Z
125	PD5 / IRQ2B	Hi-Z
126	PD6 / IRQ3B / TM12IOA	Hi-Z
127	PD7 / IRQ4B / TM12IOB	Hi-Z
128	PF3 / SBO6B	Hi-Z
129	PF4 / SBI6B	Hi-Z
130	PF5 / SBT6B	Hi-Z
131	PF6	Hi-Z
132	PA0 / AN0 / SBO7A	Hi-Z
133	PA1 / AN1 / SBI7A/ DAOUT0A	Hi-Z
134	PA2 / AN2 / SBT7A	Hi-Z
135	PA3 / AN3 / TM22IOA/ DAOUT0B	Hi-Z
136	PA4 / AN4 / TM21BKA	Hi-Z
137	AVSS	-
138	PA5 / AN5 / TM21GCPA/ DAOUT0C	Hi-Z
139	AVDD	-
140	PA6 / AN6 / TM21IOA	Hi-Z
141	PA7 / AN7 / TM20IOA	Hi-Z
142	PH0 / IRQ4C	Hi-Z
143	PH1 / IRQ5C	Hi-Z
144	VREFH	-

*1 When NOCDMOD is "H", state is "Hi-Z". When NOCDMOD is "L", state is "INPUT".
*2 CAN-embedded series only..
*3 IEBus-embedded series only..

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Table:1.5.2 Pin Specification of 128 pin Version

Pin No.	Pin Name	Pin condition at Reset
1	P00 / SBO1B / TM7IOA / SBO6A / AN8	Hi-Z
2	P01 / SBI1B / TM7OB / SBI6A / AN9 / DAOUT1A	Hi-Z
3	P02 / SBT1B / SBT6A / TM7OC / AN10	Hi-Z
4	P03 / SBO2A / SDA0A / SBO5A / AN11/ DAOUT1B	Hi-Z
5	P04 / SBI2A / SBI5A / AN12	Hi-Z
6	P05 / SBT2A / SCL0A / SBT5A / AN13/ DAOUT1C	Hi-Z
7	PB0 / SBO4C / TM21GCPB	Hi-Z
8	PB1 / SBI4C / TM21BKB	Hi-Z
9	PB2 / SBT4C / TM21IOB	Hi-Z
10	P06	Hi-Z
11	PB3 / SBO8B	Hi-Z
12	PB4 / SBI8B	Hi-Z
13	PB5 / SBT8B	Hi-Z
14	P10 / TM0IO / AN14 / (OCD_SDA)	(*1)
15	P11 / TM1IO / AN15 / (OCD_SCL)	(*1)
16	P12 / TM2IO / TM22IOB	Hi-Z
17	P07	Hi-Z
18	NOCDMOD	INPUT
19	OSCO / P44	Hi-Z
20	OSCI / P45	Hi-Z
21	VSS	-
22	XI / P46	Hi-Z
23	XO / P47	Hi-Z
24	VDD50	-
25	VOUT18	-
26	NRST	INPUT
27	VSS	-
28	ATRST	INPUT
29	P13 / IRQ5B / TM20IOB / NWDOVF2	Hi-Z
30	P14 / SBO0A / NWE0 / LINTXDA	Hi-Z
31	P15 / SBI0A / NWE1 / LINRXDA	Hi-Z
32	P16 / SBT0A / NRE	Hi-Z
33	P20 / IRQ0A / NDK	Hi-Z
34	P21 / IRQ1A / NCS1	Hi-Z
35	P22 / IRQ2A / NCS2	Hi-Z
36	P23 / IRQ3A	Hi-Z
37	P24 / IRQ4A	Hi-Z
38	P25 / IRQ5A / A20	Hi-Z
39	P30 / SBO1A / A19	Hi-Z
40	P31 / SBI1A / A18	Hi-Z
41	P32 / SBT1A / A17	Hi-Z
42	PC0 / SBO4B / SDA2B / SBO7B	Hi-Z
43	PC1 / SBI4B / SBI7B	Hi-Z
44	PC2 / SBT4B / SCL2B / SBT7B	Hi-Z
45	P33 / SBO3A / SDA1A / A16	Hi-Z
46	P34 / SBI3A / TM4IO / A15	Hi-Z
47	P35 / SBT3A / SCL1A / A14	Hi-Z
48	P50 / A13	Hi-Z
49	PC3	Hi-Z
50	PC4	Hi-Z
51	PC5	Hi-Z
52	P51 / SBO9 / A12	Hi-Z
53	P52 / SBI9 / A11	Hi-Z
54	P53 / SBT9 / A10	Hi-Z
55	P54 / SBO10 / A9	Hi-Z
56	P55 / SBI10 / A8	Hi-Z
57	P56 / SBT10 / A7	Hi-Z
58	P57 / IRQ8 / A6	Hi-Z
59	P60 / KEY0 / TM13IOA / A5	Hi-Z
60	P61 / KEY1 / TM13IOB / A4	Hi-Z
61	P62 / KEY2 / TM14IOA / A3	Hi-Z
62	P63 / KEY3 / TM14IOB / A2	Hi-Z
63	VSS	-
64	PC6	Hi-Z
65	P64 / KEY4 / TM15IOA / A1	Hi-Z
66	P65 / KEY5 / TM15IOB / A0	Hi-Z
67	P66 / KEY6 / TM16IOA / D0	Hi-Z
68	P67 / KEY7 / TM16IOB / D1	Hi-Z
69	PE0 (/ CTX0B) *2	Hi-Z
70	PE1 (/ CRX0B) *2	Hi-Z
71	PE2	Hi-Z
72	P70 / TMMOD0 / D2	Hi-Z
73	P71 / TMMOD1 / D3	Hi-Z
74	P72 / TMMOD2 / D4	Hi-Z
75	P73 / TMMOD3 / D5	Hi-Z
76	P74 / TMMOD4 / D6	Hi-Z
77	P75 / TMMOD5 / D7	Hi-Z
78	P77 / TMMIO / SYSCLK	Hi-Z
79	PE3 (/ ITX1B)*3	Hi-Z
80	PE4 (/ IRX1B)*3	Hi-Z
81	PE5 (/ ITX0B)*3	Hi-Z
82	VSS	-
83	P80 / LED0 / TM3IO	Hi-Z
84	VDD50	-
85	PE6 (/ IRX0B)*3	Hi-Z
86	P81 / LED1 / TM8IOA / D8	Hi-Z
87	P82 / LED2 / TM8IOB / D9	Hi-Z
88	P83 / LED3 / TM9IOA / D10	Hi-Z
89	P84 / LED4 / TM9IOB / D11	Hi-Z
90	P85 / LED5 / TM10IOA / D12	Hi-Z
91	P86 / LED6 / TM10IOB / D13	Hi-Z
92	P87 / LED7 / TM11IOA / D14	Hi-Z
93	P40 / SBI4A / TM11IOB / D15	Hi-Z
94	P41 / SBO4A / SDA2A / IRQ6	Hi-Z
95	P42 / SBT4A / SCL2A / IRQ7 / NMIRQ	Hi-Z
96	P43	Hi-Z
97	P90 / SBO0B / LINTXDB (/ CTX0A) *2	Hi-Z
98	P91 / SBI0B / LINRXDB (/ CRX0A) *2	Hi-Z
99	P92 / SBT0B	Hi-Z
100	P93 / SBO3B / SDA1B	Hi-Z
101	P94 / SBI3B (/ ITX0A)*3	Hi-Z
102	P95 / SBT3B / SCL1B (/ IRX0A)*3	Hi-Z
103	PD0 / SBO2B / SDA0B / SBO8A	Hi-Z
104	PD1 / SBI2B / SBI8A	Hi-Z
105	PD2 / SBT2B / SCL0B / SBT8A	Hi-Z
106	PF0 / SBO5B	Hi-Z
107	PF1 / SBI5B	Hi-Z
108	PF2 / SBT5B	Hi-Z
109	PD3 / IRQ0B (/ ITX1A)*3	Hi-Z
110	PD4 / IRQ1B (/ IRX1A)*3	Hi-Z
111	PD5 / IRQ2B	Hi-Z
112	PD6 / IRQ3B / TM12IOA	Hi-Z
113	PD7 / IRQ4B / TM12IOB	Hi-Z
114	PF3 / SBO6B	Hi-Z
115	PF4 / SBI6B	Hi-Z
116	PF5 / SBT6B	Hi-Z
117	PF6	Hi-Z
118	PA0 / AN0 / SBO7A	Hi-Z
119	PA1 / AN1 / SBI7A/ DAOUT0A	Hi-Z
120	PA2 / AN2 / SBT7A	Hi-Z
121	PA3 / AN3 / TM22IOA/ DAOUT0B	Hi-Z
122	PA4 / AN4 / TM21BKA	Hi-Z
123	AVSS	-
124	PA5 / AN5 / TM21GCPA/ DAOUT0C	Hi-Z
125	AVDD	-
126	PA6 / AN6 / TM21IOA	Hi-Z
127	PA7 / AN7 / TM20IOA	Hi-Z
128	VREFH	-

*1 When NOCDMOD is "H", state is "Hi-Z". When NOCDMOD is "L", state is "INPUT".
*2 CAN-embedded series only..
*3 IEBus-embedded series only..

Table:1.5.3 Pin Specification of 100 pin Version

Pin No.	Pin Name	Pin condition at Reset
1	P00 / SBO1B / TM7IOA / SBO6A / AN8	Hi-Z
2	P01 / SBI1B / TM7OB / SBI6A / AN9 / DAOUT1A	Hi-Z
3	P02 / SBT1B / TM7OC / SBT6A / AN10	Hi-Z
4	P03 / SBO2A / SBO5A / SDA0A / AN11/ DAOUT1B	Hi-Z
5	P04 / SBI2A / SBI5A / AN12	Hi-Z
6	P05 / SBT2A / SBT5A / SCL0A / AN13/ DAOUT1C	Hi-Z
7	P06	Hi-Z
8	P10 / TM0IO / AN14 / (OCD_SDA)	(*1)
9	P11 / TM1IO / AN15 / (OCD_SCL)	(*1)
10	P12 / TM2IO / TM22IOB	Hi-Z
11	NOCDMOD	INPUT
12	OSCO / P44	Hi-Z
13	OSCI / P45	Hi-Z
14	VSS	-
15	XI / P46	Hi-Z
16	XO / P47	Hi-Z
17	VDD50	-
18	VOUT18	-
19	NRST	INPUT
20	VSS	-
21	ATRST	INPUT
22	P13 / IRQ5B / TM20IOB / NWDOVF2	Hi-Z
23	P14 / SBO0A / NWE0 / LINTXDA	Hi-Z
24	P15 / SBI0A / NWE1 / LINRXDA	Hi-Z
25	P16 / SBT0A / NRE	Hi-Z
26	P20 / IRQ0A / NDK	Hi-Z
27	P21 / IRQ1A / NCS1	Hi-Z
28	P22 / IRQ2A / NCS2	Hi-Z
29	P23 / IRQ3A	Hi-Z
30	P24 / IRQ4A	Hi-Z
31	P25 / IRQ5A / A20	Hi-Z
32	P30 / SBO1A / A19	Hi-Z
33	P31 / SBI1A / A18	Hi-Z
34	P32 / SBT1A / A17	Hi-Z
35	P33 / SBO3A / SDA1A / A16	Hi-Z
36	P34 / SBI3A / TM4IO / A15	Hi-Z
37	P35 / SBT3A / SCL1A / A14	Hi-Z
38	P50 / A13	Hi-Z
39	P51 / SBO9 / A12	Hi-Z
40	P52 / SBI9 / A11	Hi-Z
41	P53 / SBT9 / A10	Hi-Z
42	P54 / SBO10 / A9	Hi-Z
43	P55 / SBI10 / A8	Hi-Z
44	P56 / SBT10 / A7	Hi-Z
45	P57 / IRQ8 / A6	Hi-Z
46	P60 / KEY0 / TM13IOA / A5	Hi-Z
47	P61 / KEY1 / TM13IOB / A4	Hi-Z
48	P62 / KEY2 / TM14IOA / A3	Hi-Z
49	P63 / KEY3 / TM14IOB / A2	Hi-Z
50	VSS	-
51	P64 / KEY4 / TM15IOA / A1	Hi-Z
52	P65 / KEY5 / TM15IOB / A0	Hi-Z
53	P66 / KEY6 / TM16IOA / D0	Hi-Z
54	P67 / KEY7 / TM16IOB / D1	Hi-Z
55	P70 / TMMOD0 / D2	Hi-Z
56	P71 / TMMOD1 / D3	Hi-Z
57	P72 / TMMOD2 / D4	Hi-Z
58	P73 / TMMOD3 / D5	Hi-Z
59	P74 / TMMOD4 / D6	Hi-Z
60	P75 / TMMOD5 / D7	Hi-Z
61	P77 / TMMIO / SYSCLK	Hi-Z
62	VSS	-
63	P80 / LED0 / TM3IO	Hi-Z
64	VDD50	-
65	P81 / LED1 / TM8IOA / D8	Hi-Z
66	P82 / LED2 / TM8IOB / D9	Hi-Z
67	P83 / LED3 / TM9IOA / D10	Hi-Z
68	P84 / LED4 / TM9IOB / D11	Hi-Z
69	P85 / LED5 / TM10IOA / D12	Hi-Z
70	P86 / LED6 / TM10IOB / D13	Hi-Z
71	P87 / LED7 / TM11IOA / D14	Hi-Z
72	P40 / SBI4A / TM11IOB / D15	Hi-Z
73	P41 / SBO4A / SDA2A / IRQ6	Hi-Z
74	P42 / SBT4A / SCL2A / IRQ7 / NMIRQ	Hi-Z
75	P43	Hi-Z
76	P90 / SBO0B / LINTXDB (/ CTX0A) *2	Hi-Z
77	P91 / SBI0B / LINRXDB (/ CRX0A) *2	Hi-Z
78	P92 / SBT0B	Hi-Z
79	P93 / SBO3B / SDA1B	Hi-Z
80	P94 / SBI3B (/ ITX0A) *3	Hi-Z
81	P95 / SBT3B / SCL1B (/ IRX0A) *3	Hi-Z
82	PD0 / SBO2B / SDA0B / SBO8A	Hi-Z
83	PD1 / SBI2B / SBI8A	Hi-Z
84	PD2 / SBT2B / SCL0B / SBT8A	Hi-Z
85	PD3 / IRQ0B (/ ITX1A) *3	Hi-Z
86	PD4 / IRQ1B (/ IRX1A) *3	Hi-Z
87	PD5 / IRQ2B	Hi-Z
88	PD6 / IRQ3B / TM12IOA	Hi-Z
89	PD7 / IRQ4B / TM12IOB	Hi-Z
90	PA0 / AN0 / SBO7A	Hi-Z
91	PA1 / AN1 / SBI7A / DAOUT0A	Hi-Z
92	PA2 / AN2 / SBT7A	Hi-Z
93	PA3 / AN3 / TM22IOA / DAOUT0B	Hi-Z
94	PA4 / AN4 / TM21BKA	Hi-Z
95	AVSS	-
96	PA5 / AN5 / TM21GCPA / DAOUT0C	Hi-Z
97	AVDD	-
98	PA6 / AN6 / TM21IOA	Hi-Z
99	PA7 / AN7 / TM20IOA	Hi-Z
100	VREFH	-

*1 When NOCDMOD is “H”, state is “Hi-Z”. When NOCDMOD is “L”, state is “INPUT”.
*2 CAN-embedded series only..
*3 IEBus-embedded series only..

1.5.2 Pin Functions

Table:1.5.4 shows pin functions of 144 pin version.

Table:1.5.4 Pin Functions of 144 pin Version

	Pin	Other Function					Description
Power supply / Ground *	VDD50						On-chip regulator power supply Power supply for I/O
	AVDD						Power supply for analog operation.
	VOUT18						Power supply for internal circuit.
	VREFH						Reference power supply pin for the A/D converter.
	AVSS						Ground pin for analog.
	VSS						Ground
Function control *	ATRST						Auto reset setting pin.
	NOCDMOD						On-chip debug function (OCD) control pin
Reset	NRST						Reset signal input pin (Active low)
Clock	OSCI	P45					High-speed oscillation input pin (clkosc) (4 to 20 MHz)
	OSCO	P44					High-speed oscillation output pin
	XI	P46					Low-speed oscillation input pin (clkx = 32.768 kHz)
	XO	P47					Low-speed oscillation output pin
	SYSCLK	P77	TMMIO				System clock signal output pin
Bus	A20	P25	IRQ5A				Address output pins at Memory expansion mode
	A19	P30	SBO1A				
	A18	P31	SBI1A				
	A17	P32	SBT1A				
	A16	P33	SBO3A	SDA1A			
	A15	P34	SBI3A	TM4IO			
	A14	P35	SBT3A	SCL11A			
	A13	P50					
	A12	P51	SBO9				
	A11	P52	SBI9				
	A10	P53	SBT9				
	A9	P54	SBO10				
	A8	P55	SBI10				
	A7	P56	SBT10				
	A6	P57	IRQ8				
	A5	P60	KEY0	TM13IOA			
	A4	P61	KEY1	TM13IOB			
	A3	P62	KEY2	TM14IOA			
	A2	P63	KEY3	TM14IOB			
	A1	P64	KEY4	TM15IOA			
	A0	P65	KEY5	TM15IOB			
	D15	P40	SBI4A	TM11IOB			Data I/O pins at Memory expansion mode
	D14	P87	LED7	TM11IOA			
	D13	P86	LED6	TM10IOB			
	D12	P85	LED5	TM10IOA			
	D11	P84	LED4	TM9IOB			
	D10	P83	LED3	TM9IOA			
	D9	P82	LED2	TM8IOB			
	D8	P81	LED1	TM8IOA			
	D7	P75	TMMOD5				
	D6	P74	TMMOD4				

Refer to [Chapter Overview] of LSI User's Manual for detail about note of VDD and function control pins.

	Pin	Other Function					Description
Bus	D5	P73	TMMOD3				Data I/O pins at Memory expansion mode
	D4	P72	TMMOD2				
	D3	P71	TMMOD1				
	D2	P70	TMMOD0				
	D1	P67	KEY7	TM16IOB			
	D0	P66	KEY6	TM16IOA			
	NCS2	P22	IRQ2A				Chip select signal output pins (Active low)
	NCS1	P21	IRQ1A				
	NRE	P16	SBT0A				Read enable signal output pin (Active low)
	NWE1	P15	SBI0A	LINRXDA			Write enable signal output pins (Active low)
	NWE0	P14	SBO0A	LINTXDA			
	NDK	P20	IRQ0A				Acknowledge signal input pin (Active low)
Watchdog timer 2	NWDOVF2	P13	IRQ5B	TM20IOB			Watchdog timer 2 over flow (active low)
Interrupt	NMIRQ	P42	IRQ7	SBT4A	SCL2A		Non-maskable interrupt request signal input pin (Active low)
	IRQ8	P57	A6				External interrupt request signal input pin 8
	IRQ7	P42	NMIRQ	SBT4A	SCL2A		External interrupt request signal input pin 7
	IRQ6	P41	SBO4A	SDA2A			External interrupt request signal input pin 6
	IRQ5A	P25	A20				External interrupt request signal input pin 5 (Pin change is possible)
	IRQ5B	P13	TM20IOB	NWDOVF2			
	IRQ5C	PH1					
	IRQ4A	P24					External interrupt request signal input pin 4 (Pin change is possible)
	IRQ4B	PD7	TM12IOB				
	IRQ4C	PH0					
	IRQ3A	P23					External interrupt request signal input pin 3 (Pin change is possible)
	IRQ3B	PD6	TM12IOA				
	IRQ3C	PG1					
	IRQ2A	P22	NCS2				External interrupt request signal input pin 2 (Pin change is possible)
	IRQ2B	PD5					
	IRQ2C	PG0					
	IRQ1A	P21	NCS1				External interrupt request signal input pin 1 (Pin change is possible)
	IRQ1B	PD4	(IRX1A)**				
	IRQ1C	P97					
	IRQ0A	P20	NDK				External interrupt request signal input pin 0 (Pin change is possible)
	IRQ0B	PD3	(ITX1A)**				
	IRQ0C	P96					
	KEY7	P67	D1	TM16IOB			Key input interrupt
	KEY6	P66	D0	TM16IOA			
	KEY5	P65	A0	TM15IOB			
	KEY4	P64	A1	TM15IOA			
	KEY3	P63	A2	TM14IOB			
	KEY2	P62	A3	TM14IOA			
	KEY1	P61	A4	TM13IOB			
	KEY0	P60	A5	TM13IOA			
Timer	TM0IO	P10	OCD_SDA	AN14			8-bit Timer 0 to 4 I/O pins
	TM1IO	P11	OCD_SCL	AN15			
	TM2IO	P12	TM22IOB				
	TM3IO	P80	LED0				
	TM4IO	P34	A15	SBI3A			
	TM7IOA	P00	SBO1B	SBO6A	AN8		16-bit Timer 7 I/O pin A, output pin B, C
	TM7OB	P01	SBI1B	SBI6A	AN9	DAOUT1A	
	TM7OC	P02	SBT1B	SBT6A	AN10		

* CAN-embedded series only.
** IEBus-embedded series only.

	Pin	Other Function					Description
Timer	TM8IOA	P81	D8	LED1			16-bit Timer 8 to 16 I/O pins A, B
	TM8IOB	P82	D9	LED2			
	TM9IOA	P83	D10	LED3			
	TM9IOB	P84	D11	LED4			
	TM10IOA	P85	D12	LED5			
	TM10IOB	P86	D13	LED6			
	TM11IOA	P87	D14	LED7			
	TM11IOB	P40	D15	SBI4A			
	TM12IOA	PD6	IRQ3B				
	TM12IOB	PD7	IRQ4B				
	TM13IOA	P60	KEY0	A5			
	TM13IOB	P61	KEY1	A4			
	TM14IOA	P62	KEY2	A3			
	TM14IOB	P63	KEY3	A2			
	TM15IOA	P64	KEY4	A1			
	TM15IOB	P65	KEY5	A0			
	TM16IOA	P66	KEY6	D0			
	TM16IOB	P67	KEY7	D1			
	TM20IOA	PA7	AN7				8-bit Timer 20 to 22 I/O pins (Pin change is possible)
	TM20IOB	P13	IRQ5B	NWDOVF2			
	TM21IOA	PA6	AN6				
	TM21IOB	PB2	SBT4C				
	TM22IOA	PA3	AN3	DAOUT0B			
	TM22IOB	P12	TM2IO				
	TM21BKA	PA4	AN4				8-bit Timer 21 I/O pins (Pin change is possible)
	TM21BKB	PB1	SBI4C				
	TM21GCPA	PA5	AN5	DAOUT0C			
	TM21GCPB	PB0	SBO4C				
	TMMOD0	P70	D2				Motor control 16-bit Timer I/O pins
	TMMOD1	P71	D3				
	TMMOD2	P72	D4				
	TMMOD3	P73	D5				
	TMMOD4	P74	D6				
	TMMOD5	P75	D7				
	TMMIO	P77	SYSCLK				
Serial	SBT0A	P16	NRE				Serial clock I/O pins (Pin change is possible) - Clock synchronous/UART
	SBT0B	P92					
	SBT1A	P32	A17				
	SBT1B	P02	SBT6A	TM7OC	AN10		
	SBT2A	P05	SBT5A	SCL0A	AN13	DAOUT1C	
	SBT2B	PD2	SBT8A	SCL0B			
	SBT3A	P35	A14	SCL1A			
	SBT3B	P95	SCL1B	(IRX0A)**			
	SBT4A	P42	SCL2A	IRQ7	NMIRQ		
	SBT4B	PC2	SBT7B	SCL2B			
	SBT4C	PB2	TM21IOB				
	SBT5A	P05	SBT2A	SCL0A	AN13	DAOUT1C	
	SBT5B	PF2					
	SBT6A	P02	SBT1B	TM7OC	AN10		
	SBT6B	PF5					
	SBT7A	PA2	AN2				
	SBT7B	PC2	SBT4B	SCL2B			
	SBT8A	PD2	SBT2B	SCL0B			
	SBT8B	PB5					
	SBT9	P53					
	SBT10	P56					

* CAN-embedded series only.
** IEBus-embedded series only.

	Pin	Other Function					Description
Serial	SBO0A	P14	NWE0	LINTXDA			Serial data output pins (Pin change is possible) - Clock synchronous/UART
	SBO0B	P90	(CTX0A)*	LINTXDB			
	SBO1A	P30	A19				
	SBO1B	P00	SBO6A	TM7IOA	AN8		
	SBO2A	P03	SBO5A	SDA0A	AN11	DAOUT1B	
	SBO2B	PD0	SBO8A	SDA0B			
	SBO3A	P33	A16	SDA1A			
	SBO3B	P93	SDA1B				
	SBO4A	P41	SDA2A	IRQ6			
	SBO4B	PC0	SBO7B	SDA2B			
	SBO4C	PB0	TM21GCPB				
	SBO5A	P03	SBO2A	SDA0A	AN11	DAOUT1B	
	SBO5B	PF0					
	SBO6A	P00	SBO1B	TM7IOA	AN8		
	SBO6B	PF3					
	SBO7A	PA0	AN0				
	SBO7B	PC0	SBO4B	SDA2B			
	SBO8A	PD0	SBO2B	SDA0B			
	SBO8B	PB3					
	SBO9	P51	A12				
	SBO10	P54	A9				
	SBI0A	P15	NWE1	LINRXDA			Serial data input pins (Pin change is possible) - Clock synchronous/UART
	SBI0B	P91	(CRX0A)*	LINRXDB			
	SBI1A	P31	A18				
	SBI1B	P01	SBI6A	TM7OB	AN9	DAOUT1A	
	SBI2A	P04	SBI5A	AN12			
	SBI2B	PD1	SBI8A				
	SBI3A	P34	A15	TM4IO			
	SBI3B	P94	(ITX0A)**				
	SBI4A	P40	D15	TM11IOB			
	SBI4B	PC1	SBI7B				
	SBI4C	PB1	TM21BKB				
	SBI5A	P04	SBI2A	AN12			
	SBI5B	PF1					
	SBI6A	P01	SBI1B	TM7OB	AN9	DAOUT1A	
	SBI6B	PF4					
	SBI7A	PA1	AN1	DAOUT0A			
	SBI7B	PC1	SBI4B				
	SBI8A	PD1	SBI2B				
	SBI8B	PB4					
	SBI9	P52	A11				
	SBI10	P55	A8				
IIC	SCL0A	P05	SBT2A	SBT5A	AN13	DAOUT1C	IIC clock I/O pins (Pin change is possible)
	SCL0B	PD2	SBT2B	SBT8A			
	SCL1A	P35	A14	SBT3A			
	SCL1B	P95	SBT3B	(IRX0A)**			
	SCL2A	P42	SBT4A	IRQ7	NMIRQ		
	SCL2B	PC2	SBT4B	SBT7B			
	SDA0A	P03	SBO2A	SBO5A	AN11	DAOUT1B	IIC data I/O pins (Pin change is possible)
	SDA0B	PD0	SBO2B	SBO8A			
	SDA1A	P33	A16	SBO3A			
	SDA1B	P93	SBO3B				
	SDA2A	P41	SBO4A	IRQ6			
	SDA2B	PC0	SBO4B	SBO7B			

* CAN-embedded series only.
** IEBus-embedded series only.

	Pin	Other Function					Description
LIN	LINTXDA	P14	SBO0A	NWE0			LIN data transmission pin (Pin change is possible)
	LINTXDB	P90	SBO0B	(CTX0A) *			
	LINRXDA	P15	SBI0A	NWE1			LIN data reception pin (Pin change is possible)
	LINRXDB	P91	SBI0B	(CRX0A) *			
CAN *	CTX0A	P90	SBO0B	LINTXDB			CAN data transmission pin (Pin change is possible)
	CTX0B	PE0					
	CRX0A	P91	SBI0B	LINRXDB			CAN data reception pin (Pin change is possible)
	CRX0B	PE1					
IEBus **	ITX0A	P94	SBI3B				IEBus data transmission pin (Pin change is possible)
	ITX0B	PE5					
	ITX1A	PD3	IRQ0B				
	ITX1B	PE3					
	IRX0A	P95	SBT3B	SCL1B			IEBus data reception pin (Pin change is possible)
	IRX0B	PE6					
	IRX1A	PD4	IRQ1B				
	IRX1B	PE4					
A/D converter	AN0	PA0	SBO7A				Analog input pins
	AN1	PA1	SBI7A	DAOUT0A			
	AN2	PA2	SBT7A				
	AN3	PA3	TM22IOA	DAOUT0B			
	AN4	PA4	TM21BKA				
	AN5	PA5	TM21GCPA	DAOUT0C			
	AN6	PA6	TM21IOA				
	AN7	PA7	TM20IOA				
	AN8	P00	SBO1B	TM7IOA	SBO6A		
	AN9	P01	SBI1B	TM7OB	SBI6A	DAOUT1A	
	AN10	P02	SBT1B	TM7OC	SBT6A		
	AN11	P03	SBO2A	SBO5A	SDA0A	DAOUT1B	
	AN12	P04	SBI2A	SBI5A			
	AN13	P05	SBT2A	SBT5A	SCL0A	DAOUT1C	
	AN14	P10	TM0IO	OCD_SDA			
	AN15	P11	TM1IO	OCD_SCL			
D/A converter	DAOUT0A	PA1	SBI7A	AN1			Analog output pins
	DAOUT0B	PA3	TM22IOA	AN3			
	DAOUT0C	PA5	TM21GCPA	AN5			
	DAOUT1A	P01	SBI1B	TM7OB	SBI6A	AN9	
	DAOUT1B	P03	SBO2A	SBO5A	SDA0A	AN11	
	DAOUT1C	P05	SBT2A	SBT5A	SCL0A	AN13	
I/O Port	P00	SBO1B	TM7IOA	SBO6A	AN8		General Purpose I/O port 0
	P01	SBI1B	TM7OB	SBI6A	AN9	DAOUT1A	
	P02	SBT1B	TM7OC	SBT6A	AN10		
	P03	SBO2A	SBO5A	SDA0A	AN11	DAOUT1B	
	P04	SBI2A	SBI5A	AN12			
	P05	SBT2A	SBT5A	SCL0A	AN13	DAOUT1C	
	P06						
	P07						
	P10	OCD_SDA	TM0IO	AN14			General Purpose I/O port 1
	P11	OCD_SCL	TM1IO	AN15			
	P12	TM2IO	TM22IOB				
	P13	IRQ5B	TM20IOB	NWDOVF2			
	P14	NWE0	SBO0A	LINTXDA			
	P15	NWE1	SBI0A	LINRXDA			
	P16	NRE	SBT0A				

* CAN-embedded series only.
** IEBus-embedded series only.

	Pin	Other Function					Description
I/O Port	P20	NDK	IRQ0A				General Purpose I/O port 2
	P21	NCS1	IRQ1A				
	P22	NCS2	IRQ2A				
	P23	IRQ3A					
	P24	IRQ4A					
	P25	A20	IRQ5A				
	P30	A19	SBO1A				General Purpose I/O port 3
	P31	A18	SBI1A				
	P32	A17	SBT1A				
	P33	A16	SBO3A	SDA1A			
	P34	A15	SBI3A	TM4IO			
	P35	A14	SBT3A	SCL1A			
	P40	D15	SBI4A	TM11IOB			General Purpose I/O port 4
	P41	SBO4A	SDA2A	IRQ6			
	P42	SBT4A	SCL2A	IRQ7	NMIRQ		
	P43						
	P44	OSCO					
	P45	OSCI					
	P46	XI					
	P47	XO					
	P50	A13					General Purpose I/O port 5
	P51	A12	SBO9				
	P52	A11	SBI9				
	P53	A10	SBT9				
	P54	A9	SBO10				
	P55	A8	SBI10				
	P56	A7	SBT10				
	P57	A6	IRQ8				
	P60	A5	KEY0	TM13IOA			General Purpose I/O port 6
	P61	A4	KEY1	TM13IOB			
	P62	A3	KEY2	TM14IOA			
	P63	A2	KEY3	TM14IOB			
	P64	A1	KEY4	TM15IOA			
	P65	A0	KEY5	TM15IOB			
	P66	D0	KEY6	TM16IOA			
	P67	D1	KEY7	TM16IOB			
	P70	D2	TMMOD0				General Purpose I/O port 7
	P71	D3	TMMOD1				
	P72	D4	TMMOD2				
	P73	D5	TMMOD3				
	P74	D6	TMMOD4				
	P75	D7	TMMOD5				
	P76						
	P77	SYSCLK	TMMIO				
	P80	TM3IO	LED0				General Purpose I/O port 8
	P81	D8	TM8IOA	LED1			
	P82	D9	TM8IOB	LED2			
	P83	D10	TM9IOA	LED3			
	P84	D11	TM9IOB	LED4			
	P85	D12	TM10IOA	LED5			
	P86	D13	TM10IOB	LED6			
	P87	D14	TM11IOA	LED7			

* CAN-embedded series only.
** IEBus-embedded series only.

	Pin	Other Function					Description
I/O Port	P90	SBO0B	(CTX0A)*	LINTXDB			General Purpose I/O port 9
	P91	SBI0B	(CRX0A)*	LINRXDB			
	P92	SBT0B					
	P93	SBO3B	SDA1B				
	P94	SBI3B	(ITX0A)**				
	P95	SBT3B	SCL1B	(IRX0A)**			
	P96	IRQ0C					
	P97	IRQ1C					
	PA0	SBO7A	AN0				General Purpose I/O port A
	PA1	SBI7A	AN1	DAOUT0A			
	PA2	SBT7A	AN2				
	PA3	TM22IOA	AN3	DAOUT0B			
	PA4	TM21BKA	AN4				
	PA5	TM21GCPA	AN5	DAOUT0C			
	PA6	TM21IOA	AN6				
	PA7	TM20IOA	AN7				
	PB0	SBO4C	TM21GCPB				General Purpose I/O port B
	PB1	SBI4C	TM21BKB				
	PB2	SBT4C	TM21IOB				
	PB3	SBO8B					
	PB4	SBI8B					
	PB5	SBT8B					
	PB6						
	PB7						
	PC0	SBO4B	SBO7B	SDA2B			General Purpose I/O port C
	PC1	SBI4B	SBI7B				
	PC2	SBT4B	SBT7B	SCL2B			
	PC3						
	PC4						
	PC5						
	PC6						
	PD0	SBO2B	SBO8A	SDA0B			General Purpose I/O port D
	PD1	SBI2B	SBI8A				
	PD2	SBT2B	SBT8A	SCL0B			
	PD3	(ITX1A)**	IRQ0B				
	PD4	(IRX1A)**	IRQ1B				
	PD5	IRQ2B					
	PD6	TM12IOA	IRQ3B				
	PD7	TM12IOB	IRQ4B				
	PE0	(CTX0B)*					General Purpose I/O port E
	PE1	(CRX0B)*					
	PE2						
	PE3	(ITX1B)**					
	PE4	(IRX1B)**					
	PE5	(ITX0B)**					
	PE6	(IRX0B)**					
	PE7						
	PF0	SBO5B					General Purpose I/O port F
	PF1	SBI5B					
	PF2	SBT5B					
	PF3	SBO6B					
	PF4	SBI6B					
	PF5	SBT6B					
	PF6						

* CAN-embedded series only.
** IEBus-embedded series only.

	Pin	Other Function					Description
I/O Port	PG0	IRQ2C					General Purpose I/O port G
	PG1	IRQ3C					
	PG2						
	PG3						
	PG4						
	PG5						
	PG6						
	PH0	IRQ4C					General Purpose I/O port H
	PH1	IRQ5C					
LED	LED0	P80	TM3IO				LED drive pins
	LED1	P81	D8	TM8IOA			
	LED2	P82	D9	TM8IOB			
	LED3	P83	D10	TM9IOA			
	LED4	P84	D11	TM9IOB			
	LED5	P85	D12	TM10IOA			
	LED6	P86	D13	TM10IOB			
	LED7	P87	D14	TM11IOA			
OCD	OCD_SDA	P10	TM0IO	AN14			Clock input pin for on-chip debug function.
	OCS_SCL	P11	TM1IO	AN15			Data I/O pin for on-chip debug function.

Table:1.5.5 shows pin functions of 128 pin version.

Table:1.5.5 Pin Functions of 128 pin Version

	Pin	Other Function					Description
Power supply / Ground *	VDD50						On-chip regulator power supply Power supply for I/O
	AVDD						Power supply for analog operation.
	VOUT18						Power supply for internal circuit.
	VREFH						Reference power supply pin for the A/D converter.
	AVSS						Ground pin for analog.
	VSS						Ground
Function control *	ATRST						Auto reset setting pin
	NOCDMOD						On-chip debug function (OCD) control pin
Reset	NRST						Reset signal input pin (Active low)
Clock	OSCI	P45					High-speed oscillation input pin (clkosc) (4 to 20 MHz)
	OSCO	P44					High-speed oscillation output pin
	XI	P46					Low-speed oscillation input pin (clkx = 32.768 kHz)
	XO	P47					Low-speed oscillation output pin
	SYSCLK	P77	TMMIO				System clock signal output pin
Bus	A20	P25	IRQ5A				Address output pins at Memory expansion mode
	A19	P30	SBO1A				
	A18	P31	SBI1A				
	A17	P32	SBT1A				
	A16	P33	SBO3A	SDA1A			
	A15	P34	SBI3A	TM4IO			
	A14	P35	SBT3A	SCL11A			
	A13	P50					
	A12	P51	SBO9				
	A11	P52	SBI9				
	A10	P53	SBT9				
	A9	P54	SBO10				
	A8	P55	SBI10				
	A7	P56	SBT10				
	A6	P57	IRQ8				
	A5	P60	KEY0	TM13IOA			
	A4	P61	KEY1	TM13IOB			
	A3	P62	KEY2	TM14IOA			
	A2	P63	KEY3	TM14IOB			
	A1	P64	KEY4	TM15IOA			
	A0	P65	KEY5	TM15IOB			

Refer to [Chapter Overview] of LSI User's Manual for detail about note of VDD and function control pins.

	Pin	Other Function					Description
Bus	D15	P40	SBI4A	TM11IOB			Data I/O pins at Memory expansion mode
	D14	P87	LED7	TM11IOA			
	D13	P86	LED6	TM10IOB			
	D12	P85	LED5	TM10IOA			
	D11	P84	LED4	TM9IOB			
	D10	P83	LED3	TM9IOA			
	D9	P82	LED2	TM8IOB			
	D8	P81	LED1	TM8IOA			
	D7	P75	TMMOD5				
	D6	P74	TMMOD4				
	D5	P73	TMMOD3				
	D4	P72	TMMOD2				
	D3	P71	TMMOD1				
	D2	P70	TMMOD0				
	D1	P67	KEY7	TM16IOB			
	D0	P66	KEY6	TM16IOA			
	NCS2	P22	IRQ2A				Chip select signal output pins (Active low)
	NCS1	P21	IRQ1A				
	NRE	P16	SBT0A				Read enable signal output pin (Active low)
	NWE1	P15	SBI0A	LINRXDA			Write enable signal output pins (Active low)
	NWE0	P14	SBO0A	LINTXDA			
	NDK	P20	IRQ0A				Acknowledge signal input pin (Active low)
Watchdog timer 2	NWDOVF2	P13	IRQ5B	TM20IOB			Watchdog timer 2 over flow (active low)
Interrupt	NMIRQ	P42	IRQ7	SBT4A	SCL2A		Non-maskable interrupt request signal input pin (Active low)
	IRQ8	P57	A6				External interrupt request signal input pin 8
	IRQ7	P42	NMIRQ	SBT4A	SCL2A		External interrupt request signal input pin 7
	IRQ6	P41	SBO4A	SDA2A			External interrupt request signal input pin 6
	IRQ5A	P25	A20				External interrupt request signal input pin 5 (Pin change is possible)
	IRQ5B	P13	TM20IOB	NWDOVF2			
	IRQ4A	P24					External interrupt request signal input pin 4 (Pin change is possible)
	IRQ4B	PD7	TM12IOB				
	IRQ3A	P23					External interrupt request signal input pin 3 (Pin change is possible)
	IRQ3B	PD6	TM12IOA				
	IRQ2A	P22	NCS2				External interrupt request signal input pin 2 (Pin change is possible)
	IRQ2B	PD5					
	IRQ1A	P21	NCS1				External interrupt request signal input pin 1 (Pin change is possible)
	IRQ1B	PD4	(IRX1A)**				
	IRQ0A	P20	NDK				External interrupt request signal input pin 0 (Pin change is possible)
	IRQ0B	PD3	(ITX1A)**				
	KEY7	P67	D1	TM16IOB			Key input interrupt
	KEY6	P66	D0	TM16IOA			
	KEY5	P65	A0	TM15IOB			
	KEY4	P64	A1	TM15IOA			
	KEY3	P63	A2	TM14IOB			
	KEY2	P62	A3	TM14IOA			
	KEY1	P61	A4	TM13IOB			
	KEY0	P60	A5	TM13IOA			
Timer	TM0IO	P10	OCD_SDA	AN14			8-bit Timer 0 to 4 I/O pins
	TM1IO	P11	OCD_SCL	AN15			
	TM2IO	P12	TM22IOB				
	TM3IO	P80	LED0				
	TM4IO	P34	A15	SBI3A			
	TM7IOA	P00	SBO1B	SBO6A	AN8		16-bit Timer 7 I/O pin A, output pin B, C
	TM7OB	P01	SBI1B	SBI6A	AN9	DAOUT1A	
	TM7OC	P02	SBT1B	SBT6A	AN10		

* CAN-embedded series only.
** IEBus-embedded series only.

	Pin	Other Function					Description
Timer	TM8IOA	P81	D8	LED1			16-bit Timer 8 to 16 I/O pins A, B
	TM8IOB	P82	D9	LED2			
	TM9IOA	P83	D10	LED3			
	TM9IOB	P84	D11	LED4			
	TM10IOA	P85	D12	LED5			
	TM10IOB	P86	D13	LED6			
	TM11IOA	P87	D14	LED7			
	TM11IOB	P40	D15	SBI4A			
	TM12IOA	PD6	IRQ3B				
	TM12IOB	PD7	IRQ4B				
	TM13IOA	P60	KEY0	A5			
	TM13IOB	P61	KEY1	A4			
	TM14IOA	P62	KEY2	A3			
	TM14IOB	P63	KEY3	A2			
	TM15IOA	P64	KEY4	A1			
	TM15IOB	P65	KEY5	A0			
	TM16IOA	P66	KEY6	D0			
	TM16IOB	P67	KEY7	D1			
	TM20IOA	PA7	AN7				8-bit Timer 20 to 22 I/O pins (Pin change is possible)
	TM20IOB	P13	IRQ5B	NWDOVF2			
	TM21IOA	PA6	AN6				
	TM21IOB	PB2	SBT4C				
	TM22IOA	PA3	AN3	DAOUT0B			
	TM22IOB	P12	TM2IO				
	TM21BKA	PA4	AN4				8-bit Timer 21 I/O pins (Pin change is possible)
	TM21BKB	PB1	SBI4C				
	TM21GCPA	PA5	AN5	DAOUT0C			
	TM21GCPB	PB0	SBO4C				
	TMMOD0	P70	D2				Motor control 16-bit Timer I/O pins
	TMMOD1	P71	D3				
	TMMOD2	P72	D4				
	TMMOD3	P73	D5				
	TMMOD4	P74	D6				
	TMMOD5	P75	D7				
	TMMIO	P77	SYSCLK				
Serial	SBT0A	P16	NRE				Serial clock I/O pins (Pin change is possible) - Clock synchronous/UART
	SBT0B	P92					
	SBT1A	P32	A17				
	SBT1B	P02	SBT6A	TM7OC	AN10		
	SBT2A	P05	SBT5A	SCL0A	AN13	DAOUT1C	
	SBT2B	PD2	SBT8A	SCL0B			
	SBT3A	P35	A14	SCL1A			
	SBT3B	P95	SCL1B	(IRX0A)**			
	SBT4A	P42	SCL2A	IRQ7	NMIRQ		
	SBT4B	PC2	SBT7B	SCL2B			
	SBT4C	PB2	TM21IOB				
	SBT5A	P05	SBT2A	SCL0A	AN13	DAOUT1C	
	SBT5B	PF2					
	SBT6A	P02	SBT1B	TM7OC	AN10		
	SBT6B	PF5					
	SBT7A	PA2	AN2				
	SBT7B	PC2	SBT4B	SCL2B			
	SBT8A	PD2	SBT2B	SCL0B			
	SBT8B	PB5					
	SBT9	P53					
	SBT10	P56					

* CAN-embedded series only.
** IEBus-embedded series only.

	Pin	Other Function					Description
Serial	SBO0A	P14	NWE0	LINTXDA			Serial data output pins (Pin change is possible) - Clock synchronous/UART
	SBO0B	P90	(CTX0A)*	LINTXDB			
	SBO1A	P30	A19				
	SBO1B	P00	SBO6A	TM7IOA	AN8		
	SBO2A	P03	SBO5A	SDA0A	AN11	DAOUT1B	
	SBO2B	PD0	SBO8A	SDA0B			
	SBO3A	P33	A16	SDA1A			
	SBO3B	P93	SDA1B				
	SBO4A	P41	SDA2A	IRQ6			
	SBO4B	PC0	SBO7B	SDA2B			
	SBO4C	PB0	TM21GCPB				
	SBO5A	P03	SBO2A	SDA0A	AN11	DAOUT1B	
	SBO5B	PF0					
	SBO6A	P00	SBO1B	TM7IOA	AN8		
	SBO6B	PF3					
	SBO7A	PA0	AN0				
	SBO7B	PC0	SBO4B	SDA2B			
	SBO8A	PD0	SBO2B	SDA0B			
	SBO8B	PB3					
	SBO9	P51	A12				
	SBO10	P54	A9				
	SBI0A	P15	NWE1	LINRXDA			Serial data input pins (Pin change is possible) - Clock synchronous/UART
	SBI0B	P91	(CRX0A)*	LINRXDB			
	SBI1A	P31	A18				
	SBI1B	P01	SBI6A	TM7OB	AN9	DAOUT1A	
	SBI2A	P04	SBI5A	AN12			
	SBI2B	PD1	SBI8A				
	SBI3A	P34	A15	TM4IO			
	SBI3B	P94	(ITX0A)**				
	SBI4A	P40	D15	TM11IOB			
	SBI4B	PC1	SBI7B				
	SBI4C	PB1	TM21BKB				
	SBI5A	P04	SBI2A	AN12			
	SBI5B	PF1					
	SBI6A	P01	SBI1B	TM7OB	AN9	DAOUT1A	
	SBI6B	PF4					
	SBI7A	PA1	AN1	DAOUT0A			
	SBI7B	PC1	SBI4B				
	SBI8A	PD1	SBI2B				
	SBI8B	PB4					
	SBI9	P52	A11				
	SBI10	P55	A8				
IIC	SCL0A	P05	SBT2A	SBT5A	AN13	DAOUT1C	IIC clock I/O pins
	SCL0B	PD2	SBT2B	SBT8A			
	SCL1A	P35	A14	SBT3A			
	SCL1B	P95	SBT3B	(IRX0A)**			
	SCL2A	P42	SBT4A	IRQ7	NMIRQ		
	SCL2B	PC2	SBT4B	SBT7B			
	SDA0A	P03	SBO2A	SBO5A	AN11	DAOUT1B	IIC data I/O pins
	SDA0B	PD0	SBO2B	SBO8A			
	SDA1A	P33	A16	SBO3A			
	SDA1B	P93	SBO3B				
	SDA2A	P41	SBO4A	IRQ6			
	SDA2B	PC0	SBO4B	SBO7B			

* CAN-embedded series only.
** IEBus-embedded series only.

	Pin	Other Function					Description
LIN	LINTXDA	P14	SBO0A	NWE0			LIN data transmission pin (Pin change is possible)
	LINTXDB	P90	SBO0B	(CTX0A) *			
	LINRXDA	P15	SBI0A	NWE1			LIN data reception pin (Pin change is possible)
	LINRXDB	P91	SBI0B	(CRX0A) *			
CAN *	CTX0A	P90	SBO0B	LINTXDB			CAN data transmission pin (Pin change is possible)
	CTX0B	PE0					
	CRX0A	P91	SBI0B	LINRXDB			CAN data reception pin (Pin change is possible)
	CRX0B	PE1					
IEBus **	ITX0A	P94	SBI3B				IEBus data transmission pin (Pin change is possible)
	ITX0B	PE5					
	ITX1A	PD3	IRQ0B				
	ITX1B	PE3					
	IRX0A	P95	SBT3B	SCL1B			IEBus data reception pin (Pin change is possible)
	IRX0B	PE6					
	IRX1A	PD4	IRQ1B				
	IRX1B	PE4					
A/D converter	AN0	PA0	SBO7A				Analog input pins
	AN1	PA1	SBI7A	DAOUT0A			
	AN2	PA2	SBT7A				
	AN3	PA3	TM22IOA	DAOUT0B			
	AN4	PA4	TM21BKA				
	AN5	PA5	TM21GCPA	DAOUT0C			
	AN6	PA6	TM21IOA				
	AN7	PA7	TM20IOA				
	AN8	P00	SBO1B	TM7IOA	SBO6A		
	AN9	P01	SBI1B	TM7OB	SBI6A	DAOUT1A	
	AN10	P02	SBT1B	TM7OC	SBT6A		
	AN11	P03	SBO2A	SBO5A	SDA0A	DAOUT1B	
	AN12	P04	SBI2A	SBI5A			
	AN13	P05	SBT2A	SBT5A	SCL0A	DAOUT1C	
	AN14	P10	TM0IO	OCD_SDA			
	AN15	P11	TM1IO	OCD_SCL			
D/A converter	DAOUT0A	PA1	SBI7A	AN1			Analog output pins
	DAOUT0B	PA3	TM22IOA	AN3			
	DAOUT0C	PA5	TM21GCPA	AN5			
	DAOUT1A	P01	SBI1B	TM7OB	SBI6A	AN9	
	DAOUT1B	P03	SBO2A	SBO5A	SDA0A	AN11	
	DAOUT1C	P05	SBT2A	SBT5A	SCL0A	AN13	
I/O Port	P00	SBO1B	TM7IOA	SBO6A	AN8		General Purpose I/O port 0
	P01	SBI1B	TM7OB	SBI6A	AN9	DAOUT1A	
	P02	SBT1B	TM7OC	SBT6A	AN10		
	P03	SBO2A	SBO5A	SDA0A	AN11	DAOUT1B	
	P04	SBI2A	SBI5A	AN12			
	P05	SBT2A	SBT5A	SCL0A	AN13	DAOUT1C	
	P06						
	P07						
	P10	OCD_SDA	TM0IO	AN14			General Purpose I/O port 1
	P11	OCD_SCL	TM1IO	AN15			
	P12	TM2IO	TM22IOB				
	P13	IRQ5B	TM20IOB	NWDOVF2			
	P14	NWE0	SBO0A	LINTXDA			
	P15	NWE1	SBI0A	LINRXDA			
	P16	NRE	SBT0A				

* CAN-embedded series only.
** IEBus-embedded series only.

	Pin	Other Function					Description
I/O Port	P20	NDK	IRQ0A				General Purpose I/O port 2
	P21	NCS1	IRQ1A				
	P22	NCS2	IRQ2A				
	P23	IRQ3A					
	P24	IRQ4A					
	P25	A20	IRQ5A				
	P30	A19	SBO1A				General Purpose I/O port 3
	P31	A18	SBI1A				
	P32	A17	SBT1A				
	P33	A16	SBO3A	SDA1A			
	P34	A15	SBI3A	TM4IO			
	P35	A14	SBT3A	SCL1A			
	P40	D15	SBI4A	TM11IOB			General Purpose I/O port 4
	P41	SBO4A	SDA2A	IRQ6			
	P42	SBT4A	SCL2A	IRQ7	NMIRQ		
	P43						
	P44	OSCO					
	P45	OSCI					
	P46	XI					
	P47	XO					
	P50	A13					General Purpose I/O port 5
	P51	A12	SBO9				
	P52	A11	SBI9				
	P53	A10	SBT9				
	P54	A9	SBO10				
	P55	A8	SBI10				
	P56	A7	SBT10				
	P57	A6	IRQ8				
	P60	A5	KEY0	TM13IOA			General Purpose I/O port 6
	P61	A4	KEY1	TM13IOB			
	P62	A3	KEY2	TM14IOA			
	P63	A2	KEY3	TM14IOB			
	P64	A1	KEY4	TM15IOA			
	P65	A0	KEY5	TM15IOB			
	P66	D0	KEY6	TM16IOA			
	P67	D1	KEY7	TM16IOB			
	P70	D2	TMMOD0				General Purpose I/O port 7
	P71	D3	TMMOD1				
	P72	D4	TMMOD2				
	P73	D5	TMMOD3				
	P74	D6	TMMOD4				
	P75	D7	TMMOD5				
	P77	SYSCLK	TMMIO				
	P80	TM3IO	LED0				General Purpose I/O port 8
	P81	D8	TM8IOA	LED1			
	P82	D9	TM8IOB	LED2			
	P83	D10	TM9IOA	LED3			
	P84	D11	TM9IOB	LED4			
	P85	D12	TM10IOA	LED5			
	P86	D13	TM10IOB	LED6			
	P87	D14	TM11IOA	LED7			
	P90	SBO0B	(CTX0A)*	LINTXDB			General Purpose I/O port 9
	P91	SBI0B	(CRX0A)*	LINRXDB			
	P92	SBT0B					
	P93	SBO3B	SDA1B				
	P94	SBI3B	(ITX0A)**				
	P95	SBT3B	SCL1B	(IRX0A)**			

* CAN-embedded series only.
** IEBus-embedded series only.

	Pin	Other Function					Description
I/O Port	PA0	SBO7A	AN0				General Purpose I/O port A
	PA1	SBI7A	AN1	DAOUT0A			
	PA2	SBT7A	AN2				
	PA3	TM22IOA	AN3	DAOUT0B			
	PA4	TM21BKA	AN4				
	PA5	TM21GCPA	AN5	DAOUT0C			
	PA6	TM21IOA	AN6				
	PA7	TM20IOA	AN7				
	PB0	SBO4C	TM21GCPB				General Purpose I/O port B
	PB1	SBI4C	TM21BKB				
	PB2	SBT4C	TM21IOB				
	PB3	SBO8B					
	PB4	SBI8B					
	PB5	SBT8B					
	PC0	SBO4B	SBO7B	SDA2B			General Purpose I/O port C
	PC1	SBI4B	SBI7B				
	PC2	SBT4B	SBT7B	SCL2B			
	PC3						
	PC4						
	PC5						
	PC6						
	PD0	SBO2B	SBO8A	SDA0B			General Purpose I/O port D
	PD1	SBI2B	SBI8A				
	PD2	SBT2B	SBT8A	SCL0B			
	PD3	(ITX1A)**	IRQ0B				
	PD4	(IRX1A)**	IRQ1B				
	PD5	IRQ2B					
	PD6	TM12IOA	IRQ3B				
	PD7	TM12IOB	IRQ4B				
	PE0	(CTX0B)*					General Purpose I/O port E
	PE1	(CRX0B)*					
	PE2						
	PE3	(ITX1B)**					
	PE4	(IRX1B)**					
	PE5	(ITX0B)**					
	PE6	(IRX0B)**					
	PF0	SBO5B					General Purpose I/O port F
	PF1	SBI5B					
	PF2	SBT5B					
	PF3	SBO6B					
	PF4	SBI6B					
	PF5	SBT6B					
	PF6						
LED	LED0	P80	TM3IO				LED drive pins
	LED1	P81	D8	TM8IOA			
	LED2	P82	D9	TM8IOB			
	LED3	P83	D10	TM9IOA			
	LED4	P84	D11	TM9IOB			
	LED5	P85	D12	TM10IOA			
	LED6	P86	D13	TM10IOB			
	LED7	P87	D14	TM11IOA			
OCD	OCD_SDA	P10	TM0IO	AN14			Clock input pin for on-chip debug function.
	OCS_SCL	P11	TM1IO	AN15			Data I/O pin for on-chip debug function.

* CAN-embedded series only.
** IEBus-embedded series only.

Table:1.5.6 shows pin functions of 100 pin version.

Table:1.5.6 Pin Functions of 100 pin Version

	Pin	Other Function					Description
Power supply / Ground *	VDD50						On-chip regulator power supply Power supply for I/O
	AVDD						Power supply for analog operation.
	VOUT18						Power supply for internal circuit.
	VREFH						Reference power supply pin for the A/D converter.
	AVSS						Ground pin for analog.
	VSS						Ground
Function control *	ATRST						Auto reset setting pin
	NOCDMOD						On-chip debug function (OCD) control pin
Reset	NRST						Reset signal input pin (Active low)
Clock	OSCI	P45					High-speed oscillation input pin (clkosc) (4 to 20 MHz)
	OSCO	P44					High-speed oscillation output pin
	XI	P46					Low-speed oscillation input pin (clkx = 32.768 kHz)
	XO	P47					Low-speed oscillation output pin
	SYSCLK	P77	TMMIO				System clock signal output pin
Bus	A20	P25	IRQ5A				Address output pins at Memory expansion mode
	A19	P30	SBO1A				
	A18	P31	SBI1A				
	A17	P32	SBT1A				
	A16	P33	SBO3A	SDA1A			
	A15	P34	SBI3A	TM4IO			
	A14	P35	SBT3A	SCL11A			
	A13	P50					
	A12	P51	SBO9				
	A11	P52	SBI9				
	A10	P53	SBT9				
	A9	P54	SBO10				
	A8	P55	SBI10				
	A7	P56	SBT10				
	A6	P57	IRQ8				
	A5	P60	KEY0	TM13IOA			
	A4	P61	KEY1	TM13IOB			
	A3	P62	KEY2	TM14IOA			
	A2	P63	KEY3	TM14IOB			
	A1	P64	KEY4	TM15IOA			
	A0	P65	KEY5	TM15IOB			

Refer to [Chapter Overview] of LSI User's Manual for detail about note of VDD and function control pins.

	Pin	Other Function					Description
Bus	D15	P40	SBI4A	TM11IOB			Data I/O pins at Memory expansion mode
	D14	P87	LED7	TM11IOA			
	D13	P86	LED6	TM10IOB			
	D12	P85	LED5	TM10IOA			
	D11	P84	LED4	TM9IOB			
	D10	P83	LED3	TM9IOA			
	D9	P82	LED2	TM8IOB			
	D8	P81	LED1	TM8IOA			
	D7	P75	TMMOD5				
	D6	P74	TMMOD4				
	D5	P73	TMMOD3				
	D4	P72	TMMOD2				
	D3	P71	TMMOD1				
	D2	P70	TMMOD0				
	D1	P67	KEY7	TM16IOB			
	D0	P66	KEY6	TM16IOA			
	NCS2	P22	IRQ2A				Chip select signal output pins (Active low)
	NCS1	P21	IRQ1A				
	NRE	P16	SBT0A				Read enable signal output pin (Active low)
	NWE1	P15	SBI0A	LINRXDA			Write enable signal output pins (Active low)
	NWE0	P14	SBO0A	LINTXDA			
	NDK	P20	IRQ0A				Acknowledge signal input pin (Active low)
Watchdog timer 2	NWDOVF2	P13	IRQ5B	TM20IOB			Watchdog timer 2 over flow (active low)
Interrupt	NMIRQ	P42	IRQ7	SBT4A	SCL2A		Non-maskable interrupt request signal input pin (Active low)
	IRQ8	P57	A6				External interrupt request signal input pin 8
	IRQ7	P42	NMIRQ	SBT4A	SCL2A		External interrupt request signal input pin 7
	IRQ6	P41	SBO4A	SDA2A			External interrupt request signal input pin 6
	IRQ5A	P25	A20				External interrupt request signal input pin 5 (Pin change is possible)
	IRQ5B	P13	TM20IOB	NWDOVF2			
	IRQ4A	P24					External interrupt request signal input pin 4 (Pin change is possible)
	IRQ4B	PD7	TM12IOB				
	IRQ3A	P23					External interrupt request signal input pin 3 (Pin change is possible)
	IRQ3B	PD6	TM12IOA				
	IRQ2A	P22	NCS2				External interrupt request signal input pin 2 (Pin change is possible)
	IRQ2B	PD5					
	IRQ1A	P21	NCS1				External interrupt request signal input pin 1 (Pin change is possible)
	IRQ1B	PD4	(IRX1A)**				
	IRQ0A	P20	NDK				External interrupt request signal input pin 0 (Pin change is possible)
	IRQ0B	PD3	(ITX1A)**				
	KEY7	P67	D1	TM16IOB			Key input interrupt
	KEY6	P66	D0	TM16IOA			
	KEY5	P65	A0	TM15IOB			
	KEY4	P64	A1	TM15IOA			
	KEY3	P63	A2	TM14IOB			
	KEY2	P62	A3	TM14IOA			
	KEY1	P61	A4	TM13IOB			
	KEY0	P60	A5	TM13IOA			
Timer	TM0IO	P10	OCD_SDA	AN14			8-bit Timer 0 to 4 I/O pins
	TM1IO	P11	OCD_SCL	AN15			
	TM2IO	P12	TM22IOB				
	TM3IO	P80	LED0				
	TM4IO	P34	A15	SBI3A			
	TM7IOA	P00	SBO1B	SBO6A	AN8		16-bit Timer 7 I/O pin A, output pin B, C
	TM7OB	P01	SBI1B	SBI6A	AN9	DAOUT1A	
	TM7OC	P02	SBT1B	SBT6A	AN10		

* CAN-embedded series only.
** IEBus-embedded series only.

	Pin	Other Function					Description
Timer	TM8IOA	P81	D8	LED1			16-bit Timer 8 to 16 I/O pins A, B
	TM8IOB	P82	D9	LED2			
	TM9IOA	P83	D10	LED3			
	TM9IOB	P84	D11	LED4			
	TM10IOA	P85	D12	LED5			
	TM10IOB	P86	D13	LED6			
	TM11IOA	P87	D14	LED7			
	TM11IOB	P40	D15	SBI4A			
	TM12IOA	PD6	IRQ3B				
	TM12IOB	PD7	IRQ4B				
	TM13IOA	P60	KEY0	A5			
	TM13IOB	P61	KEY1	A4			
	TM14IOA	P62	KEY2	A3			
	TM14IOB	P63	KEY3	A2			
	TM15IOA	P64	KEY4	A1			
	TM15IOB	P65	KEY5	A0			
	TM16IOA	P66	KEY6	D0			
	TM16IOB	P67	KEY7	D1			
	TM20IOA	PA7	AN7				8-bit Timer 20 to 22 I/O pins (Pin change is possible)
	TM20IOB	P13	IRQ5B	NWDOVF2			
	TM21IOA	PA6	AN6				
	TM22IOA	PA3	AN3	DAOUT0B			
	TM22IOB	P12	TM2IO				
	TM21BKA	PA4	AN4				8-bit Timer 21 I/O pins (Pin change is possible)
	TM21GCPA	PA5	AN5	DAOUT0C			
	TMMOD0	P70	D2				Motor control 16-bit Timer I/O pins
	TMMOD1	P71	D3				
	TMMOD2	P72	D4				
	TMMOD3	P73	D5				
	TMMOD4	P74	D6				
	TMMOD5	P75	D7				
	TMMIO	P77	SYSCLK				
Serial	SBT0A	P16	NRE				Serial clock I/O pins (Pin change is possible) - Clock synchronous/UART
	SBT0B	P92					
	SBT1A	P32	A17				
	SBT1B	P02	SBT6A	TM7OC	AN10		
	SBT2A	P05	SBT5A	SCL0A	AN13	DAOUT1C	
	SBT2B	PD2	SBT8A	SCL0B			
	SBT3A	P35	A14	SCL1A			
	SBT3B	P95	SCL1B	(IRX0A)**			
	SBT4A	P42	SCL2A	IRQ7	NMIRQ		
	SBT5A	P05	SBT2A	SCL0A	AN13	DAOUT1C	
	SBT6A	P02	SBT1B	TM7OC	AN10		
	SBT7A	PA2	AN2				
	SBT8A	PD2	SBT2B	SCL0B			
	SBT9	P53					
	SBT10	P56					

* CAN-embedded series only.
** IEBus-embedded series only.

	Pin	Other Function					Description
Serial	SBO0A	P14	NWE0	LINTXDA			Serial data output pins (Pin change is possible) - Clock synchronous/UART
	SBO0B	P90	(CTX0A)*	LINTXDB			
	SBO1A	P30	A19				
	SBO1B	P00	SBO6A	TM7IOA	AN8		
	SBO2A	P03	SBO5A	SDA0A	AN11	DAOUT1B	
	SBO2B	PD0	SBO8A	SDA0B			
	SBO3A	P33	A16	SDA1A			
	SBO3B	P93	SDA1B				
	SBO4A	P41	SDA2A	IRQ6			
	SBO5A	P03	SBO2A	SDA0A	AN11	DAOUT1B	
	SBO6A	P00	SBO1B	TM7IOA	AN8		
	SBO7A	PA0	AN0				
	SBO8A	PD0	SBO2B	SDA0B			
	SBO9	P51	A12				
	SBO10	P54	A9				
	SBI0A	P15	NWE1	LINRXDA			Serial data input pins (Pin change is possible) - Clock synchronous/UART
	SBI0B	P91	(CRX0A)*	LINRXDB			
	SBI1A	P31	A18				
	SBI1B	P01	SBI6A	TM7OB	AN9	DAOUT1A	
	SBI2A	P04	SBI5A	AN12			
	SBI2B	PD1	SBI8A				
	SBI3A	P34	A15	TM4IO			
	SBI3B	P94	(ITX0A)**				
	SBI4A	P40	D15	TM11IOB			
	SBI5A	P04	SBI2A	AN12			
	SBI6A	P01	SBI1B	TM7OB	AN9	DAOUT1A	
	SBI7A	PA1	AN1	DAOUT0A			
	SBI8A	PD1	SBI2B				
	SBI9	P52	A11				
	SBI10	P55	A8				
IIC	SCL0A	P05	SBT2A	SBT5A	AN13	DAOUT1C	IIC clock I/O pins
	SCL0B	PD2	SBT2B	SBT8A			
	SCL1A	P35	A14	SBT3A			
	SCL1B	P95	SBT3B	(IRX0A)**			
	SCL2A	P42	SBT4A	IRQ7	NMIRQ		
	SDA0A	P03	SBO2A	SBO5A	AN11	DAOUT1B	IIC data I/O pins
	SDA0B	PD0	SBO2B	SBO8A			
	SDA1A	P33	A16	SBO3A			
	SDA1B	P93	SBO3B				
	SDA2A	P41	SBO4A	IRQ6			
LIN	LINTXDA	P14	SBO0A	NWE0			LIN data transmission pin (Pin change is possible)
	LINTXDB	P90	SBO0B	(CTX0A) *			
	LINRXDA	P15	SBI0A	NWE1			LIN data reception pin (Pin change is possible)
	LINRXDB	P91	SBI0B	(CRX0A) *			
CAN *	CTX0A	P90	SBO0B	LINTXDB			CAN data transmission pin (Pin change is possible)
	CRX0A	P91	SBI0B	LINRXDB			CAN data reception pin (Pin change is possible)
IEBus **	ITX0A	P94	SBI3B				IEBus data transmission pin (Pin change is possible)
	ITX1A	PD3	IRQ0B				
	IRX0A	P95	SBT3B	SCL1B			IEBus data reception pin (Pin change is possible)
	IRX1A	PD4	IRQ1B	IRX1A			

* CAN-embedded series only.
** IEBus-embedded series only.

	Pin	Other Function					Description
A/D converter	AN0	PA0	SBO7A				Analog input pins
	AN1	PA1	SBI7A	DAOUT0A			
	AN2	PA2	SBT7A				
	AN3	PA3	TM22IOA	DAOUT0B			
	AN4	PA4	TM21BKA				
	AN5	PA5	TM21GCPA	DAOUT0C			
	AN6	PA6	TM21IOA				
	AN7	PA7	TM20IOA				
	AN8	P00	SBO1B	TM7IOA	SBO6A		
	AN9	P01	SBI1B	TM7OB	SBI6A	DAOUT1A	
	AN10	P02	SBT1B	TM7OC	SBT6A		
	AN11	P03	SBO2A	SBO5A	SDA0A	DAOUT1B	
	AN12	P04	SBI2A	SBI5A			
	AN13	P05	SBT2A	SBT5A	SCL0A	DAOUT1C	
	AN14	P10	TM0IO	OCD_SDA			
	AN15	P11	TM1IO	OCD_SCL			
D/A converter	DAOUT0A	PA1	SBI7A	AN1			Analog output pins
	DAOUT0B	PA3	TM22IOA	AN3			
	DAOUT0C	PA5	TM21GCPA	AN5			
	DAOUT1A	P01	SBI1B	TM7OB	SBI6A	AN9	
	DAOUT1B	P03	SBO2A	SBO5A	SDA0A	AN11	
	DAOUT1C	P05	SBT2A	SBT5A	SCL0A	AN13	
I/O Port	P00	SBO1B	TM7IOA	SBO6A	AN8		General Purpose I/O port 0
	P01	SBI1B	TM7OB	SBI6A	AN9	DAOUT1A	
	P02	SBT1B	TM7OC	SBT6A	AN10		
	P03	SBO2A	SBO5A	SDA0A	AN11	DAOUT1B	
	P04	SBI2A	SBI5A	AN12			
	P05	SBT2A	SBT5A	SCL0A	AN13	DAOUT1C	
	P06						
	P10	OCD_SDA	TM0IO	AN14			General Purpose I/O port 1
	P11	OCD_SCL	TM1IO	AN15			
	P12	TM2IO	TM22IOB				
	P13	IRQ5B	TM20IOB	NWDOVF2			
	P14	NWE0	SBO0A	LINTXDA			
	P15	NWE1	SBI0A	LINRXDA			
	P16	NRE	SBT0A				
	P20	NDK	IRQ0A				General Purpose I/O port 2
	P21	NCS1	IRQ1A				
	P22	NCS2	IRQ2A				
	P23	IRQ3A					
	P24	IRQ4A					
	P25	A20	IRQ5A				
	P30	A19	SBO1A				General Purpose I/O port 3
	P31	A18	SBI1A				
	P32	A17	SBT1A				
	P33	A16	SBO3A	SDA1A			
	P34	A15	SBI3A	TM4IO			
	P35	A14	SBT3A	SCL1A			
	P40	D15	SBI4A	TM11IOB			General Purpose I/O port 4
	P41	SBO4A	SDA2A	IRQ6			
	P42	SBT4A	SCL2A	IRQ7	NMIRQ		
	P43						
	P44	OSCO					
	P45	OSCI					
	P46	XI					
	P47	XO					

* CAN-embedded series only.
** IEBus-embedded series only.

	Pin	Other Function					Description
I/O Port	P50	A13					General Purpose I/O port 5
	P51	A12	SBO9				
	P52	A11	SBI9				
	P53	A10	SBT9				
	P54	A9	SBO10				
	P55	A8	SBI10				
	P56	A7	SBT10				
	P57	A6	IRQ8				
	P60	A5	KEY0	TM13IOA			General Purpose I/O port 6
	P61	A4	KEY1	TM13IOB			
	P62	A3	KEY2	TM14IOA			
	P63	A2	KEY3	TM14IOB			
	P64	A1	KEY4	TM15IOA			
	P65	A0	KEY5	TM15IOB			
	P66	D0	KEY6	TM16IOA			
	P67	D1	KEY7	TM16IOB			
	P70	D2	TMMOD0				General Purpose I/O port 7
	P71	D3	TMMOD1				
	P72	D4	TMMOD2				
	P73	D5	TMMOD3				
	P74	D6	TMMOD4				
	P75	D7	TMMOD5				
	P77	SYSCLK	TMMIO				
	P80	TM3IO	LED0				General Purpose I/O port 8
	P81	D8	TM8IOA	LED1			
	P82	D9	TM8IOB	LED2			
	P83	D10	TM9IOA	LED3			
	P84	D11	TM9IOB	LED4			
	P85	D12	TM10IOA	LED5			
	P86	D13	TM10IOB	LED6			
	P87	D14	TM11IOA	LED7			
	P90	SBO0B	(CTX0A)*	LINTXDB			General Purpose I/O port 9
	P91	SBI0B	(CRX0A)*	LINRXDB			
	P92	SBT0B					
	P93	SBO3B	SDA1B				
	P94	SBI3B	(ITX0A)**				
	P95	SBT3B	SCL1B	(IRX0A)**			
	PA0	SBO7A	AN0				General Purpose I/O port A
	PA1	SBI7A	AN1	DAOUT0A			
	PA2	SBT7A	AN2				
	PA3	TM22IOA	AN3	DAOUT0B			
	PA4	TM21BKA	AN4				
	PA5	TM21GCPA	AN5	DAOUT0C			
	PA6	TM21IOA	AN6				
	PA7	TM20IOA	AN7				
	PD0	SBO2B	SBO8A	SDA0B			General Purpose I/O port D
	PD1	SBI2B	SBI8A				
	PD2	SBT2B	SBT8A	SCL0B			
	PD3	(ITX1A)**	IRQ0B				
	PD4	(IRX1A)**	IRQ1B				
	PD5		IRQ2B				
	PD6		TM12IOA	IRQ3B			
	PD7	TM12IOB	IRQ4B				

* CAN-embedded series only.
** IEBus-embedded series only.

	Pin	Other Function					Description
LED	LED0	P80	TM3IO				LED drive pins
	LED1	P81	D8	TM8IOA			
	LED2	P82	D9	TM8IOB			
	LED3	P83	D10	TM9IOA			
	LED4	P84	D11	TM9IOB			
	LED5	P85	D12	TM10IOA			
	LED6	P86	D13	TM10IOB			
	LED7	P87	D14	TM11IOA			
OCD	OCD_SDA	P10	TM0IO	AN14			Clock input pin for on-chip debug function.
	OCS_SCL	P11	TM1IO	AN15			Data I/O pin for on-chip debug function.

* CAN-embedded series only.
** IEBus-embedded series only.

1.6 Electrical Characteristics

This LSI Manual describes a standard specification (Representative : MN103LF09R).

When using this LSI, consult our sales offices for the product specifications.

Structure	CMOS integrated circuit
Application	General purpose
Function	CMOS 32-bit, single chip microcomputer
Connection	Refer to [Figure:1.5.1]

1.6.1 Absolute Maximum Ratings

A. Absolute Maximum Ratings *1 *2 *3 *4 V_{SS} = 0.0 V

Parameter			Symbol	Rating	Unit
A1	Power supply voltage 1 *5		V_{DD50A}	-0.3 to +7.0	V
A2	Power supply voltage 2 *5		AV_{DDA}	-0.3 to +7.0	
A3	Input pin voltage		V_I	-0.3 to V_{DD50} + 0.3 (upper limit:7.0)	V
A4	I/O pin voltage (Other than P91, PE1)		V_{IO1}	-0.3 to V_{DD50} + 0.3 (upper limit:7.0)	
A5	I/O pin voltage (P91, PE1)		V_{IO2}	-0.3 to +7.0	
A6	Average output current *1	P80 to P87	I_{OL1}	+22.5	mA
		Other than P80 to P87	I_{OL2}	+7.5	
		All I/O pin	I_{OH}	-7.5	
A7	Power dissipation *6	T_{OPR} = 85°C	P_{D1}	400	mW
A8		T_{OPR} = 105°C	P_{D2}	300	
A9	Operating ambient temperature		T_{OPR}	-40 to +105	°C
A10	Storage temperature		T_{STG}	-50 to +125	

*1 Applied to any 100 ms period.

*2 Connect at least one bypass capacitor of 0.1 μF or larger between each power supply pin (VDD50, AVDD) and GND near the LSI for preventing latch-up.

*3 Connect appropriate capacitor of 1 μF to 4 μF between VOUT18 pin and GND for the internal power voltage stabilization near the LSI.
Also, connect one or more capacitors of 1 μF or large between VDD50 pin and VSS.

*4 The absolute maximum ratings are the limit values beyond which the LSI may be damaged LSI operation is not guaranteed.

*5 Using $V_{DD50} = AV_{DD}$

*6 Calculated using a 4-layer printed circuit board (75 mm × 75 mm × 0.8 mm).

1.6.2 Operating Conditions

B. Operating Conditions

V_{SS} = 0 V
Ta = -40 °C to +105 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage *7							
B1	Power supply voltage (VDD50)	V_{DD50}		2.2	3.3	5.5	V
B2	Power supply voltage(AVDD)	AV_{DD}			V_{DD50}		
B3	Reference power supply pin for the A/D converter (VREFH)	V_{REFH}			V_{DD50}		
B4	RAM Retention power supply voltage (VDD50)	V_{DD50_S}	In STOP mode	1.8	3.3	5.5	
Operating speed							
B5	Instruction execution time	t_{c1}	V_{DD50} = 2.2 V to 5.5 V Normal mode, clkcpu 40 MHz	25			ns
		t_{c2}	V_{DD50} = 2.2 V to 5.5V Slow mode, clkcpu 32.768 kHz	30.5			µs
Oscillation pin							
B6	Oscillation frequency	f_{OSC}	V_{DD50} = 2.2 V to 5.5V	4		20	MHz
B7		fx	V_{DD50} = 2.2 V to 5.5V		32.768		kHz
B8	External capacitor *8	C_{11}			20		pF
B9		C_{12}			20		
B10		C_{21}			47		
B11		C_{22}			47		
B12	Internal feedback resistor	R_{f1}			1.22		MΩ
B13		R_{f2}			6.78		

*7 $V_{REFH} = AV_{DD} = V_{DD50}$

*8 Connect extarnal capacitors suited for the used oscillator.
For external capacity value, consult the oscillator manufacturer and perfrom matching tests enough for determining appropriate value.

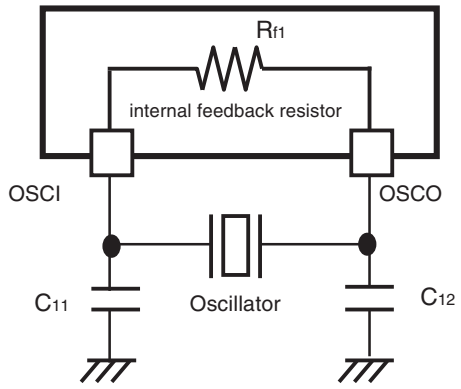


Figure:1.6.1 Oscillation Circuit 1

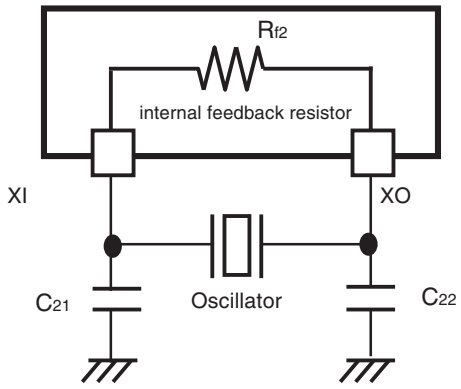


Figure:1.6.2 Oscillation Circuit 2

$V_{DD50} = AV_{DD} = V_{REFH}$ = 2.2 V to 5.5 V
V_{SS} = 0 V
Ta = -40 °C to +105 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
External clock input OSCI (OSCO is unconnected)							
B14	Clock frequency	f_{OSC}	V_{DD50} = 2.2 V to 5.5 V	4		20	MHz
B15	High-level pulse width *9	t_{wh1}	Figure:1.6.3	20			ns
B16	Low-level pulse width *9	t_{wl1}		20			
B17	Rising time *10	t_{wr1}	Figure:1.6.3			2.5	
B18	Falling time *10	t_{wf1}				2.5	
External clock input XI (XO is unconnected)							
B19	Clock frequency	f_X	V_{DD50} = 2.2 V to 5.5V		32.768		kHz
B20	High-level pulse width *9	t_{wh2}	Figure:1.6.4	5			µs
B21	Low-level pulse width *9	t_{wl2}		5			
B22	Rising time *10	t_{wr2}	Figure:1.6.4			0.5	
B23	Falling time *10	t_{wf2}				0.5	

*9 The clock duty ratio should be 45% to 55%

*10 Rising time and Falling time differ depending on the oscillation frequency.
The MAX value is not a specified value but a rough value.
Consult the oscillator manufacturer and perform matching tests enough for determining appropriate value.

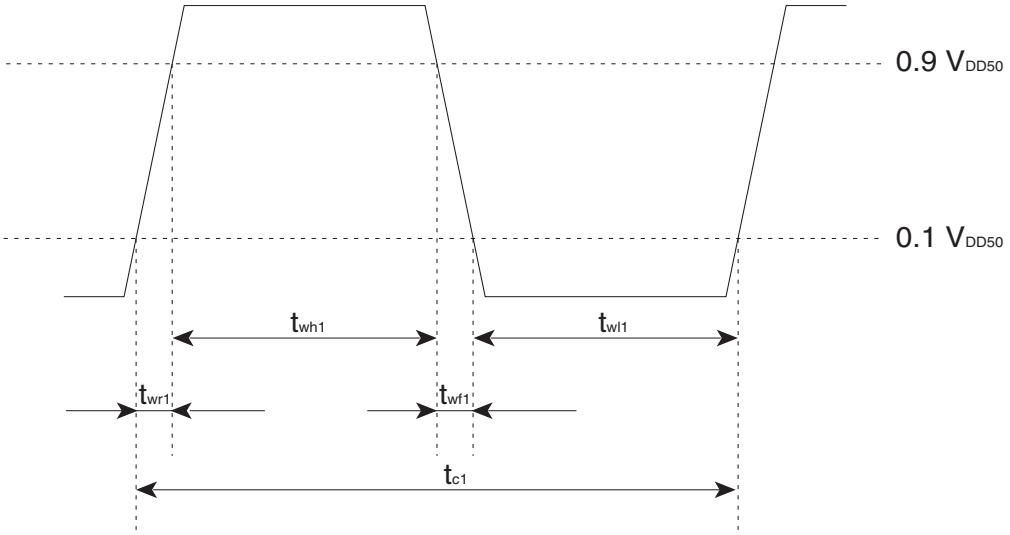


Figure:1.6.3 OSCI Timing Chart

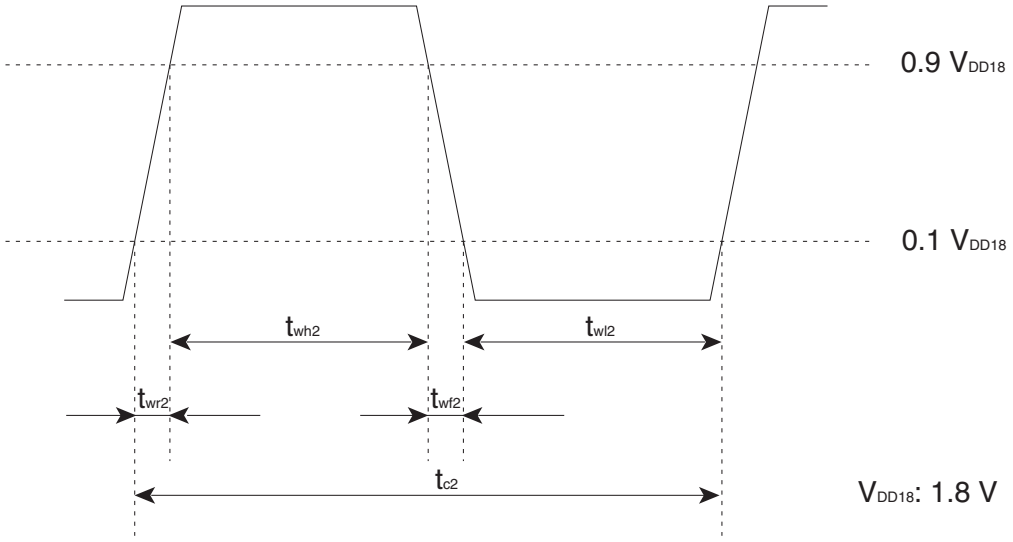


Figure:1.6.4 XI Timing Chart

C. DC Characteristics

$V_{DD50} = AV_{DD} = V_{REFH}$ = 2.2 V to 5.5 V
V_{SS} = 0 V
Ta = -40 °C to +105 °C

	Parameter	Symbol	Conditions		Rating MIN	Rating TYP	Rating MAX	Unit
Power supply current *11								
C1	Power supply current in NORMAL Mode	I_{DD1}	clkcpu = 20 MHz, V_{DD50} = 3.3 V [f_{OSC} = 20 MHz, PLL OFF, f_{rc} OFF]			13	26	mA
C2		I_{DD2}	clkcpu = 40 MHz, V_{DD50} = 3.3 V [f_{OSC} = 10 MHz, PLL multiple by 8, f_{rc} OFF]			24	48	
C3		I_{DD3}	clkcpu = 40 MHz, V_{DD50} = 3.3 V [f_X = 32.768 kHz, PLL multiple by 2440, f_{rc} OFF, f_{OSC} OFF]			23	46	
C4	Power supply current in SLOW Mode	I_{DD4}	clkcpu = 32.768 kHz, V_{DD50} = 3.3 V [f_X = 32.768 kHz, PLL OFF, f_{rc} OFF, f_{OSC} OFF, main regulator OFF] (At used the Low-Power Cache)			15	130	µA
C5	Power supply current in HALT mode	I_{DD5}	clkcpu = 20 MHz, V_{DD50} = 3.3 V [f_{OSC} = 20 MHz, PLL OFF, f_{rc} OFF, f_{rcx} OFF]			3	6	mA
C6		I_{DD6}	clkcpu = 32 kHz, V_{DD50} = 3.3 V [f_{OSC} = 4 MHz, PLL OFF, f_{rc} OFF, f_{rcx} OFF, main regulator OFF]			300	500	µA
C7		I_{DD7}	clkcpu = 32.768 kHz, V_{DD50} = 3.3 V [f_X = 32.768 kHz, PLL OFF, f_{rc} OFF, f_{rcx} OFF, f_{OSC} OFF, main regulator OFF]			5	110	
C8	Power supply current in STOP mode	I_{DD8}	V_{DD50} = 3.3 V, f_{OSC} OFF, f_X OFF, f_{rc} OFF, f_{rcx} OFF, main regurator OFF	Ta = 25 °C		2		
		I_{DD9}		Ta = 85 °C			100	

*11 I/O pin are all output setting (unloaded condition)

V_{DD50} = AV_{DD} = V_{REFH} = 2.2 V to 5.5 V
V_{SS} = 0 V
Ta = -40 °C to +105 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pin 1 NOCDMOD, ATRST							
C9	Input voltage High-level	V_{IH1}	-	$0.7V_{DD50}$		V_{DD50}	V
C10	Input voltage Low-level	V_{IL1}	-	0		$0.3V_{DD50}$	
C11	Input leakage current	I_{LK1}	V_{IN} = V_{SS} or V_{DD50}			± 5	µA
Input pin 2 NRST							
C12	Input voltage High-level	V_{IH2}	-	$0.7V_{DD50}$		V_{DD50}	V
C13	Input voltage Low-level	V_{IL2}	-	0		$0.3V_{DD50}$	
C14	Internal pull-up resistance	R_{PU2}	V_{DD50} = 3.3 V, V_{IN} = 0 V	15	30	60	kΩ
I/O pin 1 P00 to P07, P10 to P16, P20 to P25, P30 to P35, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P90, P92 to P97, PA0 to PA7, PB0 to PB7, PC0 to PC6, PD0 to PD7, PE0, PE2 to PE7, PF0 to PF6, PG0 to PG6, PH0 to PH1							
C15	Input voltage High-level	V_{IH3}	-	$0.7V_{DD50}$		V_{DD50}	V
C16	Input voltage Low-level	V_{IL3}	-	0		$0.3V_{DD50}$	
C17	Input leakage current	I_{LK3}	V_{IN} = V_{SS} or V_{DD50}			± 5	µA
C18	Internal pull-up resistance	R_{PU3}	V_{DD50} = 3.3 V, V_{IN} = 0 V	15	30	60	kΩ
C19	Output voltage High-level	V_{OH3}	V_{DD50} = 3.3 V, I_{OH} = -2.0 mA	2.7			V
C20	Output voltage Low-level	V_{OL3}	V_{DD50} = 3.3 V, I_{OL} = 2.0 mA			0.4	

V_{DD50} = AV_{DD} = V_{REFH} = 2.2 V to 5.5 V
V_{SS} = 0 V
Ta = -40 °C to +105 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
I/O pin 2 P80 to P87							
C21	Input voltage High-level	V_{IH5}	-	$0.7V_{DD50}$		V_{DD50}	V
C22	Input voltage Low-level	V_{IL5}	-	0		$0.3V_{DD50}$	
C23	Input leakage current	I_{LK5}	V_{IN} = V_{SS} or V_{DD50}			± 5	µA
C24	Internal pull-up resistance	R_{PU5}	V_{DD50} = 3.3 V, V_{IN} = 0 V	15	30	60	kΩ
C25	Output voltage High-level	V_{OH5}	V_{DD50} = 3.3 V, I_{OH} = -2.0 mA	2.7			V
C26	Output voltage Low-level 1	V_{OL5}	V_{DD50} = 3.3 V, I_{OL} = 2.0 mA			0.4	
C27	Output voltage Low-level 2	V_{OL5}	V_{DD50} = 3.3 V, I_{OL} = 8.0 mA (P8LED = "1")			0.4	
I/O pin 3 P91, PE1							
C28	Input voltage High-level	V_{IH6}	-	$0.7V_{DD50}$		5.5	V
C29	Input voltage Low-level	V_{IL6}	-	0		$0.3V_{DD50}$	
C30	Input leakage current	I_{LK6}	V_{IN} = V_{SS} or V_{DD50}			± 5	µA
C31	Output voltage High-level	V_{OH6}	V_{DD50} = 3.3 V, I_{OH} = -2.0 mA	2.7			V
C32	Output voltage Low-level	V_{OL6}	V_{DD50} = 3.3 V, I_{OL} = 2.0 mA			0.4	

D.A/D Converter Characteristics *12

V_{DD50} = AV_{DD} = 2.7 V to 5.5 V, V_{REFH} = 2.7 V to AV_{DD}
V_{SS} = 0 V
Ta = -40 °C to +105 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D1	A/D converter operation power supply voltage		V_{DD50} = AV_{DD}	2.7		5.5	V
D2	Resolution					10	bit
D3	Non-linearity error	NLE	AV_{DD} = V_{REFH} Vss = 0 V			± 3	LSB
D4	Differential linearity error	DNLE				± 3	
D5	Zero transition voltage				20	100	mV
D6	Full-scale transition voltage			AV_{DD}-100	AV_{DD}-20		
D7	A/D conversion time		AV_{DD} = 5.0 V T_{AD} = 200 ns , clkbus = 20 MHz	3.325			µs
D8			AV_{DD} = 3.3 V T_{AD} = 800 ns , clkbus = 20 MHz	12.925			
D9			T_{AD} = 15.26 µs , clkbus = 20 MHz	244.31			
D10	Sampling time	T_{S1}	T_{AD} = 200 ns	0.4		3.6	
D11		T_{S2}	T_{AD} = 15.26 µs	30.52		274.68	
D12	Analog input voltage	V_{ADIN}		Vss		V_{REFH}	V
D13	Analog input leakage current		AV_{DD} = V_{REFH}, V_{SS} = 0 V At Channel OFF: V_{ADIN} = 0 V to AV_{DD}			± 5	µA
D14	Reference voltage pin input leakage current		AV_{DD} = V_{REFH}, V_{SS} = 0 V At Channel OFF: V_{ADIN} = 0 V to AV_{DD}			± 5	
D15	Ladder resistance	R_{LADD}	V_{DD50} = V_{REFH}, Vss = 0 V	8.5	10.5	12.5	kΩ

*12 Using $AV_{DD} \geq V_{REFH}$
The values of D3 to D6 and D10 to D15 are guaranteed on the condition of AV_{DD} = V_{REFH} = 3.3 V and V_{SS} = 0 V or AV_{DD} = V_{REFH} = 5.0 V and V_{SS} = 0 V.

E.D/A converter characteristics *13

V_{DD50} = AV_{DD} = 2.7 V to 5.5 V, V_{REFH} = 2.7 V to AV_{DD}
V_{SS} = 0 V
Ta = -40 °C to +105 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
E1	D/A converter operation power supply voltage		V_{DD50} = AV_{DD}	2.7		5.5	V
E2	Resolution					10	bit
E3	Reference voltage Low-level	V_{REFL_DA}			V_{SS}		V
E4	Reference voltage High-level	V_{REFH_DA}			AV_{DD}		
E5	Non-linearity error	NLE				± 3	LSB
E6	Differential non-linearity error	DNLE				± 3	
E7	Zero-scale output voltage	V_{ZS}	D9 to D0 = ALL Low-level	0		20	mV
E8	Full-scale output voltage	V_{FS}	D9 to D0 = ALL High-level	AV_{DD}-40		AV_{DD}	
E9	Minimum reference resistance	R_{REF}		28	40	52	kΩ
E10	Settling time	T_{SET}	External capacitor C_L = 15 pF			8	μs

*13 The values of E2 to E10 are guaranteed on the condition of V_{DD50} = AV_{DD} = 3.3 V and V_{SS} = 0 V or V_{DD50} = AV_{DD} = 5.0 V and V_{SS} = 0 V.

1.6.3 AC Characteristics

F. AC Characteristics

The parameter used for the AC characteristic is integer. The range can be set and the setting condition are as follow. Refer to [Chapter Bus Controller] of LSI User's Manual for setting method of each parameter.

Parameter	At reset releasing	Settable range		Setting Condition	
		MIN	MAX		
BCS	3	1	3	-	
EA	15	0	15	-	
BCE	31	2	31	Block 1,2	Set to BCE > REN ≥ EA and BCE > WEN ≥ EA. At EA=0, set to BCN > REN.
REN	31	1	31	Block 1,2	Set to [REN ≥ EA].
WEN	31	1	31	Block 1,2	Set to [WEN ≥ EA].
DW	3	1	3	At EA = 0, set to DW > 1. At EA ≠ 0, set to DW > 0.	

$V_{DD50} = AV_{DD} = V_{REFH}$ = 2.2 V to 5.5 V
V_{SS} = 0 V, C_L = 50 pF
Ta = -40 °C to +105 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Clock Timing. Refer to Figure:1.6.5.							
F1	System clock output cycle time	t_{CYC}		100			ns
F2	System clock output high-level pulse width	t_{CH}		$\frac{t_{CYC}}{2}$ -15			
F3	System clock output low-level pulse width	t_{CL}		$\frac{t_{CYC}}{2}$ -15			

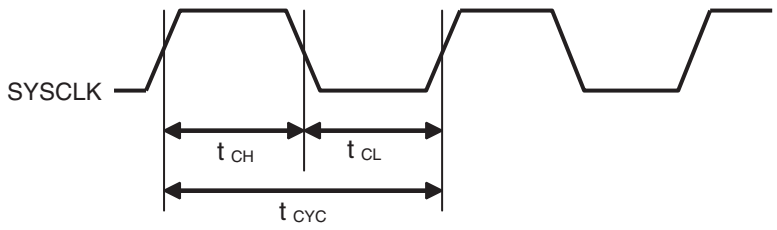
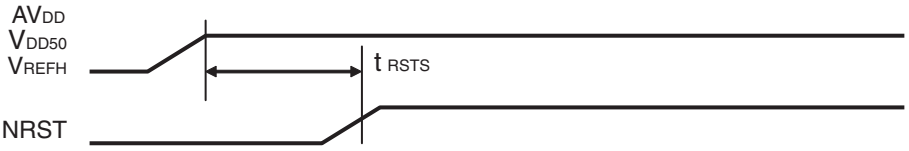


Figure:1.6.5 External Clock Timing

V_{DD50} = AV_{DD} = V_{REFH} = 2.2 V to 5.5 V
V_{SS} = 0 V, C_L = 50 pF
Ta = -40 °C to +105 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Reset timing/Power-On sequence. Refer to Figure:1.6.6							
F4	Reset release timing (NRST)	t_{RSTS}		400			µs
F5	Reset pulse width (NRST)	t_{RSTW}		400			ns
F6	Mode setup timing (NOCDMOD)	t_{MODS}		100			ns

- Power-On Sequence



- Reset pulse width

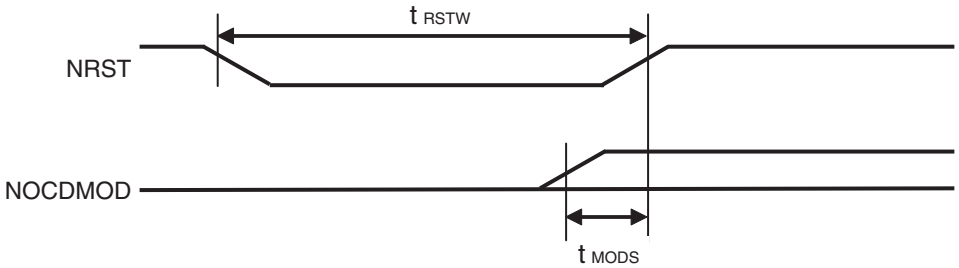


Figure:1.6.6 Power-On Sequence and Reset Pulse Width

$V_{DD50} = AV_{DD} = V_{REFH}$ = 2.2 V to 5.5 V
V_{SS} = 0 V, C_L = 50 pF
Ta = -40 °C to +105 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Address/Data Separate mode. Refer to Figure:1.6.7, Figure:1.6.8. *16							
F7	Address delay time (A[20:0])	t_{AD}		$\frac{t_{CYC}}{n_{fr}}$ x EA-10			ns
F8	Address hold time (A[20:0])	t_{AH}	At reading	$\frac{t_{CYC}}{n_{fr}}$ x (BCE-REN)-10			
			At writing	$\frac{t_{CYC}}{n_{fr}}$ x (BCE-WEN)-10			
F9	Chip select signal falling delay time (NCS[2:1])	t_{CSDF}		$\frac{t_{CYC}}{n_{fr}}$ x EA-10			
F10	Chip select signal rising delay time (NCS[2:1])	t_{CSDR}	At reading	$\frac{t_{CYC}}{n_{fr}}$ x (BCE-REN)-10			
			At writing	$\frac{t_{CYC}}{n_{fr}}$ x (BCE-WEN)-10			
F11	Read data setup time (D[15:0])	t_{RDS}		60			
F12	Read data hold time (D[15:0])	t_{RDH}		0			
F13	Write data setup time (D[15:0])	t_{WDS}		$\frac{t_{CYC}}{n_{fr}}$ x (WEN-EA)-15			
F14	Write data hold time (D[15:0])	t_{WDH}		$\frac{t_{CYC}}{n_{fr}}$ x (BCE-WEN)-15			
F15	Data acknowledge signal setup time (NDK)	t_{DKS}		50			
F16	Data acknowledge signal hold time (NDK)	t_{DKH}		0			
F17	Read enable signal falling delay time (NRE)	t_{REDF}		$\frac{t_{CYC}}{n_{fr}}$ x (BCS+EA)-10			

$V_{DD50} = AV_{DD} = V_{REFH}$ = 2.2 V to 5.5 V
V_{SS} = 0 V, C_L = 50 pF
Ta = -40 °C to +105 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Address/Data Separate mode. Refer to Figure:1.6.7, Figure:1.6.8. *16							
F18	Read enable signal pulse width (NRE)	t_{REW}	At fixed wait	$\frac{t_{CYC}}{n_{fr}}$ x (REN-EA)-10			ns
		t_{HREW}	At handshake	$\frac{t_{CYC}}{n_{fr}}$ x (REN+1)-10			
F19	Write enable signal falling delay time (NWE[1:0])	t_{WEDF}		$\frac{t_{CYC}}{n_{fr}}$ x (BCS+EA)-10			
F20	Write enable signal pulse width (NWE[1:0])	t_{WEW}	At fixed wait	$\frac{t_{CYC}}{n_{fr}}$ x (WEN-EA)-10			
		t_{HWEW}	At handshake	$\frac{t_{CYC}}{n_{fr}}$ x (WEN+1)-10			

*16 The values of F7 to F20 are guaranteed on the condition of V_{DD50} = 3.3 V and V_{SS} = 0 V.

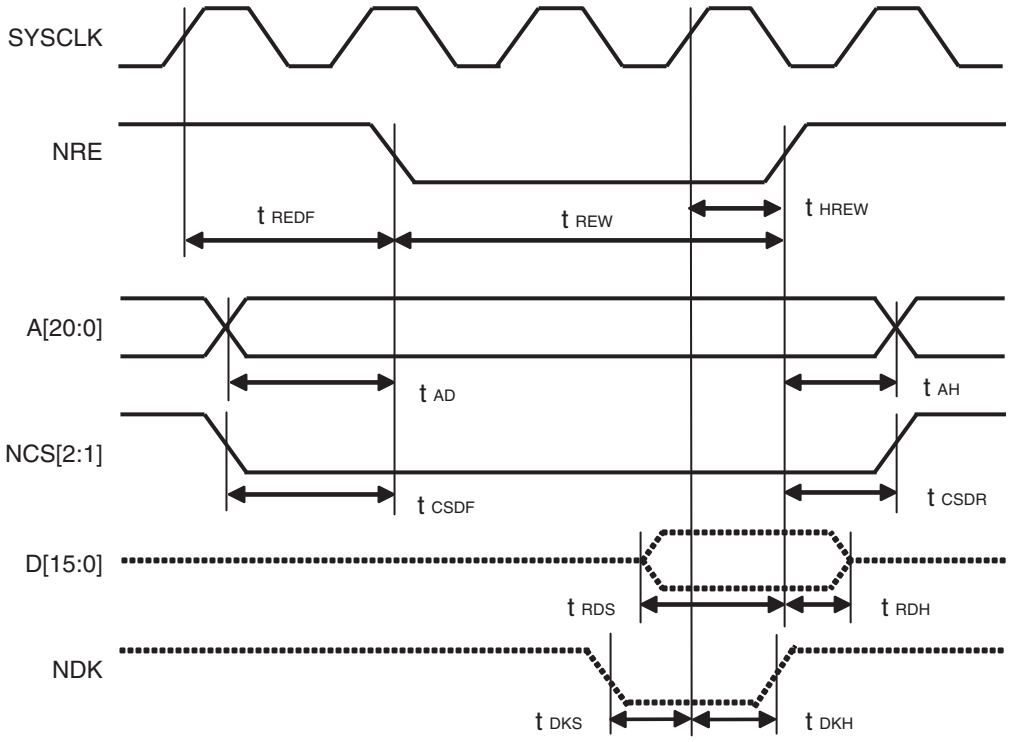


Figure:1.6.7 Separate Address/Data Synchronous Mode Read Timing

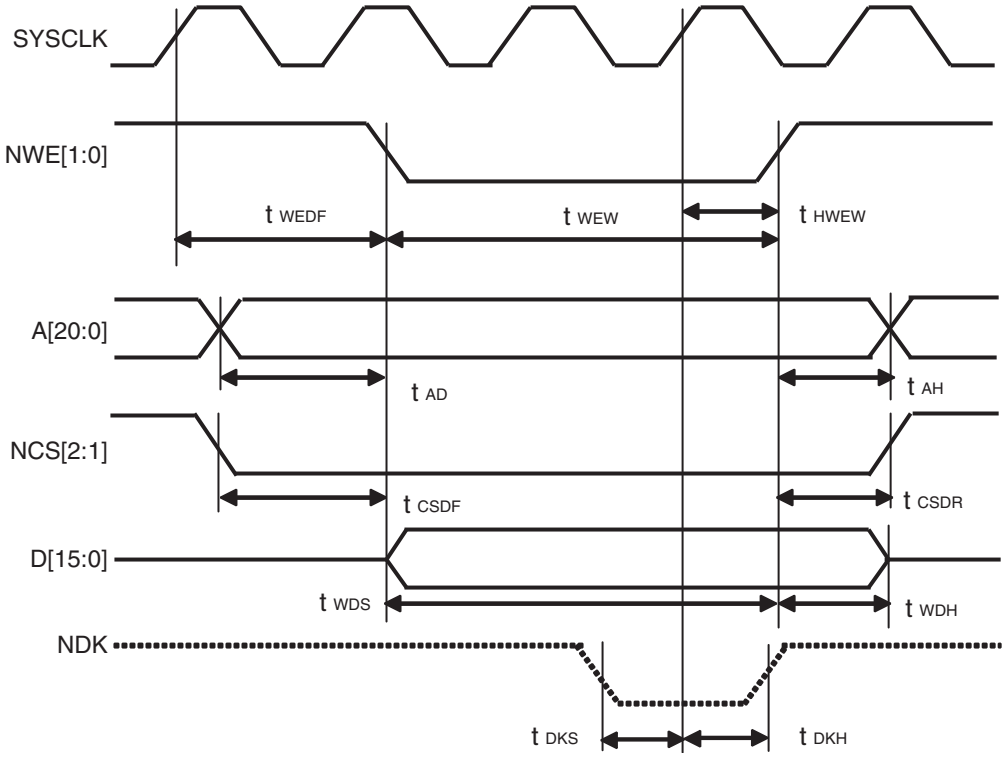


Figure:1.6.8 Separate Address/Data Synchronous Mode Write Timing

$V_{DD50} = AV_{DD} = V_{REFH}$ = 2.2 V to 5.5 V
V_{SS} = 0 V, C_L = 50 pF
Ta = -40 °C to +105 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Interrupt signal input timing Refer to Figure:1.6.9 *17							
F21	Non-maskable interrupt signal pulse width (NMIRQ)	t_{NMIW}		$\frac{t_{CYC}}{n_{fr}} \times 3$			ns
F22	Interrupt signal pulse width (IRQn)	t_{IRQW}		$\frac{t_{CYC}}{n_{fr}} \times 3$			ns

*17 The above-mentioned is standard without noise filter.
When the noise filter is used, the minimum pulse width is determined with the sampling clock.

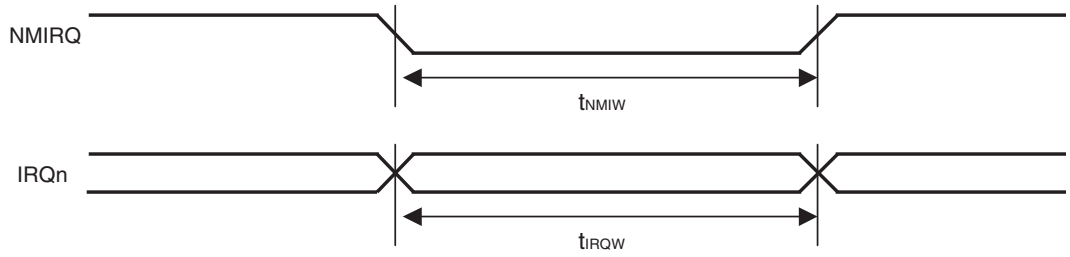


Figure:1.6.9 Interrupt Signal Input Timing

V_{DD50} = AV_{DD} = V_{REFH} = 2.2 V to 5.5 V
V_{SS} = 0 V, C_L = 50 pF
Ta = -40 °C to +105 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
IIC signal I/O timing 1 (SCL clock frequency : max 100 kHz) Refer to Figure:1.6.10.							
F23	Bus free time (SDA0-2)	t_{BUF}		4.7			µs
F24	Hold time of start condition (SCL0-2)	$t_{HD;STA}$		4.0			
F25	Clock Low-level pulse width (SCL0-2)	t_{LOW}		4.7			
F26	Clock High-level pulse width (SCL0-2)	t_{HIGH}		4.0			
F27	Setup time of repeat start condition	$t_{SU;STA}$		4.7			
F28	Hold time of data (SDA0-2)	$t_{HD;DAT}$	At SDA output	300			ns
			At SDA input	0			
F29	Setup time of data (SDA0-2)	$t_{SU;DAT}$		250			
F30	Setup time of stop condition	$t_{SU;STO}$		4.0			µs
IIC signal I/O timing 2 (SCL clock frequency : max 400 kHz) Refer to Figure:1.6.10.							
F31	Bus free time (SDA0-2)	t_{BUF}		1.3			µs
F32	Hold time of start condition (SCL0-2)	$t_{HD;STA}$		0.6			
F33	Clock Low-level pulse width (SCL0-2)	t_{LOW}		1.3			
F34	Clock High-level pulse width (SCL0-2)	t_{HIGH}		0.6			
F35	Setup time of repeat start condition	$t_{SU;STA}$		0.6			
F36	Hold time of data (SDA0-2)	$t_{HD;DAT}$	At SDA output	300			ns
			At SDA input	0			
F37	Setup time of data (SDA0-2)	$t_{SU;DAT}$		100			
F38	Setup time of stop condition	$t_{SU;STO}$		0.6			µs

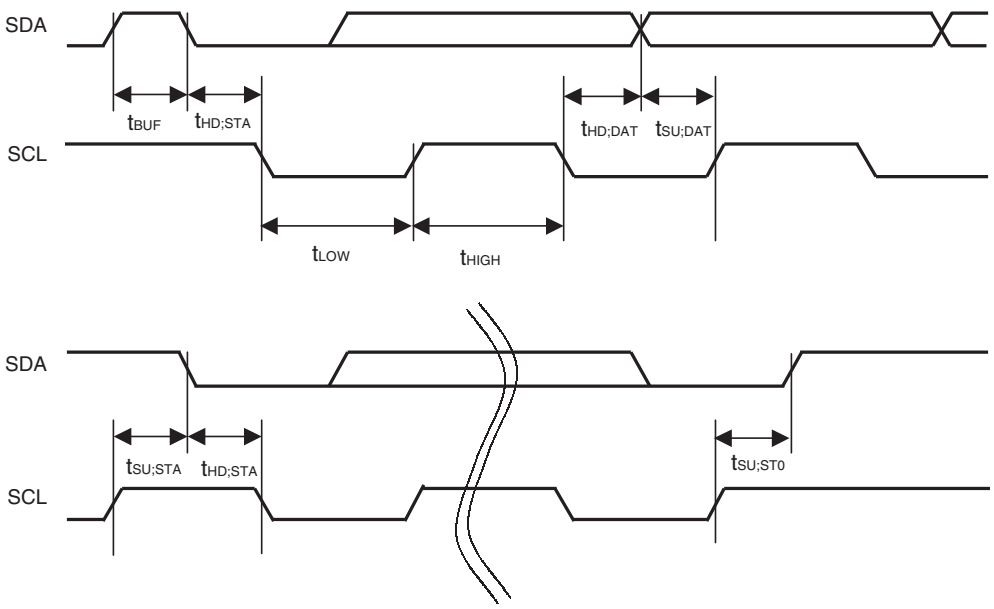


Figure:1.6.10 IIC Signal Timing

V_{DD50} = AV_{DD} = V_{REFH} = 2.2 V to 5.5 V
V_{SS} = 0 V, C_L = 50 pF
Ta = -40 °C to +105 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Serial interface 0 to 10, at Clock Synchronous, I/O timing 1 (at master (SBT polarity “H”)), refer to Figure:1.6.11							
F39	Cycle time	f_{S_CYCLE1}		300			ns
F40	SBT High width	t_{S_HIGH1}		$(t_{S\_CYCLE1}/2)$-17			
F41	SBT Low width	t_{S_LOW1}		$(t_{S\_CYCLE1}/2)$-17			
F42	SBI/SBO setup time	t_{S_SET1}		11			
F43	SBI/SBO hold time	t_{S_HOLD1}		11			
F44	SBO output delay	t_{S_OPD1}				86	
Serial interface 0 to 10, at Clock Synchronous, I/O timing 2 (at slave (SBT polarity “H”)), refer to Figure:1.6.11							
F45	Cycle time	f_{S_CYCLE1}		300			ns
F46	SBT High width	t_{S_HIGH1}		133			
F47	SBT Low width	t_{S_LOW1}		133			
F48	SBI/SBO setup time	t_{S_SET1}		11			
F49	SBI/SBO hold time	t_{S_HOLD1}		11			
F50	SBO output delay	t_{S_OPD1}				86	

V_{DD50} = AV_{DD} = V_{REFH} = 2.2 V to 5.5 V
V_{SS} = 0 V, C_L = 50 pF
Ta = -40 °C to +105 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Serial interface 0 to 4, 9, 10, at Clock Synchronous, I/O timing 3 (at master (SBT polarity “L”)), refer to Figure:1.6.12							
F51	Cycle time	f_{S_CYCLE2}		300			ns
F52	SBT High width	t_{S_HIGH2}		(t_{S_CYCLE2}/2)-17			
F53	SBT Low width	t_{S_LOW2}		(t_{S_CYCLE2}/2)-17			
F54	SBI/SBO setup time	t_{S_SET2}		11			
F55	SBI/SBO hold time	t_{S_HOLD2}		11			
F56	SBO output delay	t_{S_OPD2}				86	
Serial interface 0 to 4, 9, 10, at Clock Synchronous, I/O timing 4 (at slave (SBT polarity “L”)), refer to Figure:1.6.12							
F57	Cycle time	f_{S_CYCLE2}		300			ns
F58	SBT High width	t_{S_HIGH2}		133			
F59	SBT Low width	t_{S_LOW2}		133			
F60	SBI/SBO setup time	t_{S_SET2}		11			
F61	SBI/SBO hold time	t_{S_HOLD2}		11			
F62	SBO output delay	t_{S_OPD2}				86	

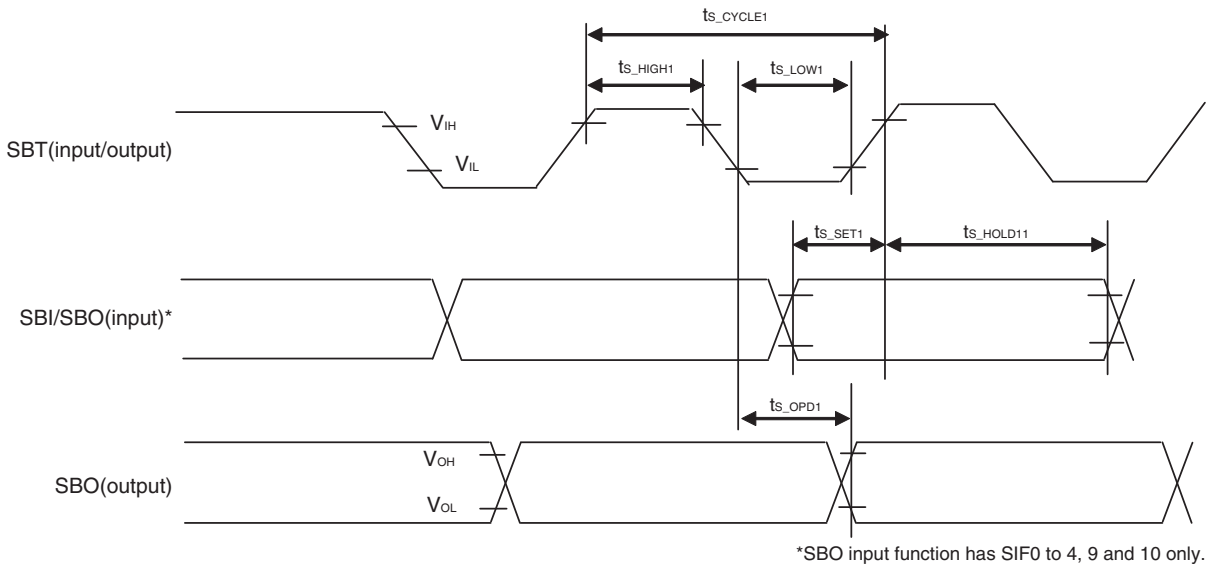


Figure:1.6.11 SIF Signal Timing 1

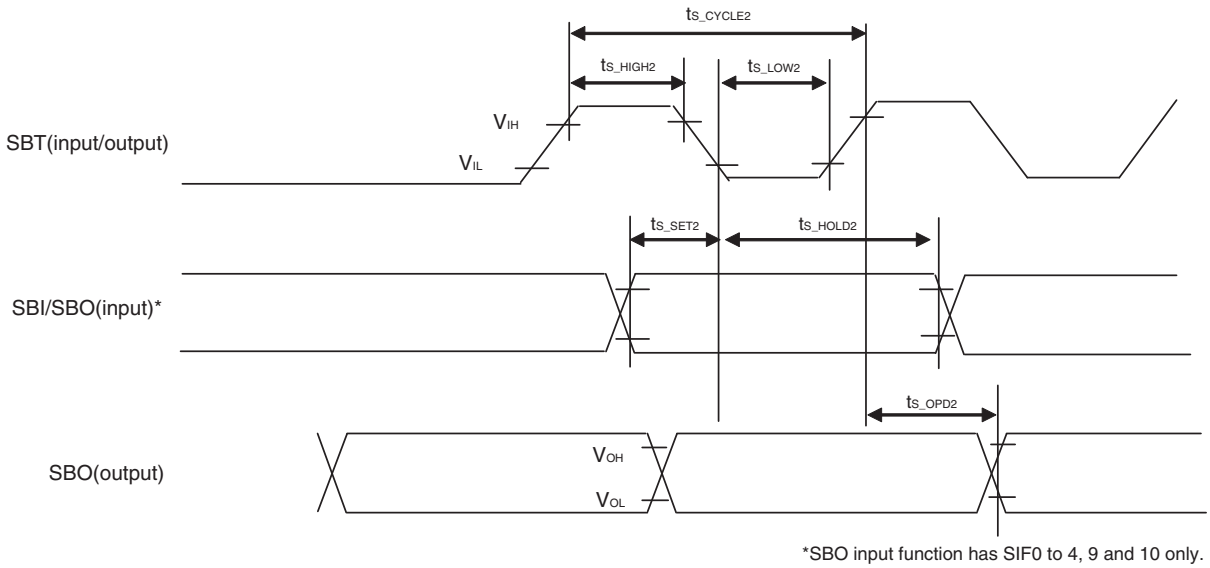


Figure:1.6.12 SIF Signal Timing 2

AC measurement points : $V_{IH} = 0.7 \times V_{DD50}$, $V_{IL} = 0.3 \times V_{DD50}$
$V_{OH} = 0.7 \times V_{DD50}$, $V_{OL} = 0.3 \times V_{DD50}$

V_{DD50} = AV_{DD} = V_{REFH} = 2.2 V to 5.5 V
V_{SS} = 0 V, C_L = 50 pF
Ta = -40 °C to +105 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Serial interface 0 to 10 (UART)							
F63	Maximum transfer rate	f_{UART}				500	Kbps
CAN							
F64	CAN system clock frequency	f_{CAN}				20	MHz
F65	CAN bit rate	bps				1	Mbps
IEBus							
F66	IEBus system clock frequency	f_{IE}	Communication mode : mode1, 2			20	MHz

G. Internal Flash Memory E/W Characteristics

V_{SS} = 0 V

Parameter			Symbol	Conditions	Rating			Unit
					MIN	TYP	MAX	
G1	Power supply voltage at E/W		V_{DD50EW}		2.7		5.5	V
G2	Ambient temperature at E/W		T_{OPREW}		-40		105	°C
G3	Writing time		t_{WRITE}	Per 64 Bytes		1		ms
G4	Blanking time	Large sector	t_{ERASE1}	Per 1 sector		1		s
G5		Small sector	t_{ERASE2}	Per 1 sector		0.5		

H. Auto Reset Characteristics

V_{DD50} = AV_{DD} = V_{REFH} = 2.2 V to 5.5 V
V_{SS} = 0 V
Ta = -40 °C to +105 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
H1	Operating power supply voltage	$V_{DDATRST}$	Auto reset ON	V_{RST}		V_{DD50}	V
H2	Power supply voltage detection level 1	V_{RST1}	At rasing	2.4	2.7	3.0	V
H3	Power supply voltage detection level 2	V_{RST2}	At falling	2.25	2.4	2.55	
H4	Change rate of power supply voltage	$\Delta t/\Delta V$		2.0			ms/V

I. Power Supply Voltage Detection Circuit Characteristics

$V_{DD50} = AV_{DD} = V_{REFH}$ = 2.2 V to 5.5 V
V_{SS} = 0 V
Ta = -40 °C to +105 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
I1	Power supply voltage detection level 1	V_{LVI11}	At rising	2.45	2.6	2.75	V
I2		V_{LVI12}	At falling	2.35	2.5	2.65	
I3	Power supply voltage detection level 2	V_{LVI21}	At rising	2.6	2.8	3.0	
I4		V_{LVI22}	At falling	2.5	2.7	2.9	
I5	Power supply voltage detection level 3	V_{LVI31}	At rising	2.8	3.0	3.2	
I6		V_{LVI32}	At falling	2.7	2.9	3.1	
I7	Power supply voltage detection level 4	V_{LVI41}	At rising	3.0	3.2	3.4	
I8		V_{LVI42}	At falling	2.9	3.1	3.3	
I9	Power supply voltage detection level 5	V_{LVI51}	At rising	3.2	3.4	3.6	
I10		V_{LVI52}	At falling	3.1	3.3	3.5	
I11	Power supply voltage detection level 6	V_{LVI61}	At rising	3.4	3.6	3.8	
I12		V_{LVI62}	At falling	3.3	3.5	3.7	
I13	Power supply voltage detection level 7	V_{LVI71}	At rising	3.6	3.8	4.0	
I14		V_{LVI72}	At falling	3.5	3.7	3.9	
I15	Power supply voltage detection level 8	V_{LVI81}	At rising	3.8	4.0	4.2	
I16		V_{LVI82}	At falling	3.7	3.9	4.1	
I17	Minimum pulse width	T_W			15		ms
I18	Change rate of power supply voltage	$\Delta t/\Delta V$		2.0			ms/V

J. Internal High-speed Oscillation Circuit Characteristics

V_{DD50} = AV_{DD} = V_{REFH} = 2.2 V to 5.5 V
V_{SS} = 0 V
Ta = -40 °C to +105 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
J1	High-speed internal oscillation circuit output frequency	f_{rc}		18	20	22	MHz
J2	Low-speed internal oscillation circuit output frequency	f_{rcx}		27	30	33	kHz

1.7 Package Dimension

■ Package of 100 Pin VersionUnit: mm

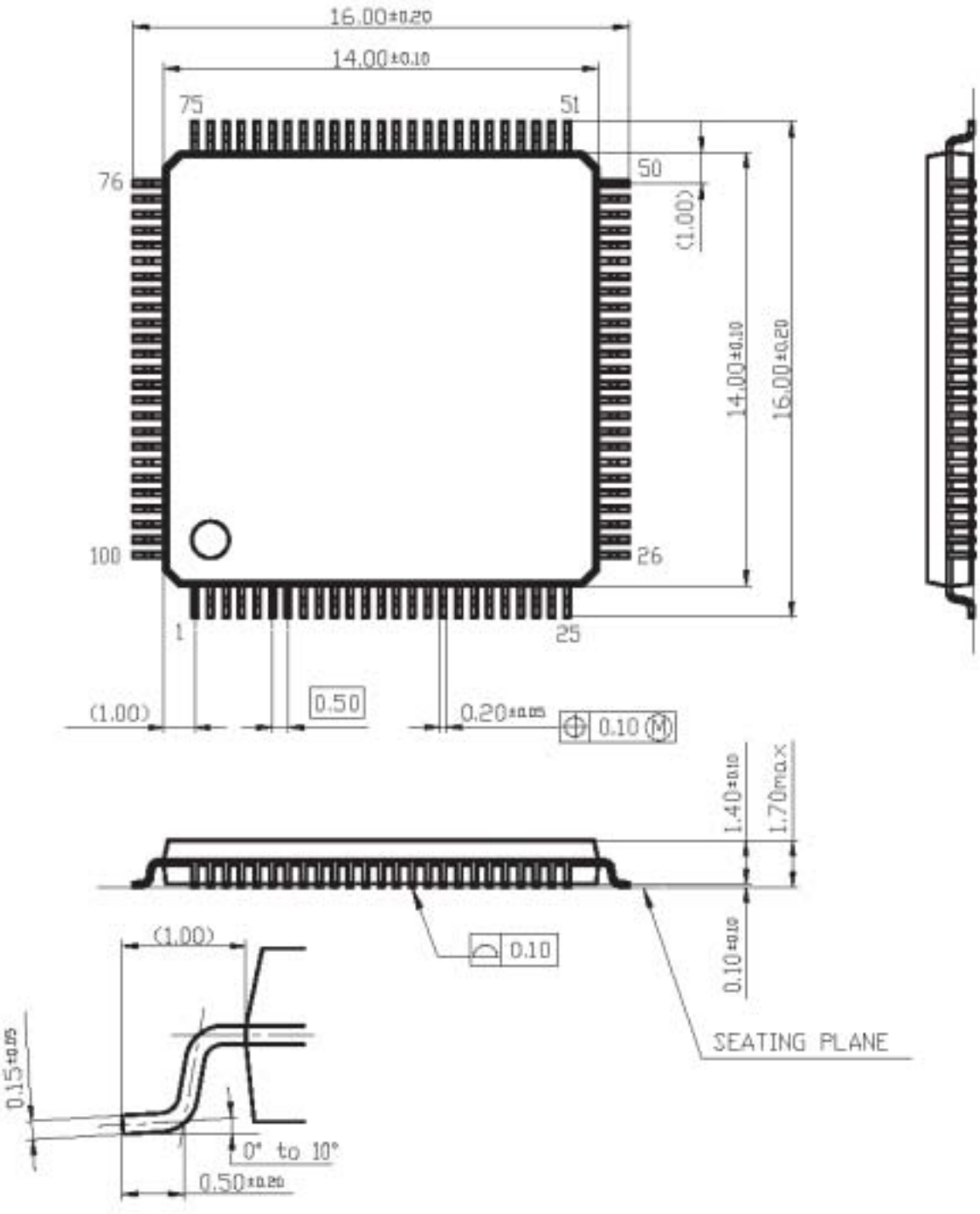


Figure:1.7.1 Package Dimension

■ Package of 128 Pin VersionUnit: mm

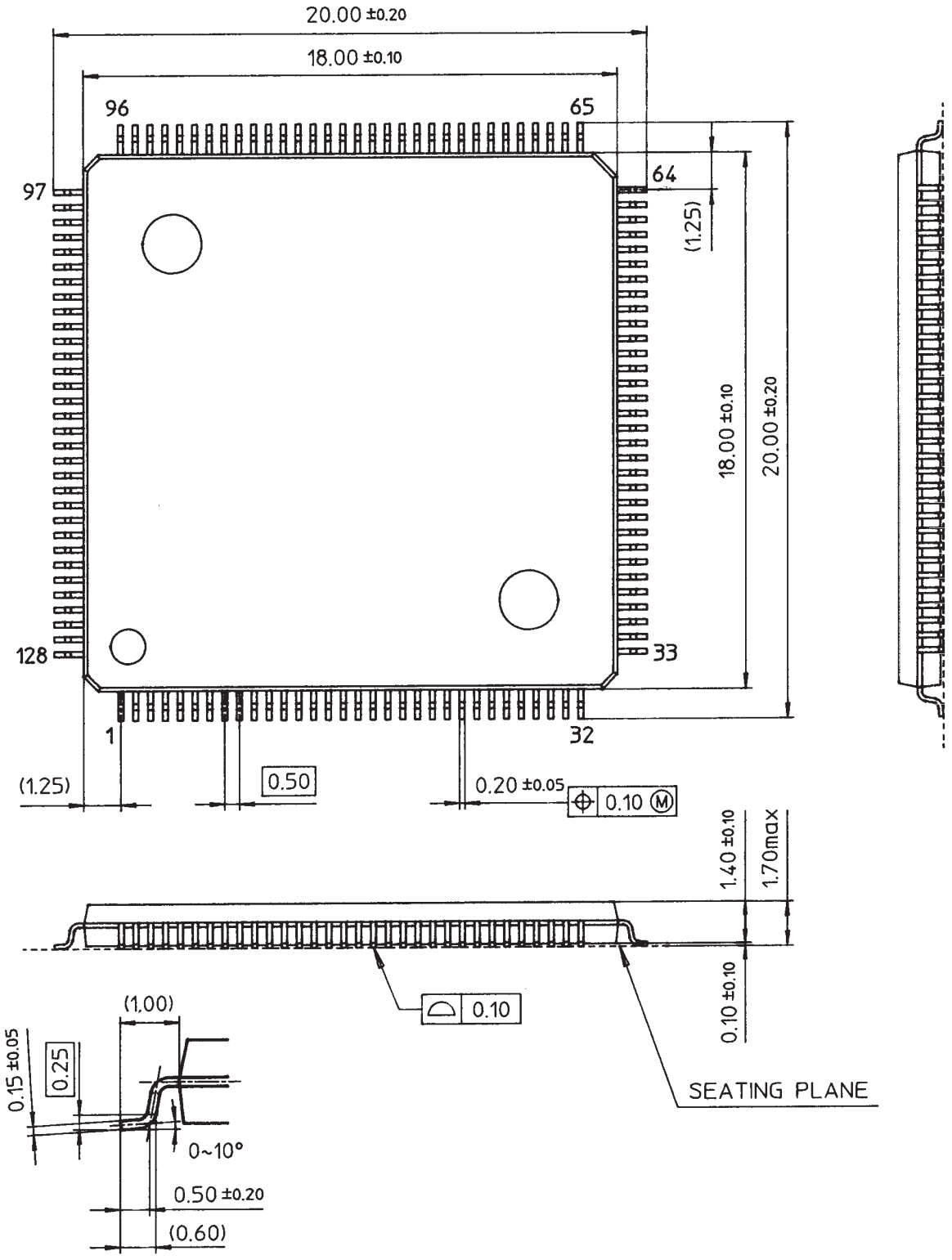


Figure:1.7.2 Package Dimension

■ Package of 144 Pin VersionUnit: mm

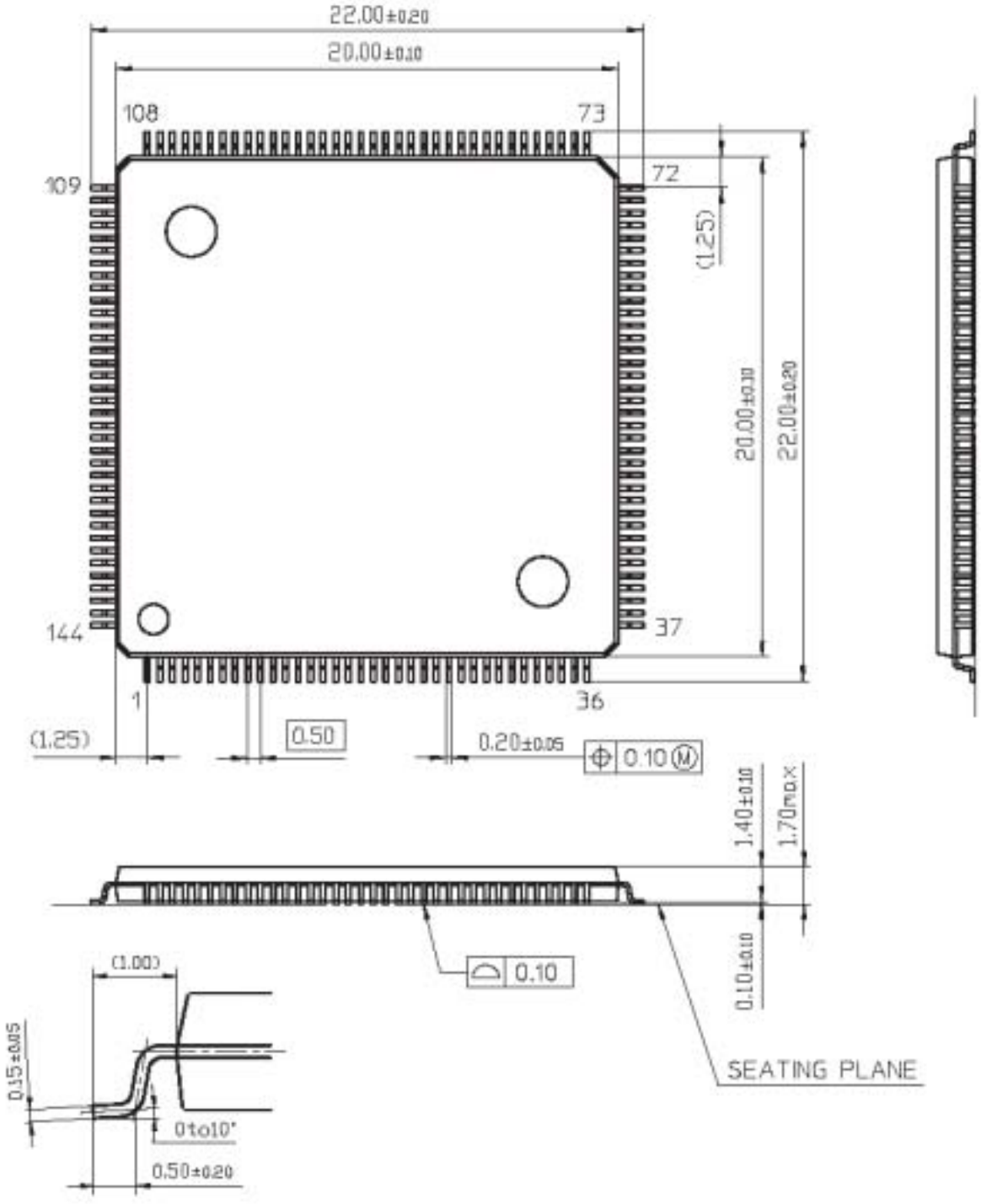


Figure:1.7.3 Package Dimension

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