Document Title
4Bank x 2M x32Bit Synchronous DRAM

Revision History

Revision No.	History	Draft Date	Remark
0.1	Initial Draft	May. 2003	Preliminary
0.2	1) Deleted Preliminary 2) Defined Input/Output Cap. Spec.	Dec. 2003	

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DESCRIPTION

The Hynix HY5V52CFP is a 268,435,456bit CMOS Synchronous DRAM, ideally suited for the memory applications which require wide data I/O and high bandwidth. HY5V52CFP is organized as 4banks of 2,097,152x32.

HY5V52CFP is offering fully synchronous operation referenced to a positive edge of the clock. All inputs and outputs are synchronized with the rising edge of the clock input. The data paths are internally pipelined to achieve very high bandwidth. All input and output voltage levels are compatible with LVTTL.

Programmable options include the length of pipeline (Read latency of 2 or 3), the number of consecutive read or write cycles initiated by a single control command (Burst length of 1,2,4,8 or full page), and the burst count sequence(sequential or interleave). A burst of read or write cycles in progress can be terminated by a burst terminate command or can be interrupted and replaced by a new burst read or write command on any cycle. (This pipelined design is not restricted by a `2N` rule.)

FEATURES

- JEDEC standard 3.3V power supply
- All device pins are compatible with LVTTL interface
- 90Ball FBGA with 0.8mm of pin pitch
- All inputs and outputs referenced to positive edge of system clock
- Data mask function by DQM0,1,2 and 3
- Internal four banks operation
- Auto refresh and self refresh
- 4096 refresh cycles / 64ms
- Programmable Burst Length and Burst Type
  - 1, 2, 4, 8 or full page for Sequential Burst
  - 1, 2, 4 or 8 for Interleave Burst
- Programmable $\overline{\text{CAS}}$ Latency ; 2, 3 Clocks
- Burst Read Single Write operation

ORDERING INFORMATION

Part No.	Clock Frequency	Organization	Interface	Package
HY5V52C(L)FP-6	166MHz	4Banks x 2Mbits x32	LVTTL	90Ball FBGA
HY5V52C(L)FP-H	133MHz	4Banks x 2Mbits x32	LVTTL	90Ball FBGA
HY5V52C(L)FP-8	125MHz	4Banks x 2Mbits x32	LVTTL	90Ball FBGA
HY5V52C(L)FP-P	100MHz	4Banks x 2Mbits x32	LVTTL	90Ball FBGA
HY5V52C(L)FP-S	100MHz	4Banks x 2Mbits x32	LVTTL	90Ball FBGA

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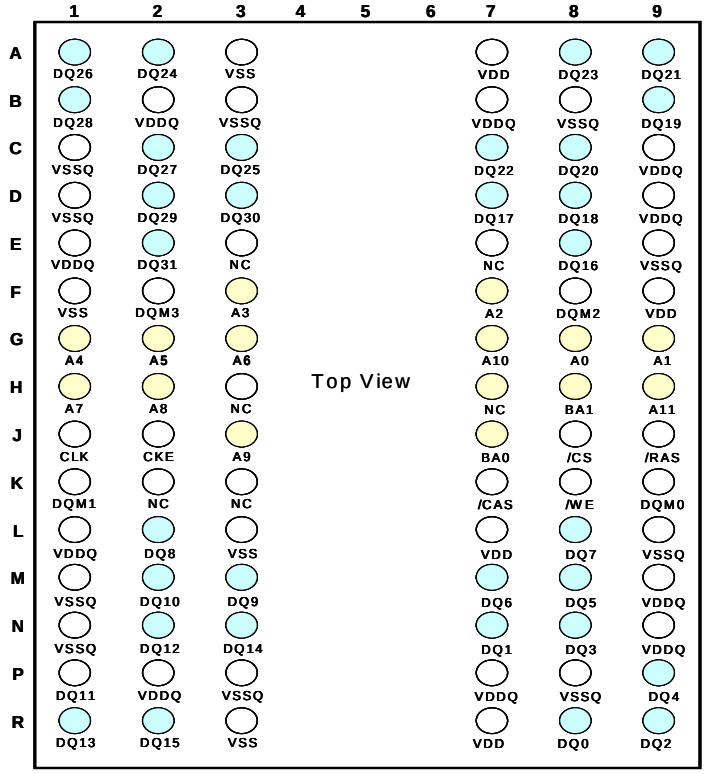
Ball CONFIGURATION



Ball DESCRIPTION

PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK.
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
$\overline{CS}$	Chip Select	Enables or disables all inputs except CLK, CKE and DQM
BA0, BA1	Bank Address	Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
A0 ~ A11	Address	Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA8 Auto-precharge flag : A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
DQM0~3	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ31	Data Input/Output	Multiplexed data input / output pin
V_{DD}/V_{SS}	Power Supply/Ground	Power supply for internal circuits and input buffers
V_{DDQ}/V_{SSQ}	Data Output Power/Ground	Power supply for output buffers
NC	No Connection	No connection

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Ambient Temperature	T_A	0 ~ 70	°C
Storage Temperature	T_{STG}	-55 ~ 125	°C
Voltage on Any Pin relative to V_{SS}	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Short Circuit Output Current	I_{OS}	50	mA
Power Dissipation	P_D	1	W
Soldering Temperature · Time	T_{SOLDER}	260 · 10	°C · Sec

Note : Operation at above absolute maximum rating can adversely affect device reliability

DC OPERATING CONDITION (TA=0 to 70°C)

Parameter	Symbol	Min	Typ.	Max	Unit	Note
Power Supply Voltage	V_{DD}, V_{DDQ}	3.135	3.3	3.6	V	1
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ} + 0.3	V	1,2
Input low voltage	V_{IL}	V_{SSQ} - 0.3	0	0.8	V	1,3

Note :
1.All voltages are referenced to V_{SS} = 0V
2.V_{IH} (max) is acceptable 5.6V AC pulse width with ≤3ns of duration with no input clamp diodes
3.V_{IL} (min) is acceptable -2.0V AC pulse width with ≤3ns of duration with no input clamp diodes

AC OPERATING CONDITION (TA=0 to 70°C, 3.0V ≤V_{DD} ≤3.6V, V_{SS}=0V - Note1)

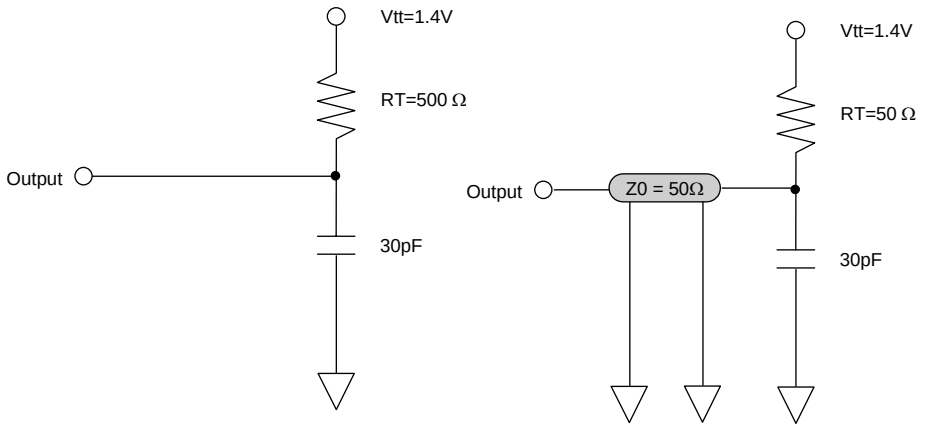
Parameter	Symbol	Value	Unit	Note
AC input high / low level voltage	V_{IH} / V_{IL}	2.4/0.4	V	
Input timing measurement reference level voltage	Vtrip	1.4	V	
Input rise / fall time	tR / tF	1	ns	
Output timing measurement reference level	Voutref	1.4	V	
Output load capacitance for access time measurement	CL	30	pF	1

Note :
1.Output load to measure access times is equivalent to two TTL gates and one capacitor (30pF)
For details, refer to AC/DC output load circuit

CAPACITANCE (TA=25℃, f=1MHz, VDD=3.3V)

Parameter	Pin	Symbol	Min	Max	Unit
Input capacitance	CLK	C_{I1}	5.0	7.0	pF
	A0 ~ A11, BA0, BA1, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$,	C_{I2}	5.0	8.0	pF
	DQM0~3	C_{I3}	2.5	5.0	pF
Data input / output capacitance	DQ0 ~ DQ31	$C_{I/O}$	4.0	6.5	pF

OUTPUT LOAD CIRCUIT



DC Output Load Circuit AC Output Load Circuit

DC CHARACTERISTICS I (DC operating conditions unless otherwise noted)

Parameter	Symbol	Min.	Max	Unit	Note
Input leakage current	I_{LI}	-1	1	uA	1
Output leakage current	I_{LO}	-1	1	uA	2
Output high voltage	V_{OH}	2.4	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	0.4	V	I_{OL} = +2mA

Note :
1.V_{IN} = 0 to 3.6V, All other pins are not under test = 0V
2.D_{OUT} is disabled, V_{OUT}=0 to 3.6V

DC CHARACTERISTICS II (DC operating conditions unless otherwise noted)

Parameter	Symbol	Test Condition		speed					Unit	Note
				-6	-H	-8	-P	S		
Operating Current	IDD1	Burst length=1, One bank active tRC ≥ tRC(min), IOL=0mA		260	240		220		mA	1
Precharge Standby Current in power down mode	IDD2P	CKE ≤ VIL(max), tCK = 10ns		4					mA	
	IDD2PS	CKE ≤ VIL(max), tCK = ∞		2						
Precharge Standby Current in non power down mode	IDD2N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 10ns Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V		30					mA	
	IDD2NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.		30						
Active Standby Current in power down mode	IDD3P	CKE ≤ VIL(max), tCK = 10ns		10					mA	
	IDD3PS	CKE ≤ VIL(max), tCK = ∞		10						
Active Standby Current in non power down mode	IDD3N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCK = 10ns Input signals are changed one time during 2clks. All other pins ≥ VDD-0.2V or ≤ 0.2V		60					mA	
	IDD3NS	CKE ≥ VIH(min), tCK = ∞ Input signals are stable.		40						
Burst Mode Operating Current	IDD4	ttCK ≥ tCK(min), IOL=0mA All banks active	CL=3	300	260		220		mA	1
			CL=2	320	280		240			
Auto Refresh Current	IDD5	tRC ≥ tRC(min), All banks active		480	440		400		mA	2
Self Refresh Current	IDD6	CKE ≤ 0.2V		4					mA	3
				1.6						4

Note :
1.IDD1 and IDD4 depend on output loading and cycle rates. Specified values are measured with the output open
2.Min. of tRRC (Refresh $\overline{RAS}$ cycle time) is shown at AC CHARACTERISTICS II
3.HY5V52CFP-6/H/8/P/S
4.HY5V52CL:FP-6/H/8/P/S

AC CHARACTERISTICS I (AC operating conditions unless otherwise noted)

Parameter		Symbol	-6		-H		-8		-P		-S		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
System clock cycle time	$\overline{CAS}$ Latency = 3	tCK3	6	1000	7.5	1000	8	1000	10	1000	10	1000	ns	
	$\overline{CAS}$ Latency = 2	tCK2	10		10		-10		10		12		ns	
Clock high pulse width		tCHW	2.5	-	3	-	3	-	3	-	3	-	ns	1
Clock low pulse width		tCLW	2.5	-	3	-	3	-	3	-	3	-	ns	1
Access time from clock	$\overline{CAS}$ Latency = 3	tAC3	-	5.4	-	5.5	-	6	-	6	-	6	ns	2
	$\overline{CAS}$ Latency = 2	tAC2	-	6	-	6	-	6	-	6	-	6	ns	
Data-out hold time		tOH	2.7	-	2	-	2	-	2	-	2	-	ns	3
Data-Input setup time		tDS	1.5	-	1.75	-	2	-	2	-	2	-	ns	1
Data-Input hold time		tDH	0.8	-	1	-	1	-	1	-	1	-	ns	1
Address setup time		tAS	1.5	-	1.75	-	2	-	2	-	2	-	ns	1
Address hold time		tAH	0.8	-	1	-	1	-	1	-	1	-	ns	1
CKE setup time		tCKS	1.5	-	1.75	-	2	-	2	-	2	-	ns	1
CKE hold time		tCKH	0.8	-	1	-	1	-	1	-	1	-	ns	1
Command setup time		tCS	1.5	-	1.75	-	2	-	2	-	2	-	ns	1
Command hold time		tCH	0.8	-	1	-	1	-	1	-	1	-	ns	1
CLK to data output in low Z-time		tOLZ	1	-	1	-	1	-	1	-	1	-	ns	
CLK to data output in high Z-time	$\overline{CAS}$ Latency = 3	tOHZ3	2.7	5.4	-	5.5	-	6	-	6	-	6	ns	
	$\overline{CAS}$ Latency = 2	tOHZ2	2.7	5.4	-	6	-	6	-	6	-	6	ns	

Note :

1.Assume tR / tF (input rise and fall time) is 1ns

2.Access times to be measured with input signals of 1v/ns edge rate, 0.8v to 2.0v

3.Data-out hold time to be measured under 30pF load condition, without Vt termination

AC CHARACTERISTICS II (AC operating conditions unless otherwise noted)

Parameter		Symbol	-6		-H		-8		-P		-S		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ cycle time	Operation	tRC	60	-	63	-	64	-	70	-	70	-	ns	
	Auto Refresh	tRRC	60	-	63	-	64	-	70	-	70	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD	18	-	20	-	20	-	20	-	20	-	ns	
$\overline{RAS}$ active time		tRAS	42	100K	42	100K	48	100K	50	100K	50	100K	ns	
$\overline{RAS}$ precharge time		tRP	18	-	20	-	20	-	20	-	20	-	ns	
$\overline{RAS}$ to $\overline{RAS}$ bank active delay		tRRD	12	-	2	-	2	-	20	-	20	-	CLK	
$\overline{CAS}$ to $\overline{CAS}$ delay		tCCD	1	-	1	-	1	-	1	-	1	-	CLK	
Write command to data-in delay		tWTL	0	-	0	-	0	-	0	-	0	-	CLK	
Data-in to precharge command		tDPL	2	-	1	-	1	-	1	-	1	-	CLK	
Data-in to active command		tDAL	5	-	4	-	4	-	4	-	4	-	CLK	
DQM to data-out Hi-Z		tDQZ	2	-	2	-	2	-	2	-	2	-	CLK	
DQM to data-in mask		tDQM	0	-	0	-	0	-	0	-	0	-	CLK	
MRS to new command		tMRD	2	-	2	-	2	-	2	-	2	-	CLK	
Precharge to data output Hi-Z	$\overline{CAS}$ Latency = 3	tPROZ3	3	-	3	-	3	-	3	-	3	-	CLK	
	$\overline{CAS}$ Latency = 2	tPROZ2	2	-	2	-	2	-	2	-	2	-	CLK	
Power down exit time		tPDE	1	-	1	-	1	-	1	-	1	-	CLK	
Self refresh exit time		tSRE	1	-	1	-	1	-	1	-	1	-	CLK	1
Refresh Time		tREF	-	64	-	64	-	64	-	64	-	64	ms	

Note :

1. A new command can be given tRRC after self refresh exit

COMMAND TRUTH TABLE

Command		CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	ADDR	A10/AP	BA	Note
Mode Register Set		H	X	L	L	L	L	X	OP code			
No Operation		H	X	H	X	X	X	X	X			
				L	H	H	H					
Bank Active		H	X	L	L	H	H	X	RA		V	
Read		H	X	L	H	L	H	X	CA	L	V	
Read with Autoprecharge										H		
Write		H	X	L	H	L	L	X	CA	L	V	
Write with Autoprecharge										H		
Precharge All Banks		H	X	L	L	H	L	X	X	H	X	
Precharge selected Bank										L	V	
Burst Stop		H	X	L	H	H	L	X	X			4
DQM		H	X					V	X			
Auto Refresh		H	H	L	L	L	H	X	X			
Burst-Read-Single-WRITE		H	X	L	L	L	L	X	A9 Pin High (Other Pins OP code)			MRS Mode
Self Refresh[1]	Entry	H	L	L	L	L	H	X	X			
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Precharge power down	Entry	H	L	H	X	X	X	X	X			
				L	H	H	H					
	Exit	L	H	H	X	X	X	X				
				L	H	H	H					
Clock Suspend	Entry	H	L	H	X	X	X	X	X			
				L	V	V	V					
	Exit	L	H	X				X				

Note :

1. Exiting Self Refresh occurs by asynchronously bringing CKE from low to high
2. X = Don′t care, H = Logic High, L = Logic Low. BA =Bank Address, RA = Row Address, CA = Column Address, Opcode = Operand Code, NOP = No Operation
3. The burst read sigle write mode is entered by programming the write burst mode bit (A9) in the mode register to a logic 1.
4. This command stops a full-page burst operation, and is illegal otherwise. Full page burst continues untill this command is input. When data input/output is completed for full-page of data, it automatically returns to the start address and input/output is performed repeatedly.

BASIC FUNCTIONAL DESCRIPTION

Mode Register

BA1	BA0		A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0		0	0	0	OP CODE	0	0	CAS Latency			BT	Burst Length		

OP CODE

A9	Write Mode
0	Burst Read and Burst Write
1	Burst Read and Single Write

Burst Type

A3	Burst Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

A2	A1	A0	Burst Length	
			A3 = 0	A3=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

PACKAGE INFORMATION

90Ball FBGA with 0.8mm of pin pitch (using 'Multi Chip Package' Technology)