

DATA SHEET



GPR23L12800B

128M-Bit Mask Rom

DEC. 14, 2009

Version 1.1

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128M-BIT MASK ROM

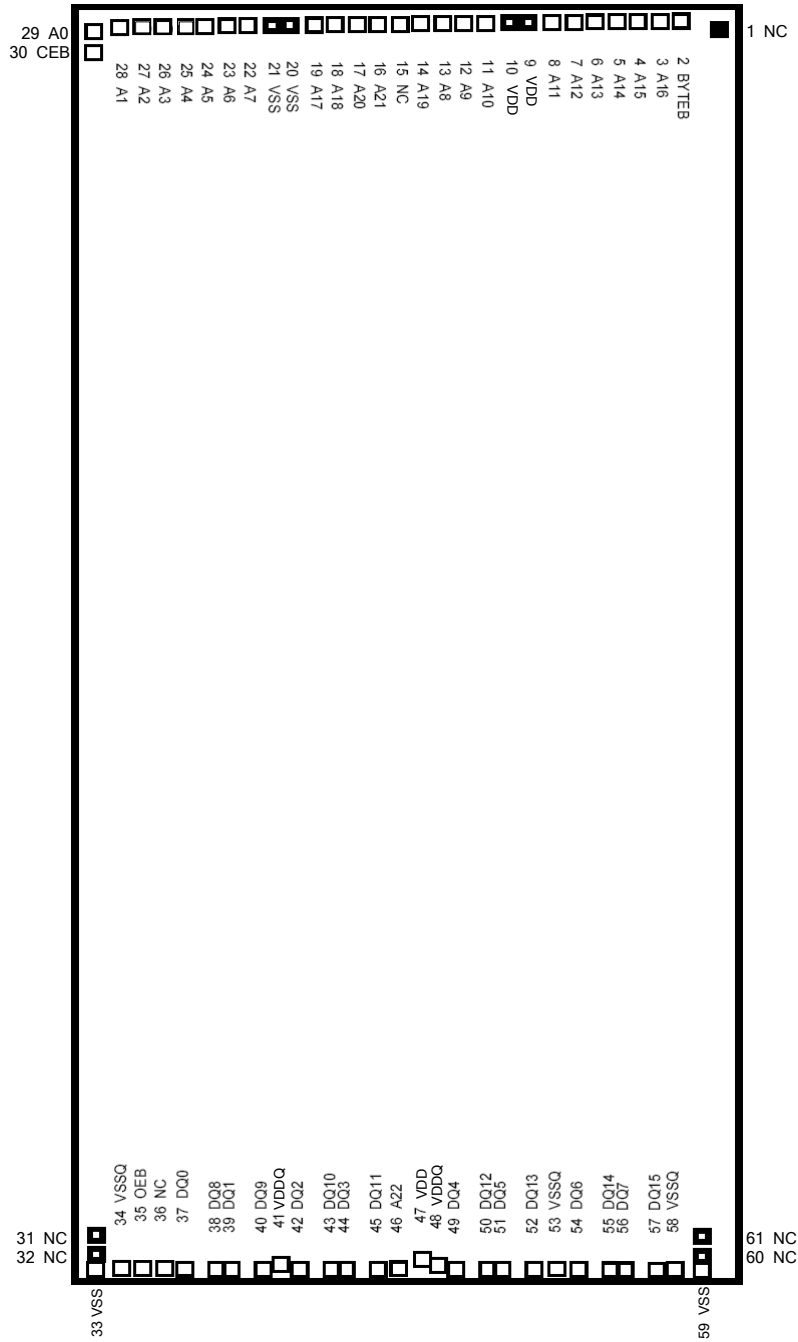
1. FEATURES

- Bit organization
 - 16M x 8 (byte mode)
 - 8M x 16 (word mode)
- Fast access time
 - Random access: 85ns @ 3.0V - 3.6V
90ns @ 2.7V - 3.6V
- Current
 - Operating: 25mA
 - Standby: 15uA
- Temperature
 - 0°C ~ 50°C

2. PIN DESCRIPTION

| Symbol | PIN Function |
|----------|--|
| A0~A22 | Address Inputs |
| DQ0~DQ14 | Data Outputs |
| DQ15/A-1 | D15 (Word Mode)/ LSB Address (Byte Mode) |
| CEB | Chip Enable Input |
| OEB | Output Enable Input |
| BYTEB | Word/ Byte Mode Selection |
| VDD | Power Supply Pin(For Internal Core) |
| VDDQ | Power Supply Pin(For I/O) |
| VSS | Ground Pin(For Internal Core) |
| VSSQ | Ground Pin(For I/O) |
| NC | No Connection |

2.1. Pad Assignment



3. MODE SELECTION

| CEB | OEB | BYTEB | DQ15/A-1 | DQ0~DQ7 | DQ8~DQ15 | Mode | Power |
|-----|-----|-------|----------|---------|----------|------|----------|
| H | X | X | X | High Z | High Z | - | Stand-by |
| L | H | X | X | High Z | High Z | - | Active |
| L | L | H | Output | D0~D7 | D8~D15 | Word | Active |
| L | L | L | Input | D0~D7 | High Z | Byte | Active |

4. ELECTRICAL SPECIFICATIONS

4.1. Absolute Maximum Ratings

| Item | Symbol | Ratings |
|------------------------------------|------------------|----------------|
| Voltage on any Pin Relative to VSS | VIN | -0.3V to 3.9V |
| Ambient Operating Temperature | T _{OPR} | 0°C to 50°C |
| Storage Temperature | T _{STG} | -65°C to 125°C |

4.2. DC Characteristics (T_A = 0°C ~ 50°C, VDD = 2.7V~3.6V)

| Item | Symbol | Min. | Max. | Conditions |
|------------------------|--------|---------|---------|---|
| Output High Voltage | VOH | 2.4V | - | IOH = -400uA |
| Output Low Voltage | VOL | - | 0.4V | IOL = 1.6mA |
| Input High Voltage | VIH | 0.7xVDD | VDD+0.3 | |
| Input Low Voltage | VIL | -0.3V | 0.8V | |
| Input Leakage Current | ILI | - | 5uA | 0V, VDD |
| Output Leakage Current | ILO | - | 5uA | 0V, VDD |
| Operating Current | ICC | - | 25mA | f=5MHz, CEB=VIL, OEB=VIH all output open |
| Standby Current (CMOS) | ISTB | - | 15uA | CEB>VDD-0.2V |
| Input Capacitance | CIN | - | 10pF | T _A = 25°C, f = 1MHZ |
| Output Capacitance | COUT | - | 10pF | T _A = 25°C, f = 1MHZ |

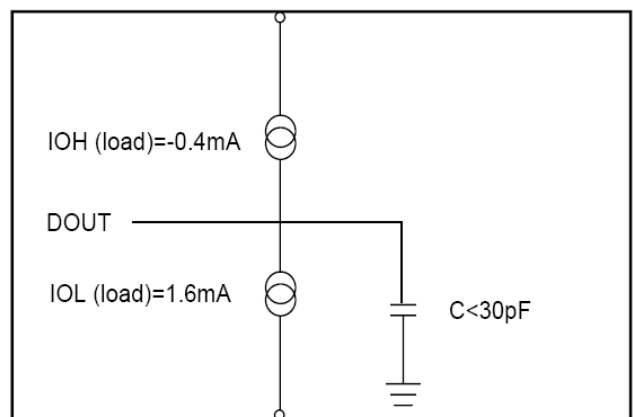
4.3. AC Characteristics (T_A = 0°C ~ 50°C)

| Item | Symbol | VDD=2.7V~3.6V | | VDD=3.0V~3.6V | |
|---------------------------|--------|---------------|------|---------------|------|
| | | Min. | Min. | Max. | Max. |
| Read Cycle Time | tRC | 90ns | - | 85ns | - |
| Address Access Time | tAA | - | 90ns | - | 85ns |
| Chip Enable Access Time | tCE | - | 90ns | - | 85ns |
| Output Enable Time | tOE | - | 25ns | - | 25ns |
| Output Hold After Address | tOH | 0ns | - | 0ns | - |
| Output High Z Delay | tHZ | - | 20ns | - | 20ns |

4.4. AC Test Conditions

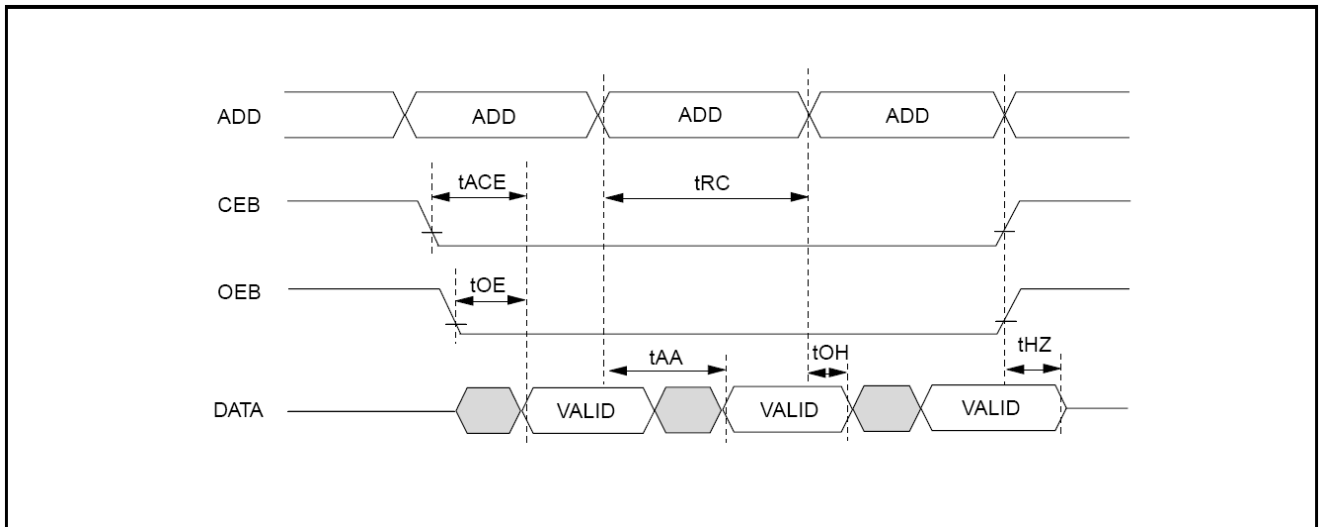
| | |
|---------------------------|------------|
| Input Pulse Levels | 0.4V~ 2.4V |
| Input Rise and Fall Times | 5ns |
| Input Timing Level | 1.5V |
| Output Timing Level | 1.5V |
| Output Load | See Figure |

Note: No output loading is present in tester load board. Active loading is used and under software programming control. Output loading capacitance includes load board's and all stray capacitance.



4.5. Timing Diagram

4.5.1. Random Read



Note: It will fail to read 1st data from GPR23L12800B after power on if CEB is always set to ground level. Please refer the application note for further details.

5. APPLICATION NOTE

5.1. Power Pad Bonding Guideline

1. Except NC pads, all the other Power pads should be wire bonded, please do not keep them floating.
2. Please keep the PCB layout width \geq 20 mil for the VDD/VDDQ and VSS/VSSQ.(Figure 2)
3. For better noise immunity, it is recommended to add Bead (300mA minimum) and Bypass capacitor near to the VDD/VDDQ pins. (Figure 3)

5.2. PCB Layout Suggestion

1. The Substrate should be floating, not connected to GROUND.
2. Each Power pad (VDD/VDDQ, VSS/VSSQ) should be wire bonded to a dedicated power pin, then keep one centimeter distance at least before the user want to merge the PCB layout for those pins , can not be just bonded each Power pad to the same power pin.(Figure 4)
3. The Address and Data bus lines of MROM should be separated away in PCB layout.
4. Each Control pin (CEB or OEB) should be shielded by GROUND lines.
5. If the Connector is adopted in the PCB, it is recommended to connect more sets of connections to VSS/VSSQ and VDD/VDDQ for both the PCB and the system.

Figure 2. Power Pin Pitch

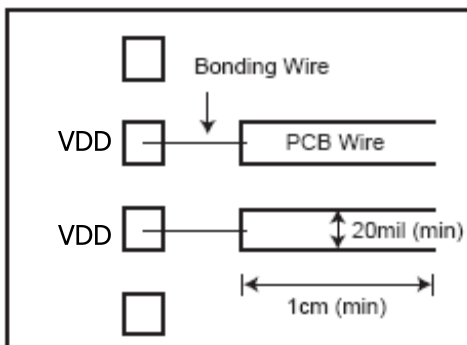


Figure 4. Dedicated Power Pin

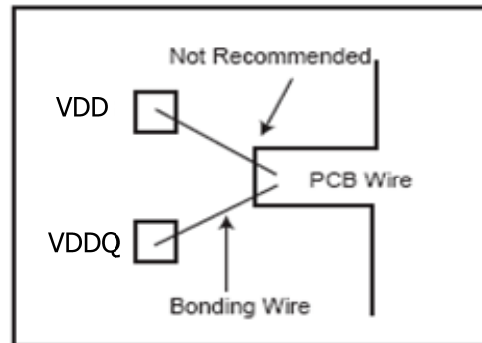
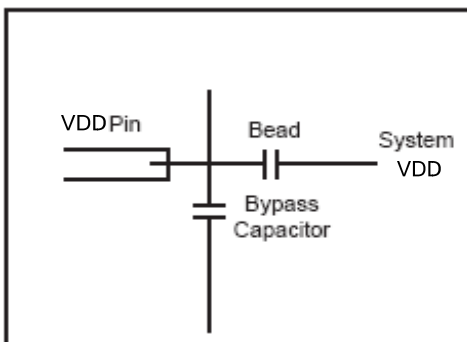


Figure 3. Bead and Bypass Capacitor to Power Pin



6. PACKAGE/PAD LOCATIONS

6.1. Ordering Information

| Product Number | Package Type |
|---------------------|--------------|
| GPR23L12800B-NnnV-C | Chip form |

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

7.DISCLAIMER

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8. REVISION HISTORY

| Date | Revision # | Description | Page |
|---------------|------------|--|------|
| DEC. 14, 2009 | 1.1 | 1. Modify 1.FEATURES. | 3 |
| | | 2. Modify 2.Pin Description. | 3 |
| | | 3. Modify 2.1 Pad Assignment. | 4 |
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| | | 6. Add 5. APPLICATION NOTE. | 8 |
| AUG. 16, 2007 | 1.0 | Original | 8 |