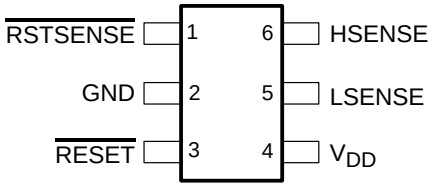
- **Dual Voltage Detector With Adjustable Hysteresis 3.3-V/Adjustable and 2-V/Adjustable**
- **Assured Reset at V_{DD} = 0.8 V**
- **Supply Current: 3 μA Typical at V_{DD} = 3.3 V**
- **Independent Open-Drain Reset Outputs**
- **Temperature Range . . . –40°C to 85°C**
- **Six-Pin SOT-23 Package**

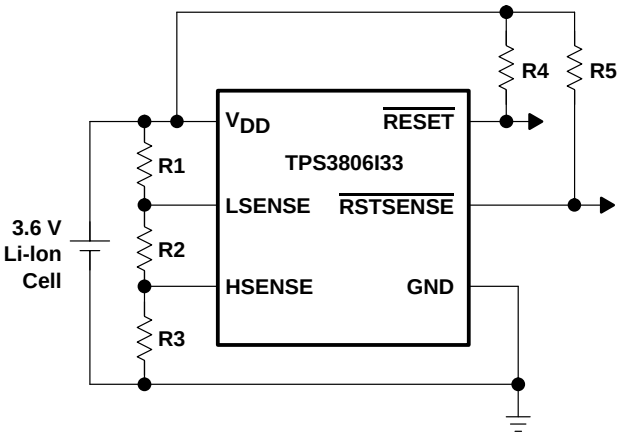
TPS3806
DBV PACKAGE
(TOP VIEW)



description

The TPS3806 integrates two independent voltage detectors for battery voltage monitoring. During power-on, $\overline{\text{RESET}}$ and $\overline{\text{RSTSENSE}}$ are asserted when supply voltage V_{DD} or the voltage at LSENSE input become higher than 0.8 V. Thereafter, the supervisory circuit monitors V_{DD} and LSENSE, keeping $\overline{\text{RESET}}$ and $\overline{\text{RSTSENSE}}$ active as long as V_{DD} and LSENSE remain below the threshold voltage V_{IT}. As soon as V_{DD} or LSENSE rise above the threshold voltage V_{IT}, $\overline{\text{RESET}}$ or $\overline{\text{RSTSENSE}}$ is deasserted, respectively. The TPS3806 device has a fixed-sense threshold voltage V_{IT} set by an internal voltage divider at V_{DD} and an adjustable second-LSENSE input. In addition, an upper voltage threshold can be set at HSENSE to allow a wide adjustable hysteresis window.

typical operating circuit



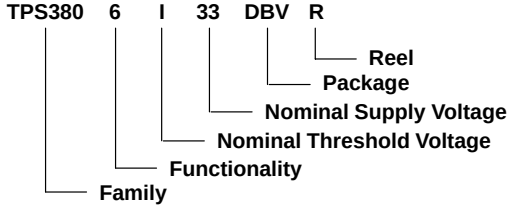
The devices are available in a 6-pin SOT-23 package. The TPS3806 device is characterized for operation over a temperature range of –40°C to 85°C.

PACKAGE INFORMATION

T_A	DEVICE NAME		THRESHOLD VOLTAGE		MARKING
			V_{DD}	SENSE	
–40°C to 85°C	TPS3806J20DBVR†	TPS3806J20DBVT‡	1.8 V	1.207 V	PGQI
	TPS3806I33DBVR†	TPS3806I33DBVT‡	3 V	1.207 V	PGPI

† The DBVR passive indicates tape and reel containing 3000 parts.
‡ The DBVT passive indicates tape and reel containing 250 parts.

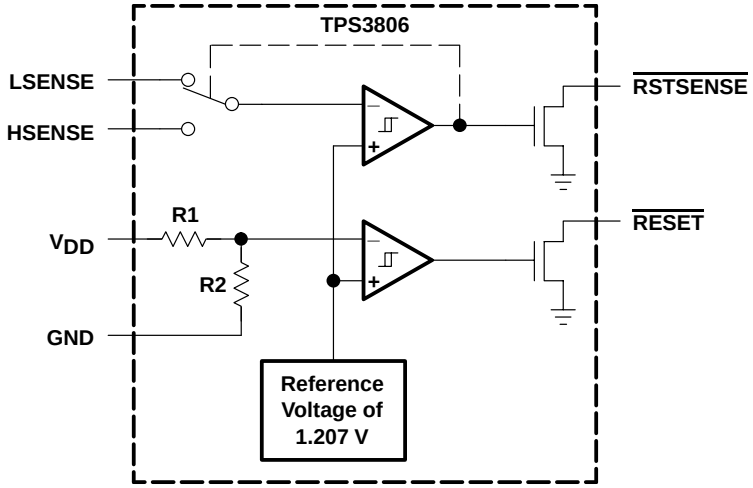
ordering information



Function/Truth Tables

TPS3806			
$V_{DD} > V_{IT}$	$\overline{\text{RESET}}$	LSENSE > V_{IT}	$\overline{\text{RSTSENSE}}$
0	L	0	L
1	H	1	H

functional block diagram



detailed description

operation

The TPS3806 is used for monitoring battery voltage and asserting $\overline{\text{RESET}}$ when battery gets discharged below a certain threshold voltage. The battery voltage is monitored by a comparator via an external resistor divider. When the voltage at the LSENSE input drops below the internal reference voltage the $\overline{\text{RSTSENSE}}$ output pulls low. The output remains low until the battery is replaced, or recharged above a second higher trip-point,set at HSENSE. A second voltage can be monitored at V_{DD}. The independent $\overline{\text{RESET}}$ output pulls low when the voltage at V_{DD} drops below the fixed threshold voltage. Because the TPS3806 outputs are open-drain MOSFETs, most applications may require a pullup resistor.

programming the threshold voltage levels

The low-voltage threshold at LSENSE is calculated as follows:

$$V_{(LSENSE)} = V_{ref}\left(\frac{R1 + R2 + R3}{R2 + R3}\right)$$

where V_{ref} = 1.207 V

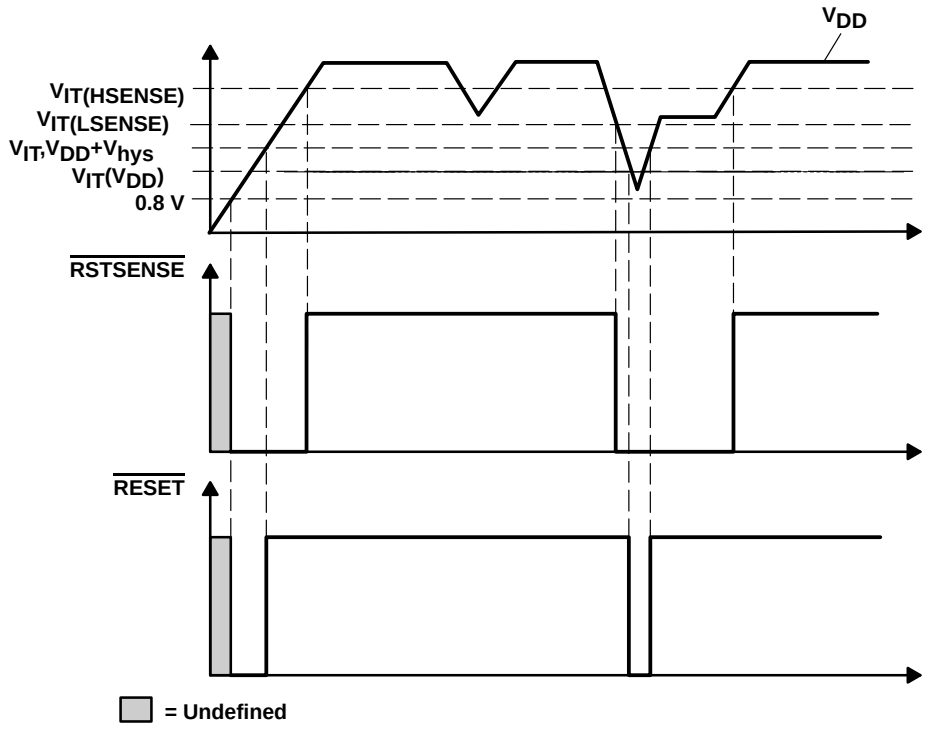
The high-voltage threshold at HSENSE is calculated as follows:

$$V_{(HSENSE)} = V_{ref}\left(\frac{R1 + R2 + R3}{R3}\right)$$

where V_{ref} = 1.207 V

To minimize battery current draw it is recommended to use 1-MΩ as the total resistor value $R_{(tot)}$ = R1 + R2 + R3.

timing requirements



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	2	I	Ground
HSENSE	6	I	Adjustable hysteresis input
LSENSE	5	I	Adjustable sense input
$\overline{\text{RESET}}$	3	O	Active-low open drain reset output (from V_{DD})
$\overline{\text{RSTSENSE}}$	1	O	Active-low open-drain reset output (from LSENSE)
V_{DD}	4	I	Input supply voltage and fixed sense input

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note1) . . . . . 7 V
All other pins (see Note 1) . . . . . –0.3 V to 7 V
Maximum low-output current, I_{OL} . . . . . 5 mA
Maximum high-output current, I_{OH} . . . . . –5 mA
Input clamp current, I_{IK} (V_I<0 or V_I>V_{DD}) . . . . . ±10 mA
Output clamp current, I_{OK} (V_O<0 or V_O>V_{DD}) . . . . . ±10 mA
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Soldering temperature . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to GND. For reliable operation the device must not be continuously operated at 7 V for more than t=1000 h.

DISSIPATION RATING TABLE

PACKAGE	T_A <25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DBV	437 mW	3.5 mW/°C	280 mW	227 mW

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{DD}	1.3	6	V
Input voltage, V_I	0	V_{DD}+0.3	V
Operating free-air temperature range, T_A	–40	85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage		V_{DD} = 1.5 V, I_{OL} = 1 mA				
			V_{DD} = 3.3 V, I_{OL} = 2 mA			0.3	V
			V_{DD} = 6 V, I_{OL} = 3 mA				
	Power-up reset voltage (see Note 2)		$V_{DD} \geq$ 0.8 V, I_{OL} = 50 µA			0.2	V
V_{IT}	Negative-going input threshold voltage (see Note 3)	LSENSE	T_A =25°C	1.198	1.207	1.216	V
		TPS3806J20		1.787	1.8	1.813	
		TPS3806I33		2.978	3	3.022	
		LSENSE	T_A = –40°C to 85°C	1.183	1.207	1.231	V
		TPS3806J20		1.764	1.8	1.836	
		TPS3806I33		2.94	3	3.06	
V_{hys}	Hysteresis		1.2 V < V_{IT} < 2.5 V		60		mV
			2.5 V < V_{IT} < 3.5 V		90		
I_I	Input current	LSENSE, HSENSE		–25		25	nA
I_{OH}	High-level output current		V_{DD} = V_{IT} + 0.2 V, V_{OH} = V_{DD}			300	nA
I_{DD}	Supply current		V_{DD} = 3.3 V, Output unconnected		3	5	µA
			V_{DD} = 6 V, Output unconnected		4	6	
C_i	Input capacitance		V_I = 0 V to V_{DD}		1		pF

NOTES: 2. The lowest supply voltage at which $\overline{\text{RESET}}$ becomes active. $t_{r,VDD} \geq 15$ µs/V
3. To ensure best stability of the threshold voltage, place a bypass capacitor (ceramic, 0.1 µF) near the supply terminals.

timing requirements at R_L = 1 MΩ, C_L = 50 pF, T_A = –40°C to 85°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_w	Pulse width	At V_{DD}	V_{IH} = 1.05 x V_{IT}, V_{IL} = 0.95 x V_{IT}	5.5			µs
		At SENSE					

switching characteristics at R_L = 1 MΩ, C_L = 50 pF, T_A = –40°C to 85°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to $\overline{\text{RESET}}$ delay	V_{IH} = 1.05 x V_{IT}, V_{IL} = 0.95 x V_{IT}		5	100	µs
		LSENSE to $\overline{\text{RSTSENSE}}$ delay					
t_{PLH}	Propagation (delay) time, low-to-high-level output	V_{DD} to $\overline{\text{RESET}}$ delay			5	100	µs
		HSENSE to $\overline{\text{RSTSENSE}}$ delay					

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

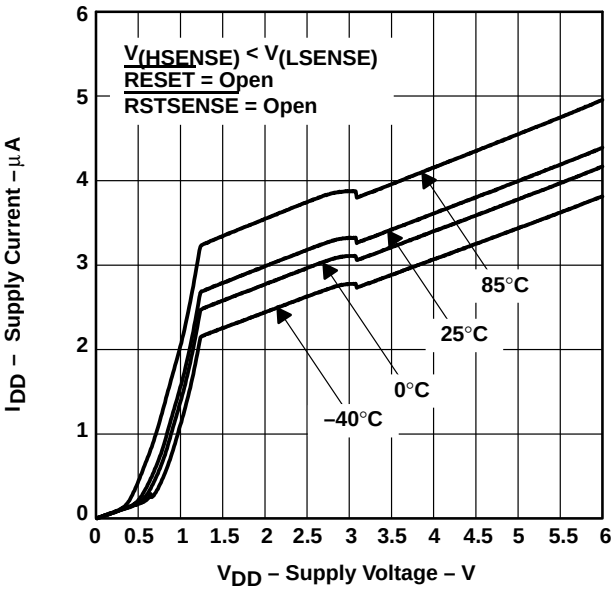


Figure 1

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

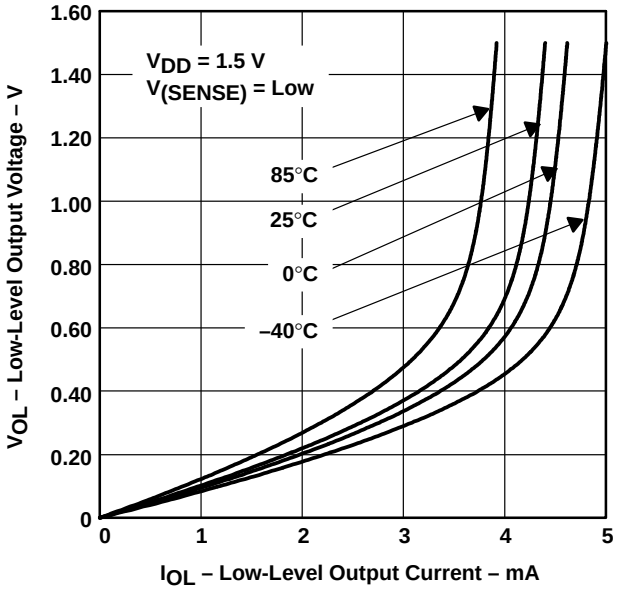


Figure 2

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

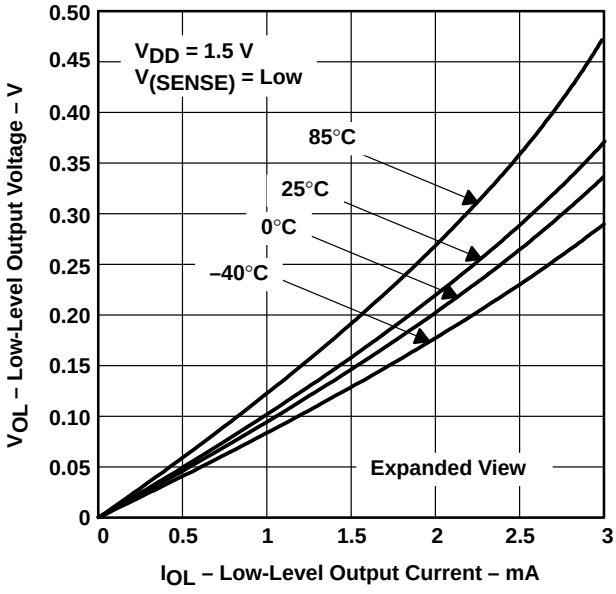


Figure 3

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

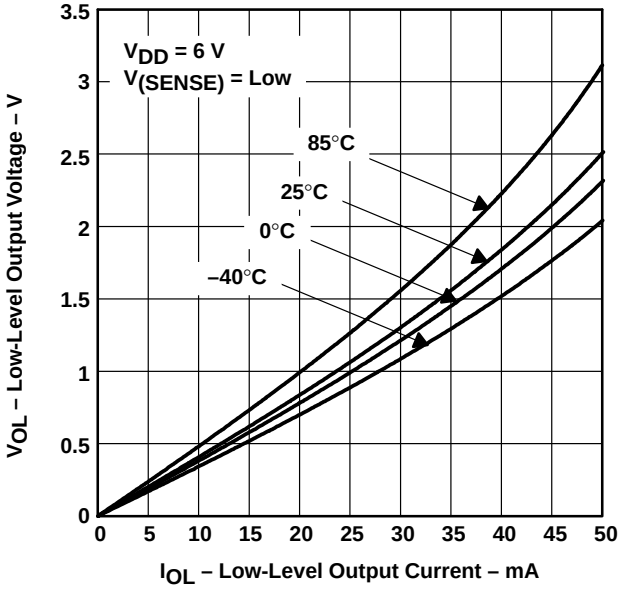


Figure 4

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

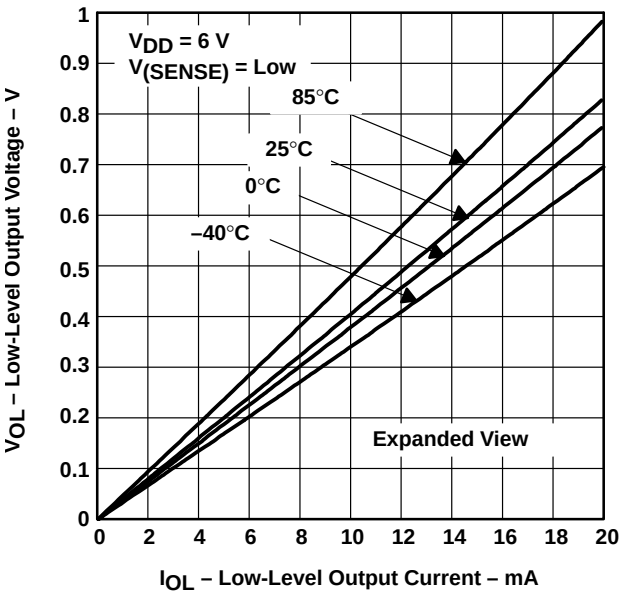


Figure 5

NORMALIZED INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE AT V_{DD}

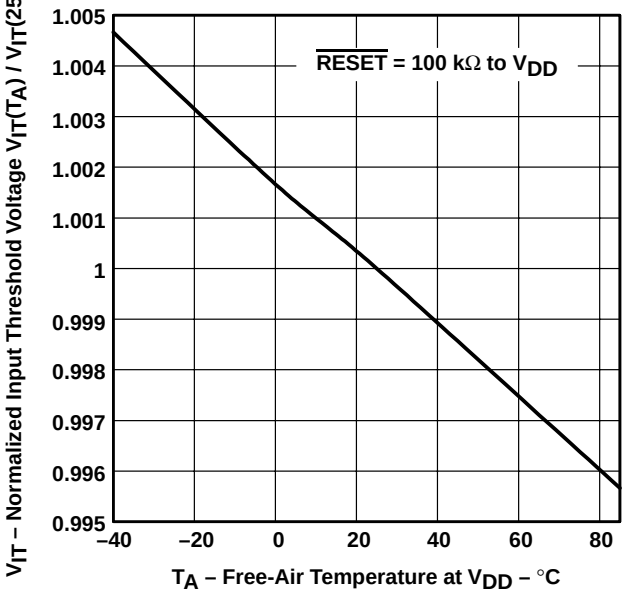


Figure 6

MINIMUM PULSE DURATION AT V_{DD} vs V_{DD} THRESHOLD OVERDRIVE VOLTAGE

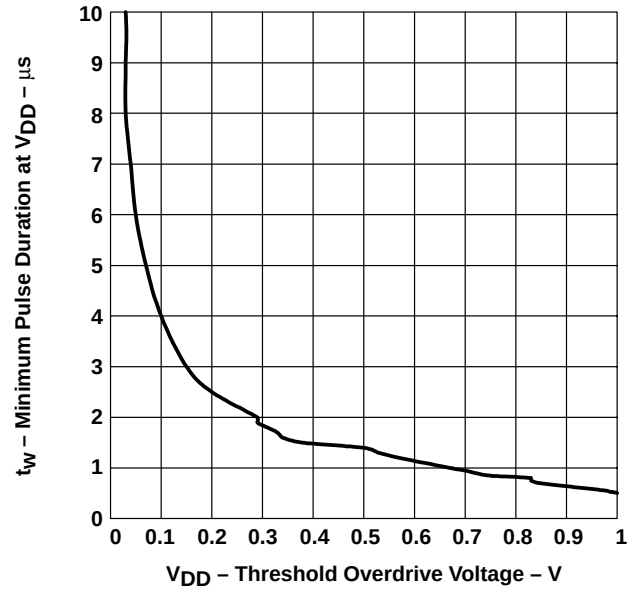


Figure 7

MINIMUM PULSE DURATION AT LSENSE vs LSENSE THRESHOLD OVERDRIVE VOLTAGE

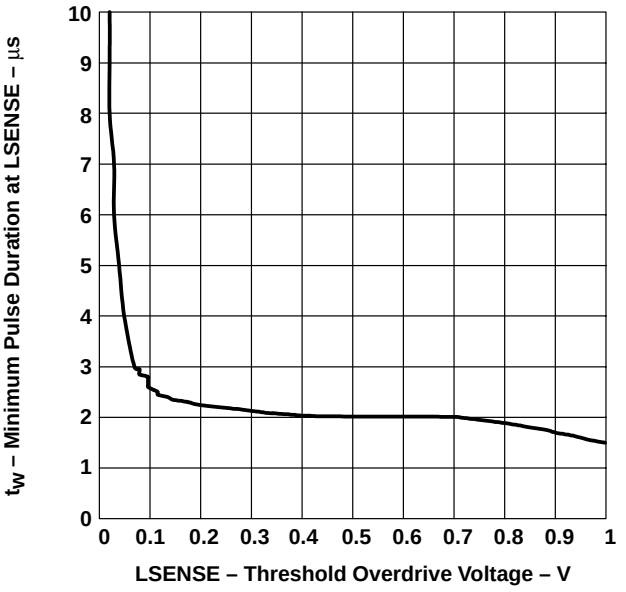
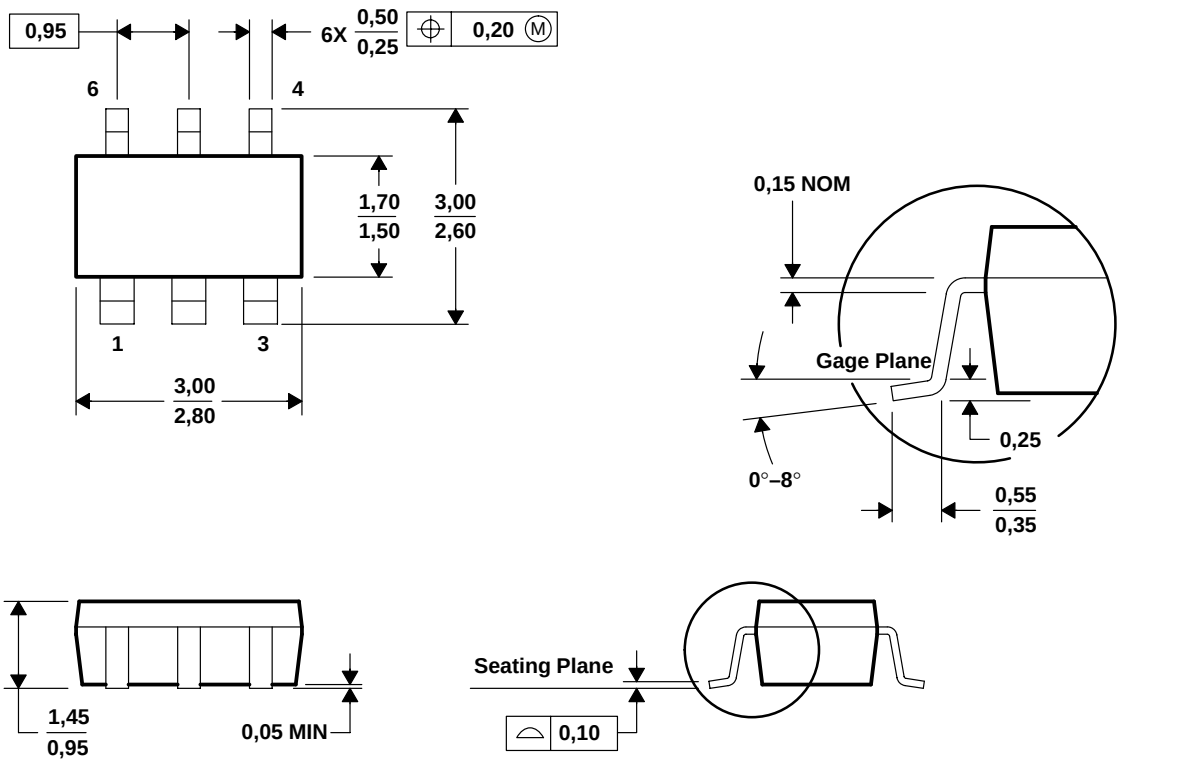


Figure 8

MECHANICAL DATA

DBV (R-PDSO-G6) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Leads 1, 2, 3 are wider than leads 4, 5, 6 for package orientation.

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