3.3V PROGRAMMABLE SKEW PLL CLOCK DRIVER TURBOCLOCK™ II PLUS

IDT5V996

FEATURES:

- **3.3V operation**
- **4 pairs of programmable skew outputs**
- **Low skew: 150ps same pair, 350ps all outputs**
- **Selectable positive or negative edge synchronization: Excellent for DSP applications**
- **Synchronous output enable**
- **Input frequency: 25MHz to 225MHz**
- **Output frequency: 25MHz to 225MHz**
- **2x, 4x, 1/2, and 1/4 outputs (of VCO frequency)**
- **3-level inputs for skew control**
- **PLL bypass for DC testing**
- **External feedback, internal loop filter**
- **12mA balanced drive outputs**
- **Low Jitter: <150ps peak-to-peak**
- **Available in 144-pin BGA package**

DESCRIPTION:

The IDT5V996 is a high fanout PLL based clock driver intended for high performance computing and data-communication applications. The IDT5V996 has eight programmable skew outputs organized in four banks of two. Skew is controlled by 3-level input signals that may be hard wired to appropriate HIGH-MID-LOW levels. The IDT5V996 provides up to 18 programmable levels of output skew, prescaling, and other features.

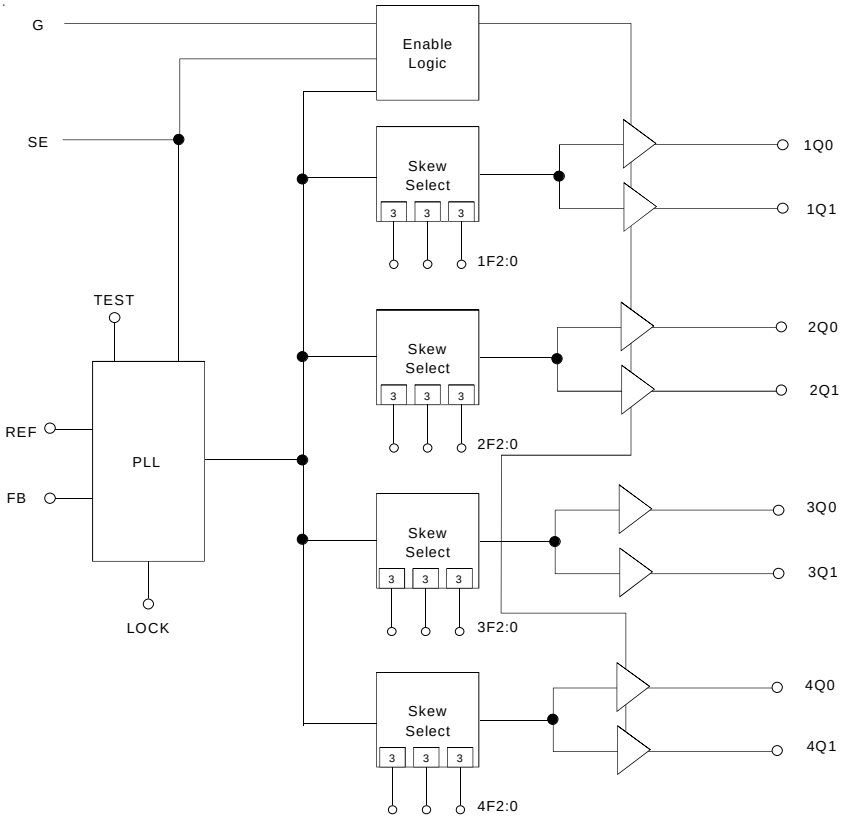
Other features of IDT5V996 are synchronous output enable (G), TEST, and lock detect indicator (LOCK). When G is held low, all the outputs are synchronously enabled, however, if G is held high, all outputs except 3Q0 and 3Q1 are in the state designated by SE (HIGH or LOW).

When TEST is held low, the chip operates in normal condition. When held high, the PLL is shut off and the chip functions as a buffer. The lock detect indicator asserts high when the phase lock loop has acquired lock. During acquisition, the indicator is in the low state. Once the PLL has reached the steady-state condition within a specified frequency range, LOCK is asserted high.

The PLL is closed externally to provide more flexibility by allowing the user to control the delay between the input clock and the outputs. The IDT5V996 has LVTTL outputs with 12mA balanced drive outputs.

The IDT5V996 is characterized for operation from –40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	
A	VDDQ	VDDQ	VDDQ	GND	GND	LOCK	GND	GND	GND	VDDQ	VDDQ	VDDQ	A
B	VDDQ	VDDQ	VDDQ	GND	2Q1	2Q0	1Q1	1Q0	GND	VDDQ	VDDQ	VDDQ	B
C	VDDQ	VDDQ	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDQ	VDDQ	C
D	VDDQ	VDDQ	VDD	GND	GND	GND	GND	GND	GND	VDD	2F2	2F1	D
E	VDDQ	G	VDD	GND	GND	GND	GND	GND	GND	VDD	2F0	1F2	E
F	TEST	REF	VDD	GND	GND	GND	GND	GND	GND	VDD	1F1	1F0	F
G	VDDQ	FB	VDD	GND	GND	GND	GND	GND	GND	VDD	4F1	4F0	G
H	VDDQ	SE	VDD	GND	GND	GND	GND	GND	GND	VDD	3F0	4F2	H
J	VDDQ	VDDQ	VDD	GND	GND	GND	GND	GND	GND	VDD	3F2	3F1	J
K	VDDQ	VDDQ	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDDQ	VDDQ	K
L	VDDQ	VDDQ	VDDQ	GND	3Q1	3Q0	4Q1	4Q0	GND	VDDQ	VDDQ	VDDQ	L
M	VDDQ	VDDQ	VDDQ	GND	GND	GND	GND	GND	GND	VDDQ	VDDQ	VDDQ	M
	1	2	3	4	5	6	7	8	9	10	11	12	

BGA
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{DDQ}, V_{DD}	Supply Voltage Range	–0.5 to +4.6	V
V_I(2)	Input Voltage Range	–0.5 to 4.6	V
V_O(2)	Voltage range applied to any output in the high or low state	–0.5 to V_{DDQ} + 0.5	V
I_{IK} (V_I < 0)	Input Clamp Current	–50	mA
I_O (V_O = 0 to V_{DDQ})	Continuous Output Current	±50	mA
V_{DDQ} or GND	Continuous Current	±100	mA
T_{STG}	Storage Temperature Range	–65 to +150	°C

NOTES:
1. Stresses beyond those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

CAPACITANCE(1,2) (T_A = +25°C, f = 1MHz, V_{IN} = 0V)

Parameter	Description	Min	Typ.	Max.	Unit
C_{IN}	Input Capacitance V_I = V_{DDQ} or GND	—	8	—	pF

NOTES:
1. Unused inputs must be held high or low to prevent them from floating.
2. Capacitance applies to all inputs except $nF_{2:0}$. This value is characterized but not production tested.

PIN DESCRIPTION

Pin Name	Type	Description
REF	IN	Reference Clock Input
SE	IN	Selectable positive or negative edge control. When LOW / HIGH, the outputs are synchronized with the negative/positive edge of the reference clock. When outputs are synchronously stopped with the G pin, SE determines the level at which outputs stop. When SE is LOW/HIGH, outputs synchronously stop HIGH/LOW.
FB	IN	Feedback Input
G	IN	Output gate for "true" $nQ_{[1:0]}$ outputs. When G is LOW, the "true" $nQ_{[1:0]}$ outputs are enabled. When G is HIGH, the "true" $nQ_{[1:0]}$ outputs are in the state designated by SE (HIGH or LOW) (except $3Q_0$ and $3Q_1$) - $3Q_0$ and $3Q_1$ may be used as the feedback signal to maintain phase lock.
TEST	IN	TEST = LOW means normal operation. TEST = HIGH means that the PLL is powered down and REF is routed to all the outputs. The skews selected with the $nF_{[2:0]}$ pins are still in effect. (The TEST pin is a TTL input.)
$nF_{[2:0]}$	IN	3-level inputs for selecting 1 of 18 skew taps or frequency functions
$nQ_{[1:0]}$	OUT	Clock Output Pairs
V_{DDQ}	PWR	Power supply for output buffers
V_{DD}	PWR	Power supply for phase locked loop and other internal circuitry
GND	PWR	Ground
LOCK	OUT	Lock Detect. Asserted (HIGH) when the PLL is locked. The REF input must be oscillating.

PROGRAMMABLE SKEW

Output skew with respect to the REF input is adjustable to compensate for PCB trace delays, backplane propagation delays or to accommodate requirements for special timing relationships between clocked components. Skew is selectable as a multiple of a time unit (t_U) which ranges from 278ps to 625ps (see Programmable Skew Range and Resolution Table). There are 16 skew configurations available for each output pair. These configurations are chosen by the $nF_{2:0}$ control pins. In order to minimize the number of control pins, 3-level inputs (HIGH-MID-LOW) are used, they are intended for but not restricted to hard-wiring. Undriven 3-level inputs default to the MID level. Where programmable skew is not a requirement, the control pins can be left open for the zero skew default setting. The Control Summary Table shows how to select specific skew taps by using the $nF_{2:0}$ control pins.

EXTERNAL FEEDBACK

By providing external feedback, the IDT5V996 gives users flexibility with regard to skew adjustment. The FB signal is compared with the input REF signal at the phase detector in order to drive the VCO. Phase differences cause the VCO of the PLL to adjust upwards or downwards accordingly.

An internal loop filter moderates the response of the VCO to the phase detector. The loop filter transfer function has been chosen to provide minimal jitter (or frequency variation) while still providing accurate responses to input frequency changes.

PLL PROGRAMMABLE SKEW RANGE AND RESOLUTION TABLE

		Comments
Timing Unit Calculation (t_U)	1/(16 x F_{NOM})	
VCO Frequency Range (F_{NOM})(1)	100 to 225 MHz	
Skew Adjustment Range(2) Max Adjustment:	±4.375ns	ns
	±157.5°	Phase Degrees
	±43.75%	% of Cycle Time
Example 1, F_{NOM} = 100MHz	t_U = 0.625ns	—
Example 2, F_{NOM} = 167MHz	t_U = 0.374ns	—
Example 3, F_{NOM} = 225MHz	t_U = 0.278ns	—

NOTES:

1. The VCO frequency always appears at $nQ_{1:0}$ outputs when they are operated in their undivided modes. The frequency appearing at the REF and FB inputs will be F_{NOM} when the output connected to FB is undivided. The frequency of the REF and FB inputs will be F_{NOM} /2 or F_{NOM} /4 when the part is configured for frequency multiplication by using a divided output as the FB input. Using the $nF_{[2:0]}$ inputs allows a different method for frequency multiplication (see Control Summary Table for Feedback Signals).
2. Skew adjustment range assumes that a zero skew output is used for feedback. If a skewed Q output is used for feedback, then adjustment range will be greater. For example if a 4t_U skewed output is used for feedback, all other outputs will be skewed –4t_U in addition to whatever skew value is programmed for those outputs. 'Max adjustment' range applies to all output pairs where ± 7t_U skew adjustment is possible and at the lowest F_{NOM} value.

CONTROL SUMMARY TABLE FOR FEEDBACK SIGNALS(1)

nF_2	nF_1	nF_0	Output Skew
L	L	L	Disable(2)
L	H	L	-7t_U
L	H	M	-6t_U
L	H	H	-5t_U
M	L	L	-4t_U
M	L	M	-3t_U
M	L	H	-2t_U
M	M	L	-1t_U
M	M	M	Zero Skew
M	M	H	+1t_U
M	H	L	+2t_U
M	H	M	+3t_U
M	H	H	+4t_U
H	L	L	+5t_U
H	L	M	+6t_U
H	L	H	+7t_U
H	M	L	Inverted
H	M	M	Divide by 2
H	M	H	Divide by 4

NOTES:

1. All unused/unnoted combinations are reserved.
2. When G is LOW, all output pairs are individually disabled to the level designated by SE. When SE is LOW/HIGH, output pairs disable HIGH/LOW.

RECOMMENDED OPERATING RANGE

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD} / V_{DDQ}	Power Supply Voltage	3	3.3	3.6	V
T_A	Ambient Operating Temperature	-40	+25	+85	°C

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Conditions		Min.	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH (REF, FB Inputs Only)		2	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW (REF, FB Inputs Only)		—	0.8	V
V_{IHH}	Input HIGH Voltage Level(1)	3-Level Inputs Only		V_{DD}—0.6	—	V
V_{IMM}	Input MID Voltage Level(1)	3-Level Inputs Only		V_{DD}/2—0.3	V_{DD}/2+0.3	V
V_{ILL}	Input LOW Voltage Level(1)	3-Level Inputs Only		—	0.6	V
I_{IN}	Input Leakage Current (REF, FB Inputs Only)	V_{IN} = V_{CC} or GND V_{CC} = Max.		-5	+5	µA
I_3	3-Level Input DC Current ($nF_{2:0}$)	V_{IN} = V_{DD}	HIGH Level	—	+200	µA
		V_{IN} = V_{DD}/2	MID Level	-50	+50	
		V_{IN} = GND	LOW Level	-200	—	
V_{OH}	Output HIGH Voltage Level	V_{DD} = Min., I_{OH} = —12mA		2.4	—	V
V_{OL}	Output LOW Voltage Level	V_{DD} = Min., I_{OL} = 12mA		—	0.4	V

NOTE:

1. These inputs are normally wired to V_{DDQ}, GND, or unconnected. Internal termination resistors bias unconnected inputs to V_{DDQ}/2. If these inputs are switched, the function and timing of the outputs may be glitched, and the PLL may require an additional t_{LOCK} time before all datasheet limits are achieved.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions(1)	Typ.(2)	Max.	Unit
I_{DDQ}	Quiescent Power Supply Current	V_{DDQ} = Max., REF = FB = SE = G = LOW, TEST = HIGH, All $nF_{2:0}$ = HHM(3), All outputs floating	—	30	mA
I_{DDD}	Dynamic Power Supply Current per Output	V_{DDQ} = Max., C_L = 0pF	410	650	µA/MHz
I_{TOT}	Total Power Supply Current	V_{DDQ} = 3.3V, F_{VCO} = 100MHz, C_L = 20pF	124	—	mA
		V_{DDQ} = 3.3V, F_{VCO} = 167MHz, C_L = 20pF	197	—	
		V_{DDQ} = 3.3V, F_{VCO} = 225MHz, C_L = 20pF	253	—	

NOTES:

1. Measurements are for divide-by-1 outputs.
2. For nominal voltage and temperature.
3. This configuration is only specific for I_{DDQ} measurements.

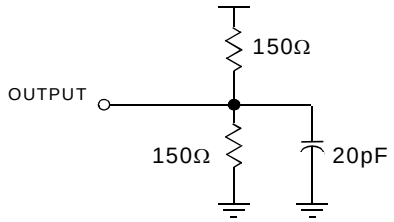
SWITCHING CHARACTERISTICS OVER OPERATING RANGE(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{NOM}	VCO Frequency Range	See PLL Programmable Skew Range and Resolution Table			
F_{REF}	REF Clock Input Frequency	25	—	225	MHz
t_{REF}	REF Clock Duty Cycle	10	—	90	%
t_U	Programmable Skew Time Unit	See Control Summary Table			
t_{SKEWPR}	Matched-Pair Skew (xQ_0, xQ_1)(1,2,3)	—	—	150	ps
$t_{SK(0)}$	Output Skew (Rise-Rise, Fall-Fall, Same Frequency and Phase)(1,2)	—	—	350	
$t_{SK(\omega)}$	Multiple Frequency Skew(1,2)	—	—	550	
$t_{SK(INV)}$	Inverting Skew Between Nominal and Inverted(1,2,4)	—	—	500	
t_{SKEW1}	Output Skew (Rise-Fall, Inverted-Divided)(1,2)	—	—	500	
t_{SKEW4}	Output Skew (Rise-Fall, Divided-Divided)(1,2,4)	—	—	500	
t_{DEV}	Device-to-Device Skew(2,5)	—	—	250	
t_ϕ	REF Input to FB Static Phase Offset ($V_{TH} = V_{DDQ}/2$)	-250	—	+250	
t_{ODCV}	Output Duty Cycle Variation from 50%(1,7)	-0.75	—	+0.75	ns
t_R	Output Rise Time (0.8V to 2V)(1)	—	—	2.2	
t_F	Output Fall Time (2V to 0.8V)(1)	—	—	2.2	
t_{LOCK}	PLL Lock Time(6)	—	—	0.5	ms
t_J	Cycle-to-Cycle Output Jitter, Peak-to-Peak(1)	—	—	150	ps

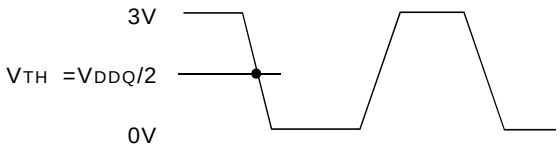
NOTES:

1. Measured at $V_{TH} = V_{DDQ}/2$, output load C_L = 20pF.
2. Skew is the time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with the specified load.
3. t_{SKEWPR} is the skew between a pair of outputs (xQ_0 and xQ_1) when all eight outputs are selected for $0t_U$.
4. There are 3 classes of outputs: Nominal (multiple of t_U delay), Inverted, and Divided (Divide-by-2 or Divide-by-4 mode).
5. t_{DEV} is the output-to-output skew between any two devices operating under the same conditions (V_{DD} and V_{DDQ}, ambient temperature, air flow, etc.)
6. t_{LOCK} is the time that is required before synchronization is achieved. This specification is valid only after V_{DD} and V_{DDQ} are stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.
7. t_{ODCV} is measured with $nF_{[2:0]}$ = MMM.

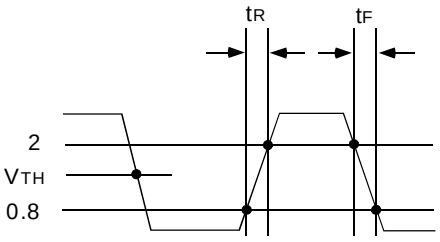
AC TEST LOADS AND WAVEFORMS



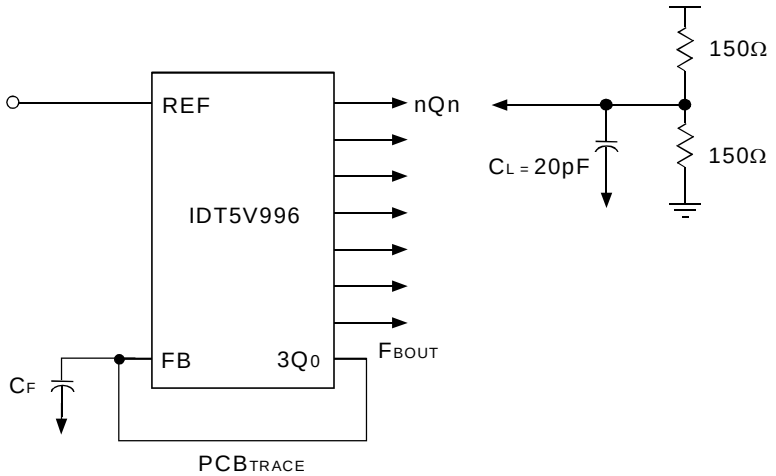
AC Load



Input Waveform



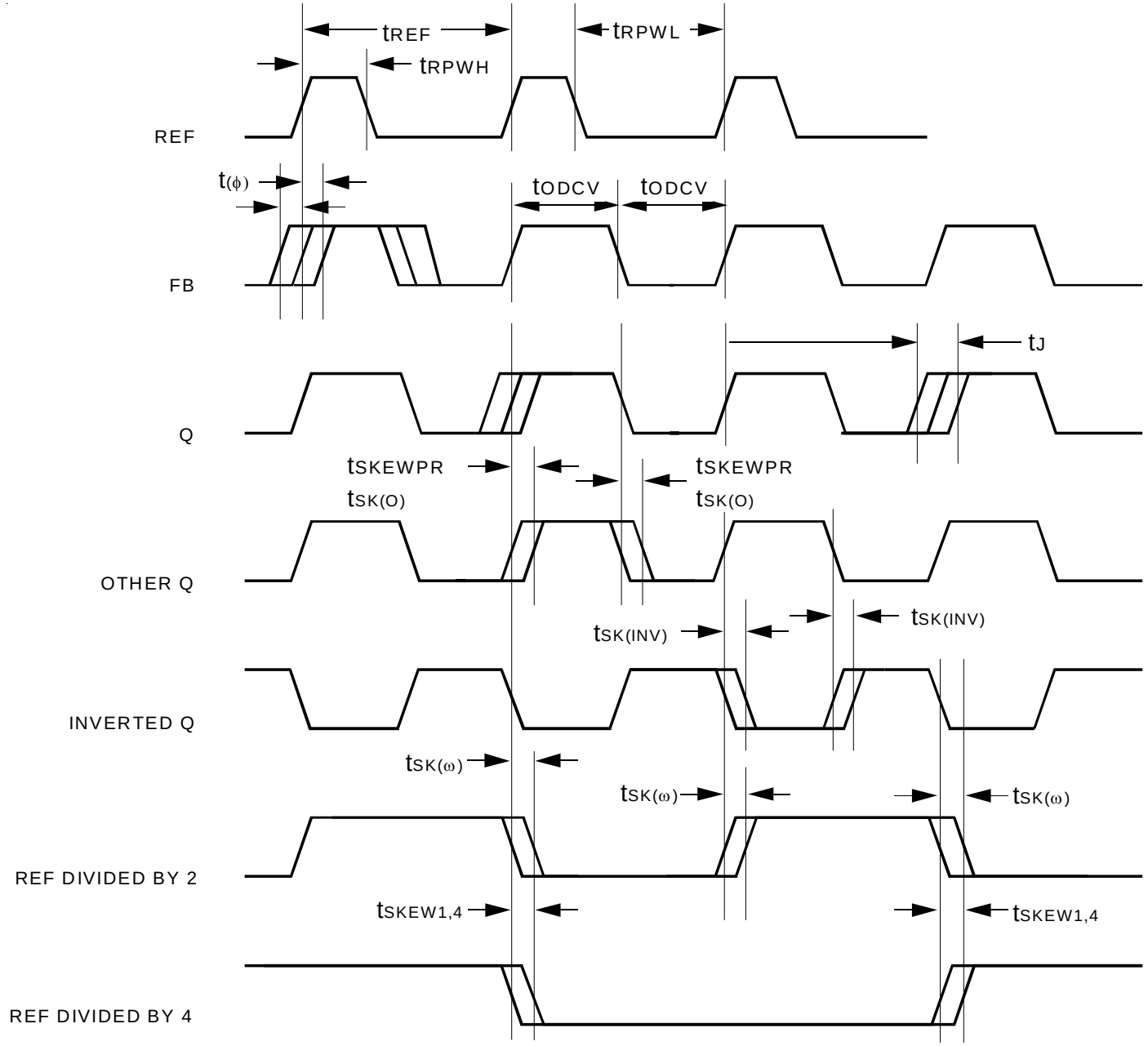
Output Waveform



Static Phase Offset and Skew Calculations (2,3)

NOTES:
1. $V_{TH} = V_{DDQ}/2$.
2. $C_F = C_L - C_{FBIN} - C_{PCBTRACE}$; $C_{FBIN} \cong 6pF$
3. Calculations were done by adjusting the input slew rate to match with the output slew rate.

AC TIMING DIAGRAM



NOTES:

SE: The AC Timing Diagram applies to SE=V_{DD}. For SE=GND, the negative edge of FB aligns with the negative edge of REF, divided outputs change on the negative edge of REF, and the positive edges of the divide-by-2 and the divide-by-4 signals align.

Skew: The time between the earliest and the latest output transition among all outputs for which the same t_U delay has been selected when all are loaded with 20pF and terminated with 75Ω to $V_{DDQ}/2$.

t_{SKEWPR}: The skew between a pair of outputs (xQ_0 and xQ_1) when all eight outputs are selected for $0t_U$.

$t_{SK(0)}$: The skew between outputs when they are selected for $0t_U$.

t_{DEV}: The output-to-output skew between any two devices operating under the same conditions (V_{DDQ}, V_{DD}, ambient temperature, air flow, etc.)

t_{ODCV}: The deviation of the output from a 50% duty cycle. Output pulse width variations are included in t_{SKEW1} and t_{SKEW4} specifications.

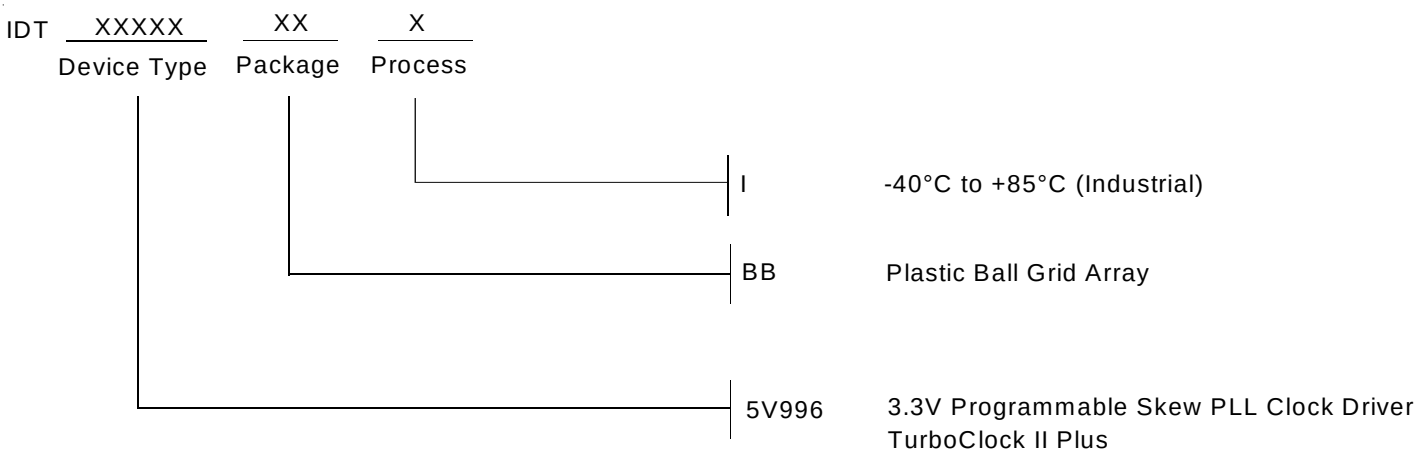
$t_{SK(\omega)}$: The skew between outputs of different frequencies.

$t_{SK(INV)}$: The skew between inverting and non-inverting outputs.

t_R and t_F are measured between 0.8V and 2V.

t_{LOCK}: The time that is required before synchronization is achieved. This specification is valid only after V_{DD}/V_{DDQ} is stable and within normal operating limits. This parameter is measured from the application of a new signal or frequency at REF or FB until t_{PD} is within specified limits.

ORDERING INFORMATION



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