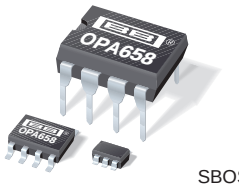
OPA658



SBOS045A – MARCH 1994 – REVISED JUNE 2003

Wideband, Low-Power, Current-Feedback Operational Amplifier

FEATURES

- **UNITY-GAIN STABLE BANDWIDTH: 900MHz**
- **LOW POWER: 50mW**
- **LOW DIFFERENTIAL GAIN/PHASE ERRORS: 0.025%/0.02°**
- **HIGH SLEW RATE: 1700V/μs**
- **GAIN FLATNESS: 0.1dB to 135MHz**
- **HIGH OUTPUT CURRENT (80mA)**

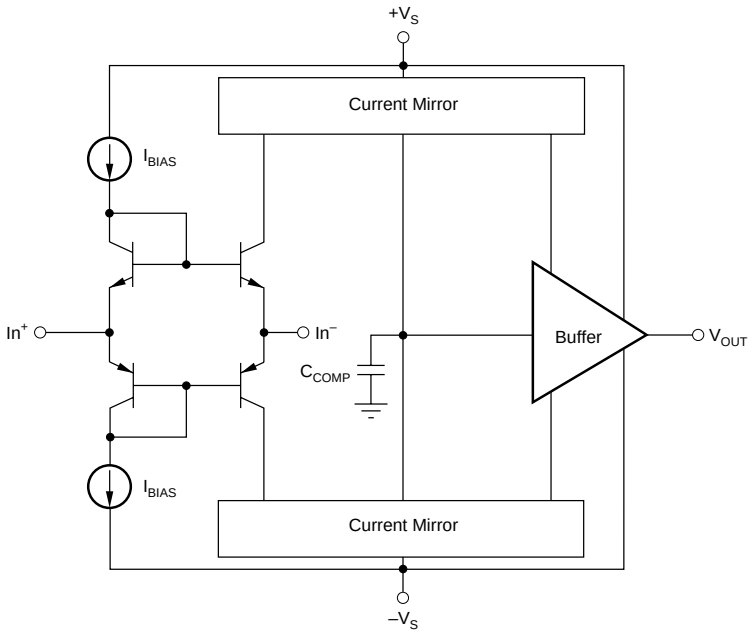
APPLICATIONS

- **MEDICAL IMAGING**
- **HIGH-RESOLUTION VIDEO**
- **HIGH-SPEED SIGNAL PROCESSING**
- **COMMUNICATIONS**
- **PULSE AMPLIFIERS**
- **ADC/DAC GAIN AMPLIFIER**
- **MONITOR PREAMPLIFIER**
- **CCD IMAGING AMPLIFIER**

DESCRIPTION

The OPA658 is an ultra-wideband, low power current feedback video operational amplifier featuring high slew rate and low differential gain/phase error. The current feedback design allows for superior large signal bandwidth, even at high gains. The low differential gain/phase errors, wide bandwidth and low quiescent current make the OPA658 a perfect choice for numerous video, imaging and communications applications.

The OPA658 is optimized for low gain operation and is also available in dual (OPA2658) configurations.



ABSOLUTE MAXIMUM RATINGS[1]

Supply	±5.5V
Internal Power Dissipation	See Thermal Characteristics
Differential Input Voltage	±1.2V
Input Voltage Range	$\pm V_S$
Storage Temperature Range: P, U, UB, N	–40°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
(soldering, SO 3s)	+260°C
Junction Temperature (T_J)	+150°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

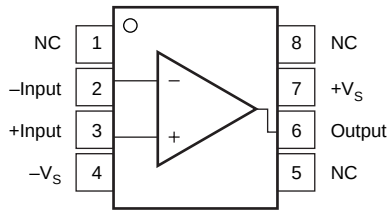
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA658	SO-8 Surface-Mount	D	–40°C to +85°C	OPA658U	OPA658U	Rails, 100
"	"	"	"	"	OPA658U/2K5	Tape and Reel, 2500
OPA658	SO-8 Surface-Mount	D	–40°C to +85°C	OPA658UB	OPA658UB	Rails, 100
"	"	"	"	"	OPA658UB/2K5	Tape and Reel, 2500
OPA658	SOT23-5	DBV	–40°C to +85°C	A58	OPA658N/250	Tape and Reel, 250
"	"	"	"	"	OPA658N/3K	Tape and Reel, 3000
OPA658	DIP-8	P	–40°C to +85°C	OPA658P	OPA658P	Rails, 50

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

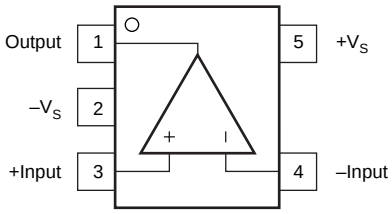
PIN CONFIGURATION

Top View **DIP, SO**



NC = No Connection

Top View **SOT23**



ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω, unless otherwise noted.

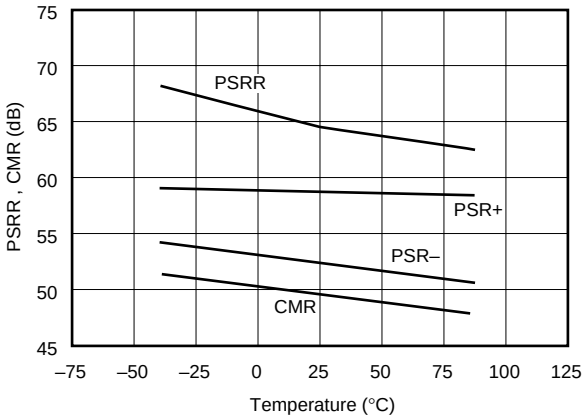
PARAMETER	CONDITION	OPA658P, U, N			OPA658UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
FREQUENCY RESPONSE								
Closed-Loop Bandwidth[1]	G = +1[2]		900			*[3]		MHz
	G = +2		680		400	*		MHz
	G = +5		370			*		MHz
	G = +10		200			*		MHz
Slew Rate[4]	G = +2, 2V Step		1700		1000	*		V/µs
At Minimum Specified Temperature			1500		900	*		V/µs
Settling Time: 0.01%	G = +2, 2V Step		15			*		ns
0.1%	G = +2, 2V Step		11.5			*		ns
1%	G = +2, 2V Step		6			*		ns
Spurious-Free Dynamic Range	f = 5MHz, G = +2, V_O = $2V_{PP}$		68			*		dBc
	f = 20MHz, G= +2, V_O = $2V_{PP}$		56			*		dBc
3rd-Order Intercept Point	f = 10MHz, 4dBm Each Tone		40			*		dBm
Differential Gain	G = +2, NTSC, V_O = $1.4V_{PP}$, R_L = 150Ω		0.025			*		%
Differential Phase	G = +2, NTSC, V_O = $1.4V_{PP}$, R_L = 150Ω		0.02			*		degrees
Bandwidth for 0.1dB Flatness	G = +2		135[5]			*		MHz
OFFSET VOLTAGE								
Input Offset Voltage	V_{CM} = 0V		±3	±5.5		±2	±4.5	mV
Over Temperature Range			±5	±8		±4	±7	mV
Power-Supply Rejection Ratio	V_S = ±4.7 to ±5.5V	55	64		58	67		dB
INPUT BIAS CURRENT								
Noninverting	V_{CM} = 0V		±5.7	±30		*	±18	µA
Over Temperature Range			±10	±80		*	±35	µA
Inverting	V_{CM} = 0V		±1.1	±35		*	*	µA
Over Temperature Range			±30	±75		*	*	µA
NOISE								
Input Voltage Noise Density								
f = 100Hz			16			*		nV/√Hz
f = 2kHz			4.9			*		nV/√Hz
f = 10kHz			3.2			*		nV/√Hz
f = 1MHz			3.2			*		nV/√Hz
f_B = 100Hz to 200MHz			45.3			*		µVrms
Input Bias Current Noise Density								
Inverting: f = 1MHz			32			*		pA/√Hz
Noninverting: f = 1MHz			11.9			*		pA/√Hz
INPUT VOLTAGE RANGE								
Common-Mode Input Range								
Over Temperature Range		±2.5	±2.9		*	*		V
Common-Mode Rejection	V_{CM} = ±1V	45	50		*	*		dB
INPUT IMPEDANCE								
Noninverting			500 || 1			*		kΩ || pF
Inverting			50			*		Ω
OPEN-LOOP TRANSRESISTANCE								
Open-Loop Transresistance	V_O = ±2V, R_L = 100Ω	150	190		200	250		kΩ
Over Temperature Range	V_O = ±2V, R_L = 100Ω	100			150			kΩ
OUTPUT								
Voltage Output	No Load	±2.7	±2.9		*	*		V
Over Temperature Range		±2.5	±2.75		*	*		V
Voltage Output	R_L = 250Ω	±2.7	±2.9		*	*		V
Over Temperature Range		±2.5	±2.7		*	*		V
Voltage Output	R_L = 100Ω	±2.2	±2.8		*	*		V
Over Temperature Range		±2.0	±2.5		*	*		V
Output Current, Sourcing		80	120		*	*		mA
Over Temperature		70			*			mA
Output Current, Sinking		60	80		*	*		mA
Over Temperature		35			*			mA
Short Circuit Current			150			*		mA
Output Resistance	0.1MHz, G = +2		0.02			*		Ω
POWER SUPPLY								
Specified Operating Voltage			±5			*		V
Operating Voltage Range		±4.5		±5.5	*		*	V
Quiescent Current	V_S = ±5V		±5	±7.75		±4.5	±5.75	mA
Over Temperature Range			±5.5	±8.5		±4.7	±6.5	mA
TEMPERATURE RANGE								
Specification: P, U, N, UB		–40		+85	*		*	°C
Thermal Resistance, θ_{JA}								
P DIP-8			100			*		°C/W
U SO-8			125			*		°C/W
N SOT23-5			150			*		°C/W

(1) Frequency response can be strongly influenced by PC board parasitics. The demonstration boards show low parasitic layouts for this part. Refer to the demonstration board layout for details.
(2) At G = +1, R_{FB} = 560Ω for DIP and 402Ω for SO-8.
(3) An asterisk (*) specifies the same value as the grade to the left.
(4) Slew rate is rate of change from 10% to 90% of output voltage step.
(5) This specification is PC board layout dependent.

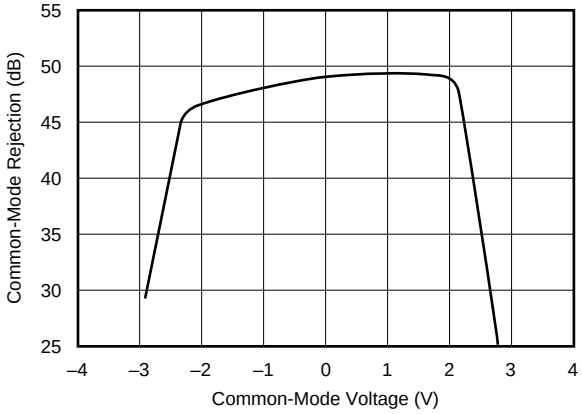
TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω, unless otherwise noted.

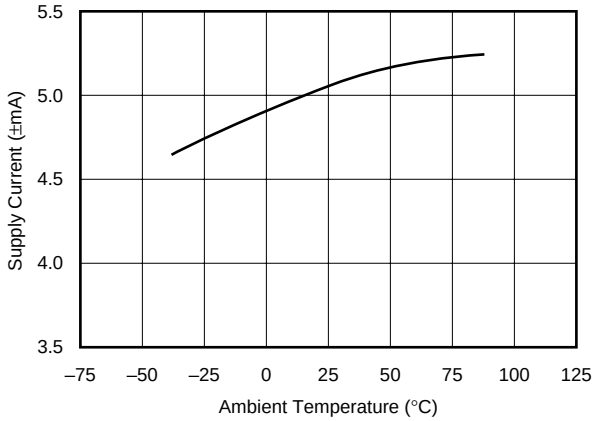
POWER-SUPPLY REJECTION RATIO AND
COMMON-MODE REJECTION vs TEMPERATURE



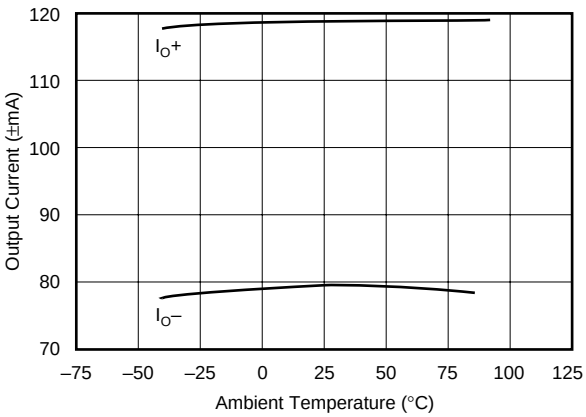
COMMON-MODE REJECTION
vs INPUT COMMON-MODE VOLTAGE



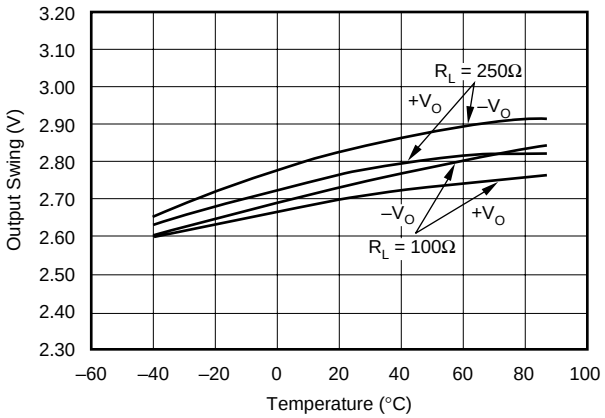
SUPPLY CURRENT vs TEMPERATURE



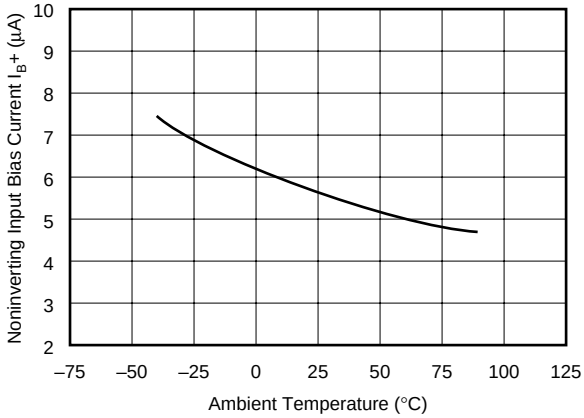
OUTPUT CURRENT vs TEMPERATURE



OUTPUT SWING vs TEMPERATURE



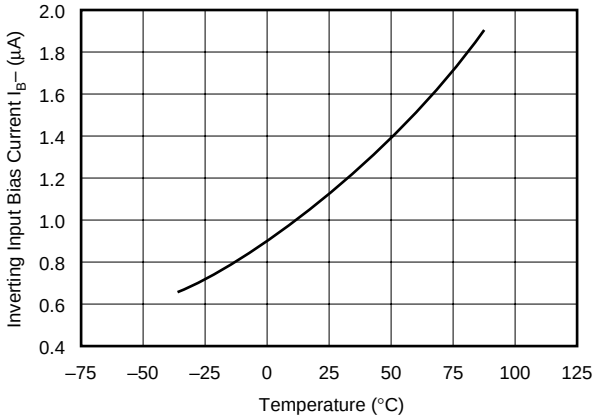
NONINVERTING INPUT BIAS CURRENT
vs TEMPERATURE



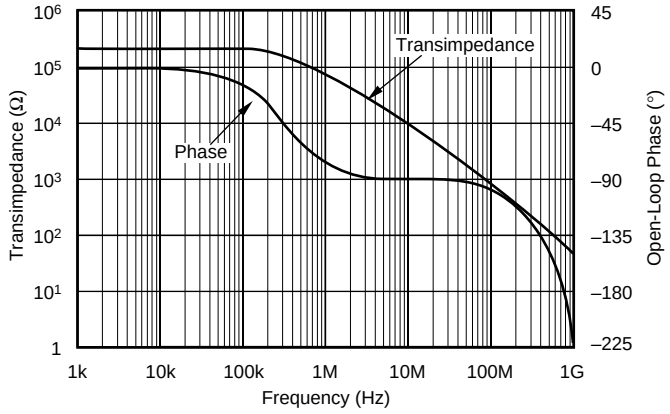
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω, unless otherwise noted.

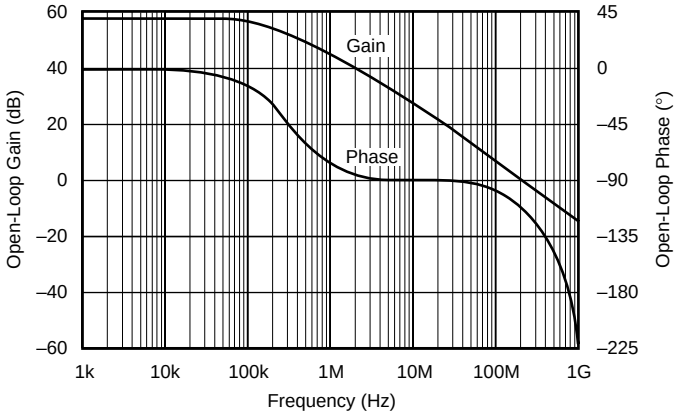
INVERTING INPUT BIAS CURRENT vs TEMPERATURE



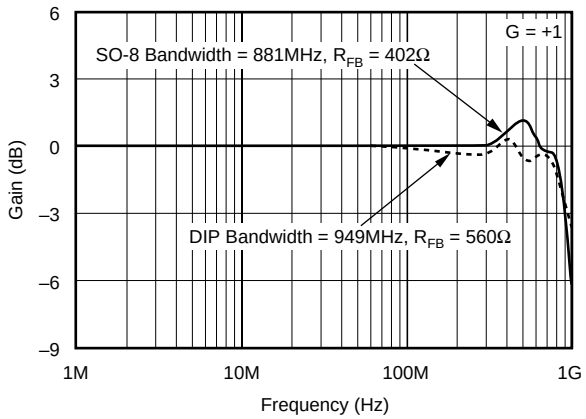
OPEN-LOOP TRANSIMPEDANCE AND PHASE vs FREQUENCY



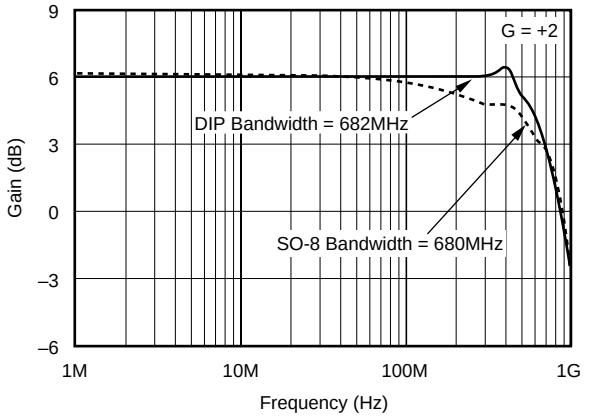
OPEN-LOOP GAIN AND PHASE vs FREQUENCY



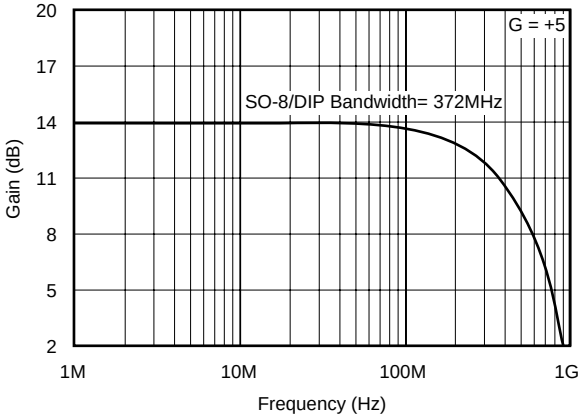
CLOSED-LOOP BANDWIDTH



CLOSED-LOOP BANDWIDTH



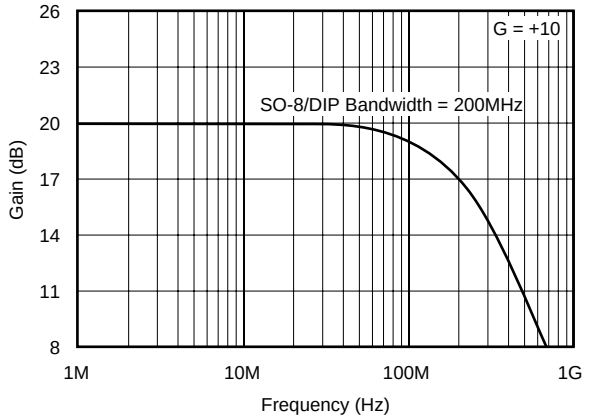
CLOSED-LOOP BANDWIDTH



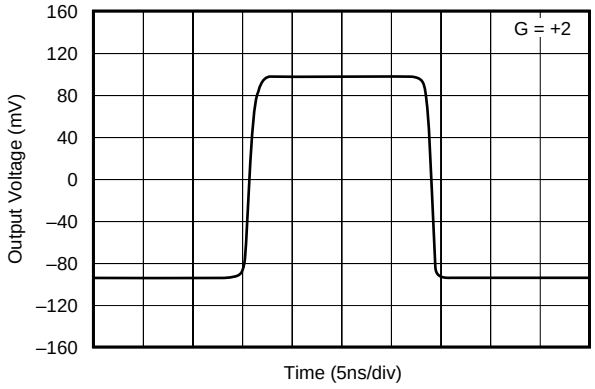
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω, unless otherwise noted.

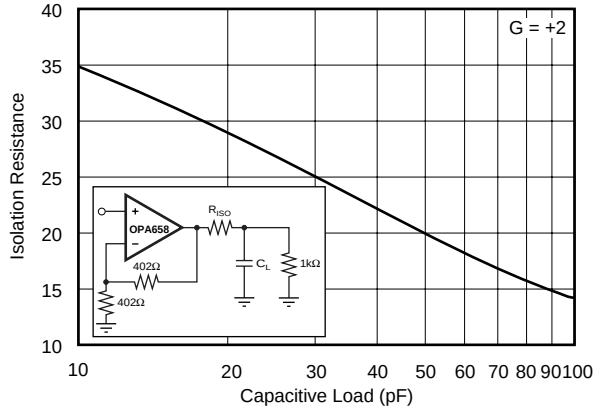
CLOSED-LOOP BANDWIDTH



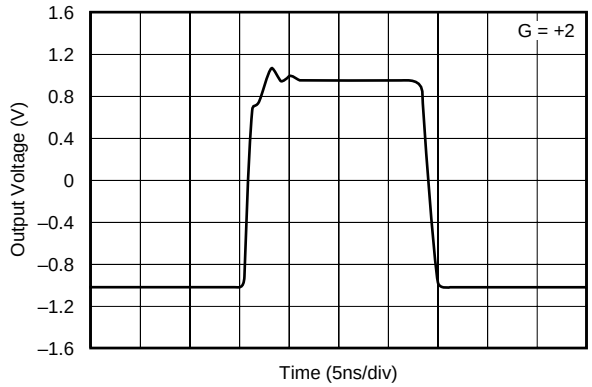
SMALL-SIGNAL TRANSIENT RESPONSE



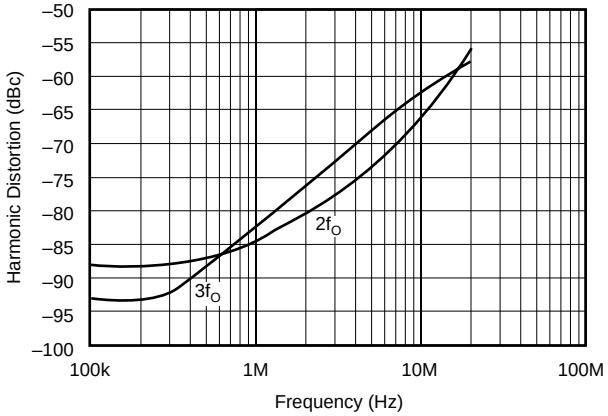
RECOMMENDED ISOLATION RESISTANCE vs CAPACITIVE LOAD



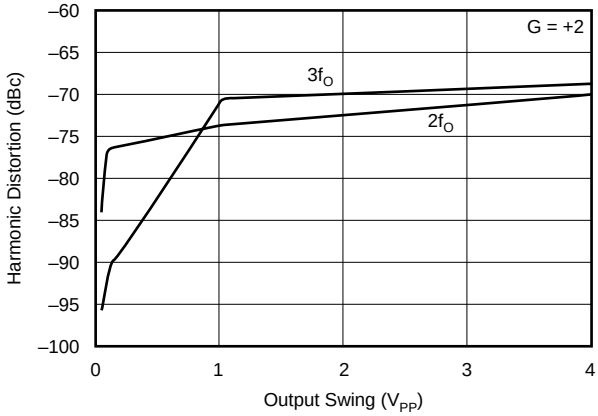
LARGE-SIGNAL TRANSIENT RESPONSE



HARMONIC DISTORTION vs FREQUENCY



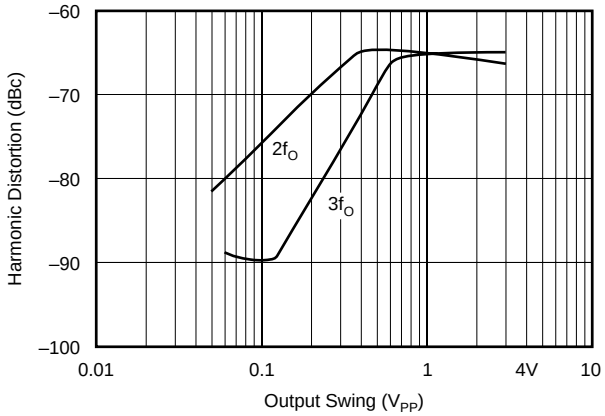
5MHz HARMONIC DISTORTION vs OUTPUT SWING



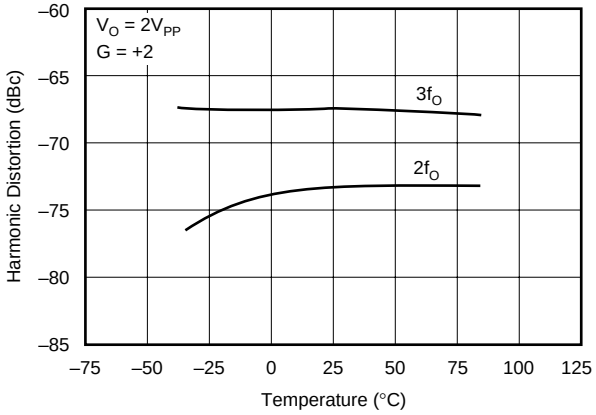
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, V_S = ±5V, R_L = 100Ω, and R_{FB} = 402Ω, unless otherwise noted.

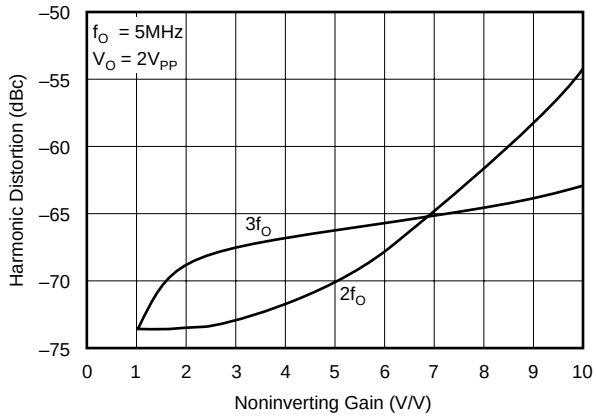
10MHz HARMONIC DISTORTION vs OUTPUT SWING



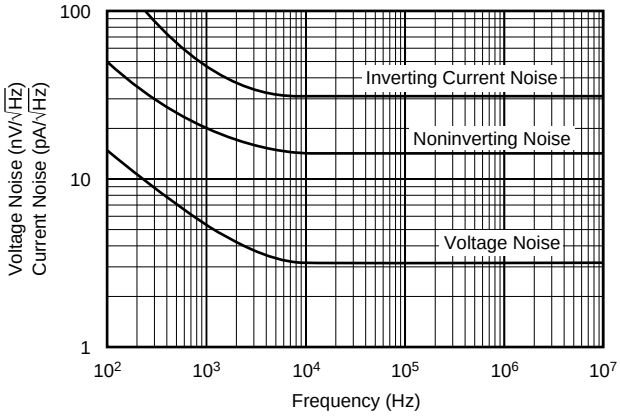
HARMONIC DISTORTION vs TEMPERATURE



HARMONIC DISTORTION vs GAIN



INPUT VOLTAGE AND CURRENT NOISE vs FREQUENCY



APPLICATIONS INFORMATION

THEORY OF OPERATION

Conventional op amps depend on feedback to drive their inputs to the same potential, however the current-feedback op amp's inverting and noninverting inputs are connected by a unity-gain buffer, thus enabling the inverting input to automatically assume the same potential as the noninverting input. This results in very low impedance at the inverting input to sense the feedback as an error current signal.

DISCUSSION OF PERFORMANCE

The OPA658 is a low-power, unity-gain stable, current-feedback operational amplifier which operates on ±5V power supply. The current-feedback architecture offers the following important advantages over voltage-feedback architectures: (1) the high slew rate allows the large-signal performance to approach the small-signal performance, and (2) there is very little bandwidth degradation at higher gain settings.

The current-feedback architecture of the OPA658 provides the traditional strength of excellent large-signal response plus wide bandwidth, making it a good choice for use in high-resolution video, medical imaging and Digital-to-Analog Converter (DAC) I/V Conversion. The low-power requirements make it an excellent choice for numerous portable applications.

DC GAIN TRANSFER CHARACTERISTICS

The circuit in Figure 1 shows the equivalent circuit for calculating the DC gain. When operating the device in the inverting mode, the input signal error current (I_E) is amplified by the open loop transimpedance gain (T_O). The output signal generated is equal to T_O x I_E. Negative feedback is applied through R_{FB} such that the device operates at a gain equal to $-R_{FB}/R_{FF}$.

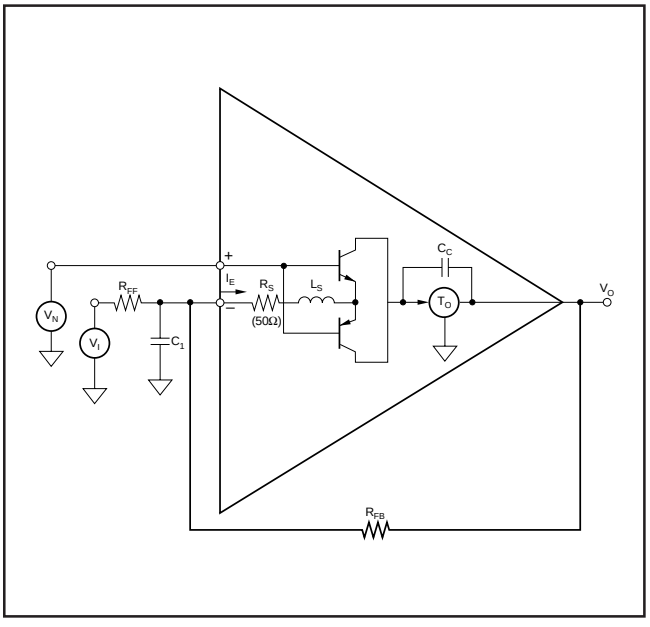


FIGURE 1. Equivalent Circuit.

For noninverting operation, the input signal is applied to the noninverting (high impedance buffer) input. The output (buffer) error current (I_E) is generated at the low impedance inverting input. The signal generated at the output is fed back to the inverting input such that the overall gain is $(1 + R_{FB}/R_{FF})$. Where a voltage-feedback amplifier has two symmetrical high impedance inputs, a current-feedback amplifier has a low inverting (buffer output) impedance and a high noninverting (buffer input) impedance.

The closed-loop gain for the OPA658 can be calculated using Equations 1 and 2.

$$\text{Inverting Gain} = \frac{-\left(\frac{R_{FB}}{R_{FF}}\right)}{1 + \frac{1}{\text{Loop Gain}}} \qquad (1)$$

$$\text{Noninverting Gain} = \frac{\left[1 + \frac{R_{FB}}{R_{FF}}\right]}{1 + \frac{1}{\text{Loop Gain}}}$$

$$\text{where Loop Gain} = \left[\frac{T_O}{R_{FB} + R_S\left(1 + \frac{R_{FB}}{R_{FF}}\right)}\right] \qquad (2)$$

At higher gains, the small value inverting input impedance causes an apparent loss in bandwidth. This can be seen from Equation 3.

$$f_{ACTUAL}BW \approx \frac{\left[f_{(A_V = +2)}BW\right] \times (1.25)}{\left[1 + \left(\frac{R_S}{R_{FB}}\right) \times \left(1 + \frac{R_{FB}}{R_{FF}}\right)\right]} \qquad (3)$$

This loss in bandwidth at high gains can be corrected without affecting stability by lowering the value of the feedback resistor from the specified value of 402Ω.

OFFSET VOLTAGE AND NOISE

The output offset is the algebraic sum of the input offset voltage and bias current errors. The output offset for the model of Figure 2 is calculated by Equation 4.

$$\text{Output Offset Voltage} =$$
$$\pm Ib_N \times R_N\left(1 + \frac{R_{FB}}{R_{FF}}\right) \pm V_{IO}\left(1 + \frac{R_{FB}}{R_{FF}}\right) \pm Ib_N \times R_{FB} \qquad (4)$$

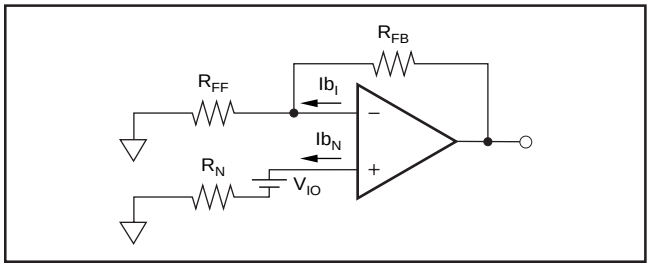


FIGURE 2. Output Offset Voltage Equivalent Circuit.

If all terms are divided by the gain ($1 + R_{FB}/R_{FF}$) it can be observed that input referred offsets improve as gain increases. The effective noise at the output can be determined by taking the root sum of the squares of Equation 4 and applying the spectral noise values found in the Typical Characteristics section. This applies to noise from the op amp only. Note that both the noise figure (NF) and the equivalent input offset voltages improve as the closed-loop gain increases (by keeping R_{FB} fixed and reducing R_{FF} with $R_N = 0\Omega$).

INCREASING BANDWIDTH AT HIGH GAINS

The closed-loop bandwidth can be extended at high gains by reducing the value of the feedback resistor R_{FB}. This bandwidth reduction is caused by the feedback current being split between R_S and R_{FF} (refer to Figure 1). As the gain increases (for a fixed R_{FB}), more feedback current is shunted through R_{FF}, which reduces closed-loop bandwidth.

CIRCUIT LAYOUT AND BASIC OPERATION

Achieving optimum performance with a high-frequency amplifier such as the OPA658 requires careful attention to layout parasitics and selection of external components. Recommendations for PC board layout and component selection include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the two power pins to high-frequency 0.1µF decoupling capacitors. At the pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequencies, should also be used. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high-frequency performance of the OPA658. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads as short as possible. Never use wirewound type resistors in a high-frequency application.

Since the output pin and the inverting input pin are most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the package pins. Other network components, such as noninverting input termination resistors, should also be placed close to the package.

The feedback resistor value acts as the frequency response compensation element for a current-feedback type amplifier. The 402Ω used in setting the specification achieves a nominal maximally-flat butterworth response while assuming a 2pF output pin parasitic. Increasing the feedback resistor will overcompensate the amplifier, rolling off the frequency response, while decreasing it will decrease phase margin, peaking up the frequency response. Note that a noninverting, unity-gain buffer application still requires a feedback resistor for stability (560Ω for SO-8, 402Ω for DIP, and 324Ω for SOT23).

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50 mils to 100 mils) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_{ISO} from the plot of recommended R_{ISO} vs capacitive load. Low parasitic loads may not need an R_{ISO} since the OPA658 is nominally compensated to operate with a 2pF parasitic load.

If a long trace is required and the 6dB signal loss intrinsic to doubly-terminated transmission lines is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is not necessary onboard, and in fact a higher impedance environment will improve distortion as shown in the distortion vs load plot. With a characteristic impedance defined based on board material and desired trace dimensions, a matching series resistor into the trace from the output of the amplifier is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; the total effective impedance should match the trace impedance. Multiple destination devices are best handled as separate transmission lines, each with their own series and shunt terminations.

If the 6dB attenuation loss of a doubly-terminated line is unacceptable, a long trace can be series-terminated at the source end only. This will help isolate the line capacitance from the op amp output, but will not preserve signal integrity as well as a doubly-terminated line. If the shunt impedance at the destination end is finite, there will be some signal attenuation due to the voltage divider formed by the series and shunt impedances.

e) Socketing a high-speed part like the OPA658 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket creates an extremely troublesome parasitic network which can make it almost impossible to achieve a smooth, stable response. Best results are obtained by soldering the part onto the board. If socketing for the DIP package is desired, high-frequency, flush-mount pins (for instance, McKenzie Technology #710C) can give good results.

The OPA658 is nominally specified for operation using ±5V power supplies. A 10% tolerance on the supplies, or an ECL –5.2V for the negative supply, is within the maximum specified total supply voltage of 11V. Higher supply voltages can break down internal junctions possibly leading to catastrophic failure. Single-supply operation is possible as long as common-mode voltage constraints are observed. The common-mode input and output voltage specifications can be interpreted as a required headroom to the supply voltage. Observing this input and output headroom requirement will allow non-standard or single-supply operation. Figure 3 shows one approach to single-supply operation.

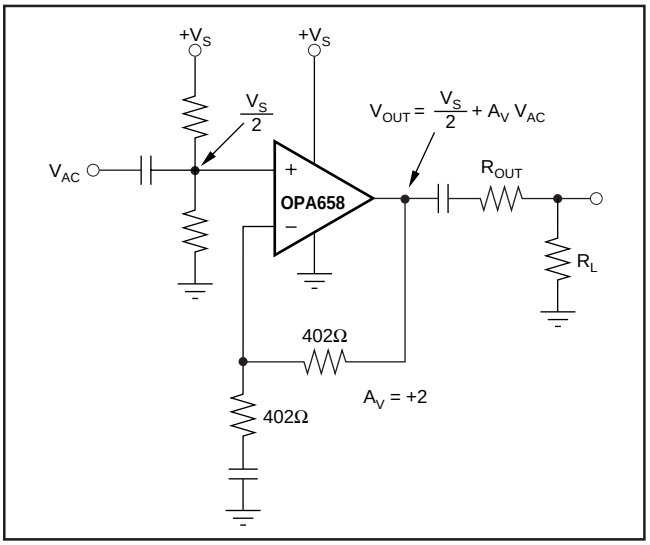


FIGURE 3. Single-Supply Operation.

ESD PROTECTION

ESD static damage has been well recognized for MOSFET devices, but any semiconductor device deserves protection from this potentially damaging source. This is particularly true for very high-speed, fine geometry processes.

ESD static damage can cause subtle changes in amplifier input characteristics without necessarily destroying the device. In precision operational amplifiers, this may cause a noticeable degradation of offset voltage and drift. Therefore, static protection is strongly recommended when handling the OPA658.

OUTPUT DRIVE CAPABILITY

The OPA658 has been optimized to drive 75Ω and 100Ω resistive loads. The device can drive $2V_{PP}$ into a 75Ω load. This high-output drive capability makes the OPA658 an ideal choice for a wide range of RF, IF, and video applications. In many cases, additional buffer amplifiers are unneeded.

Many demanding high-speed applications such as Analog-to-Digital Converter (ADC)/DAC buffers require op amps with low wideband output impedance. For example, low output impedance is essential when driving the signal-dependent capacitances at the inputs of flash ADCs. As shown in Figure 4, the OPA658 maintains very low closed-loop output impedance over frequency. Closed-loop output impedance increases with frequency since loop gain is decreasing with frequency.

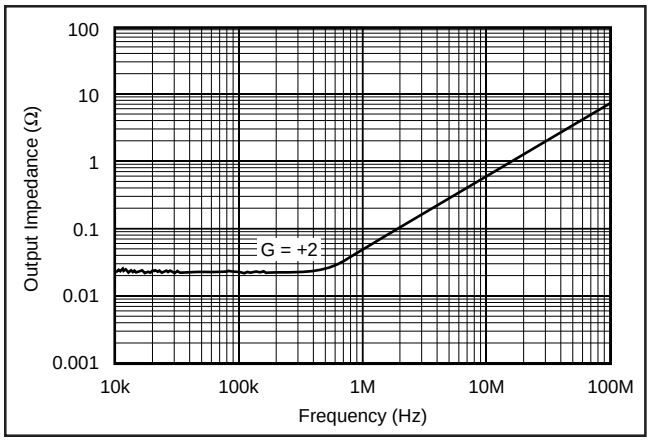


FIGURE 4. Closed-Loop Output Impedance vs Frequency.

THERMAL CONSIDERATIONS

The OPA658 will not require heatsinking under most operating conditions. Maximum desired junction temperature will set a maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed 175°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 either supply voltage (for equal bipolar supplies). Under this condition $P_{DL} = V_S^2/(4 \times R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As an example, compute the maximum T_J for an OPA658N at A_V = +2, R_L = 100Ω, R_{FB} = 402Ω, $\pm V_S$ = ±5V, and the specified maximum T_A = +85°C.

$P_D = 10V \times 8.5mA + 5^2/[4 \times (100\Omega \parallel 804\Omega)] = 155mW$

Maximum $T_J = 85°C + 0.155W \times 150°C/W = 108°C$

DRIVING CAPACITIVE LOADS

The OPA658's output stage has been optimized to drive low resistive loads. Capacitive loads, however, will decrease the amplifier's phase margin which may cause high-frequency peaking or oscillations. Capacitive loads greater than 5pF should be buffered by connecting a small resistance, usually 10Ω to 35Ω, in series with the output as illustrated in Figure 5. This is particularly important when driving high capacitance loads such as flash ADCs.

In general, capacitive loads should be minimized for optimum high-frequency performance. Coaxial lines can be driven if the cable is properly terminated. The capacitance of coaxial cable (29pF/foot for RG-58) will not load the amplifier when the coaxial cable or transmission line is terminated with its characteristic impedance.

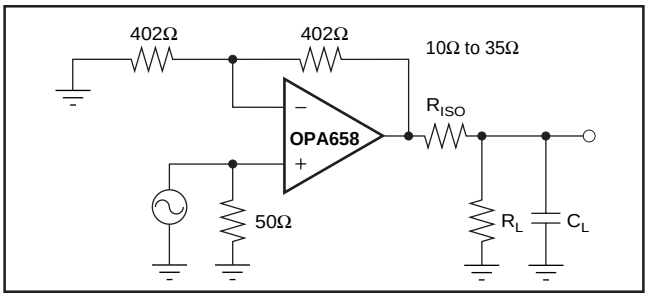


FIGURE 5. Driving Capacitive Loads.

COMPENSATION

The OPA658 is internally compensated and is stable in unity gain with a phase margin of approximately 62°, and approximately 64° in a gain of +2V/V when used with the recommended feedback resistor value. Frequency response for other gains are shown in the Typical Characteristics.

The high-frequency response of the OPA658 in a good layout is very flat with frequency.

DISTORTION

The OPA658's Harmonic Distortion characteristics into a 100Ω load are shown versus frequency and power output in the Typical Characteristics. Distortion can be further improved by increasing the load resistance as illustrated in Figure 6. Remember to include the contribution of the feedback resistance when calculating the effective load resistance seen by the amplifier.

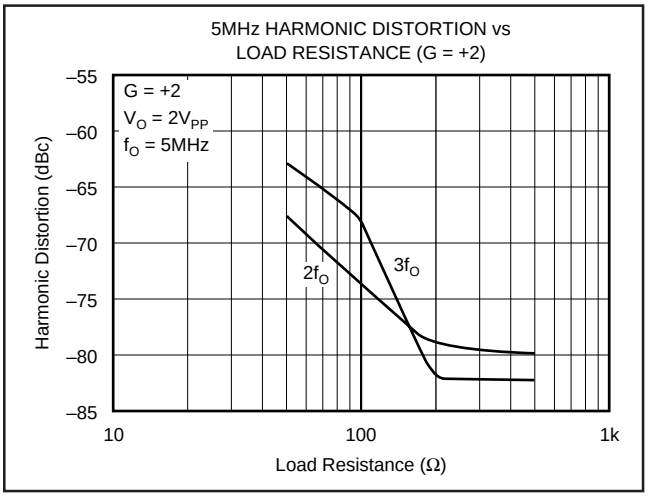


FIGURE 6. 5MHz Harmonic Distortion vs Load Resistance.

Narrowband communication channel requirements will benefit from the OPA658's wide bandwidth and low intermodulation distortion on low quiescent power. If output signal power at two closely spaced frequencies is required, 3rd-order nonlinearities in any amplifier will cause spurious power at frequencies very near the two fundamental frequencies. If the two test frequencies, f_1 and f_2, are specified in terms of average and delta frequency, $f_O = (f_1 + f_2)/2$ and $Df = \Omega f_2 – f_1\Omega$, the two, 3rd-order, close-in spurious tones will appear at $f_O \pm 3 \times Df$. The 2-tone, 3rd-order spurious plot shown in Figure 7 indicates how far below these two equal power, closely-spaced tones the intermodulation spurious will be. The single-tone power is at a matched 50Ω load. The unique design of the OPA658 provides much greater spurious free range than what a 2-tone, 3rd-order intermodulation intercept specification would predict. This can be seen in Figure 7 as the spurious-free range actually increases at the higher output power levels.

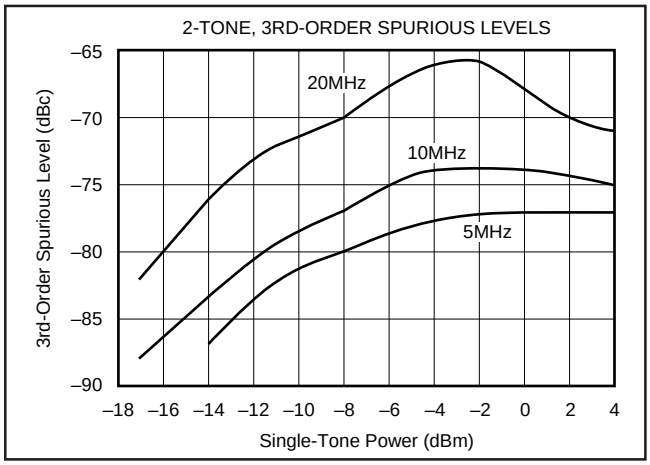


FIGURE 7. 3rd-Order Spurious Level vs Frequency.

DIFFERENTIAL GAIN AND PHASE

Differential Gain (dG) and Differential Phase (dP) are among the more important specifications for video applications. dG is defined as the percent change in closed-loop gain over a specified change in output voltage level. dP is defined as the change in degrees of the closed-loop phase over the same output voltage change. Both dG and dP are specified at the NTSC sub-carrier frequency of 3.58MHz and the PAL sub-carrier of 4.43MHz. All NTSC measurements were performed using a Tektronix model VM700A Video Measurement Set.

dG/dP of the OPA658 were measured with the amplifier in a gain of +2V/V with 75Ω input impedance and the output back-terminated in 75Ω. The input signal selected from the generator was a 0V to 1.4V modulated ramp with sync pulse. With these conditions the test circuit shown in Figure 8 delivered a 100IRE modulated ramp to the 75Ω input of the videoanalyzer. The signal averaging feature of the analyzer was used to establish a reference against which the perfor-

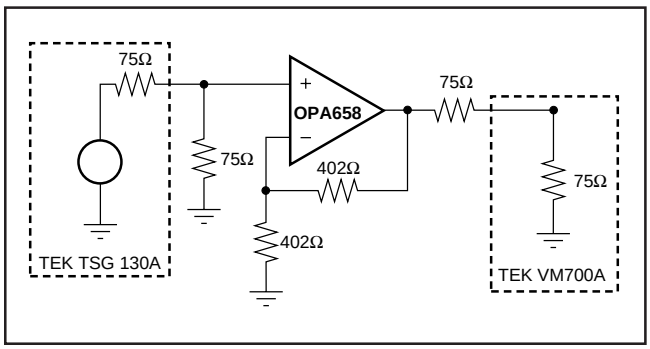


FIGURE 8. Configuration for Testing Differential Gain/Phase.

mance of the amplifier was measured. Signal averaging was also used to measure the dg and dp of the test signal in order to eliminate the generator's contribution to measured amplifier performance. Typical performance of the OPA658 is 0.025% differential gain and 0.02° differential phase to both NTSC and PAL standards.

DESIGN-IN TOOLS

DEMONSTRATION BOARDS

Several PC boards are available to assist in the initial evaluation of circuit performance using the OPA658 in its three package styles. All of these are available free as an unpopulated PC board delivered with descriptive documentation. The summary information for these boards is shown in Table I.

PRODUCT	PACKAGE	BOARD PART NUMBER	LITERATURE REQUEST NUMBER
OPA658U	SO-8	DEM-OPA68xU	SBOU009
OPA658N	SOT23-5	DEM-OPA6xxN	SBOU010
OPA658P	DIP-8	DEM-OPA68xP	SBOU008

TABLE I. Demo Board Part/Ordering Numbers.

To request any of these boards, check the Texas Instruments web site at www.ti.com.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA658N/250	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	0 to 70		
OPA658N/3K	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI			
OPA658NB/250	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI			
OPA658NB/3K	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI			
OPA658P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI			
OPA658U	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI			
OPA658U-1	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI			
OPA658U/2K5	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI			
OPA658UB	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI			
OPA658UB/2K5	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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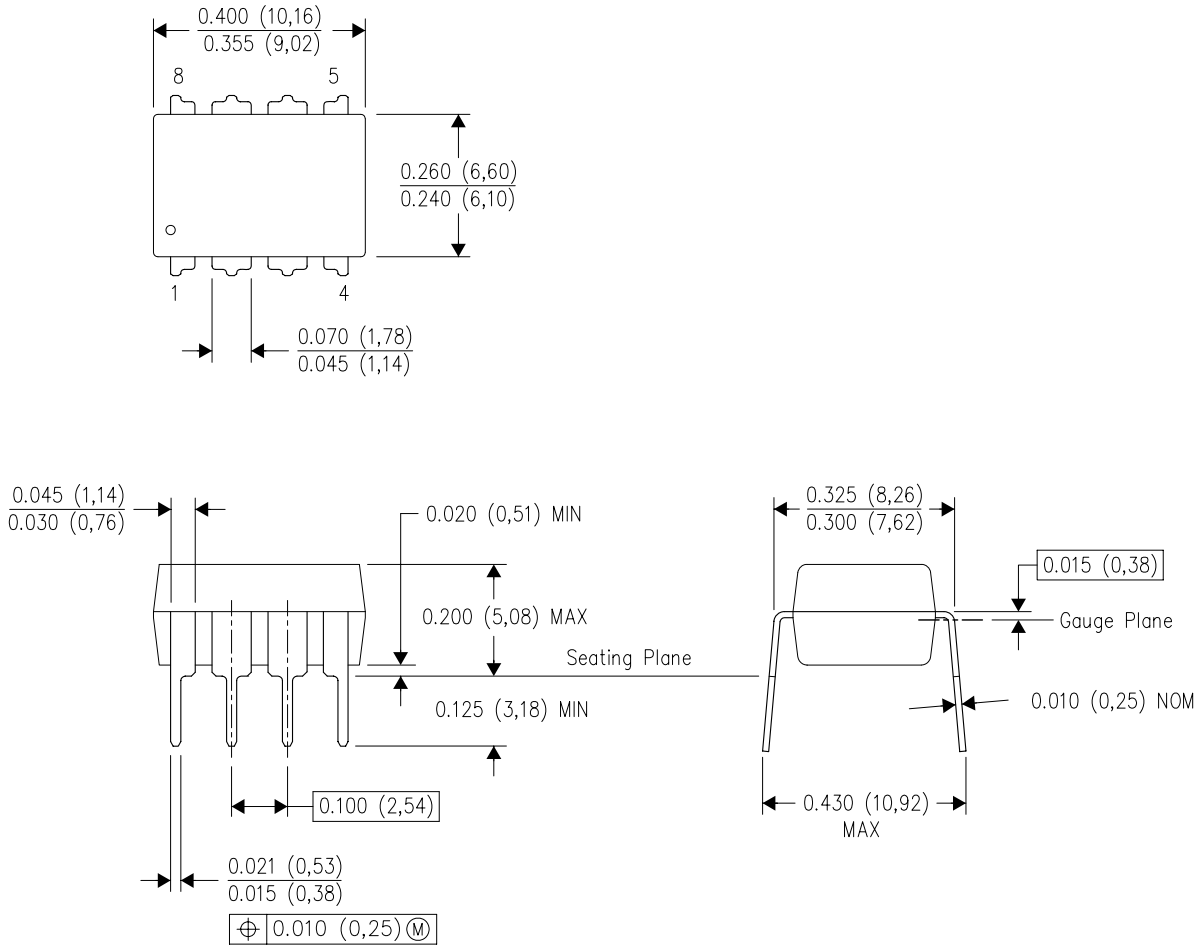
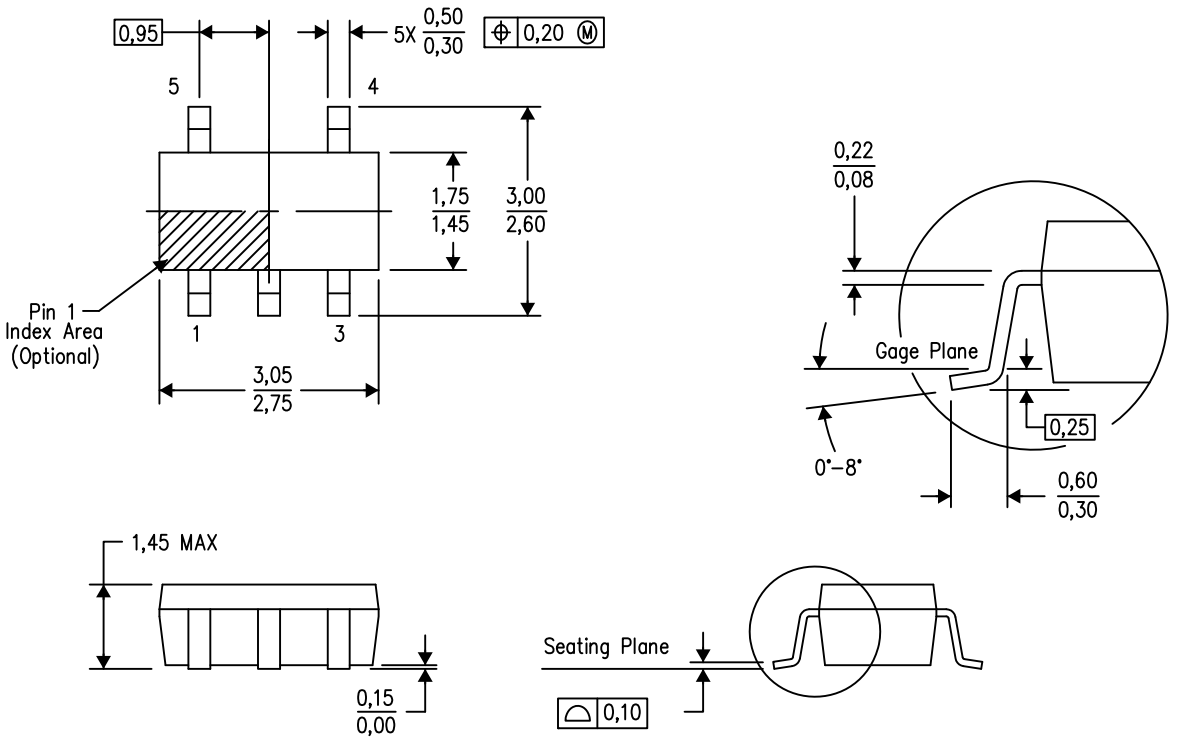
P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



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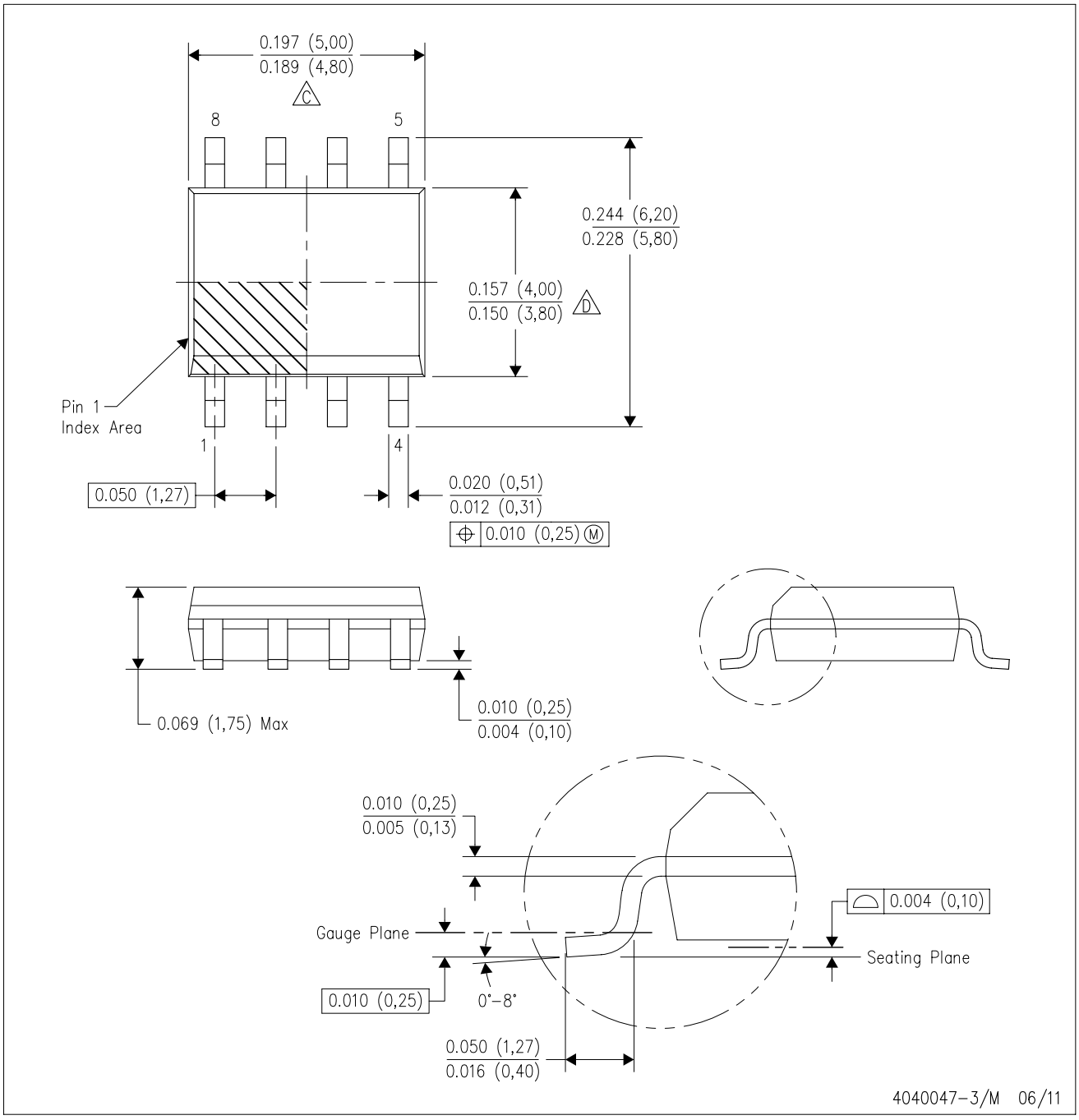
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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