# NT128S64VH8C0GM
# 128MB : 16M x 64
# SDRAM SODIMM

16Mx64 bit Two Bank Small Outline SDRAM Module

based on 8Mx16, 4Banks, 4K Refresh, 3.3V Synchronous DRAMs with SPD

## Features

- 144 Pin JEDEC Standard, 8 Byte Small Outline Dual-In-line Memory Module
- 16Mx64 Synchronous DRAM SO DIMM
- Inputs and outputs are LVTTL (3.3V) compatible
- 10 Ohm Resistors on DQs
- Single 3.3V ± 0.3V Power Supply
- Single Pulsed $\overline{RAS}$ interface
- SDRAMs have four internal banks
- Fully Synchronous to positive Clock Edge
- Data Mask for Byte Read/Write control
- Auto Refresh (CBR) and Self Refresh
- Automatic and controlled Precharge Commands

- Programmable Operation:
  - CAS Latency: 2, 3
  - Burst Type: Sequential or Interleave
  - Burst Length: 1, 2, 4, 8,
  - Operation: Burst Read and Write or Multiple Burst Read with Single Write
- Suspend Mode and Power Down Mode
- 12/9/2 Addressing (Row/Column/Bank)
- 4096 refresh cycles distributed across 64ms
- Serial Presence Detect
- Gold contacts , JEDEC MO-190 outline dimensions

## Description

NT128S64VH8C0GM is a 144-pin Synchronous DRAM Small Outline Dual In-line Memory Module (SO DIMM) that is organized as a 16Mx64 high-speed memory array. The SO DIMM uses eight 8Mx16 SDRAMs in 400mil TSOP II packages and achieves high-speed data transfer rates of up to 133 MHz by employing a prefetch / pipeline hybrid architecture that supports the JEDEC 1N rule while allowing very low burst power.

All control, address, and data input/output circuits are synchronized with the positive edge of the externally supplied clock inputs. All inputs are sampled at the positive edge of the externally supplied clock (CK0,CK1). Internal operating modes are defined by combinations of the $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ , $\overline{S0}$ , $\overline{S1}$, DQMB, and CKE0,CKE1 signals. A command decoder initiates the necessary timings for each operation. A 14 bit address bus accepts address information in a row/column multiplexing arrangement.

Prior to any access operation, the $\overline{CAS}$ latency, burst type, burst length, and burst operation type must be programmed into the SO DIMM by address inputs A0-A9 during the mode register set cycle. The SO DIMM uses serial presence detects implemented via a serial EEPROM using the two pin IIC protocol. The first 128 bytes of serial PD data are used by the DIMM manufacturer. The last 128 bytes are available to the customer.

All Nanya 144-pin SO DIMMs provide a high performance, flexible 8-byte interface in a 2.66" long space-saving footprint.

## Ordering Information

| Part Number | Speed | | | | Organization | Leads | Power |
|---|---|---|---|---|---|---|---|
| | MHz. | CL | t RCD | t RP | | | |
| NT128S64VH8C0GM-7K | 143MHz | 3 | 3 | 3 | | | |
| | 133MHz | 2 | 2 | 2 | | | |
| NT128S64VH8C0GM-75B | 133MHz | 3 | 3 | 3 | 16Mx64 | Gold | 3.3V |
| | 100MHz | 2 | 2 | 2 | | | |
| NT128S64VH8C0GM-8B | 125MHz | 3 | 3 | 3 | | | |
| | 100MHz | 2 | 2 | 2 | | | |

* CL = CAS Latency

**NT128S64VH8C0GM**
**128MB : 16M x 64**
**SDRAM SODIMM**

## Pin Description

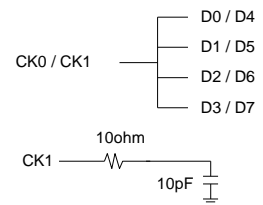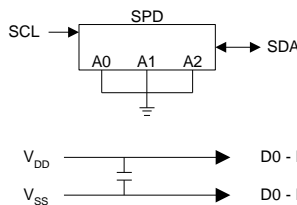| CK0, CK1 | Clock Inputs | DQ0-DQ63 | Data input/output |
|---|---|---|---|
| CKE0, CKE1 | Clock Enable | DQMB0-DQMB7 | Data Mask |
| $\overline{RAS}$ | Row Address Strobe | VDD | Power (3.3V) |
| $\overline{CAS}$ | Column Address Strobe | VSS | Ground |
| $\overline{WE}$ | Write Enable | NC | No Connect |
| $\overline{S0}$ , $\overline{S1}$ | Chip Selects | SCL | Serial Presence Detect Clock Input |
| A0-A9, A11 | Address Inputs | SDA | Serial Presence Detect Data input/output |
| A10 / AP | Address Input/Autoprecharge | DU | Don't use |
| BA0, BA1 | SDRAM Bank Address | | |

## Pinout

| Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | VSS | 2 | VSS | 51 | DQ14 | 52 | DQ46 | 95 | DQ21 | 96 | DQ53 |
| 3 | DQ0 | 4 | DQ32 | 53 | DQ15 | 54 | DQ47 | 97 | DQ22 | 98 | DQ54 |
| 5 | DQ1 | 6 | DQ33 | 55 | VSS | 56 | VSS | 99 | DQ23 | 100 | DQ55 |
| 7 | DQ2 | 8 | DQ34 | 57 | NC | 58 | NC | 101 | VDD | 102 | VDD |
| 9 | DQ3 | 10 | DQ35 | 59 | NC | 60 | NC | 103 | A6 | 104 | A7 |
| 11 | VDD | 12 | VDD | | | | | 105 | A8 | 106 | BA0 |
| 13 | DQ4 | 14 | DQ36 | | Voltage Key | | | 107 | VSS | 108 | VSS |
| 15 | DQ5 | 16 | DQ37 | | | | | 109 | A9 | 110 | BA1 |
| 17 | DQ6 | 18 | DQ38 | 61 | CK0 | 62 | CKE0 | 111 | A10/ AP | 112 | A11 |
| 19 | DQ7 | 20 | DQ39 | 63 | VDD | 64 | VDD | 113 | VDD | 114 | VDD |
| 21 | VSS | 22 | VSS | 65 | $\overline{RAS}$ | 66 | $\overline{CAS}$ | 115 | DQMB2 | 116 | DQMB6 |
| 23 | DQMB0 | 24 | DQMB4 | 67 | $\overline{WE}$ | 68 | CKE1 | 117 | DQMB3 | 118 | DQMB7 |
| 25 | DQMB1 | 26 | DQMB5 | 69 | $\overline{S0}$ | 70 | NC | 119 | VSS | 120 | VSS |
| 27 | VDD | 28 | VDD | 71 | $\overline{S1}$ | 72 | NC | 121 | DQ24 | 122 | DQ56 |
| 29 | A0 | 30 | A3 | 73 | DU | 74 | CK1 | 123 | DQ25 | 124 | DQ57 |
| 31 | A1 | 32 | A4 | 75 | VSS | 76 | VSS | 125 | DQ26 | 126 | DQ58 |
| 33 | A2 | 34 | A5 | 77 | NC | 78 | NC | 127 | DQ27 | 128 | DQ59 |
| 35 | VSS | 36 | VSS | 79 | NC | 80 | NC | 129 | VDD | 130 | VDD |
| 37 | DQ8 | 38 | DQ40 | 81 | VDD | 82 | VDD | 131 | DQ28 | 132 | DQ60 |
| 39 | DQ9 | 40 | DQ41 | 83 | DQ16 | 84 | DQ48 | 133 | DQ29 | 134 | DQ61 |
| 41 | DQ10 | 42 | DQ42 | 85 | DQ17 | 86 | DQ49 | 135 | DQ30 | 136 | DQ62 |
| 43 | DQ11 | 44 | DQ43 | 87 | DQ18 | 88 | DQ50 | 137 | DQ31 | 138 | DQ63 |
| 45 | VDD | 46 | VDD | 89 | DQ19 | 90 | DQ51 | 139 | VSS | 140 | VSS |
| 47 | DQ12 | 48 | DQ44 | 91 | VSS | 92 | VSS | 141 | SDA | 142 | SCL |
| 49 | DQ13 | 50 | DQ45 | 93 | DQ20 | 94 | DQ52 | 143 | VDD | 144 | VDD |

Note: All pin assignments are consistent for all 8-byte versions.

## SDRAM DIMM Block Diagram (2 Bank, 8Mx16 SDRAMs)
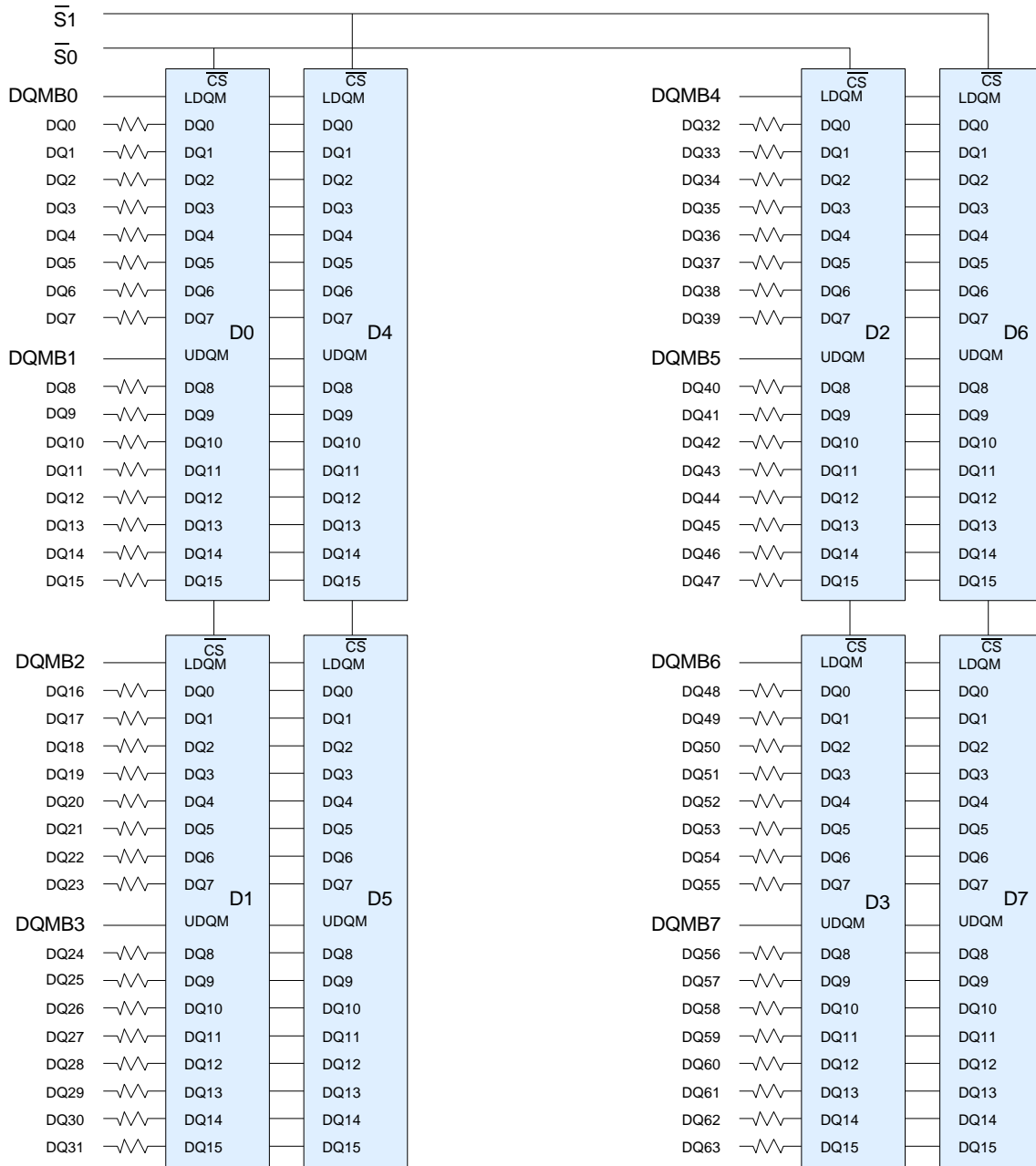


| Signal | Destination |
|---|---|
| $\overline{RAS}$ | SDRAMs D0-D7 |
| $\overline{CAS}$ | SDRAMs D0-D7 |
| CKE0 | SDRAMs D0-D3 |
| CKE1 | SDRAMs D4-D7 |
| $\overline{WE}$ | SDRAMs D0-D7 |
| A0-A11 | SDRAMs D0-D7 |
| BA0 | SDRAMs D0-D7 |
| BA1 | SDRAMs D0-D7 |
| DQn | Every DQ pin of SDRAM |

SPD — SCL, SDA, A0 A1 A2

$V_{DD}$ → D0 - D7
$V_{SS}$ → D0 - D7

CK0 / CK1 — D0 / D4, D1 / D5, D2 / D6, D3 / D7

CK1 — 10ohm — 10pF

## Input/Output Functional Description

| Symbol | Type | Signal | Polarity | Function |
|---|---|---|---|---|
| CK0, CK1 | Input | Pulse | Positive Edge | The system clock inputs. All of the SDRAM inputs are sampled on the rising edge of their associated clock. |
| CKE0, CKE1 | Input | Level | Active High | Activates the SDRAM CK0 and CK1 signals when high and deactivates them when low. By deactivating the clocks, CKE0 low initiates the Power Down mode, Suspend mode, or the Self-Refresh mode. |
| $\overline{S0}$, $\overline{S1}$ | Input | Pulse | Active Low | Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | Input | Pulse | Active Low | When sampled at the positive rising edge of the clock, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ define the operation to be executed by the SDRAM. |
| BA0, BA1 | Input | Level | - | Selects which SDRAM bank is to be active. |
| A0 – A11 A10/AP | Input | Level | - | During a Bank Activate command cycle, A0-A11 defines the row address (RA0-RA11) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0/BA1 define the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0/BA1 to control which bank(s) to precharge. If AP is high all 4 banks will be precharged regardless of the state of BA0/BA1. If AP is low, then BA0/BA1 are used to define which bank to pre-charge. |
| DQ0 - DQ63 | Input /Output | Level | - | Data and Check Bit input/output pins operate in the same manner as on conventional DRAMs. |
| DQMB0 -DQMB7 | Input | Pulse | Active High | The Data input/output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a byte mask by allowing input data to be written if it is low but blocks the Write operation if DQM is high. |
| SDA | Input /Output | Level | - | Serial Data. Bi-directional signal used to transfer data into and out of the Serial Presence Detect EEPROM. Since the SDA signal is Open Drain/Open Collector at the EEPROM, a pull-up resistor is required on the system board. |
| SCL | Input | Pulse | - | Serial Clock. Used to clock all Serial Presence Detect data into and out of the EEPROM. Since the SCL signal is inactive in the "high" state, a pull-up resistor is recommended on the system board. |
| VDD , VSS | Supply | | | Power and ground for the module. |

## Absolute Maximum Ratings

| Symbol | Parameter | Rating | Units | Notes |
|--------|-----------|--------|-------|-------|
| $V_{DD}$ | Power Supply Voltage | -0.3 to +4.6 | V | 1 |
| $V_{IN}$ | Input Voltage | -0.3 to $V_{DD}$ +0.3 | | |
| $V_{OUT}$ | Output Voltage | -0.3 to $V_{DD}$ +0.3 | | |
| $T_A$ | Operating Temperature (ambient) | 0 to +70 | °C | 1 |
| $T_{STG}$ | Storage Temperature | -55 to +125 | °C | 1 |
| $P_D$ | Power Dissipation | 3.5 | W | 1 |
| $I_{OUT}$ | Short Circuit Output Current | 50 | mA | 1 |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
   This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational
   sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

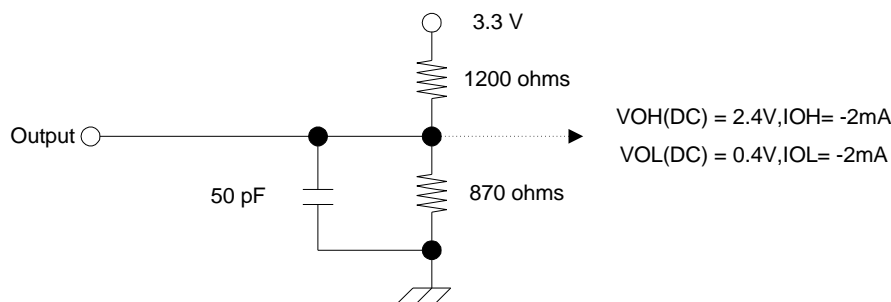## Recommended DC Operating Conditions ($T_A$ =0 to 70 °C)

| Symbol | Parameter | Rating | | | Units | Notes |
|--------|-----------|--------|--------|--------|-------|-------|
| | | Min. | Typ. | Max. | | |
| $V_{DD}$ | Power Voltage | 3.0 | 3.3 | 3.6 | V | 1 |
| $V_{IH}$ | Input High Voltage | 2.0 | - | $V_{DD}$ + 0.3 | V | 1,2 |
| $V_{IL}$ | Input Low Voltage | -0.3 | - | 0.8 | V | 1,3 |
| $V_{OH}$ | Output High Voltage | 2.4 | - | - | V | |
| $V_{OL}$ | Output Low Voltage | - | - | 0.4 | V | |
| $I_{IL}$ | Input Leakage current | -10 | - | 10 | µA | |

1. All voltages referenced to $V_{SS}$ .
2. $V_{IH}$ (max) = $V_{DD}$ / $V_{DDQ}$ + 1.2V for pulse width ≤ 5ns
3. $V_{IL}$ (min) = $V_{SS}$ / $V_{SSQ}$ - 1.2V for pulse width ≤ 5ns .

## Capacitance ($T_A$ =25 °C , f =1MHz, $V_{DD}$ =3.3 ± 0.3V)

| Symbol | Parameter | Max. | Unit |
|--------|-----------|------|------|
| $C_{I1}$ | Input Capacitance (A0-A9, A10/AP, A11, A12, BA0, BA1, $\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$ ) | 58 | pF |
| $C_{I2}$ | Input Capacitance (CKE0,CKE1) | 28 | |
| $C_{I3}$ | Input Capacitance ( $\overline{S0}$ , $\overline{S1}$ ) | 28 | |
| $C_{I4}$ | Input Capacitance (CK0,CK1 ) | 32 | |
| $C_{I5}$ | Input Capacitance (DQMB0 - DQMB7) | 14 | |
| $C_{I6}$ | Input Capacitance (SCL) | 13 | |
| $C_{IO1}$ | Input/Output Capacitance (DQ0 - DQ63) | 17 | |
| $C_{IO2}$ | Input/Output Capacitance (SDA) | 15 | |

## DC Output Load Circuit



3.3 V

1200 ohms

Output

VOH(DC) = 2.4V,IOH= -2mA
VOL(DC) = 0.4V,IOL= -2mA

50 pF

870 ohms

## Operating, Standby, and Refresh Currents ($T_A$ =0 to 70 °C , $V_{DD}$ =3.3 ± 0.3V)

| Parameter | Symbol | Test condition | Speed | | | Unit | Note |
|---|---|---|---|---|---|---|---|
| | | | - 7K | - 75B | - 8B | | |
| Operating current | $I_{CC1}$ | 1 bank operation , $t_{RC}$ = $t_{RC}$(mim), $t_{CK}$ = min<br>Active-Precharge Command cycling<br>without burst operation | 720 | 680 | 640 | mA | 1, 2 |
| Precharge<br>standby current<br>in power-down mode | $I_{CC2P}$ | CKE ≤ $V_{IL}$ (max), $t_{CK}$ = min,<br>$\overline{S0}$ , $\overline{S1}$= $V_{IH}$ (min) | | 16 | | mA | |
| | $I_{CC2PS}$ | CKE ≤ $V_{IL}$ (max), $t_{CK}$ =∞,<br>$\overline{S0}$ , $\overline{S1}$= $V_{IH}$ (min) | | 16 | | mA | |
| Precharge<br>standby current in non<br>power-down mode | $I_{CC2N}$ | CKE0 ≥ $V_{IH}$ (min), $t_{CK}$ = min<br>$\overline{S0}$ , $\overline{S1}$= $V_{IH}$ (min) | 400 | 360 | 280 | mA | 3 |
| | $I_{CC2NS}$ | CKE ≥ $V_{IH}$ (min), $t_{CK}$ =∞,<br>$\overline{S0}$ , $\overline{S1}$= $V_{IH}$ (min) | 72 | 72 | 72 | mA | 4 |
| No Operating current<br>( Active state : 4 bank) | $I_{CC3P}$ | CKE ≤ $V_{IL}$ (max), $t_{CK}$ =min.<br>$\overline{S0}$ , $\overline{S1}$= $V_{IH}$ (min) , (Power Down Mode) | 72 | 72 | 72 | mA | 5 |
| | $I_{CC3N}$ | CKE0 ≥ $V_{IH}$ (min), $t_{CK}$ =min<br>$\overline{S0}$ = $V_{IH}$ (min) | 400 | 400 | 320 | mA | 3 |
| Operating current<br>( Burst mode ) | $I_{CC4}$ | $t_{CK}$ =min , Read/ Write command cycling,<br>Multiple banks active, gapless data, BL=4 | 810 | 720 | 540 | mA | 2, 6 |
| Auto(CBR)<br>refresh current | $I_{CC5}$ | $t_{CK}$ =min, CBR command cycling | 960 | 960 | 860 | mA | |
| Self refresh current | $I_{CC6}$ | CKE0 ≤ 0.2V | | 16 | | mA | |
| Serial PD Device<br>Standby Current | $I_{SB}$ | $V_{IN}$ = GND or $V_{DD}$ | | 30 | | μA | 7 |

1. These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of $t_{CK}$ and $t_{RC}$ . Input signals
   are changed up to three times during $t_{RC}$ (min).
2. The specified values are obtained with the output open.
3. Input signals are changed once during three clock cycles.
4. Input signals are stable.
5. Active standby current will be higher if Clock Suspend is entered during a Burst Read cycle (add 1mA per DQ).
6. Input signals are changed once during $t_{CK}$(min) .
7. VDD =3.3V

## AC Characteristics (T$_A$ =0 to 70 °C , V$_{DD}$ =3.3 ± 0.3V)

1. An initial pause of 200μ,with DQMB0-7 and CKE held high, is required after power-up. A Precharge All Banks command must be given followed by a minimum of eight Auto (CBR) Refresh cycles before or after the Mode Register Set operation.

2. The Transition time is measured between V$_{IH}$ and V$_{IL}$ (or between V$_{IH}$ and V$_{IL}$ ).

3. In addition to meeting the transition rate specification, the CLK and CKE signals must transit between V$_{IH}$ and V$_{IL}$ (or between V$_{IL}$ and V$_{IH}$ ) in a monotonic manner.

4. AC timing tests have V$_{IL}$ =0.8V and V$_{IH}$ = 2.0 V with the timing referenced to the 1.40V cross over point.

5. AC measurements assume t T =1.2 ns.

## AC Output Load Circuits
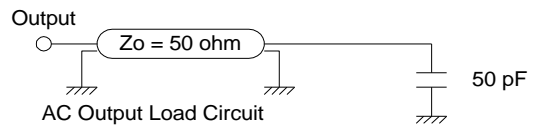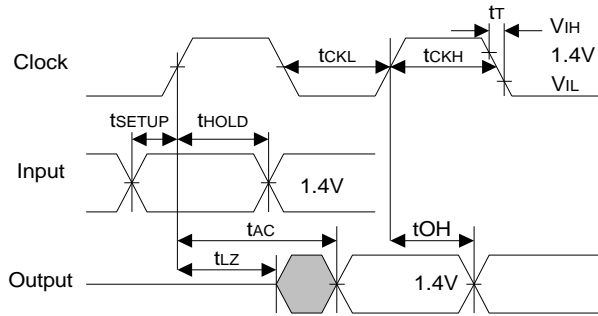
## AC Timing Parameters

### Clock and Clock Enable Parameters

| Symbol | Parameter | - 7K | | - 75B | | - 8B | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| tCK3 | Clock Cycle Time, $\overline{CAS}$ Latency = 3 | 7 | 1000 | 7.5 | 1000 | 8 | 1000 | ns | |
| tCK2 | Clock Cycle Time, $\overline{CAS}$ Latency = 2 | 7.5 | 1000 | 10 | 1000 | 10 | 1000 | ns | |
| tAC3(B) | Clock Access Time, $\overline{CAS}$ Latency = 3 | - | 5.4 | - | 5.4 | - | 6 | ns | 1 |
| tAC2(B) | Clock Access Time, $\overline{CAS}$ Latency = 2 | - | 5.4 | - | 6 | - | 6 | ns | 1 |
| tCKH | Clock High Pulse Width | 2.5 | - | 2.5 | - | 3 | - | ns | 2 |
| tCKL | Clock Low Pulse Width | 2.5 | - | 2.5 | - | 3 | - | ns | 2 |
| tCES | Clock Enable Set-up Time | 1.5 | - | 1.5 | - | 2 | - | ns | |
| tCEH | Clock Enable Hold Time | 0.8 | - | 0.8 | - | 1 | - | ns | |
| tSB | Power down mode Entry Time | 0 | 7.5 | 0 | 7.5 | 0 | 12 | ns | |
| tT | Transition Time (Rise and Fall) | 0.5 | 10 | 0.5 | 10 | 0.5 | 10 | ns | |

1.  Access time is measured at 1.4V. In AC Characteristics section, see notes.
2.  t CKH is the pulse width of CLK measured from the positive edge to the negative edge referenced to V$_{IH}$ (min). t CKL is the pulse width of CLK measured from the negative edge to the positive edge referenced to V$_{IL}$ (max).

### Common Parameters

| Symbol | Parameter | - 7K | | - 75B | | - 8B | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| tCS | Command Setup Time | 1.5 | - | 1.5 | - | 2 | - | ns | |
| tCH | Command Hold Time | 0.8 | - | 0.8 | - | 1 | - | ns | |
| tAS | Address and Bank Select Set-up Time | 1.5 | - | 1.5 | - | 2 | - | ns | |
| tAH | Address and Bank Select Hold Time | 0.8 | - | 0.8 | - | 1 | - | ns | |
| tRCD | $\overline{RAS}$ to $\overline{CAS}$ Delay | 20 | - | 20 | - | 20 | - | ns | 1 |
| tRC | Bank Cycle Time | 60 | - | 67.5 | - | 70 | - | ns | 1 |
| tRFC | Auto Refresh to Active/Auto Refresh | 60 | - | 67.5 | - | 70 | - | | |
| tRAS | Active Command Period | 45 | 100K | 45 | 100K | 50 | 100K | ns | 1 |
| tRP | Precharge Time | 20 | - | 20 | - | 20 | - | ns | 1 |
| tRRD | Bank to Bank Delay Time | 15 | - | 15 | - | 20 | - | ns | 1 |
| tCCD | $\overline{CAS}$ to $\overline{CAS}$ Delay Time | 1 | - | 1 | - | 1 | - | CLK | |

1.  These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows:
    the number of clock cycles = specified value of timing / clock period (count fractions as a whole number).

### Mode Register Set Cycle

| Symbol | Parameter | - 7K | | - 75B | | - 8B | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| tRSC | Mode Register Set Cycle Time | 2 | - | 2 | - | 2 | - | CLK | 1 |

1.  These parameters account for the number of clock cycle and depend on the operating frequency of the clock, as follows:
    the number of clock cycles = specified value of timing / clock period (count fractions as a whole number).

## Read Cycle

| Symbol | Parameter | - 7K | | - 75B | | - 8B | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| tOH | Data Out Hold Time | - | - | - | - | 2.5 | - | ns | |
| | | 2.7 | - | 2.7 | - | 3 | - | ns | |
| tLZ | Data Out to Low Impedance Time | 0 | - | 0 | - | 0 | - | ns | |
| tHZ3 | Data Out to High Impedance Time | 3 | 5.4 | 3 | 5.4 | 3 | 6 | ns | 1 |
| tDQZ | DQM Data Out Disable Latency | 2 | - | 2 | - | 2 | - | CLK | |

1. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.

## Refresh Cycle

| Symbol | Parameter | - 7K | | - 75B | | - 8B | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| tREF | Refresh Period | - | 64 | - | 64 | - | 64 | ms | |
| tSREX | Self Refresh Exit Time | 10 | - | 10 | - | 10 | - | ns | |

## Write Cycle

| Symbol | Parameter | - 7K | | - 75B | | - 8B | | Unit | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| tDS | Data In Set-up Time | 1.5 | - | 1.5 | - | 2 | - | ns | |
| tDH | Data In Hold Time | 0.8 | - | 0.8 | - | 1 | - | ns | |
| tDPL | Data input to Precharge | 15 | - | 15 | - | 15 | - | ns | |
| tDAL3 | Data In to Active Delay $\overline{CAS}$ Latency = 3 | 5 | - | 5 | - | 5 | - | CLK | |
| tDAL2 | Data In to Active Delay $\overline{CAS}$ Latency = 2 | 5 | - | - | - | - | - | CLK | |
| tDQW | DQM Write Mask Latency | 0 | - | 0 | - | 0 | - | ns | |

## Serial Presence Detect -- **Part 1 of 2**

*32Mx64 SDRAM SODIMM based on 8Mx16, 4Banks, 4K Refresh, 3.3V SDRAMs with SPD*

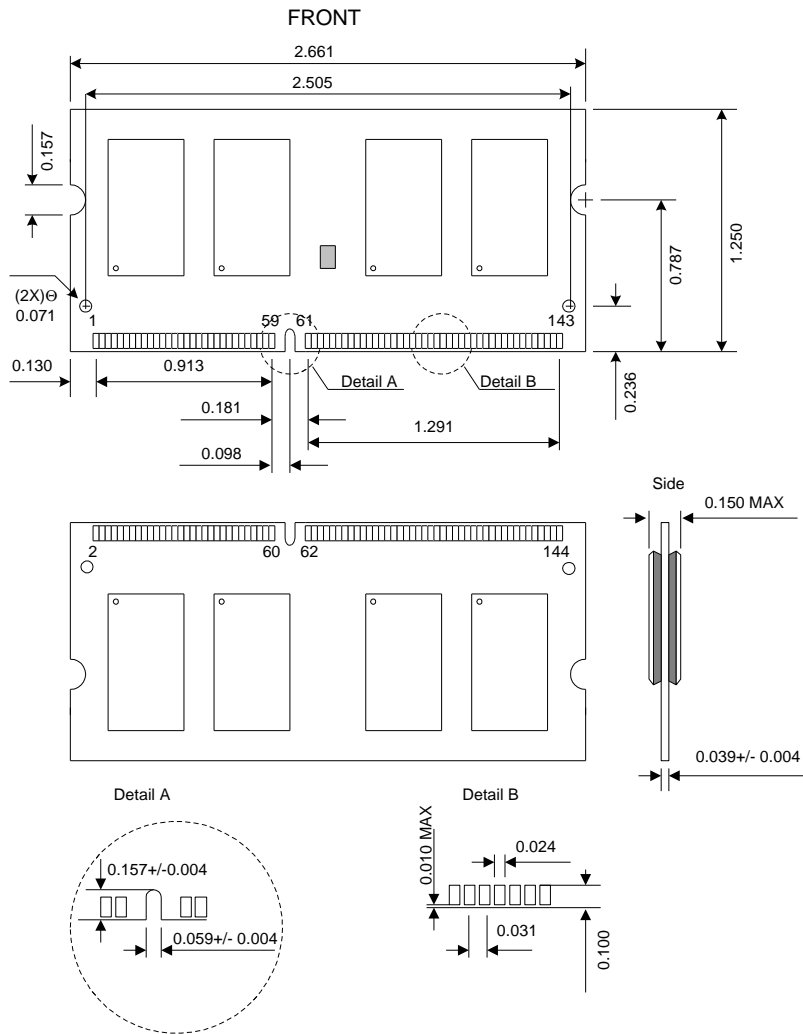| Byte | Description | SPD Entry Value | | | Serial PD Data Entry (Hexadecimal) | | | Note |
|------|-------------|-----|-----|-----|-----|-----|-----|------|
| | | -7K | -75B | -8B | -7K | -75 | -8B | |
| 0 | Number of Serial PD Bytes Written during Production | 128 | | | 80 | | | |
| 1 | Total Number of Bytes in Serial PD device | 256 | | | 08 | | | |
| 2 | Fundamental Memory Type | SDRAM | | | 04 | | | |
| 3 | Number of Row Addresses on Assembly | 12 | | | 0C | | | |
| 4 | Number of Column Addresses on Assembly | 9 | | | 09 | | | |
| 5 | Number of DIMM Bank | 2 | | | 02 | | | |
| 6 | Data Width of Assembly | X64 | | | 40 | | | |
| 7 | Data Width of Assembly (cont') | X64 | | | 00 | | | |
| 8 | Voltage Interface Level of this Assembly | LVTTL | | | 01 | | | |
| 9 | SDRAM Device Cycle Time at CL=3 | 7ns | 7.5ns | 8ns | 70 | 75 | 80 | |
| 10 | SDRAM Device Access Time from Clock at CL=3 | 5.4ns | 5.4ns | 6ns | 54 | 54 | 60 | |
| 11 | DIMM Configuration Type | Non-Parity | | | 00 | | | |
| 12 | Refresh Rate/Type | 15.625μs / SR | | | 80 | | | |
| 13 | Primary SDRAM Width | X16 | | | 10 | | | |
| 14 | Error Checking SDRAM Device Width | N/A | | | 00 | | | |
| 15 | SDRAM Device Attributes : Minimum Clock Delay, Random Column Access | 1 Clock | | | 01 | | | |
| 16 | SDRAM Device Attributes: Burst Length Supported | 1,2,4,8 | | | 0F | | | |
| 17 | SDRAM Device Attributes: Number of Device Banks | 4 | | | 04 | | | |
| 18 | SDRAM Device Attributes:  $\overline{\text{CAS}}$  Latency | 2, 3 | 2, 3 | 2, 3 | 06 | 06 | 06 | |
| 19 | SDRAM Device Attributes:  $\overline{\text{CS}}$  Latency | 0 | | | 01 | | | |
| 20 | SDRAM Device Attributes:  $\overline{\text{WE}}$  Latency | 0 | | | 01 | | | |
| 21 | SDRAM Module Attributes | Unbuffered | | | 00 | | | |
| 22 | SDRAM Device Attributes: General | Wr-1/Rd Burst, Precharge All, Auto-Precharge, VDD +/- 10% | | | 0E | | | |
| 23 | Minimum Clock Cycle at CL=2 | 7.5ns | 10ns | 10ns | 75 | A0 | A0 | |
| 24 | Maximum Data Access Time from Clock at CL=2 | 5.4ns | 6ns | 6ns | 54 | 60 | 60 | |
| 25 | Minimum Clock Cycle Time at CL=1 | N/A | | | 00 | | | |
| 26 | Maximum Data Access Time from Clock at CL=1 | N/A | | | 00 | | | |
| 27 | Minimum Row Precharge Time (t$_{RP}$) | 15ns | 20ns | 20ns | 0F | 14 | 14 | |
| 28 | Minimum Row Active to Row Active delay (t$_{RRD}$) | 15ns | 15ns | 20ns | 0F | 0F | 14 | |
| 29 | Minimum RAS to CAS delay (t$_{RCD}$) | 15ns | 20ns | 20ns | 0F | 14 | 14 | |
| 30 | Minimum RAS Pulse Width (t$_{RAS}$) | 45ns | 45ns | 50ns | 2D | 2D | 32 | |
| 31 | Module Bank Density | 64MB | | | 10 | | | |
| 32 | Address and Command Setup Time Before Clock | 1.5ns | 1.5ns | 2ns | 15 | 15 | 20 | |
| 33 | Address and Command Hold Time After Clock | 0.8ns | 0.8ns | 1ns | 08 | 08 | 10 | |
| 34 | Data Input Setup Time Before Clock | 1.5ns | 1.5ns | 2ns | 15 | 15 | 20 | |
| 35 | Data Input Hold Time After Clock | 0.8ns | 0.8ns | 1ns | 08 | 08 | 10 | |
| 36-61 | Reserved | Undefined | | | 00 | | | |
| 62 | SPD Revision | 1.2 | 1.2 | 1.2 | 12 | 12 | 12 | |
| 63 | Checksum for bytes 0 - 62 | | | | E1 | 27 | 6E | |

## Serial Presence Detect -- Part 2 of 2

*32Mx64 SDRAM SODIMM based on 8Mx16, 4Banks, 4K Refresh, 3.3V SDRAMs with SPD*

| Byte | Description | SPD Entry Value | | | Serial PD Data Entry (Hexadecimal) | | | Note |
|---|---|---|---|---|---|---|---|---|
| | | -7K | -75B | -8B | -7K | -75B | -8B | |
| 64-71 | Manufacturer's JEDED ID Code | 0B Hex. Bank 3 | | | 7F7F7F0B00000000 | | | 3 |
| 72 | Module Manufacturing Location | N/A | | | 00 | | | |
| 73-90 | Module Part number | N/A | N/A | N/A | 00 | 00 | 00 | |
| 91-92 | Module Revision Code | N/A | | | 00 | | | |
| 93-94 | Module Manufacturing Data | Year/Week Code | | | yy/ww | | | 1,2 |
| 95-98 | Module Serial Number | Serial Number | | | 00 | | | |
| 99-125 | Reserved | Undefined | | | 00 | | | |
| 126 | Modules Supports this Clock Frequency | 100MHz | | | 64 | | | |
| 127 | Attributes for Clock Frequency defined in byte 126 | CK0, CK1, CK2,CK3, CL3, CL2 Concurrent AP | | | FF | | | |
| 128-255 | Open for customer Use | Undefined | | | 00 | | | |

1. yy= Binary coded decimal year code, 0-99(Decimal), 00-63(Hex)

2. ww= Binary coded decimal year code, 01-52(Decimal), 01-34(Hex)

3. NANYA 11decimal (bank four) 0000 1011 binary 0B Hex.

## Package Dimensions

FRONT

2.661

2.505

0.157

1.250

0.787

(2X)Θ
0.071

1    59   61    143

0.130    0.913    Detail A    Detail B

0.236

0.181

0.098    1.291

Side

0.150 MAX

2    60   62    144

0.039+/- 0.004

Detail A    Detail B

0.010 MAX    0.024

0.157+/-0.004

0.059+/- 0.004    0.031    0.100

Note : All dimensions are typical unless otherwise stated.
Unit : Inches