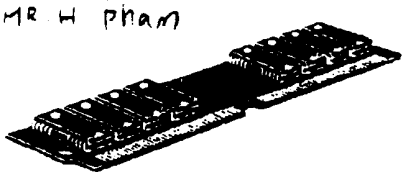
MELA/SVDL
MR H Pham



2/21/91

MITSUBISHI LSIs

MH25632BJ-7, -8, -10

8388608-BIT(262144-WORD BY 32-BIT)DYNAMIC RAM

(1/12) T.T.

DESCRIPTION

This is consists of eight industry 256K x 4 bit dynamic RAMs in SOJ.

The mounting of TSOP on a single in-line package provides any application where high densities and large quantities of memory are required.

This is a socket-type memory module, suitable for easy interchange or addition of module.

FEATURES

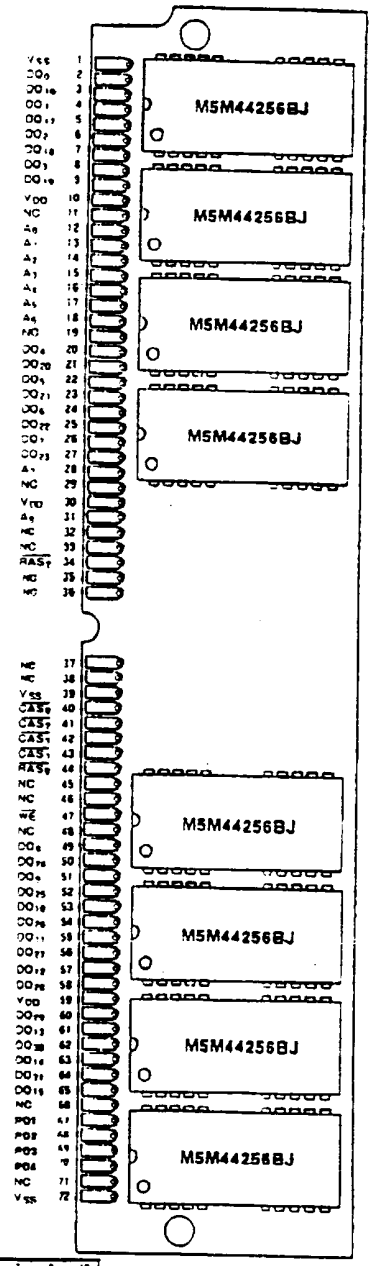
Type name	Access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
MH25632BJ-7	70	140	1840
MH25632BJ-8	80	160	1600
MH25632BJ-10	100	190	1400

- Single +5V (±10%) supply operation.
- 72-pins Single in-line package.
- Directly TTL Compatible: All Inputs and Outputs.
- Low standby power dissipation 22 mW (max) CMOS input level.
- Low operation power dissipation.
  - MH25632BJ-7 . . . . . 3.52 W (max)
  - MH25632BJ-8 . . . . . 3.08 W (max)
  - MH25632BJ-10 . . . . . 2.64 W (max)
- Includes (0.22 μF x 8) decoupling capacitors.
- 512 refresh cycles every 8ms.
- Fast page mode capability.
- The common I/O feature dictates the use of only early write operation to prevent contention on Data-in and Data-out.

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT.

PIN CONFIGURATION (TOP VIEW)



	-7	-8	-10
PD1	V_{SS}	V_{SS}	V_{SS}
PD2	NC	NC	NC
PD3	V_{SS}	NC	V_{SS}
PD4	NC	V_{SS}	V_{SS}

NC: NO CONNECTION

Outline 72N9

MITSUBISHI ELECTRIC

(2/12) T.T.

FUNCTION

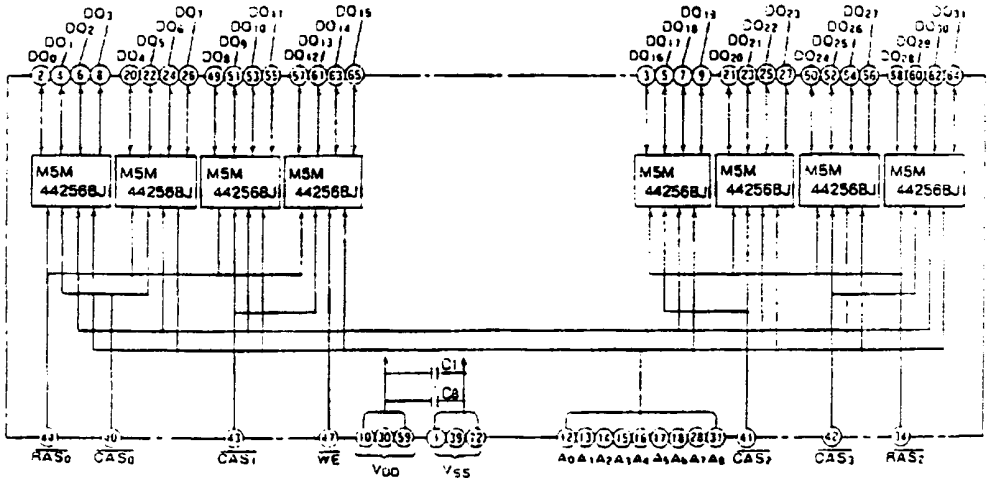
The MH25632BJ provide, in addition to normal read, and early write operations, a number of other functions, e.g., fast-page mode, $\overline{RAS}$-only refresh and $\overline{CAS}$ before $\overline{RAS}$ refresh. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Input					Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	APD	APD	OPN	VLD	YES	Fast page mode identical
Early write	ACT	ACT	ACT	APD	APD	VLD	OPN	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	DNC	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note: ACT: active, NAC: nonactive, DNC: don't care, VLD: valid, APD: applied, OPN: open

BLOCK DIAGRAM



(2/12) T-T

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−1−7	V
V_I	Input voltage		−1−7	V
V_O	Output voltage		−1−7	V
I_O	Output current		50	mA
P_d	Power dissipation	T_a=25°C	9	W
T_{opr}	Operating temperature		0−70	°C
T_{stg}	Storage temperature		-40−125	°C

RECOMMENDED OPERATING CONDITIONS (T_a=0−70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.5	V
V_{IL}	Low-level input voltage all inputs	-1.0		0.8	V

Note 1: All voltage values are with respect to V_{SS}.

ELECTRICAL CHARACTERISTICS (T_a=0−70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=−5mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≦V_{OUT}≦5.5V	−20		20	μA
I_I	Input current		0V≦V_{IH}≦6.5V, Other input pins=0V	-80		80	μA
$I_{CC1(AV)}$	Average supply current from V_{CC} operating (Note 3, 4)	MH25632BJ-7	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min, output open			640	mA
		MH25632BJ-8				560	
		MH25632BJ-10				480	
$I_{CC2(AV)}$	Supply current from V_{CC}, standby		$\overline{RAS}$=$\overline{CAS}$=V_{IH}, output open			16	mA
			$\overline{RAS}$=$\overline{CAS}$≧V_{CC}−0.5, output open			4	
$I_{CC3(AV)}$	Average supply current from V_{CC} refreshing (Note 3)	MH25632BJ-7	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min, output open			640	mA
		MH25632BJ-8				560	
		MH25632BJ-10				480	
$I_{CC4(AV)}$	Average supply current from V_{CC} Fast page mode (Note 3, 4)	MH25632BJ-7	$\overline{RAS}$=V_{IL}, $\overline{CAS}$=cycling t_{PC}=min, output open			560	mA
		MH25632BJ-8				480	
		MH25632BJ-10				400	
$I_{CC6(AV)}$	Average supply current from V_{CC} $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	MH25632BJ-7	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min, output open			640	mA
		MH25632BJ-8				560	
		MH25632BJ-10				480	

Note 2: Current flowing into an IC is positive, out is negative.
3: $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (T_a=0−70°C, V_{CC}=5V±10%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	V_I=V_{SS} f=1MHz V_i=25mVrms			88	pF
$C_{I(DQ)}$	Data input/data output capacitance				22	pF
$C_{I(\overline{W})}$	Input capacitance, write control input				104	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				57	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				36	pF

(4/12) T-T

SWITCHING CHARACTERISTICS (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 5)

Symbol	Parameter		Limits						Unit
			MH25632BJ-7		MH25632BJ-8		MH25632BJ-10		
			Min	Max	Min	Max	Min	Max	
t_{CAC}	Access time from $\overline{CAS}$	(Note 6, 7)		20		20		25	ns
t_{RAC}	Access time from $\overline{RAS}$	(Note 6, 8)		70		80		100	ns
t_{CAA}	Column address access time	(Note 6, 9)		35		40		50	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge	(Note 6, 10)		40		45		55	ns
t_{CLZ}	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		5		ns
t_{OFF}	Output disable time after $\overline{CAS}$ high	(Note 11)	0	20	0	20	0	25	ns

Note 5 An initial pause of 500μs is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles before proper device operation is achieved. Note that $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods of $\overline{RAS}$ inactivity before proper device operation is achieved.

6 Measured with a load circuit equivalent to 2TTL loads and 100pF.

7 Assume that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD(max)} \geq t_{RAD}$.

8 Assume that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$.

9 Assume that $t_{RCD} - t_{RAD} \leq t_{CAA(max)} - t_{CAC(max)}$ and $t_{RCD} \geq t_{RCD(max)}$.

10 Assume that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

11 $t_{OFF(max)}$ define the time at which the output achieves the high impedance state ($I_{OUT} \leq \pm 20\mu A$) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (For Read, Early Write, Fast-Page Mode Cycles)

(T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, V_{SS} = 0V, unless otherwise noted) (Note 12, 13)

Symbol	Parameter		Limits						Unit
			MH25632BJ-7		MH25632BJ-8		MH25632BJ-10		
			Min	Max	Min	Max	Min	Max	
t_{REF}	Refresh cycle time			8		8		8	ms
t_{RP}	$\overline{RAS}$ high pulse width		60		70		80		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 14)	20	50	25	60	25	75	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	(Note 15)	10		10		10		ns
t_{CPN}	$\overline{CAS}$ high pulse width		10		10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low	(Note 16)	15	35	20	40	20	50	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low		0		0		0		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low	(Note 17)	0	10	0	15	0	20	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low		10		15		15		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low or $\overline{W}$ low		15		20		20		ns
t_T	Transition time	(Note 18)	3	50	3	50	3	50	ns

Note 12 The timing requirements are assumed t_T = 5ns

13 $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

14 $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is less than $t_{RCD(max)}$, access time is t_{RAC}. If t_{RCD} is greater than $t_{RCD(max)}$, access time is defined as t_{CAC} and t_{CAA} as shown in note 7, 9.

15 t_{CRP} requirement is applicable for all $\overline{RAS}$/$\overline{CAS}$ cycles.

16 $t_{RAD(max)}$ is specified as a reference point only. If $t_{RAD} \geq t_{RAD(min)}$, access time is assumed by t_{CAA} for read cycle.

17 $t_{ASC(max)}$ is specified as a reference point only of address access time.

18 t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

(5/12) T-T

Read and Refresh Cycles

Symbol	Parameter		Limits						Unit
			MH25632BJ-7		MH25632BJ-8		MH25632BJ-10		
			Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time		140		160		190		ns
t_{RAS}	$\overline{RAS}$ low pulse width		70	10000	80	10000	100	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		20	10000	20	10000	25	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		70		80		100		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		20		20		25		ns
t_{RCS}	Read setup time before $\overline{CAS}$ low		0		0		0		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	(Note 19)	0		0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	(Note 19)	10		10		10		ns
t_{RAL}	Column address to $\overline{RAS}$ setup time		35		40		50		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time		0		0		0		ns

Note 19: Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.

Write Cycle (Early Write)

Symbol	Parameter		Limits						Unit
			MH25632BJ-7		MH25632BJ-8		MH25632BJ-10		
			Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time		140		160		190		ns
t_{RAS}	$\overline{RAS}$ low pulse width		70	10000	80	10000	100	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width		20	10000	20	10000	25	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low		70		80		100		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		20		20		25		ns
t_{WCS}	Write setup time before $\overline{CAS}$ low	(Note 20)	0		0		0		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low		15		15		20		ns
t_{WP}	Write pulse width		15		15		20		ns
t_{DS}	Data setup time		0		0		0		ns
t_{DH}	Data hold time after $\overline{CAS}$ low		15		15		20		ns

Note 20: When $t_{WCS} < t_{WCS(min)}$, Data input will contend with the data output because of the common I/O feature.

Fast Page Mode Cycle (Read, Early write Cycles)

Symbol	Parameter		Limits						Unit
			MH25632BJ-7		MH25632BJ-8		MH25632BJ-10		
			Min	Max	Min	Max	Min	Max	
t_{PC}	Fast page mode cycle time		45		50		60		ns
t_{RAS}	$\overline{RAS}$ low pulse width for read, write cycle		115	100000	130	100000	160	100000	ns
t_{CAS}	$\overline{CAS}$ low pulse width for read cycle		20	10000	20	10000	25	10000	ns
t_{CP}	$\overline{CAS}$ high pulse width	(Note 21)	10	25	10	25	10	25	ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low		20		20		25		ns

Note 21: $t_{CP(max)}$ is specified as a reference point only. If $t_{CP(max)} \leq t_{CP}$, access time is assumed by t_{CAC}.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 22)

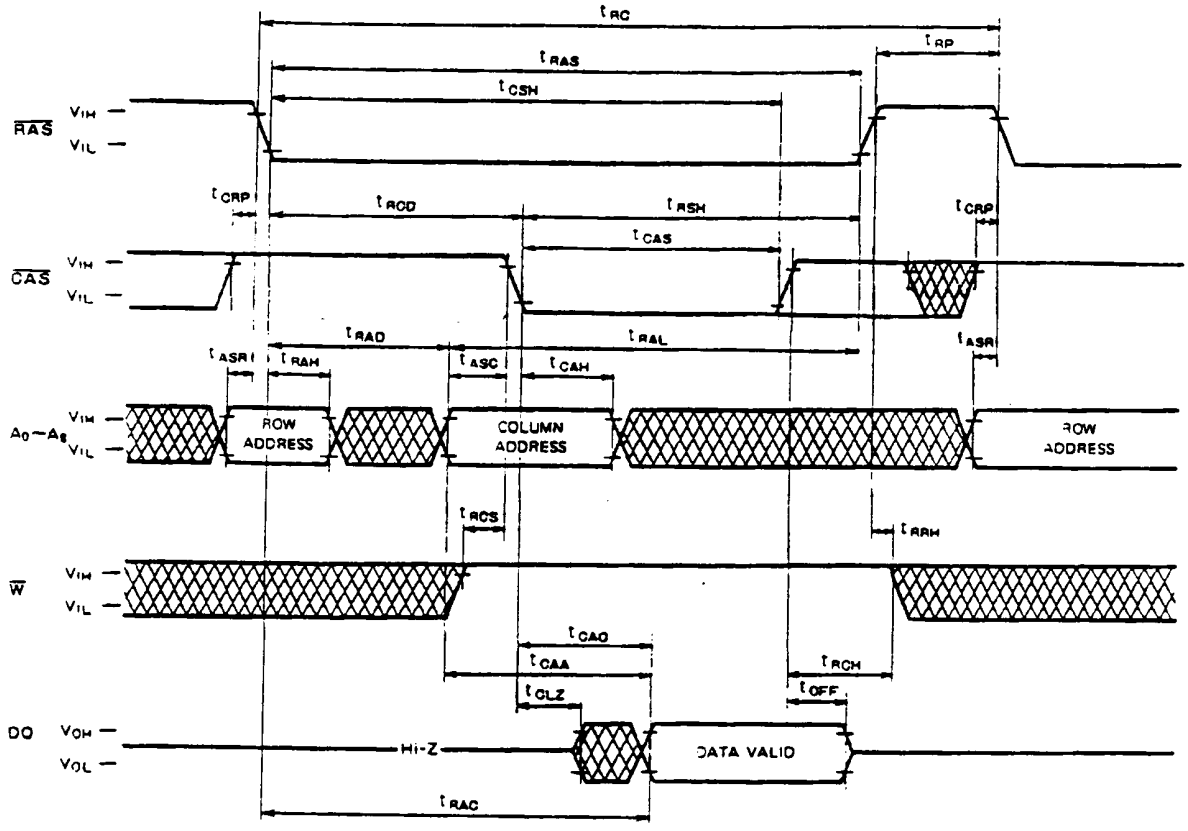
Symbol	Parameter	Limits						Unit
		MH25632BJ-7		MH25632BJ-8		MH25632BJ-10		
		Min	Max	Min	Max	Min	Max	
t_{CSR}	$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	10		10		10		ns
t_{CHR}	$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	15		15		20		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time	0		0		0		ns

Note 22: Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles is necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

(6/12) T.T.

Timing Diagrams (Note 23)

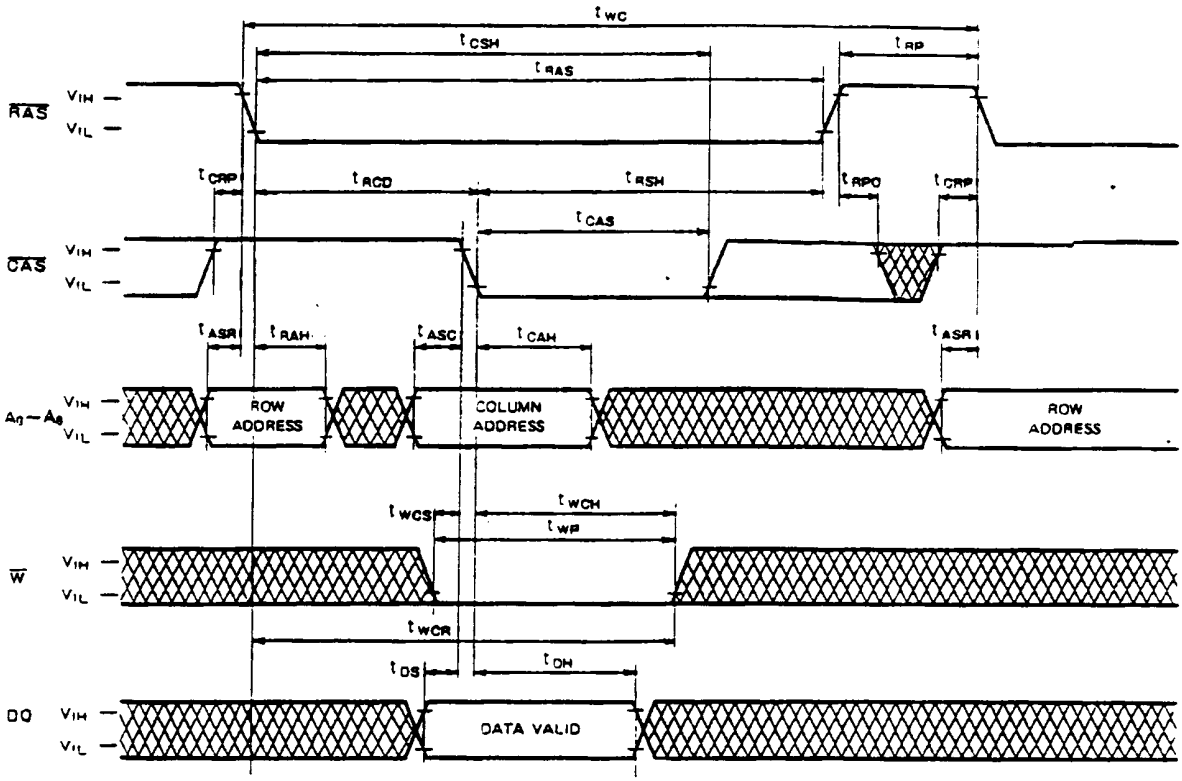
Read Cycle



Note 23. Indicates the don't care input.

(7/12)T.T.

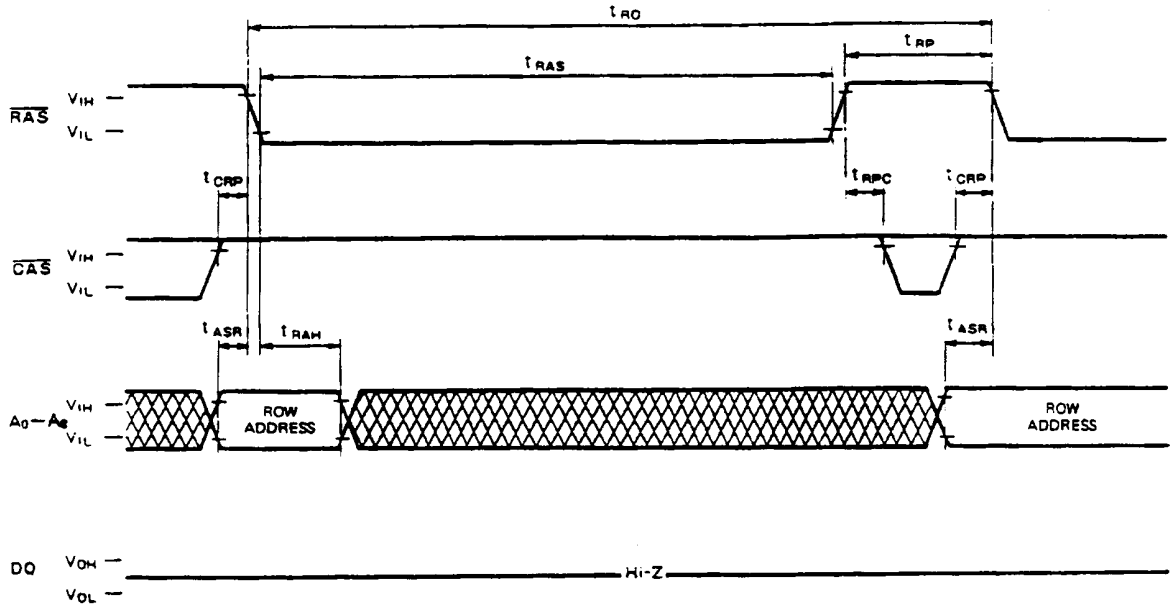
Early Write Cycle



(7/12)T.T.

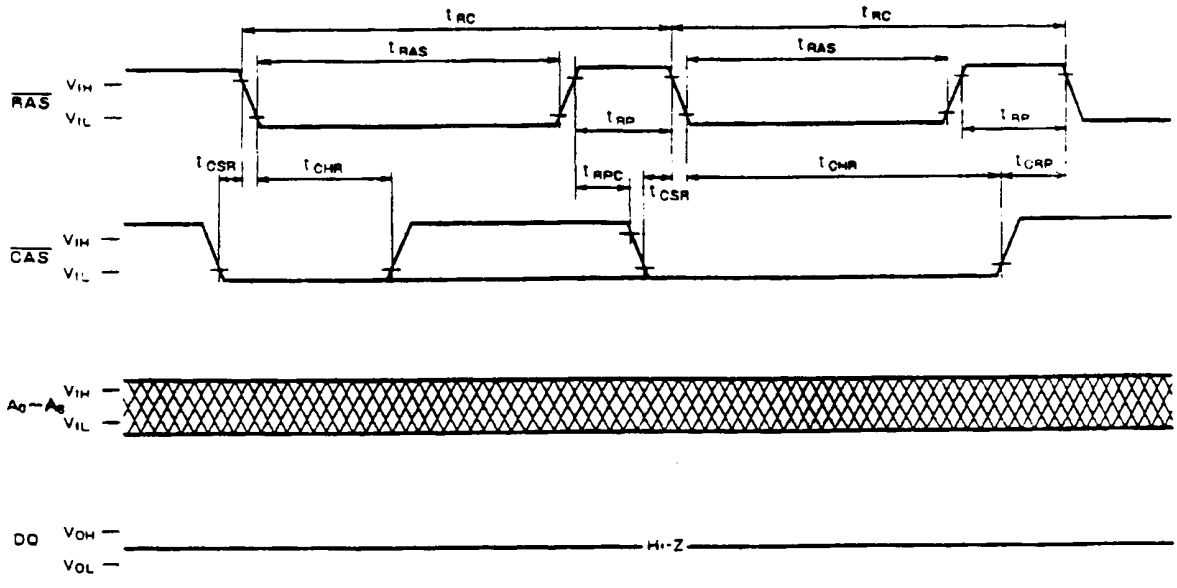
(8/12) T-T.

$\overline{RAS}$ only Refresh Cycle (Note 24)



Note 24. $\overline{W}$ = don't care.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 25)

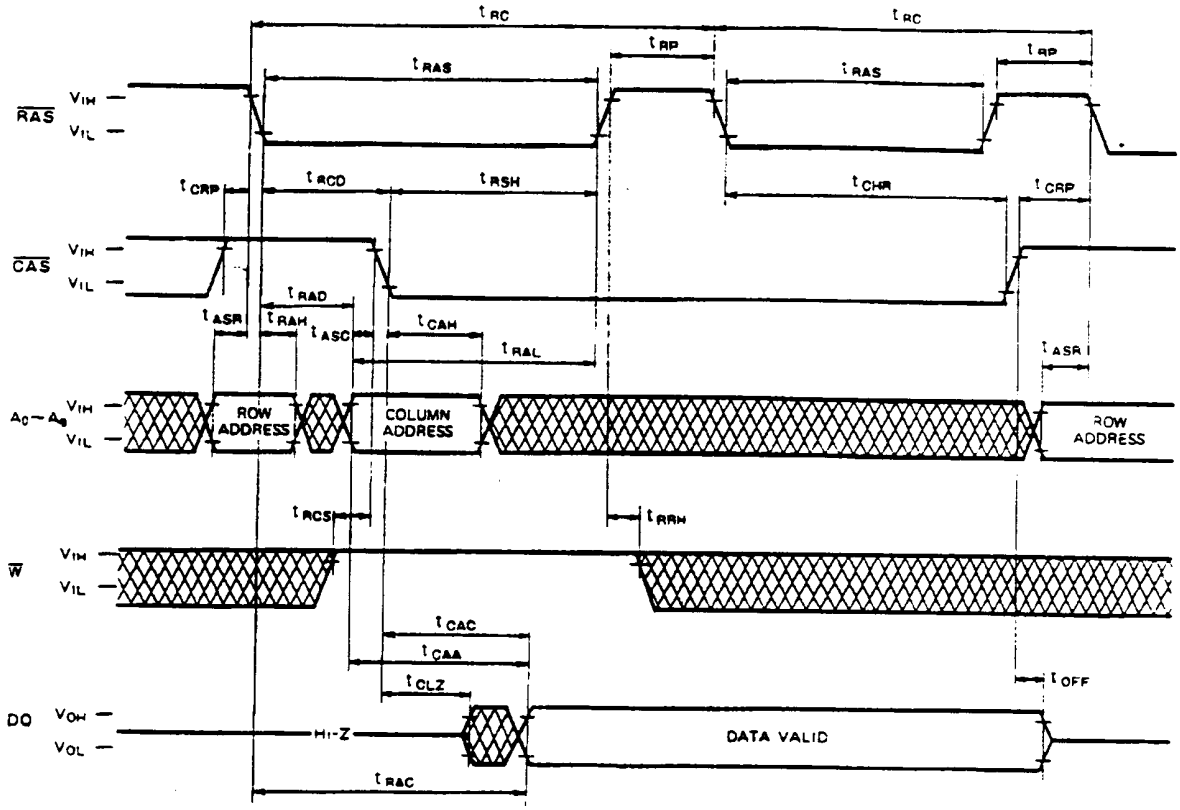


Note 25. $\overline{W}$ = don't care

(8/12) T-T.

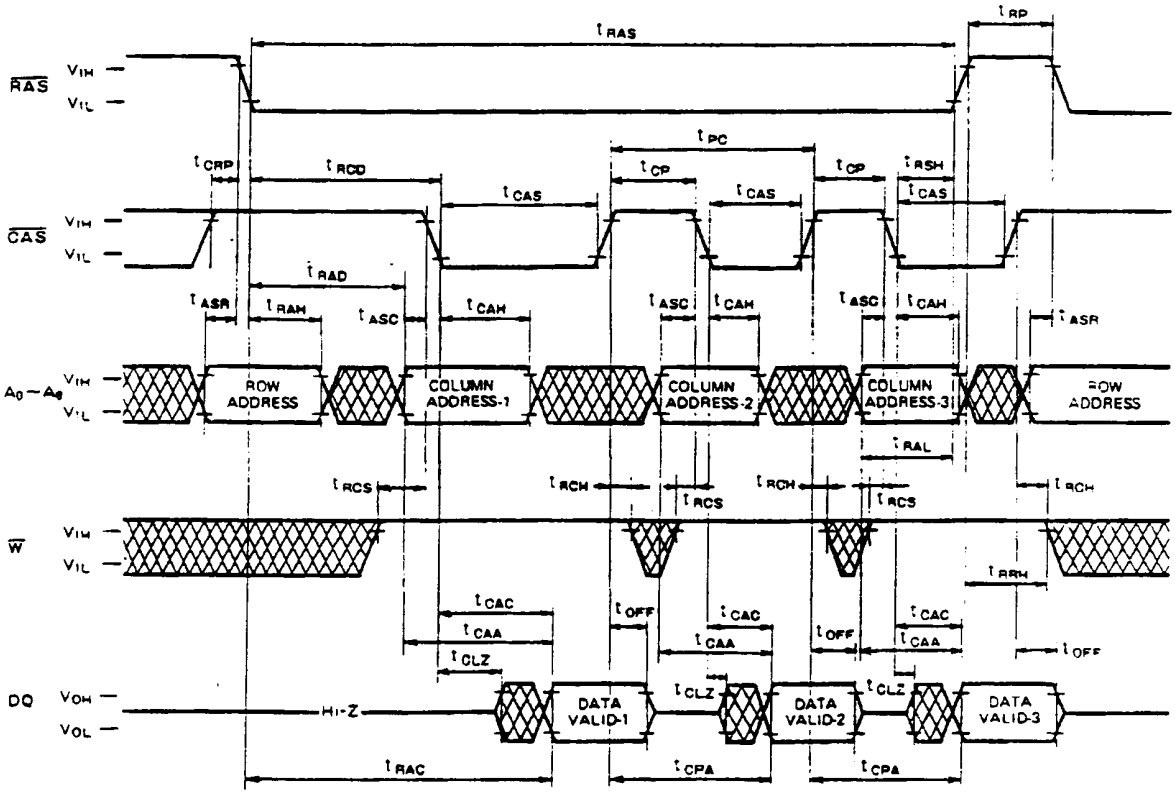
(9/12)T-T.

Hidden Refresh Cycle



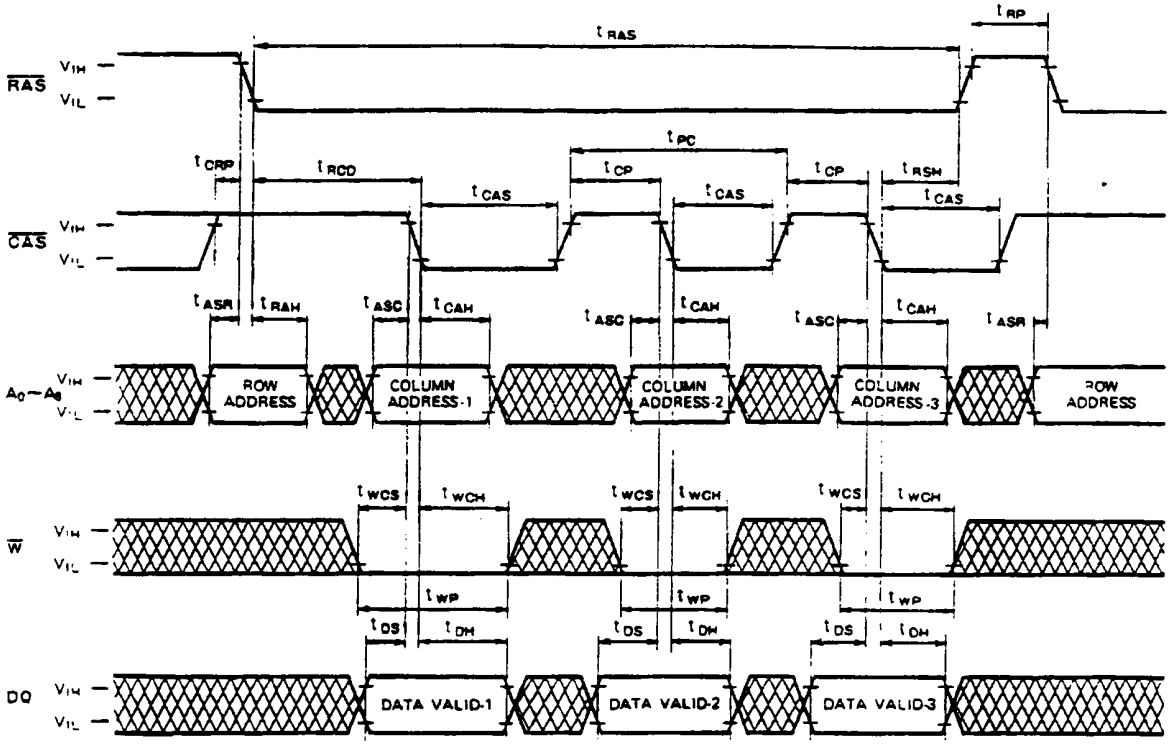
(10/12) T-T-

Fast-Page-Mode Read Cycle



(11/12)T-T-

Fast-Page-Mode Early Write Cycle



MECA/SUVL
MR. H. Pham

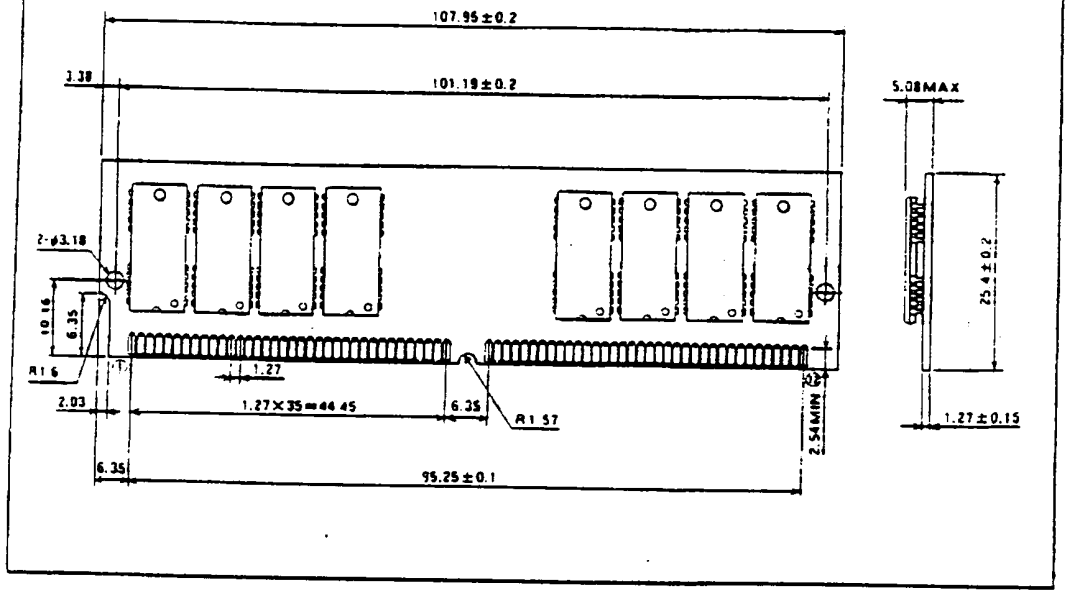
MH25632BJ-7, -8, -10

8388608-BIT(262144-WORD BY 32-BIT)DYNAMIC RAM

(12/12) T-T-

72N9 72pin Memory Module (MH25632BJ)

Dimension in mm



H-L0165-A KI-9003 Printed in Japan (TOT) III
New publication, effective Mar. 1990.
Specifications subject to change without notice.

(12/12) T-T-

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