MAX3986

1Gbps to 10.3Gbps Linear Equalizer

General Description

The MAX3986 is a 4-channel low-power linear equalizer optimized for use up to 10.3Gbps and compensates for losses encountered with FR-4 stripline and twin-ax cable. This linear equalizer is intended for use with decision-feedback equalizers (DFEs) integrated into ASICs as well as other applications where increased margin is needed rather than full signal regeneration. DFEs can typically handle 20dB of channel loss at a frequency half the bit rate, assuming the channel is not degraded by reflections and crosstalk. The extended linear range of the MAX3986 preserves the essential signal characteristics needed for optimum DFE performance. The 9dB of analog equalization of the MAX3986 adds to the effectiveness of the DFE. This increases margin to tolerate environmental and manufacturing variations or to increase the length of the transmission line. The MAX3986 operates from a single 3.3V supply and is housed in a lead-free, 5mm x 7mm TQFN package.

Applications

Serial 10.3Gbps Ethernet
8.5Gbps Fibre Channel
OIF-CEI-6G
DDR, 6.25Gbps IEEE 802.3ae XAUI
QDR, 10.0Gbps InfiniBand℠
6Gbps SAS
High-Speed Backplanes
Active Copper Cable Assemblies

Features

- **Increases Margin of Decision-Feedback Equalizers**
- **Compatible with OOB Signals**
- **Extends Transmission Line Length**
- **Coding Independent, 8b/10b or Scrambled**
- **4 Channels per Device**
- **9dB Analog Equalization at 5.15GHz**
- **Better Than 18dB Return Loss at 5.15GHz**
- **33mA per Channel Supply Current**
- **Single 3.3V Supply**
- **5mm x 7mm, Lead-Free TQFN Package**

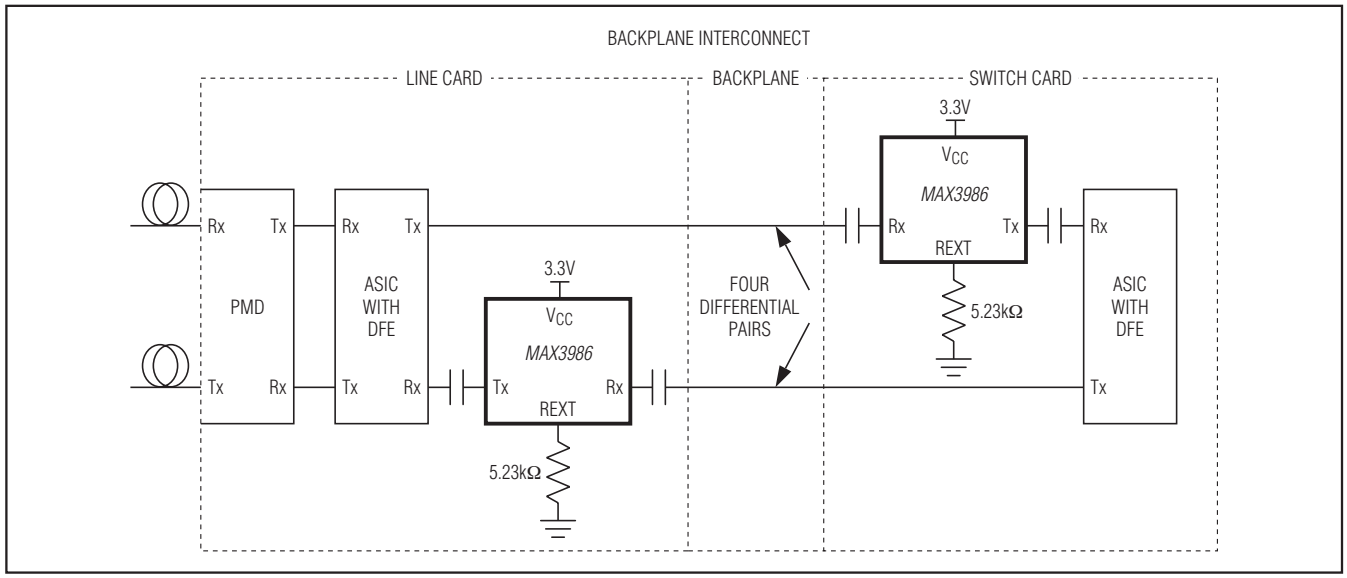
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3986UTU+	0°C to +85°C	38 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configuration appears at end of data sheet.

Typical Application Circuit



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For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-4403; Rev 0; 12/08

ABSOLUTE MAXIMUM RATINGS

(Operating beyond these limits will cause permanent damage.)

Supply Voltage Range, V_{CC} .....-0.5V to +4.1V
ESD Protection: Human Body Model
(Class 2 per JEDEC EIA/JESD22-A114-B).....≥ 2kV
Continuous Output Current Range
(OUT_+, OUT_-).....-25mA to +25mA
Data Input Range (IN_+, IN_-) .....-0.5V to (V_{CC} + 0.5V)
Bias Input Range (REXT, RINT).....-0.5V to (V_{CC} + 0.5V)
Operating Ambient Temperature.....0°C to +85°C
Continuous Power Dissipation (T_A = +70°C)
38-Pin TQFN (derate 35.7 mW/°C above +70°C) 2.85W
Storage Ambient Temperature Range.....-55°C to +150°C
Lead Temperature (soldering, 10s).....300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values measured at T_A = +25°C and V_{CC} = 3.3V, unless otherwise noted. All specifications in this table apply when $R_{EXTERNAL}$ is equal to 5.23kΩ.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	For all four channels		133	157	mA
Input Swing (IN)	Measured differentially at data source before encountering loss (point A in Figure 1) (Note 1)	200		1600	mV_{P-P}
Input Common-Mode Voltage Range			2.2		V
Input Return Loss	100MHz to 5.15GHz (Note 1)	19	24		dB
Differential Input Resistance	IN+ to IN-		100		Ω
Frequency Response	Sinewave, 80mV_{P-P} to 100mV_{P-P} (Notes 1, 2)	See limits in Table 1			
Large-Signal Gain	At 5.15GHz; sinewave, 80mV_{P-P} to 100mV_{P-P} (Notes 1, 2)	7	10	13	dB
Gain Variation with Temperature	Sinewave, 80mV_{P-P} to 100mV_{P-P}		0.6		dB
Compensation	At 5.15GHz relative to 100MHz; sinewave, 80mV_{P-P} to 100mV_{P-P}		9.4		dB
Output Swing Measured Differentially at OUT_+/- with 50Ω ±1% at Each Side	100MHz to 5.15GHz, 1600mV_{P-P} input (Note 3)		770	1000	mV_{P-P}
	0V applied to input (Note 1)			10	
Output Resistance	OUT_+ or OUT_-		50		Ω
Output Return Loss	100MHz to 5.15GHz (Note 1)	18	26		dB
Output Transition Time (t_R, t_F)	20% to 80% (Note 4)		45		ps
Propagation Delay			130		ps
Channel-to-Channel Isolation	Output relative to the input, 100MHz to 5.15GHz (Notes 1, 5)	31	33		dB
Channel-to-Channel Skew	Difference in propagation delay from one channel to any other channel (Note 1)			16	ps
Residual Deterministic Jitter Output	20in stripline FR-4 (Notes 1, 6, 7); 1Gbps ≤ data rate ≤ 6.25Gbps; data source amplitude = 200mV_{P-P}			0.1	UI

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +3.6V, T_A = 0°C to +85°C. Typical values measured at T_A = +25°C and V_{CC} = 3.3V, unless otherwise noted. All specifications in this table apply when $R_{EXTERNAL}$ is equal to 5.23kΩ.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Residual Deterministic Jitter Output	20in stripline FR-4 (Notes 1, 6, 7); 1Gbps ≤ data rate ≤ 6.25Gbps; data source amplitude = 500mV$_{P-P}$			0.09	UI
	20in stripline FR-4 (Notes 1, 6, 7); 1Gbps ≤ data rate ≤ 6.25Gbps; data source amplitude = 1600mV$_{P-P}$			0.1	
	20in stripline FR-4 (Notes 1, 6, 7); 6.25Gbps < data rate ≤ 8.5Gbps; data source amplitude = 200mV$_{P-P}$			0.18	
	20in stripline FR-4 (Notes 1, 6, 7); 6.25Gbps < Data Rate ≤ 8.5Gbps; data source amplitude = 500mV$_{P-P}$			0.15	
	20in stripline FR-4 (Notes 1, 6, 7); 6.25Gbps < data rate ≤ 8.5Gbps; data source amplitude = 1600mV$_{P-P}$			0.21	
	20in stripline FR-4 (Notes 1, 6, 7); 8.5Gbps < data rate ≤ 10.3Gbps; data source amplitude = 200mV$_{P-P}$			0.2	
	20in stripline FR-4 (Notes 1, 6, 7); 8.5Gbps < data rate ≤ 10.3Gbps; data source amplitude = 500mV$_{P-P}$			0.24	
	20in stripline FR-4 (Notes 1, 6, 7); 8.5Gbps < data rate ≤ 10.3Gbps; data source amplitude = 1600mV$_{P-P}$			0.26	
Output Referred Noise	10MHz to 5GHz, no other noise sources present (Notes 1, 8)		650	700	μV$_{RMS}$

Note 1: Guaranteed by design and characterization.

Note 2: With 50Ω terminations at OUT_+ and OUT_-, the gain is the ratio of the output swing to the input swing as measured at the input and output pins.

Note 3: Typical value is shown for 4.25GHz input frequency. Output swing is tested at 4.25GHz. Maximum value is guaranteed by design and characterization at all other frequencies between 100MHz and 5.15GHz.

Note 4: Using 0000011111 or equivalent pattern at 10.3Gbps. The signal generator transition time must be 20ps or less and an amplitude of 1600mV$_{P-P}$ differential applied to the inputs pins. The 0% reference should be established at least two bit intervals prior to the transition and the 100% reference level established at least two bit intervals after the transition.

Note 5: Measured using a vector-network analyzer (VNA) with 0dBm power level applied to the adjacent input. The VNA detects the signal at the output of the victim channel. All other inputs and outputs are terminated with 50Ω. 30dB includes the forward gain of the amplifier. See Figure 3.

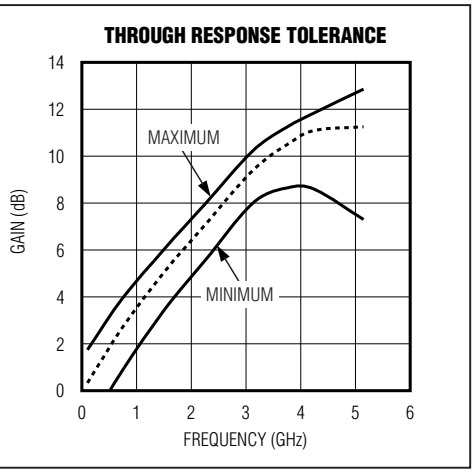
Note 6: Difference in deterministic jitter between the reference data source and equalizer output. Evaluated at 2.5Gbps, 3.2Gbps, 5Gbps, 6.25Gbps, 8.5Gbps, and 10.3Gbps. Pattern: PRBS 2^7, 100 zeros, 1, 0, 1, 0 PRBS 2^7, 100 ones, 0, 1, 0, 1. The data source amplitude is 200mV$_{P-P}$ to 1600mV$_{P-P}$ applied to the transmission line.

Note 7: Signal is applied differentially at input to a 6-mil-wide differential stripline. The deterministic jitter at the output of the transmission line must be from media-induced loss and not from clock source modulation. See Figure 1 for more information.

Note 8: Measured using a broadband power meter with BW ≤ 18GHz and a 17GHz differential to single-ended adapter (i.e., balun) for approximately 10GHz bandwidth. An additional filter is necessary to create a combined, total upper limit of 5GHz. See Figure 2.

Table 1. Response Tolerance Values

INPUT FREQUENCY (GHz)	LOW LIMIT (dB)	TYP (dB)	UPPER LIMIT (dB)
+0.1	-1.61	+0.34	+1.75
+0.75	+0.9	+2.74	+3.98
+1.5	+3.44	+5.05	+6.03
+2.25	+5.56	+7.09	+7.97
+3.125	+8.01	+9.40	+10.24
+3.75	+8.64	+10.50	+11.25
+4.25	+8.6	+11.10	+11.85
+5.15	+7.3	+11.26	+12.86



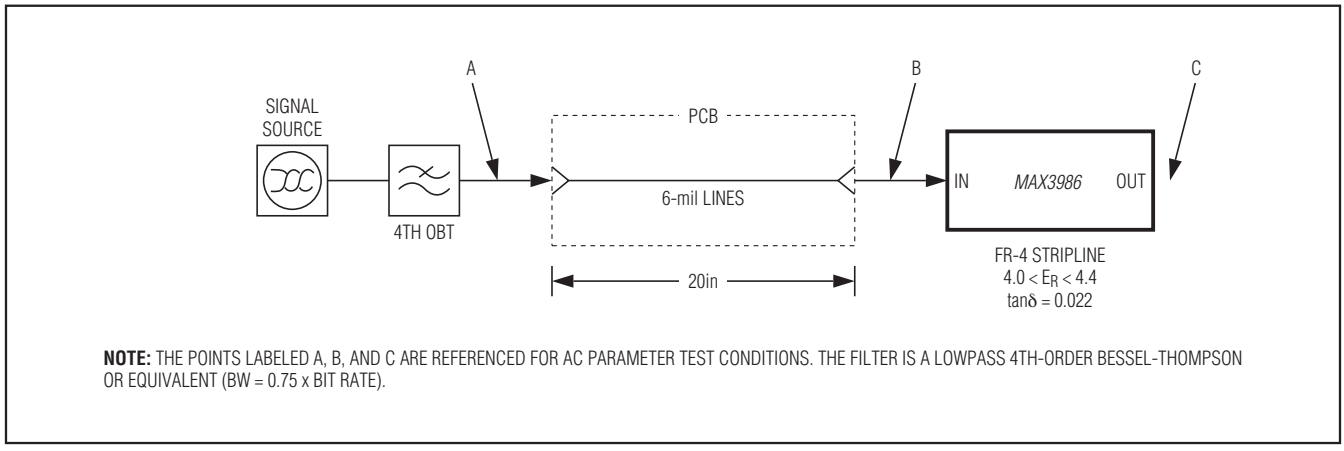


Figure 1. Conditions of Testing

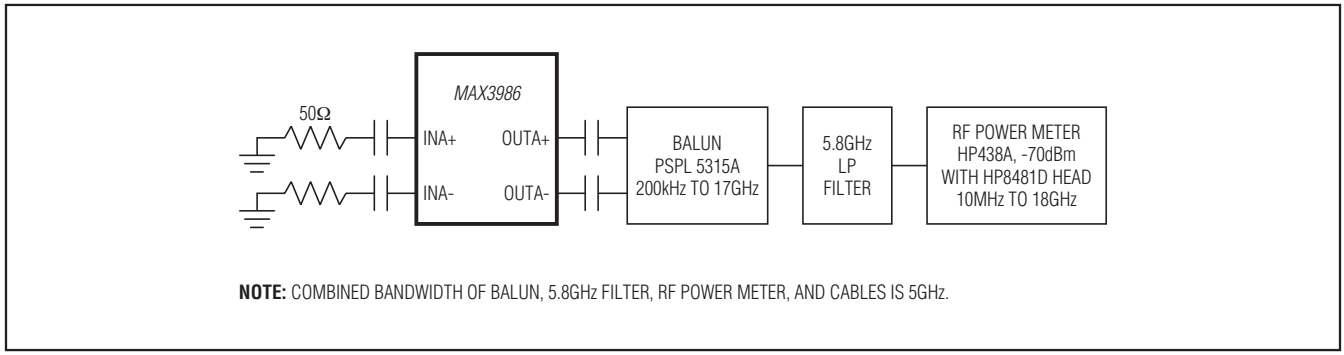


Figure 2. Noise Measurement Setup

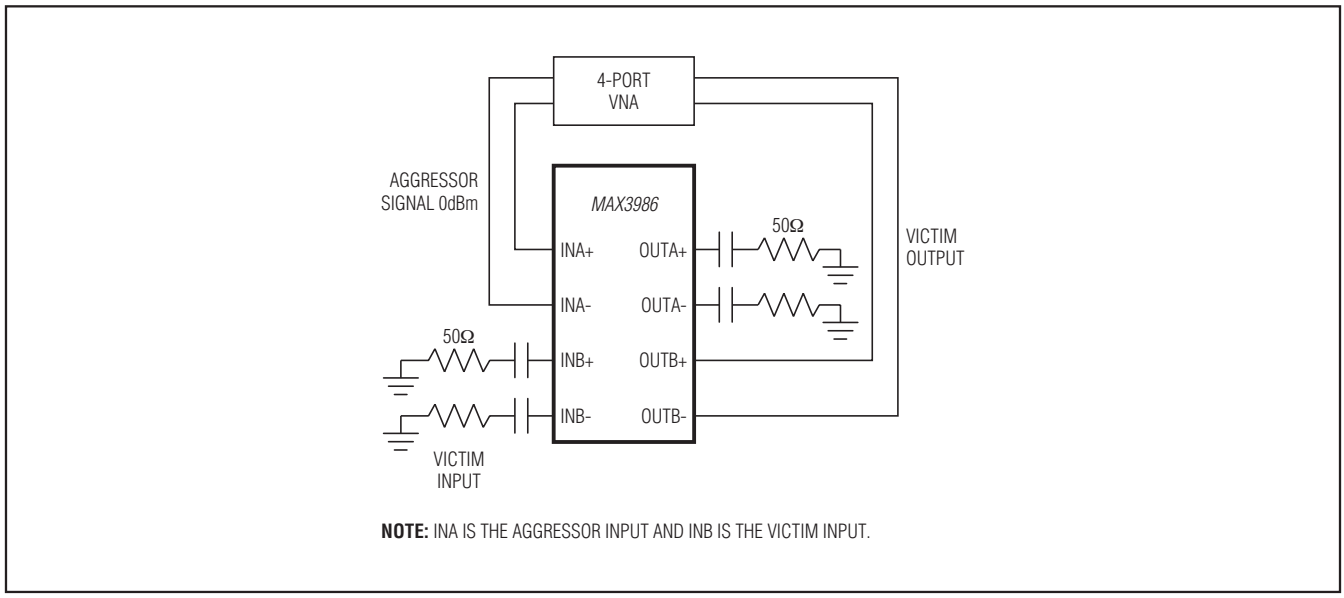
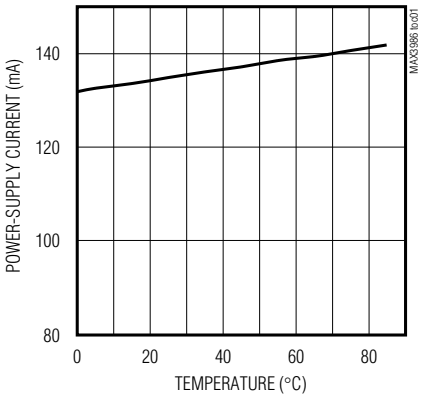


Figure 3. Channel Isolation Test Configuration

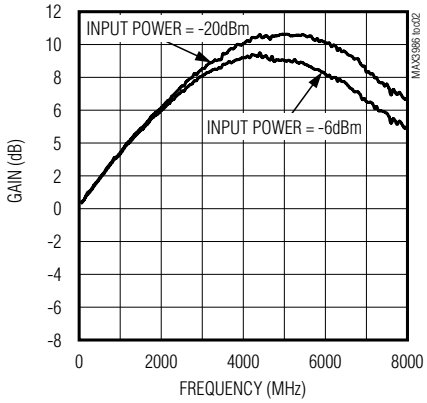
Typical Operating Characteristics

(All time domain measurements below 8.5Gbps use a 4th-order Bessel-Thompson filter with a bandwidth of 0.75 x bit rate. All time domain measurements are made with input signal amplitude of 500mVP-P. Data pattern: PRBS 2^7 , 100 zeros, 1, 0, 1, 0 PRBS 2^7, 100 ones, 0, 1, 0, 1. T_A = +25°C, unless otherwise noted.)

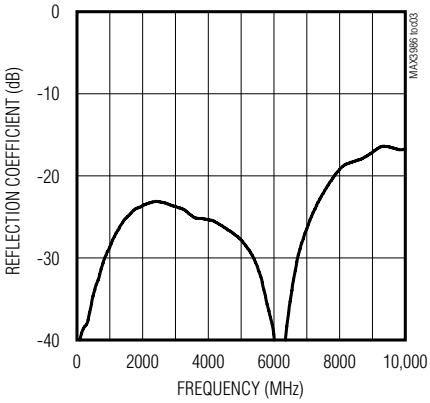
POWER-SUPPLY CURRENT vs. TEMPERATURE



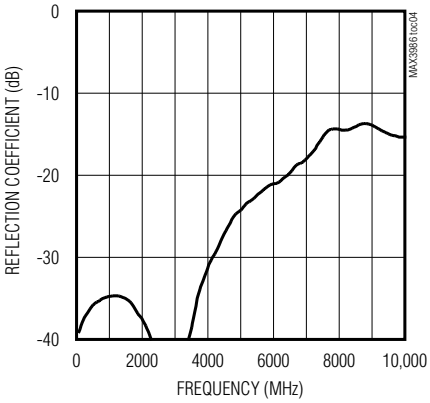
SDD21 vs. FREQUENCY GAIN (INPUT POWER = -20dBm and -6dBm)



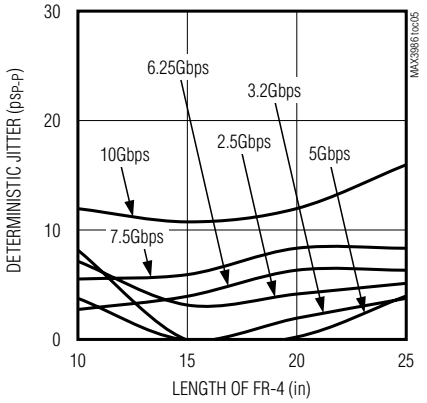
INPUT RETURN GAIN (SDD11) (INPUT SIGNAL OF -22dBm)



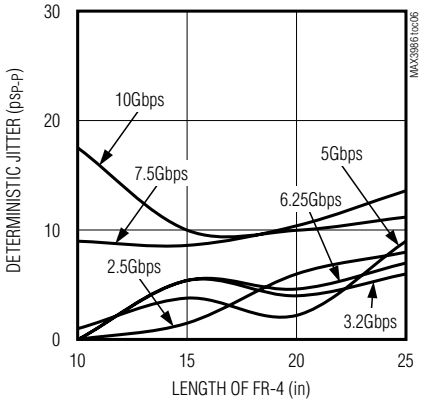
OUTPUT RETURN GAIN (SDD22) (INPUT SIGNAL OF -22dBm)



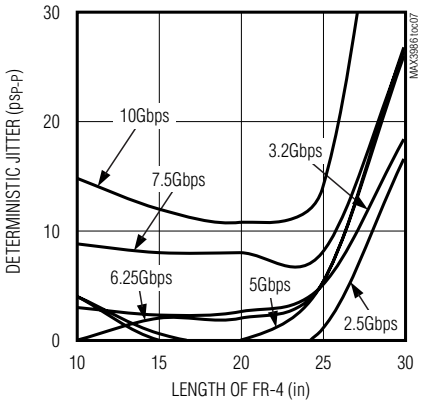
DETERMINISTIC JITTER vs. BOARD LENGTH (V_{IN} = 200mVP-P)



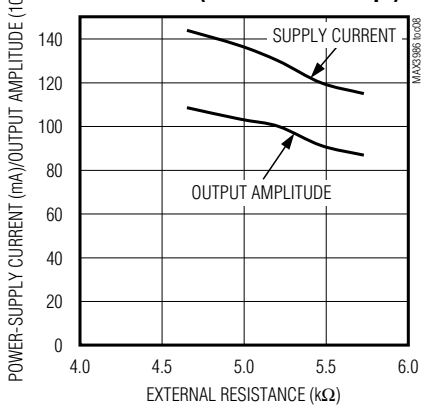
DETERMINISTIC JITTER vs. LENGTH (V_{IN} = 800mVP-P)



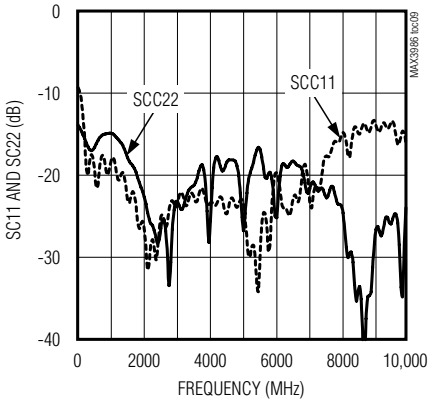
DETERMINISTIC JITTER vs. FREQUENCY (V_{IN} = 1600mVP-P)



NORMALIZED PERCENTAGE OUTPUT AMPLITUDE AND SUPPLY CURRENT vs. EXTERNAL RESISTANCE (DATA RATE = 7.5Gbps)



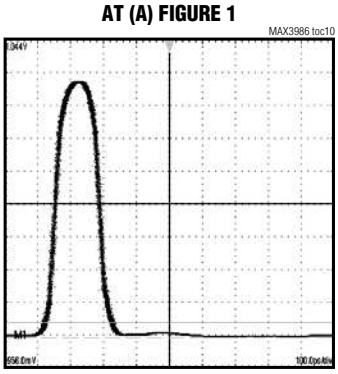
INPUT COMMON-MODE AND OUTPUT COMMON-MODE RATIO



Typical Operating Characteristics (continued)

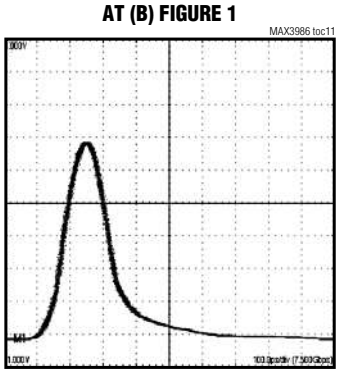
(All time domain measurements below 8.5Gbps use a 4th-order Bessel-Thompson filter with a bandwidth of 0.75 x bit rate. All time domain measurements are made with input signal amplitude of 500mV$_{P-P}$. Data pattern: PRBS 2^7 , 100 zeros, 1, 0, 1, 0 PRBS 2^7, 100 ones, 0, 1, 0, 1. T_A = +25°C, unless otherwise noted.)

INPUT PULSE TO 10in FR-4 BOARD AT (A) FIGURE 1



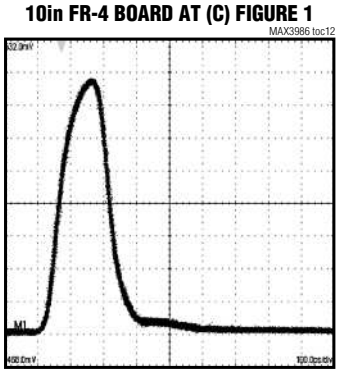
V - 200mV/div, H - 100ps/div

PULSE AFTER 10in FR-4 BOARD AT (B) FIGURE 1



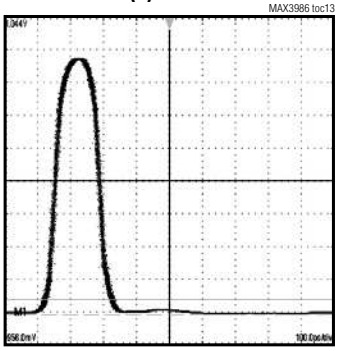
V - 200mV/div, H - 100ps/div

EQUALIZER OUTPUT PULSE AFTER 10in FR-4 BOARD AT (C) FIGURE 1



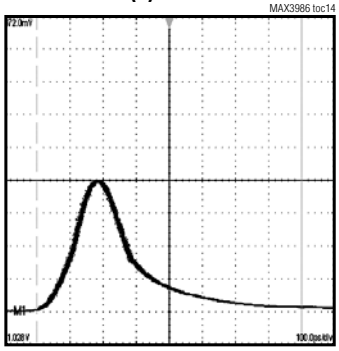
V - 100mV/div, H - 100ps/div

INPUT PULSE TO 20in FR-4 BOARD AT (A) FIGURE 1



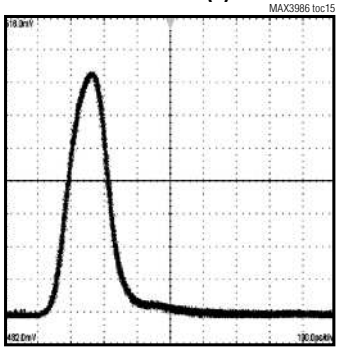
V - 200mV/div, H - 100ps/div

PULSE AFTER 20in FR-4 BOARD AT (B) FIGURE 1



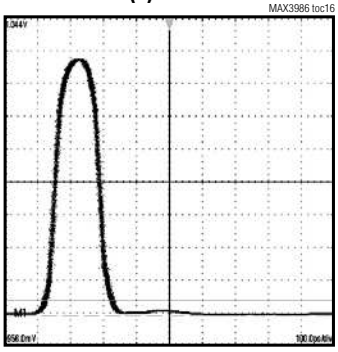
V - 200mV/div, H - 100ps/div

EQUALIZER OUTPUT PULSE AFTER 20in FR-4 BOARD AT (C) FIGURE 1



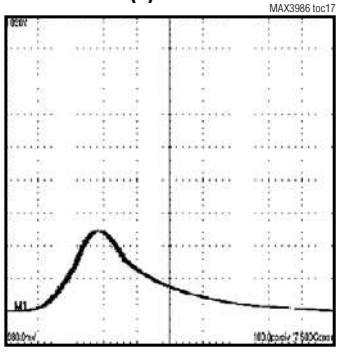
V - 100mV/div, H - 100ps/div

INPUT PULSE TO 30in FR-4 BOARD AT (A) FIGURE 1



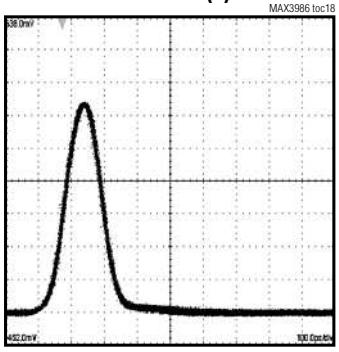
V - 200mV/div, H - 100ps/div

PULSE AFTER 30in FR-4 BOARD AT (B) FIGURE 1



V - 200mV/div, H - 100ps/div

EQUALIZER OUTPUT PULSE AFTER 30in FR-4 BOARD AT (C) FIGURE 1

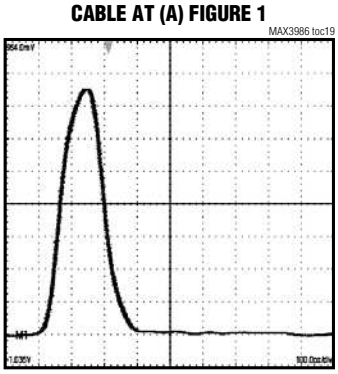


V - 100mV/div, H - 100ps/div

Typical Operating Characteristics (continued)

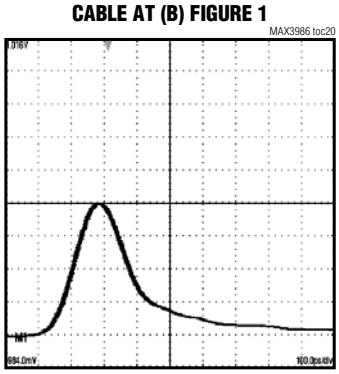
(All time domain measurements below 8.5Gbps use a 4th-order Bessel-Thompson filter with a bandwidth of 0.75 x bit rate. All time domain measurements are made with input signal amplitude of 500mV$_{P-P}$. Data pattern: PRBS 2^7 , 100 zeros, 1, 0, 1, 0 PRBS 2^7, 100 ones, 0, 1, 0, 1. T_A = +25°C, unless otherwise noted.)

INPUT PULSE TO 5m TWIN AX 24 AWG CABLE AT (A) FIGURE 1



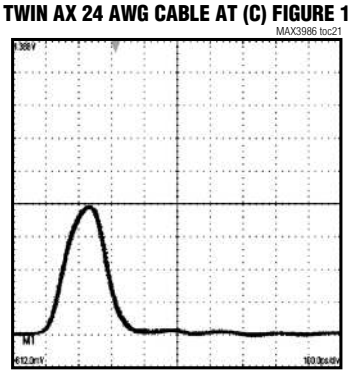
V - 200mV/div, H - 100ps/div

PULSE AFTER 5m TWIN AX 24 AWG CABLE AT (B) FIGURE 1



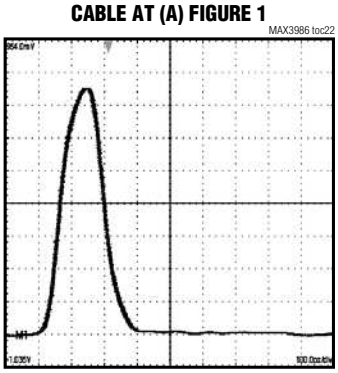
V - 200mV/div, H - 100ps/div

EQUALIZER OUTPUT PULSE AFTER 5m TWIN AX 24 AWG CABLE AT (C) FIGURE 1



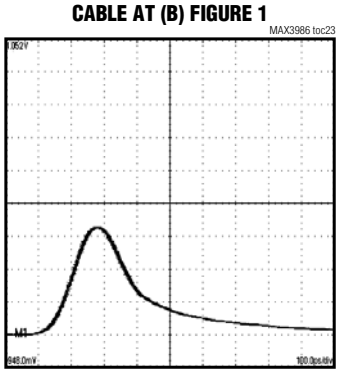
V - 200mV/div, H - 100ps/div

INPUT PULSE TO 7m TWIN AX 24 AWG CABLE AT (A) FIGURE 1



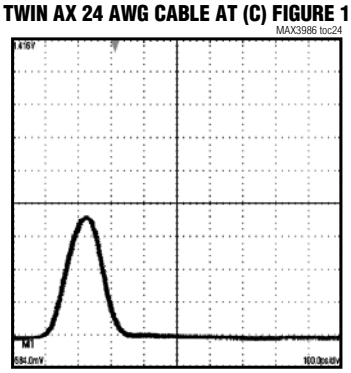
V - 200mV/div, H - 100ps/div

PULSE AFTER 7m TWIN AX 24 AWG CABLE AT (B) FIGURE 1



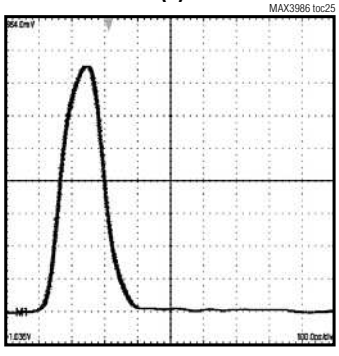
V - 200mV/div, H - 100ps/div

EQUALIZER OUTPUT PULSE AFTER 7m TWIN AX 24 AWG CABLE AT (C) FIGURE 1



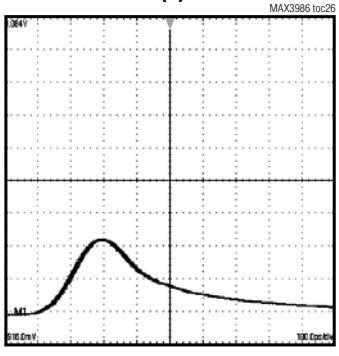
V - 200mV/div, H - 100ps/div

INPUT PULSE TO 10m TWIN AX 24 AWG CABLE AT (A) FIGURE 1



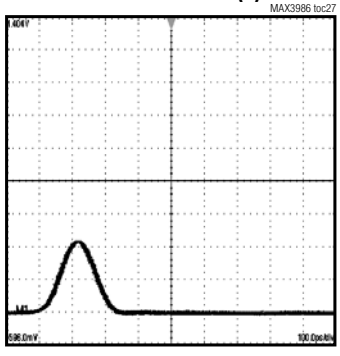
V - 200mV/div, H - 100ps/div

PULSE AFTER 10m TWIN AX 24 AWG CABLE AT (B) FIGURE 1



V - 200mV/div, H - 100ps/div

EQUALIZER OUTPUT PULSE AFTER 10m TWIN AX 24 AWG CABLE AT (C) FIGURE 1

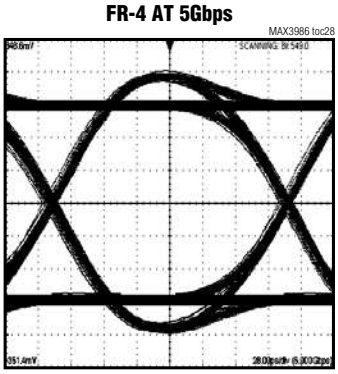


V - 200mV/div, H - 100ps/div

Typical Operating Characteristics (continued)

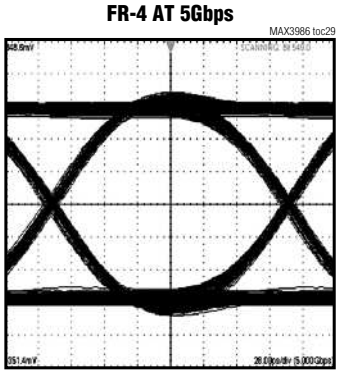
(All time domain measurements below 8.5Gbps use a 4th-order Bessel-Thompson filter with a bandwidth of 0.75 x bit rate. All time domain measurements are made with input signal amplitude of 500mV$_{P-P}$. Data pattern: PRBS 2^7 , 100 zeros, 1, 0, 1, 0 PRBS 2^7, 100 ones, 0, 1, 0, 1. T_A = +25°C, unless otherwise noted.)

MAX3986 OUTPUT FOR 15in FR-4 AT 5Gbps



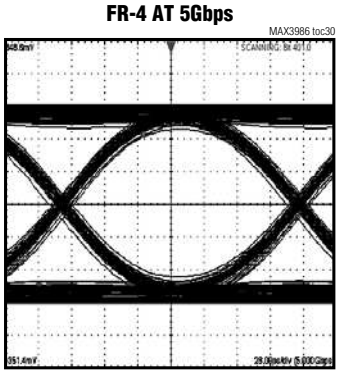
V - 70mV/div, H - 28ps/div

MAX3986 OUTPUT FOR 20in FR-4 AT 5Gbps



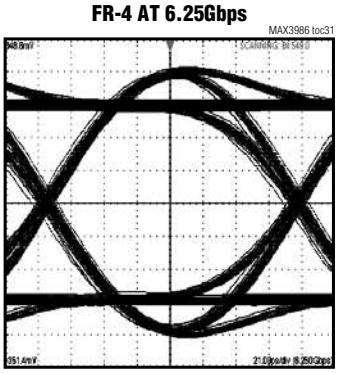
V - 70mV/div, H - 28ps/div

MAX3986 OUTPUT FOR 25in FR-4 AT 5Gbps



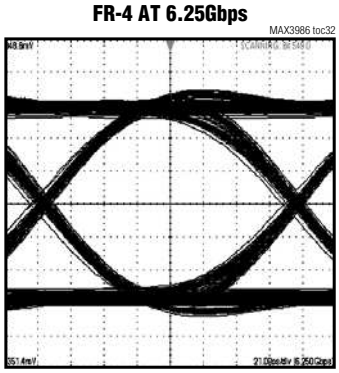
V - 70mV/div, H - 28ps/div

MAX3986 OUTPUT FOR 15in FR-4 AT 6.25Gbps



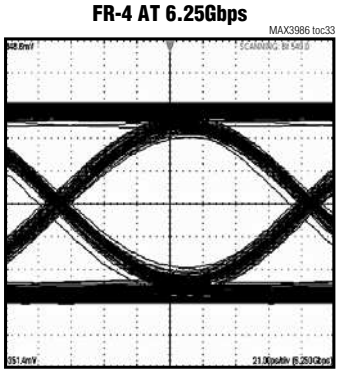
V - 70mV/div, H - 21ps/div

MAX3986 OUTPUT FOR 20in FR-4 AT 6.25Gbps



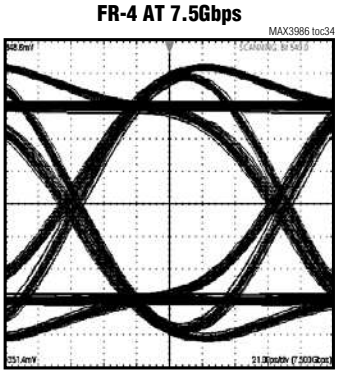
V - 70mV/div, H - 21ps/div

MAX3986 OUTPUT FOR 25in FR-4 AT 6.25Gbps



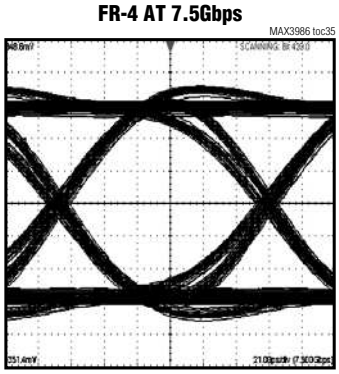
V - 70mV/div, H - 21ps/div

MAX3986 OUTPUT FOR 15in FR-4 AT 7.5Gbps



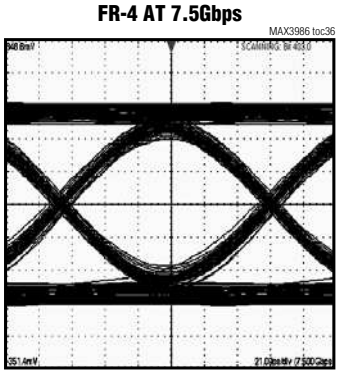
V - 70mV/div, H - 21ps/div

MAX3986 OUTPUT FOR 20in FR-4 AT 7.5Gbps



V - 70mV/div, H - 21ps/div

MAX3986 OUTPUT FOR 25in FR-4 AT 7.5Gbps

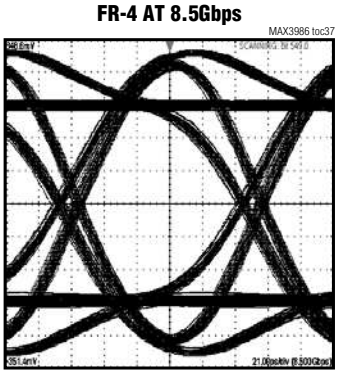


V - 70mV/div, H - 21ps/div

Typical Operating Characteristics (continued)

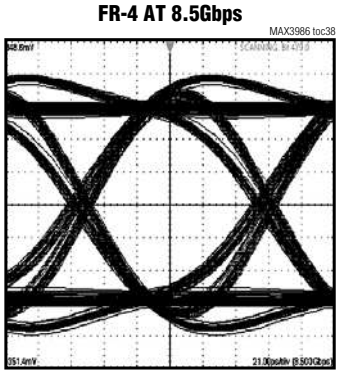
(All time domain measurements below 8.5Gbps use a 4th-order Bessel-Thompson filter with a bandwidth of 0.75 x bit rate. All time domain measurements are made with input signal amplitude of 500mV$_{P-P}$. Data pattern: PRBS 2^7 , 100 zeros, 1, 0, 1, 0 PRBS 2^7, 100 ones, 0, 1, 0, 1. T_A = +25°C, unless otherwise noted.)

MAX3986 OUTPUT FOR 15in FR-4 AT 8.5Gbps



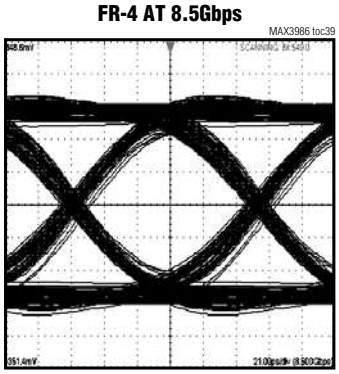
V - 70mV/div, H - 21ps/div

MAX3986 OUTPUT FOR 20in FR-4 AT 8.5Gbps



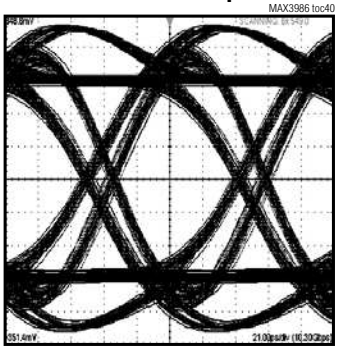
V - 70mV/div, H - 21ps/div

MAX3986 OUTPUT FOR 25in FR-4 AT 8.5Gbps



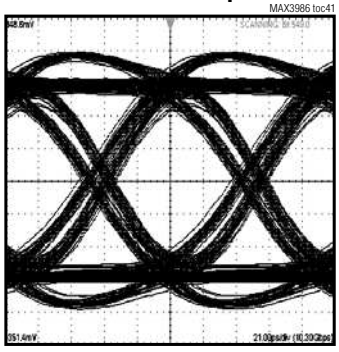
V - 70mV/div, H - 21ps/div

MAX3986 OUTPUT FOR 15in FR-4 AT 10.3Gbps



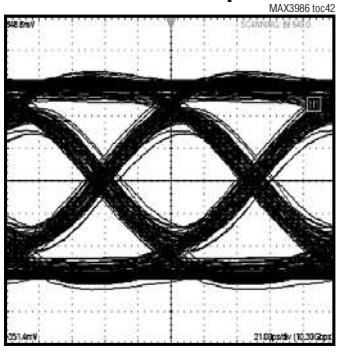
V - 70mV/div, H - 21ps/div

MAX3986 OUTPUT FOR 20in FR-4 AT 10.3Gbps



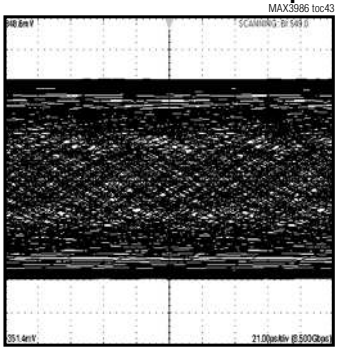
V - 70mV/div, H - 21ps/div

MAX3986 OUTPUT FOR 25in FR-4 AT 10.3Gbps



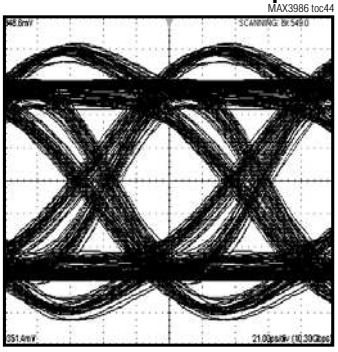
V - 70mV/div, H - 21ps/div

5m 24 AWG CABLE ASSEMBLY OUTPUT WITHOUT MAX3986 AT 10.3Gbps



V - 70mV/div, H - 21ps/div

5m 24 AWG CABLE ASSEMBLY OUTPUT WITH MAX3986 AT 10.3Gbps



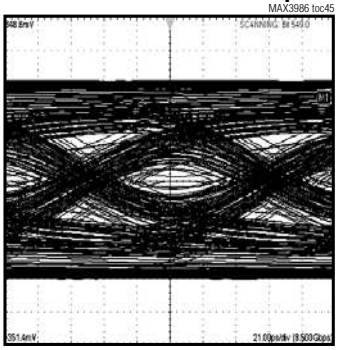
V - 70mV/div, H - 21ps/div

Typical Operating Characteristics (continued)

(All time domain measurements below 8.5Gbps use a 4th-order Bessel-Thompson filter with a bandwidth of 0.75 x bit rate. All time domain measurements are made with input signal amplitude of 500mV$_{P-P}$. Data pattern: PRBS 2^7 , 100 zeros, 1, 0, 1, 0 PRBS 2^7, 100 ones, 0, 1, 0, 1. T_A = +25°C, unless otherwise noted.)

5m 24 AWG CABLE ASSEMBLY OUTPUT WITHOUT MAX3986 AT 8.5Gbps

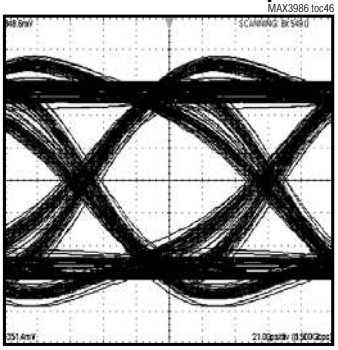
MAX3986 toc45



V - 70mV/div, H - 21ps/div

5m 24 AWG CABLE ASSEMBLY OUTPUT WITH MAX3986 AT 8.5Gbps

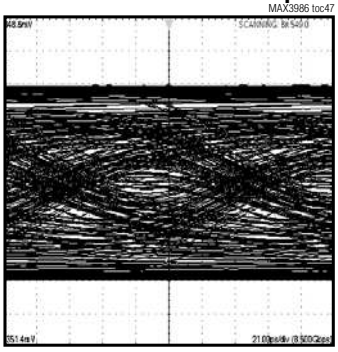
MAX3986 toc46



V - 70mV/div, H - 21ps/div

7m 24 AWG CABLE ASSEMBLY OUTPUT WITHOUT MAX3986 AT 8.5Gbps

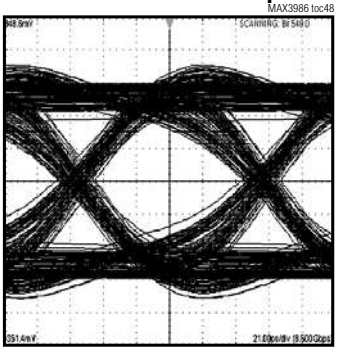
MAX3986 toc47



V - 70mV/div, H - 21ps/div

7m 24 AWG CABLE ASSEMBLY OUTPUT WITH MAX3986 AT 8.5Gbps

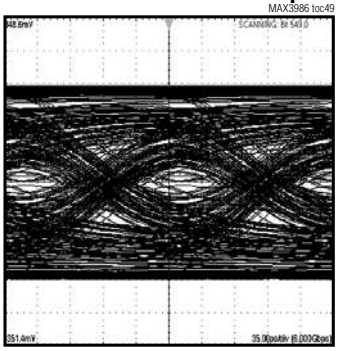
MAX3986 toc48



V - 70mV/div, H - 21ps/div

7m 24 AWG CABLE ASSEMBLY OUTPUT WITHOUT MAX3986 AT 6.25Gbps

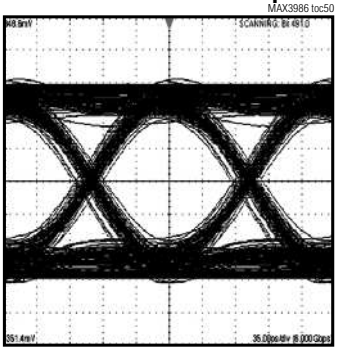
MAX3986 toc49



V - 70mV/div, H - 35ps/div

7m 24 AWG CABLE ASSEMBLY OUTPUT WITH MAX3986 AT 6.25Gbps

MAX3986 toc50



V - 70mV/div, H - 35ps/div

Pin Description

PIN	NAME	FUNCTION
1, 4, 7, 10, 13, 18, 32, 37	V_{CC}	Supply Voltage
2	OUT1+	Differential Positive CML Data Output. CML output with 50Ω to V_{CC}.
3	OUT1-	Differential Negative CML Data Output. CML output with 50Ω to V_{CC}.
5	OUT2+	Differential Positive CML Data Output. CML output with 50Ω to V_{CC}.
6	OUT2-	Differential Negative CML Data Output. CML output with 50Ω to V_{CC}.
8	OUT3+	Differential Positive CML Data Output. CML output with 50Ω to V_{CC}.
9	OUT3-	Differential Negative CML Data Output. CML output with 50Ω to V_{CC}.
11	OUT4+	Differential Positive CML Data Output. CML output with 50Ω to V_{CC}.
12	OUT4-	Differential Negative CML Data Output. CML output with 50Ω to V_{CC}.
14, 17, 19, 22, 25, 28, 31, 33, 38	GND	Ground
15	RINT	Internal Bias Resistor. When not used connect to GND.
16	REXT	External Bias Resistor. Connect to an external resistor, nominally a 5.23kΩ (1%) resistor.
20	IN4-	Differential Negative CML Data Input
21	IN4+	Differential Positive CML Data Input
23	IN3-	Differential Negative CML Data Input
24	IN3+	Differential Positive CML Data Input
26	IN2-	Differential Negative CML Data Input
27	IN2+	Differential Positive CML Data Input
29	IN1-	Differential Negative CML Data Input
30	IN1+	Differential Positive CML Data Input
34, 35, 36	N.C.	No Connection
—	EP	Exposed Pad. Signal and supply common. For optimum thermal conductivity and supply return (GND), this pad must be soldered to the circuit board ground.

Input and Output Structures

The input structure for each of the four channels to the MAX3986 is shown in Figure 4. The value of the DC differential input resistance is 100Ω.

The output structure for each of the four channels is shown in Figure 5. When REXT is connected to an external resistor, $R_{EXTERNAL}$ = 5.23kΩ (±1%), the output signal swing is the value specified in the *Electrical Characteristics* table. For convenience, however, REXT can be connected to RINT rather than to the external resistor $R_{EXTERNAL}$. Here the output signal swing is nominally the same as before, but the tolerance and temperature coefficient of RINT causes some of EC table specifications to widen. When not used, RINT should be connected to GND.

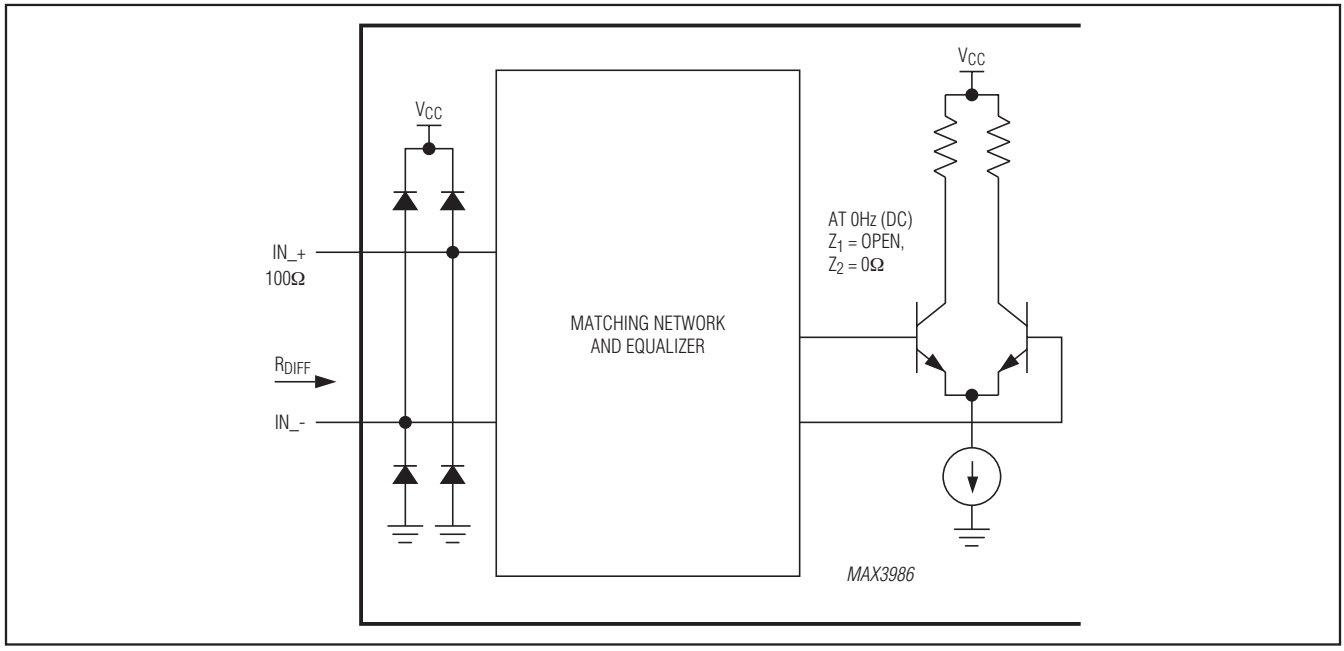


Figure 4. Equalizer Input Equivalent Circuit

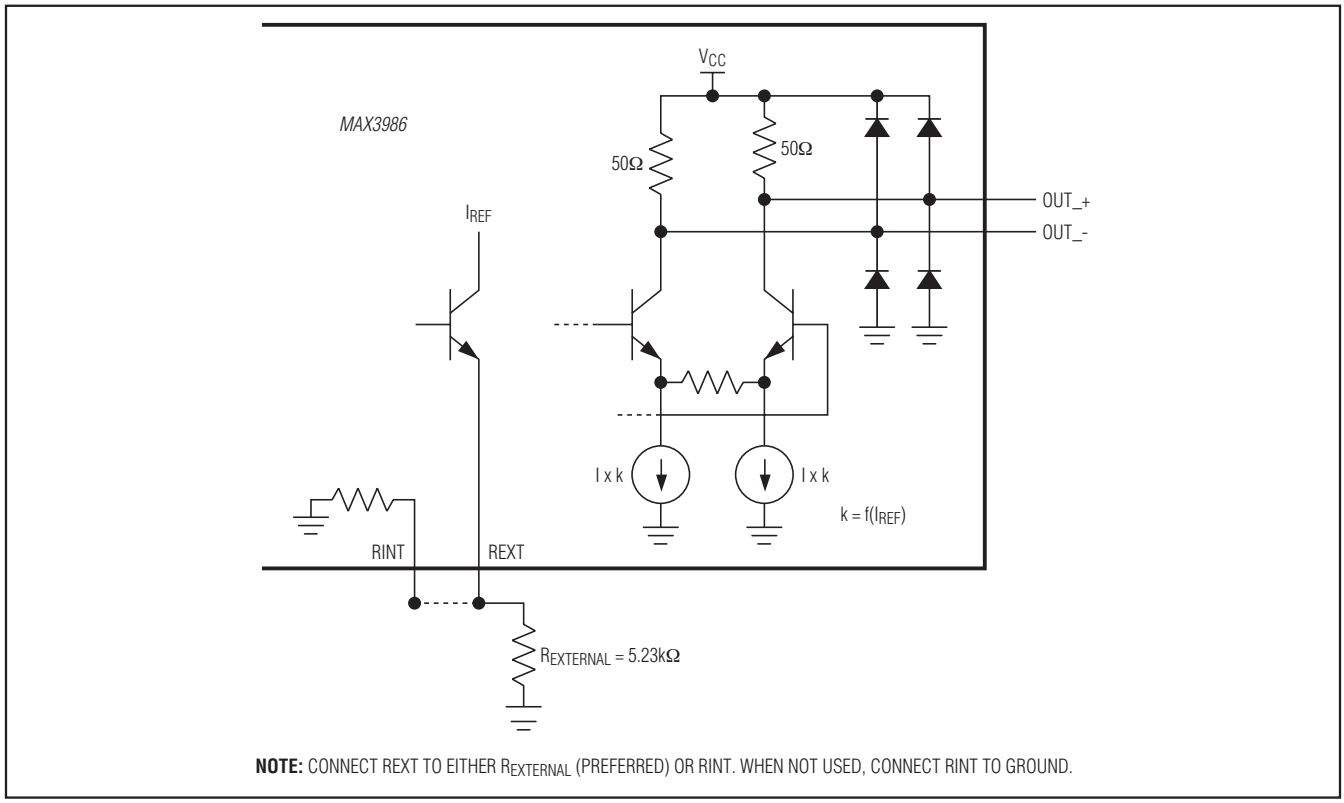


Figure 5. CML Output Equivalent Circuit

Output Amplitude Adjust

For the maximum input signal level of 1600mV$_{P-P}$, the output level can be adjusted by changing the values of $R_{EXTERNAL}$. This resistor controls the value of the tail current in the output driver. As the value of $R_{EXTERNAL}$ decreases, the value of the current increases, resulting in an increase in output signal swing. Results are shown in the Normalized Percentage Output Amplitude and Supply Current vs. External Resistance graph.

When $R_{EXTERNAL}$ is 5.23kΩ, the value of I_{CC} is approximately 130mA. The output signal swing is 100% of the nominal output swing of the EC table. When $R_{EXTERNAL}$ is lowered to 4.65kΩ, the output signal level and supply current increases by approximately 9%. Similarly, the values for current and output signal levels are lowered about 13% for $R_{EXTERNAL}$ = 5.73kΩ.

Channel Isolation

The coupling of adjacent input signals degrades overall performance. Care must be taken to eliminate conditions in which large amplitude signals (aggressors) are routed near low amplitude signals (victims). The MAX3986 provides adequate isolation for signals with similar amplitudes such as all four inputs coming from the same source and incurring the same transmission losses. The effect of crosstalk must be considered when applying input signals of different amplitudes to adjacent channels of the MAX3986. Applying a large amplitude signal and a small amplitude signal to adjacent channels is not recommended.

Using the MAX3986 in SAS Applications

The MAX3986 can be used in SAS applications where the maximum noise on the link during out-of-band (OOB) idle time does not exceed 10mV$_{P-P}$. With small amplitude input signals, each channel behaves as a linear amplifier. During idle time, a channel has zero differential output voltage and the outputs are at the common-mode output level. Because the channels do not include squelch circuitry, noise on the inputs during idle time is amplified and passed through the device. The link must be designed to ensure that the output of the MAX3986 does not produce an output swing that is greater than 50mV during idle time.

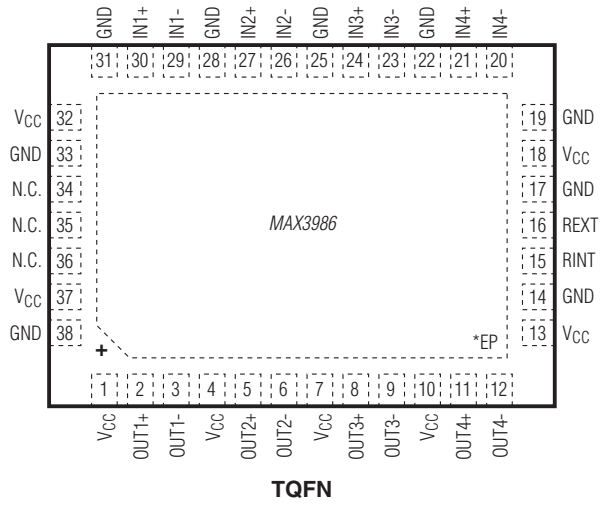
Layout Considerations

Circuit board layout and design can significantly affect the performance of the MAX3986. Use good high-frequency design techniques, including minimizing ground inductance and using controlled-impedance transmission lines on the data signals. Power-supply decoupling should also be placed as close as possible to the V_{CC} pins. Always connect all V_{CC} pins to a power plane. Take care to isolate the input from the output signals to reduce feedthrough.

Exposed-Pad Package

The exposed-pad, 38-pin TQFN package incorporates features that provide a very low thermal resistance path for heat removal from the IC. The exposed pad on the MAX3986 must be soldered to the circuit board for proper thermal performance. Refer to Application Note 862: *HFAN-08.1: Thermal Considerations of QFN and Other Exposed-Paddle Packages* for additional information.

Pin Configuration



TQFN

*THE EXPOSED PAD OF THE TQFN PACKAGE MUST BE SOLDERED TO GROUND FOR PROPER THERMAL OPERATION OF THE MAX3986.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
38 TQFN-EP	T3857+1	21-0172

maxim integrated™