Octal, 18-Bit, 200ksps Differential ±10.24V Input SoftSpan ADC with Wide Input Common Mode Range

FEATURES

- **200ksps per Channel Throughput**
- **Eight Simultaneous Sampling Channels**
- **±3LSB INL (Maximum, ±10.24V Range)**
- **Guaranteed 18-Bit, No Missing Codes**
- **Differential, Wide Common Mode Range Inputs**
- **Per-Channel SoftSpan Input Ranges:**
  ±10.24V, 0V to 10.24V, ±5.12V, 0V to 5.12V
  ±12.5V, 0V to 12.5V, ±6.25V, 0V to 6.25V
- **96.7dB Single-Conversion SNR (Typical)**
- **–109dB THD (Typical) at f_{IN} = 2kHz**
- **118dB CMRR (Typical) at f_{IN} = 200Hz**
- **Rail-to-Rail Input Overdrive Tolerance**
- Guaranteed Operation to 125°C
- Integrated Reference and Buffer (4.096V)
- SPI CMOS (1.8V to 5V) and LVDS Serial I/O
- Internal Conversion Clock, No Cycle Latency
- 140mW Power Dissipation (Typical)
- 48-Lead (7mm x 7mm) LQFP Package

APPLICATIONS

- Programmable Logic Controllers
- Industrial Process Control
- Power Line Monitoring
- Test and Measurement

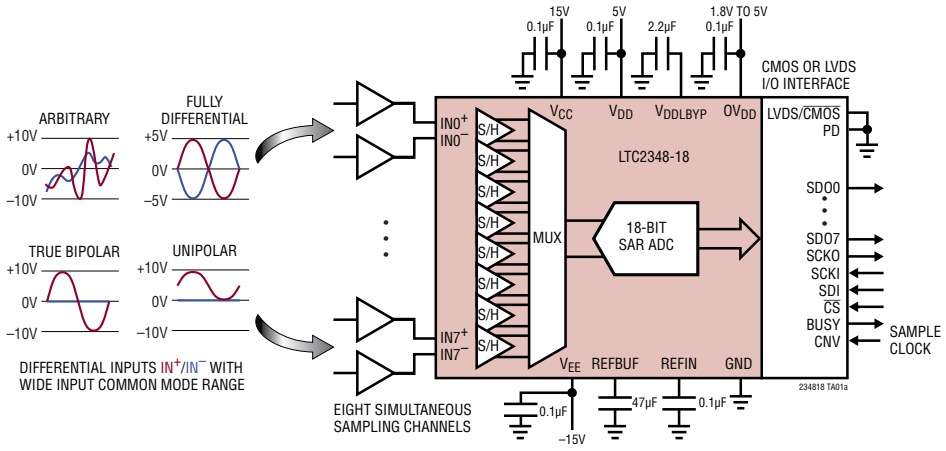
DESCRIPTION

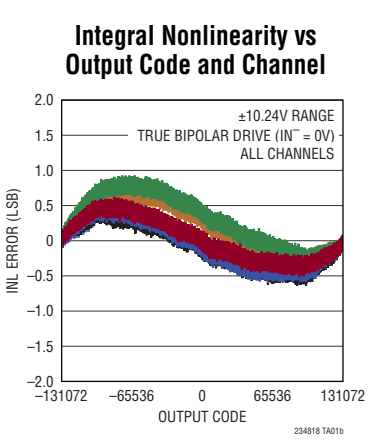
The LTC®2348-18 is an 18-bit, low noise 8-channel simultaneous sampling successive approximation register (SAR) ADC with differential, wide common mode range inputs. Operating from a 5V low voltage supply, flexible high voltage supplies, and using the internal reference and buffer, each channel of this SoftSpan™ ADC can be independently configured on a conversion-by-conversion basis to accept ±10.24V, 0V to 10.24V, ±5.12V, or 0V to 5.12V signals. Individual channels may also be disabled to increase throughput on the remaining channels.

The wide input common mode range and 118dB CMRR of the LTC2348-18 analog inputs allow the ADC to directly digitize a variety of signals, simplifying signal chain design. This input signal flexibility, combined with ±3LSB INL, no missing codes at 18 bits, and 96.7dB SNR, makes the LTC2348-18 an ideal choice for many high voltage applications requiring wide dynamic range.

The LTC2348-18 supports pin-selectable SPI CMOS (1.8V to 5V) and LVDS serial interfaces. Between one and eight lanes of data output may be employed in CMOS mode, allowing the user to optimize bus width and throughput.

TYPICAL APPLICATION



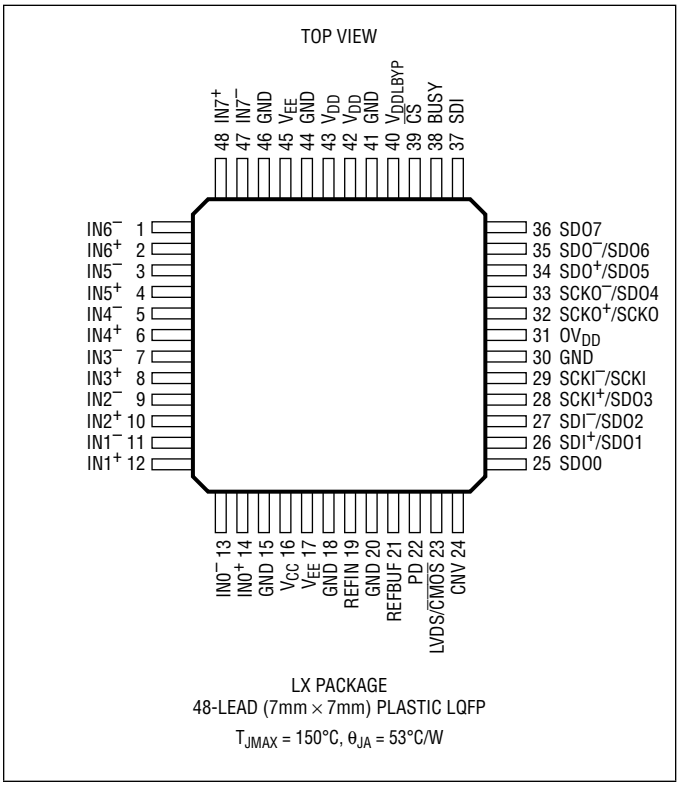


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) .....–0.3V to (V_{EE} + 40V)
Supply Voltage (V_{EE}).....–17.4V to 0.3V
Supply Voltage Difference (V_{CC} – V_{EE}).....40V
Supply Voltage (V_{DD}).....6V
Supply Voltage (OV_{DD}).....6V
Internal Regulated Supply Bypass (V_{DDLBYP}) ... (Note 3)
Analog Input Voltage
  $IN0^+$ to $IN7^+$,
  $IN0^-$ to $IN7^-$ (Note 4) ..... (V_{EE} – 0.3V) to (V_{CC} + 0.3V)
  REFIN..... –0.3V to 2.8V
  REFBUF, CNV (Note 5) ..... –0.3V to (V_{DD} + 0.3V)
Digital Input Voltage (Note 5).....–0.3V to (OV_{DD} + 0.3V)
Digital Output Voltage (Note 5) ..–0.3V to (OV_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range
  LTC2348C..... 0°C to 70°C
  LTC2348I .....–40°C to 85°C
  LTC2348H..... –40°C to 125°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



LX PACKAGE
48-LEAD (7mm × 7mm) PLASTIC LQFP
T_{JMAX} = 150°C, θ_{JA} = 53°C/W

ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2348CLX-18#PBF	LTC2348CLX-18#PBF	LTC2348LX-18	48-Lead (7mm × 7mm) Plastic LQFP	0°C to 70°C
LTC2348ILX-18#PBF	LTC2348ILX-18#PBF	LTC2348LX-18	48-Lead (7mm × 7mm) Plastic LQFP	–40°C to 85°C
LTC2348HLX-18#PBF	LTC2348HLX-18#PBF	LTC2348LX-18	48-Lead (7mm × 7mm) Plastic LQFP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
For more information on lead free part marking, go to: http://www.linear.com/leadfree/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN}+$	Absolute Input Range ($IN0^+$ to $IN7^+$)	(Note 7)	●	V_{EE}		V_{CC} – 4	V
$V_{IN}–$	Absolute Input Range ($IN0^–$ to $IN7^–$)	(Note 7)	●	V_{EE}		V_{CC} – 4	V
$V_{IN}+ – V_{IN}–$	Input Differential Voltage Range	SoftSpan 7: ±2.5 • V_{REFBUF} Range (Note 7)	●	–2.5 • V_{REFBUF}		2.5 • V_{REFBUF}	V
		SoftSpan 6: ±2.5 • V_{REFBUF}/1.024 Range (Note 7)	●	–2.5 • V_{REFBUF}/1.024		2.5 • V_{REFBUF}/1.024	V
		SoftSpan 5: 0V to 2.5 • V_{REFBUF} Range (Note 7)	●	0		2.5 • V_{REFBUF}	V
		SoftSpan 4: 0V to 2.5 • V_{REFBUF}/1.024 Range (Note 7)	●	0		2.5 • V_{REFBUF}/1.024	V
		SoftSpan 3: ±1.25 • V_{REFBUF} Range (Note 7)	●	–1.25 • V_{REFBUF}		1.25 • V_{REFBUF}	V
		SoftSpan 2: ±1.25 • V_{REFBUF}/1.024 Range (Note 7)	●	–1.25 • V_{REFBUF}/1.024		1.25 • V_{REFBUF}/1.024	V
		SoftSpan 1: 0V to 1.25 • V_{REFBUF} Range (Note 7)	●	0		1.25 • V_{REFBUF}	V
V_{CM}	Input Common Mode Voltage Range	(Note 7)	●	V_{EE}		V_{CC} – 4	V
$V_{IN}+ – V_{IN}–$	Input Differential Overdrive Tolerance	(Note 8)	●	–(V_{CC} – V_{EE})		(V_{CC} – V_{EE})	V
I_{IN}	Analog Input Leakage Current		●	–1		1	µA
C_{IN}	Analog Input Capacitance	Sample Mode			50		pF
		Hold Mode			10		pF
CMRR	Input Common Mode Rejection Ratio	$V_{IN}+ = V_{IN}– = 18V_{P-P}$ 200Hz Sine	●	100	118		dB
V_{IHCNV}	CNV High Level Input Voltage		●	1.3			V
V_{ILCNV}	CNV Low Level Input Voltage		●			0.5	V
I_{INCNV}	CNV Input Current	V_{IN} = 0V to V_{DD}	●	–10		10	µA

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution		●	18			Bits
	No Missing Codes		●	18			Bits
	Transition Noise	SoftSpans 7 and 6: ±10.24V and ±10V Ranges			1.3		LSB_{RMS}
		SoftSpans 5 and 4: 0V to 10.24V and 0V to 10V Ranges			2.6		LSB_{RMS}
		SoftSpans 3 and 2: ±5.12V and ±5V Ranges			2.0		LSB_{RMS}
		SoftSpan 1: 0V to 5.12V Range			4.0		LSB_{RMS}
INL	Integral Linearity Error	SoftSpans 7 and 6: ±10.24V and ±10V Ranges (Note 10)	●	–3	±1	3	LSB
		SoftSpans 5 and 4: 0V to 10.24V and 0V to 10V Ranges (Note 10)	●	–4	±1.5	4	LSB
		SoftSpans 3 and 2: ±5.12V and ±5V Ranges (Note 10)	●	–2.5	±0.75	2.5	LSB
		SoftSpan 1: 0V to 5.12V Range (Note 10)	●	–2.5	±0.75	2.5	LSB
DNL	Differential Linearity Error	(Note 11)	●	–0.9	±0.2	0.9	LSB
ZSE	Zero-Scale Error	(Note 12)	●	–550	±80	550	µV
	Zero-Scale Error Drift				±2		µV/°C
FSE	Full-Scale Error	(Note 12)	●	–0.1	±0.025	0.1	%FS
	Full-Scale Error Drift				±2.5		ppm/°C

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Notes 9, 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	SoftSpans 7 and 6: ±10.24V and ±10V Ranges, f_{IN} = 2kHz SoftSpans 5 and 4: 0V to 10.24V and 0V to 10V Ranges, f_{IN} = 2kHz SoftSpans 3 and 2: ±5.12V and ±5V Ranges, f_{IN} = 2kHz SoftSpan 1: 0V to 5.12V Range, f_{IN} = 2kHz	● ● ● ●	93.0 87.6 90.0 84.2	96.5 90.6 93.2 87.3		dB dB dB dB
SNR	Signal-to-Noise Ratio	SoftSpans 7 and 6: ±10.24V and ±10V Ranges, f_{IN} = 2kHz SoftSpans 5 and 4: 0V to 10.24V and 0V to 10V Ranges, f_{IN} = 2kHz SoftSpans 3 and 2: ±5.12V and ±5V Ranges, f_{IN} = 2kHz SoftSpan 1: 0V to 5.12V Range, f_{IN} = 2kHz	● ● ● ●	93.7 87.7 90.2 84.3	96.7 90.7 93.2 87.3		dB dB dB dB
THD	Total Harmonic Distortion	SoftSpans 7 and 6: ±10.24V and ±10V Ranges, f_{IN} = 2kHz SoftSpans 5 and 4: 0V to 10.24V and 0V to 10V Ranges, f_{IN} = 2kHz SoftSpans 3 and 2: ±5.12V and ±5V Ranges, f_{IN} = 2kHz SoftSpan 1: 0V to 5.12V Range, f_{IN} = 2kHz	● ● ● ●		–109 –111 –113 –114	–101 –104 –104 –103	dB dB dB dB
SFDR	Spurious Free Dynamic Range	SoftSpans 7 and 6: ±10.24V and ±10V Ranges, f_{IN} = 2kHz SoftSpans 5 and 4: 0V to 10.24V and 0V to 10V Ranges, f_{IN} = 2kHz SoftSpans 3 and 2: ±5.12V and ±5V Ranges, f_{IN} = 2kHz SoftSpan 1: 0V to 5.12V Range, f_{IN} = 2kHz	● ● ● ●	101 105 105 105	110 112 114 115		dB dB dB dB
	Channel-to-Channel Crosstalk	One Channel Converting 18V_{P-P} 200Hz Sine in ±10.24V Range, Crosstalk to All Other Channels			–109		dB
	–3dB Input Bandwidth				7		MHz
	Aperture Delay				1		ns
	Aperture Delay Matching				150		ps
	Aperture Jitter				3		ps_{RMS}
	Transient Response	Full-Scale Step, 0.005% Settling			360		ns

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REFIN}	Internal Reference Output Voltage			2.043	2.048	2.053	V
	Internal Reference Temperature Coefficient	(Note 14)	●		5	20	ppm/°C
	Internal Reference Line Regulation	V_{DD} = 4.75V to 5.25V			0.1		mV/V
	Internal Reference Output Impedance				20		kΩ
V_{REFIN}	REFIN Voltage Range	REFIN Overdriven (Note 7)		1.25		2.2	V

REFERENCE BUFFER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REFBUF}	Reference Buffer Output Voltage	REFIN Overdriven, V_{REFIN} = 2.048V	●	4.091	4.096	4.101	V
	REFBUF Voltage Range	REFBUF Overdriven (Notes 7, 15)	●	2.5		5	V
	REFBUF Input Impedance	V_{REFIN} = 0V, Buffer Disabled			13		kΩ
I_{REFBUF}	REFBUF Load Current	V_{REFBUF} = 5V, 8 Channels Enabled (Notes 15, 16) V_{REFBUF} = 5V, Acquisition or Nap Mode (Note 15)	●		1.5 0.39	1.9	mA mA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMOS Digital Inputs and Outputs							
V_{IH}	High Level Input Voltage		●	0.8 • OV_{DD}			V
V_{IL}	Low Level Input Voltage		●			0.2 • OV_{DD}	V
I_{IN}	Digital Input Current	V_{IN} = 0V to OV_{DD}	●	–10		10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	I_{OUT} = –500µA	●	OV_{DD} – 0.2			V
V_{OL}	Low Level Output Voltage	I_{OUT} = 500µA	●			0.2	V
I_{OZ}	Hi-Z Output Leakage Current	V_{OUT} = 0V to OV_{DD}	●	–10		10	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–50		mA
I_{SINK}	Output Sink Current	V_{OUT} = OV_{DD}			50		mA
LVDS Digital Inputs and Outputs							
V_{ID}	Differential Input Voltage		●	200	350	600	mV
R_{ID}	On-Chip Input Termination Resistance	$\overline{CS}$ = 0V, V_{ICM} = 1.2V $\overline{CS}$ = OV_{DD}	●	90	106 10	125	Ω MΩ
V_{ICM}	Common-Mode Input Voltage		●	0.3	1.2	2.2	V
I_{ICM}	Common-Mode Input Current	V_{IN}+ = V_{IN}– = 0V to OV_{DD}	●	–10		10	µA
V_{OD}	Differential Output Voltage	R_L = 100Ω Differential Termination	●	275	350	425	mV
V_{OCM}	Common-Mode Output Voltage	R_L = 100Ω Differential Termination	●	1.1	1.2	1.3	V
I_{OZ}	Hi-Z Output Leakage Current	V_{OUT} = 0V to OV_{DD}	●	–10		10	µA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	0		38	V
V_{EE}	Supply Voltage		●	–16.5		0	V
V_{CC} – V_{EE}	Supply Voltage Difference		●	10		38	V
V_{DD}	Supply Voltage		●	4.75	5.00	5.25	V
I_{VCC}	Supply Current	200ksps Sample Rate, 8 Channels Enabled Acquisition Mode Nap Mode Power Down Mode	● ● ● ●		1.8 3.8 0.7 1	2.2 4.5 0.9 15	mA mA mA µA
I_{VEE}	Supply Current	200ksps Sample Rate, 8 Channels Enabled Acquisition Mode Nap Mode Power Down Mode	● ● ● ●	–2.8 –4.9 –1.1 –15	–2.2 –4.0 –0.8 –1		mA mA mA µA
CMOS I/O Mode							
OV_{DD}	Supply Voltage		●	1.71		5.25	V
I_{VDD}	Supply Current	200ksps Sample Rate, 8 Channels Enabled 200ksps Sample Rate, 8 Channels Enabled, V_{REFBUF} = 5V (Note 15) Acquisition Mode Nap Mode Power Down Mode (C-Grade and I-Grade) Power Down Mode (H-Grade)	● ● ● ● ● ●		15.2 13.4 1.6 1.4 65 65	17.5 15.4 2.1 1.9 175 450	mA mA mA mA µA µA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{OVDD}	Supply Current	200ksps Sample Rate, 8 Channels Enabled (C_L = 25pF)	●		1.6	2.6	mA
		Acquisition or Nap Mode	●		1	20	µA
		Power Down Mode	●		1	20	µA
P_D	Power Dissipation	200ksps Sample Rate, 8 Channels Enabled	●		140	169	mW
		Acquisition Mode	●		125	152	mW
		Nap Mode	●		30	40	mW
		Power Down Mode (C-Grade and I-Grade)	●		0.36	1.4	mW
		Power Down Mode (H-Grade)	●		0.36	2.8	mW
LVDS I/O Mode							
OV_{DD}	Supply Voltage		●	2.375		5.25	V
I_{VDD}	Supply Current	200ksps Sample Rate, 8 Channels Enabled	●		17.7	20.4	mA
		200ksps Sample Rate, 8 Channels Enabled, V_{REFBUF} = 5V (Note 15)	●		16.1	18.5	mA
		Acquisition Mode	●		3.2	3.8	mA
		Nap Mode	●		3.0	3.7	mA
		Power Down Mode (C-Grade and I-Grade)	●		65	175	µA
		Power Down Mode (H-Grade)	●		65	450	µA
I_{OVDD}	Supply Current	200ksps Sample Rate, 8 Channels Enabled (R_L = 100Ω)	●		7	8.5	mA
		Acquisition or Nap Mode (R_L = 100Ω)	●		7	8.0	mA
		Power Down Mode	●		1	20	µA
P_D	Power Dissipation	200ksps Sample Rate, 8 Channels Enabled	●		166	199	mW
		Acquisition Mode	●		151	180	mW
		Nap Mode	●		55	69	mW
		Power Down Mode (C-Grade and I-Grade)	●		0.36	1.4	mW
		Power Down Mode (H-Grade)	●		0.36	2.8	mW

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SMPL}	Maximum Sampling Frequency	8 Channels Enabled	●			200	ksps
		7 Channels Enabled	●			225	ksps
		6 Channels Enabled	●			266	ksps
		5 Channels Enabled	●			300	ksps
		4 Channels Enabled	●			375	ksps
		3 Channels Enabled	●			450	ksps
		2 Channels Enabled	●			625	ksps
		1 Channel Enabled	●			1000	ksps
t_{CYC}	Time Between Conversions	8 Channels Enabled, f_{SMPL} = 200ksps	●	5000			ns
		7 Channels Enabled, f_{SMPL} = 225ksps	●	4444			ns
		6 Channels Enabled, f_{SMPL} = 266ksps	●	3750			ns
		5 Channels Enabled, f_{SMPL} = 300ksps	●	3333			ns
		4 Channels Enabled, f_{SMPL} = 375ksps	●	2666			ns
		3 Channels Enabled, f_{SMPL} = 450ksps	●	2222			ns
		2 Channels Enabled, f_{SMPL} = 625ksps	●	1600			ns
		1 Channel Enabled, f_{SMPL} = 1000ksps	●	1000			ns
t_{CONV}	Conversion Time	N Channels Enabled, 1 ≤ N ≤ 8	●	450•N	500•N	550•N	ns
t_{ACQ}	Acquisition Time ($t_{ACQ} = t_{CYC} - t_{CONV} - t_{BUSYLH}$)	8 Channels Enabled, f_{SMPL} = 200ksps	●	570	980		ns
		7 Channels Enabled, f_{SMPL} = 225ksps	●	564	924		ns
		6 Channels Enabled, f_{SMPL} = 266ksps	●	420	730		ns
		5 Channels Enabled, f_{SMPL} = 300ksps	●	553	813		ns
		4 Channels Enabled, f_{SMPL} = 375ksps	●	436	646		ns
		3 Channels Enabled, f_{SMPL} = 450ksps	●	542	702		ns
		2 Channels Enabled, f_{SMPL} = 625ksps	●	470	580		ns
		1 Channel Enabled, f_{SMPL} = 1000ksps	●	420	480		ns

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{CNVH}	CNV High Time		●	40			ns
t_{CNVL}	CNV Low Time		●	420			ns
t_{BUSYLH}	CNV↑ to BUSY Delay	C_L = 25pF	●			30	ns
t_{QUIET}	Digital I/O Quiet Time from CNV↑		●	20			ns
t_{PDH}	PD High Time		●	40			ns
t_{PDL}	PD Low Time		●	40			ns
t_{WAKE}	REFBUF Wake-Up Time	C_{REFBUF} = 47µF, C_{REFIN} = 0.1µF			200		ms
CMOS I/O Mode							
t_{SCKI}	SCKI Period	(Notes 17, 18)	●	10			ns
t_{SCKIH}	SCKI High Time		●	4			ns
t_{SCKIL}	SCKI Low Time		●	4			ns
$t_{SSDISCKI}$	SDI Setup Time from SCKI↑	(Note 17)	●	2			ns
$t_{HSDISCKI}$	SDI Hold Time from SCKI↑	(Note 17)	●	1			ns
$t_{DSDOSCKI}$	SDO Data Valid Delay from SCKI↑	C_L = 25pF (Note 17)	●			7.5	ns
$t_{HSDOSCKI}$	SDO Remains Valid Delay from SCKI↑	C_L = 25pF (Note 17)	●	1.5			ns
t_{SKEW}	SDO to SCKO Skew	(Note 17)	●	–1	0	1	ns
$t_{DSDOBUSYL}$	SDO Data Valid Delay from BUSY↓	C_L = 25pF (Note 17)	●	0			ns
t_{EN}	Bus Enable Time After $\overline{CS}$↓	(Note 17)	●			15	ns
t_{DIS}	Bus Relinquish Time After $\overline{CS}$↑	(Note 17)	●			15	ns
LVDS I/O Mode							
t_{SCKI}	SCKI Period	(Note 19)	●	4			ns
t_{SCKIH}	SCKI High Time	(Note 19)	●	1.5			ns
t_{SCKIL}	SCKI Low Time	(Note 19)	●	1.5			ns
$t_{SSDISCKI}$	SDI Setup Time from SCKI	(Notes 11, 19)	●	1.2			ns
$t_{HSDISCKI}$	SDI Hold Time from SCKI	(Notes 11, 19)	●	–0.2			ns
$t_{DSDOSCKI}$	SDO Data Valid Delay from SCKI	(Notes 11, 19)	●			6	ns
$t_{HSDOSCKI}$	SDO Remains Valid Delay from SCKI	(Notes 11, 19)	●	1			ns
t_{SKEW}	SDO to SCKO Skew	(Note 11)	●	–0.4	0	0.4	ns
$t_{DSDOBUSYL}$	SDO Data Valid Delay from BUSY↓	(Note 11)	●	0			ns
t_{EN}	Bus Enable Time After $\overline{CS}$↓		●			50	ns
t_{DIS}	Bus Relinquish Time After $\overline{CS}$↑		●			15	ns

ADC TIMING CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground.

Note 3: V_{DDLBYP} is the output of an internal voltage regulator, and should only be connected to a 2.2µF ceramic capacitor to bypass the pin to GND, as described in the Pin Functions section. Do not connect this pin to any external circuitry.

Note 4: When these pin voltages are taken below V_{EE} or above V_{CC}, they will be clamped by internal diodes. This product can handle input currents of up to 100mA below V_{EE} or above V_{CC} without latch-up.

Note 5: When these pin voltages are taken below ground or above V_{DD} or OV_{DD}, they will be clamped by internal diodes. This product can handle currents of up to 100mA below ground or above V_{DD} or OV_{DD} without latch-up.

Note 6: $-16.5V \le V_{EE} \le 0V$, $0V \le V_{CC} \le 38V$, $10V \le (V_{CC} - V_{EE}) \le 38V$, $V_{DD} = 5V$, unless otherwise specified.

Note 7: Recommended operating conditions.

Note 8: Exceeding these limits on any channel may corrupt conversion results on other channels. Refer to Absolute Maximum Ratings section for pin voltage limits related to device reliability.

Note 9: $V_{CC} = 15V$, $V_{EE} = -15V$, $V_{DD} = 5V$, $OV_{DD} = 2.5V$, $f_{SMPL} = 200ksps$, internal reference and buffer, true bipolar input signal drive in bipolar SoftSpan ranges, unipolar signal drive in unipolar SoftSpan ranges, unless otherwise specified.

Note 10: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 11: Guaranteed by design, not subject to test.

Note 12: For bipolar SoftSpan ranges 7, 6, 3, and 2, zero-scale error is the offset voltage measured from –0.5LSB when the output code flickers between 00 0000 0000 0000 0000 and 11 1111 1111 1111 1111. Full-scale error for these SoftSpan ranges is the worst-case deviation of the first and last code transitions from ideal and includes the effect of offset error. For unipolar SoftSpan ranges 5, 4, and 1, zero-scale error is the offset voltage measured from 0.5LSB when the output code flickers between 00 0000 0000 0000 0000 and 00 0000 0000 0000 0001. Full-scale error for these SoftSpan ranges is the worst-case deviation of the last code transition from ideal and includes the effect of offset error.

Note 13: All specifications in dB are referred to a full-scale input in the relevant SoftSpan input range, except for crosstalk, which is referred to the crosstalk injection signal amplitude.

Note 14: Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

Note 15: When REFBUF is overdriven, the internal reference buffer must be disabled by setting REFIN = 0V.

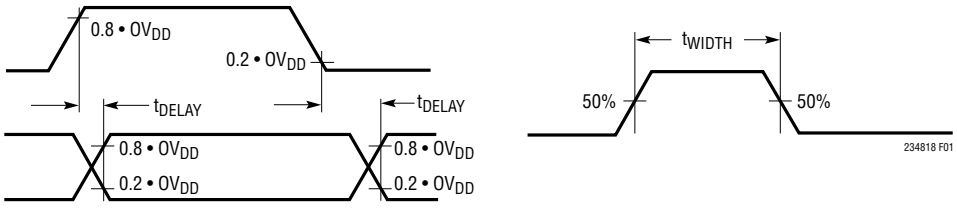
Note 16: I_{REFBUF} varies proportionally with sample rate and the number of active channels.

Note 17: Parameter tested and guaranteed at $OV_{DD} = 1.71V$, $OV_{DD} = 2.5V$, and $OV_{DD} = 5.25V$.

Note 18: A t_{SCKI} period of 10ns minimum allows a shift clock frequency of up to 100MHz for rising edge capture.

Note 19: $V_{ICM} = 1.2V$, $V_{ID} = 350mV$ for LVDS differential input pairs.

CMOS Timings



LVDS Timings (Differential)

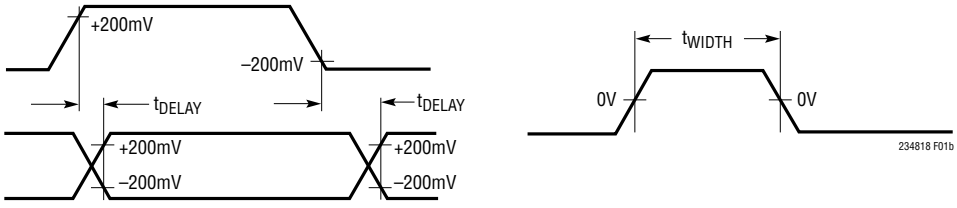
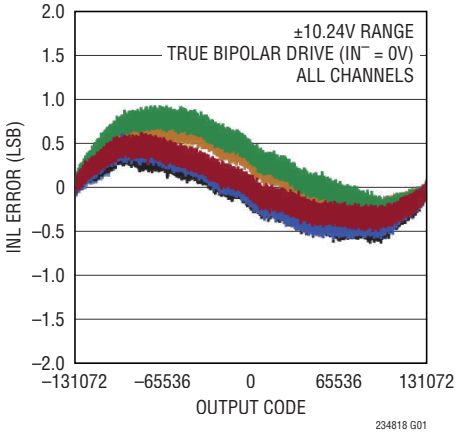


Figure 1. Voltage Levels for Timing Specifications

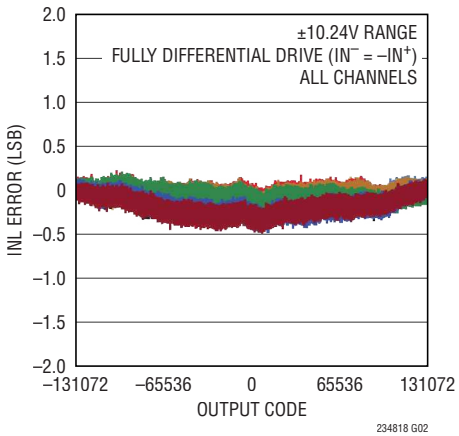
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = +15V, V_{EE} = –15V, V_{DD} = 5V, OV_{DD} = 2.5V, Internal Reference and Buffer (V_{REFBUF} = 4.096V), f_{SMPL} = 200ksps, unless otherwise noted.

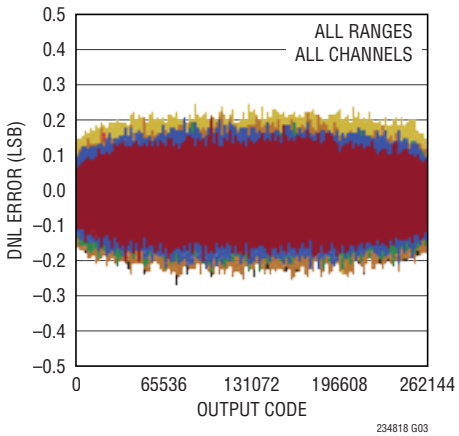
Integral Nonlinearity vs Output Code and Channel



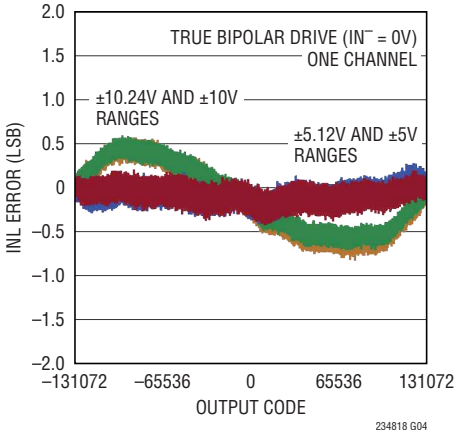
Integral Nonlinearity vs Output Code and Channel



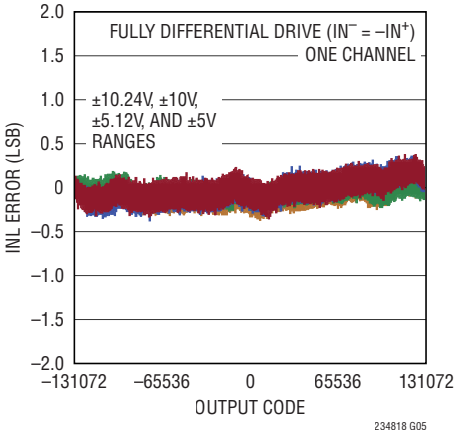
Differential Nonlinearity vs Output Code and Channel



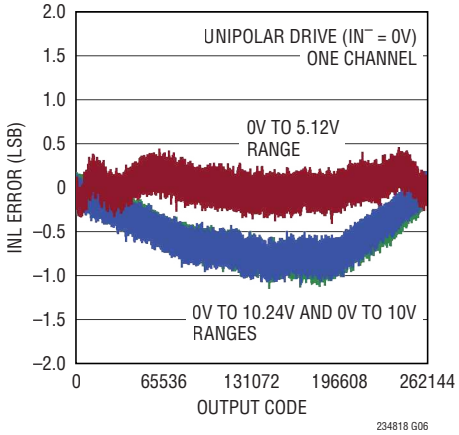
Integral Nonlinearity vs Output Code and Range



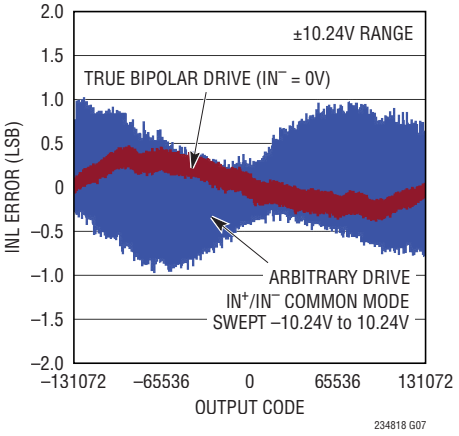
Integral Nonlinearity vs Output Code and Range



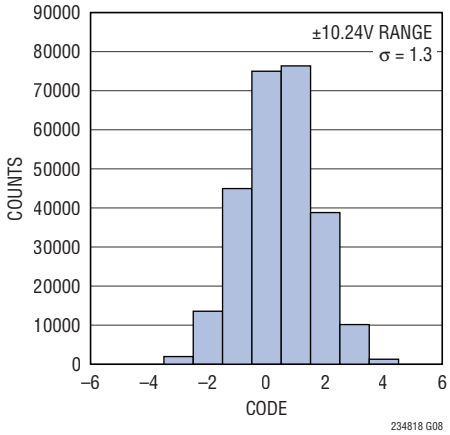
Integral Nonlinearity vs Output Code and Range



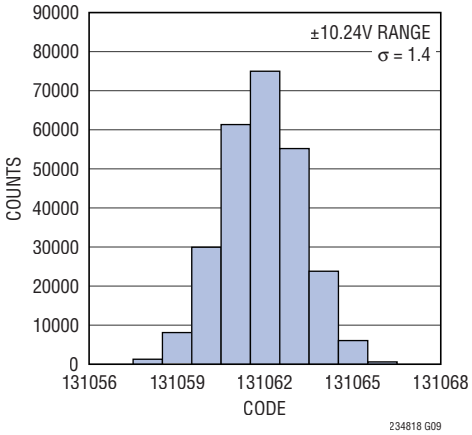
Integral Nonlinearity vs Output Code



DC Histogram (Zero-Scale)



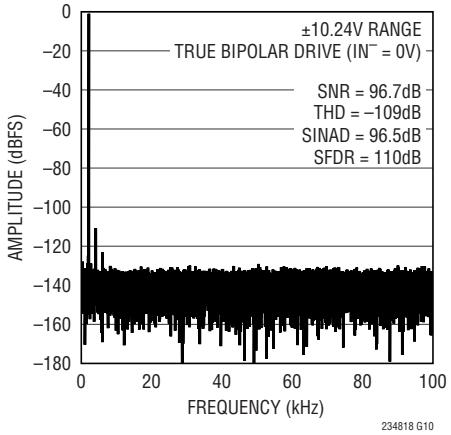
DC Histogram (Near Full-Scale)



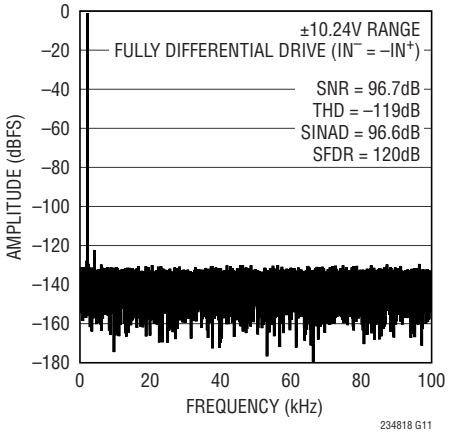
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = +15V, V_{EE} = –15V, V_{DD} = 5V, OV_{DD} = 2.5V, Internal Reference and Buffer (V_{REFBUF} = 4.096V), f_{SMPL} = 200ksps, unless otherwise noted.

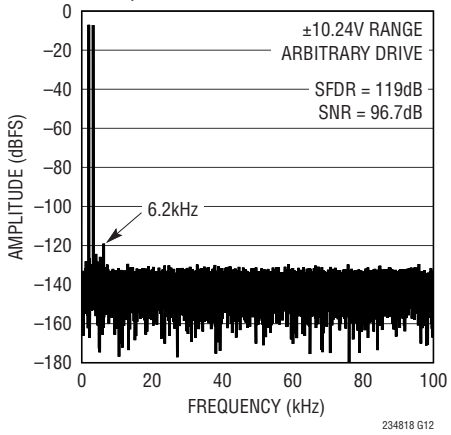
32k Point FFT f_{SMPL} = 200kHz, f_{IN} = 2kHz



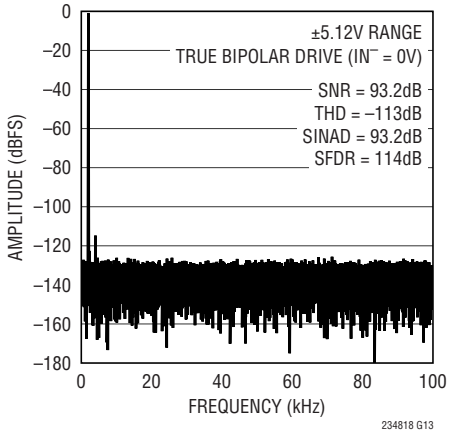
32k Point FFT f_{SMPL} = 200kHz, f_{IN} = 2kHz



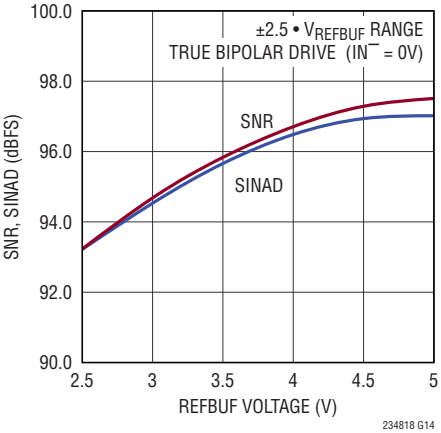
32k Point Arbitrary Two-Tone FFT f_{SMPL} = 200kHz, IN^+ = –7dBFS 2kHz Sine, IN^- = –7dBFS 3.1kHz Sine



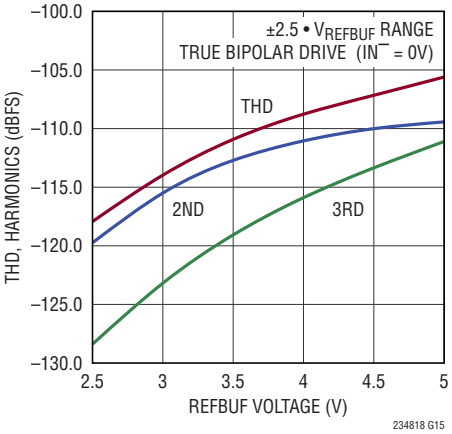
32k Point FFT f_{SMPL} = 200kHz, f_{IN} = 2kHz



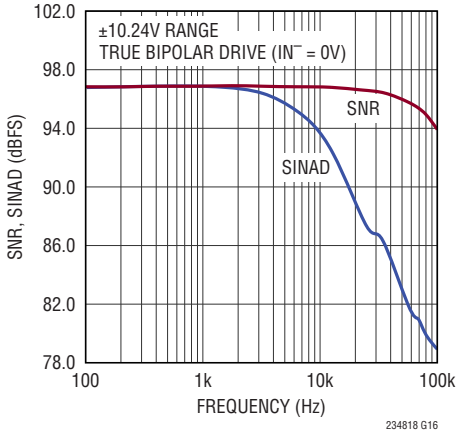
SNR, SINAD vs V_{REFBUF}, f_{IN} = 2kHz



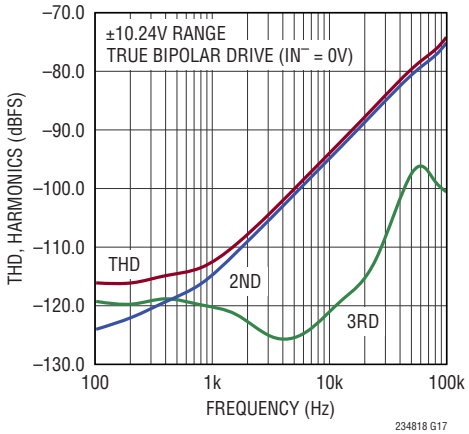
THD, Harmonics vs V_{REFBUF}, f_{IN} = 2kHz



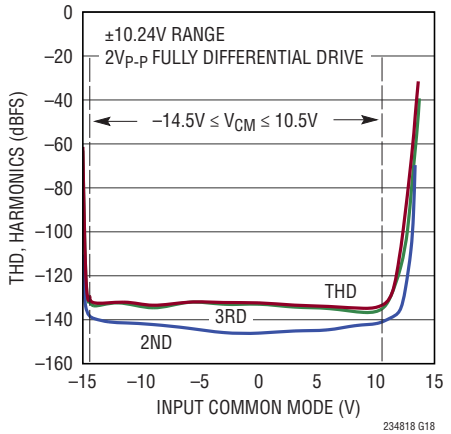
SNR, SINAD vs Input Frequency



THD, Harmonics vs Input Frequency



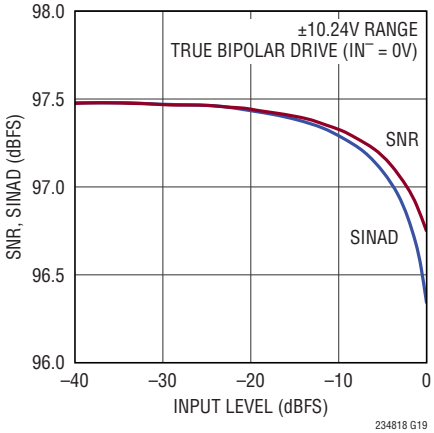
THD, Harmonics vs Input Common Mode, f_{IN} = 2kHz



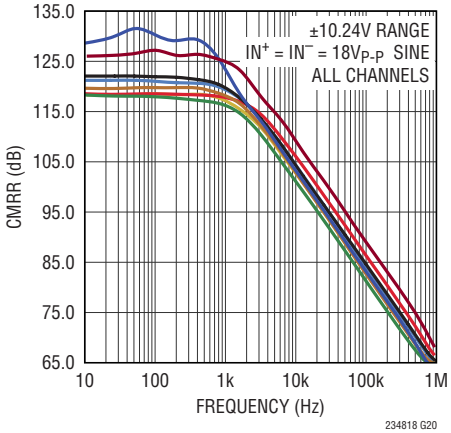
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = +15V, V_{EE} = –15V, V_{DD} = 5V, OV_{DD} = 2.5V, Internal Reference and Buffer (V_{REFBUF} = 4.096V), f_{SMPL} = 200ksps, unless otherwise noted.

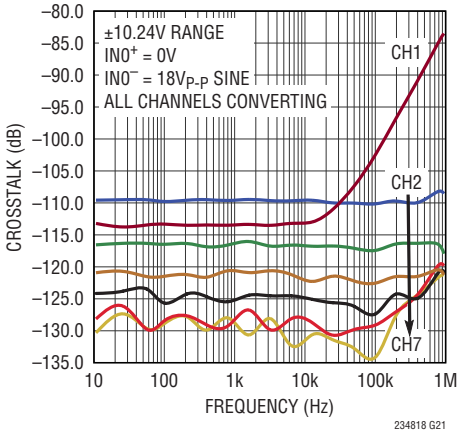
SNR, SINAD vs Input Level, f_{IN} = 2kHz



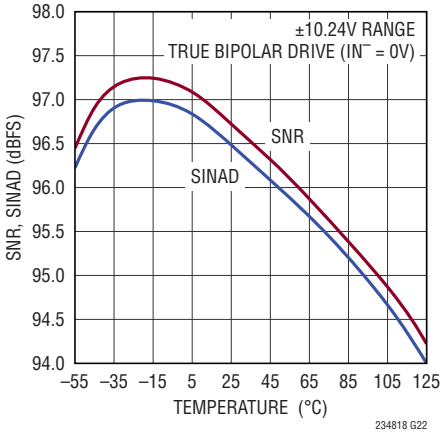
CMRR vs Input Frequency and Channel



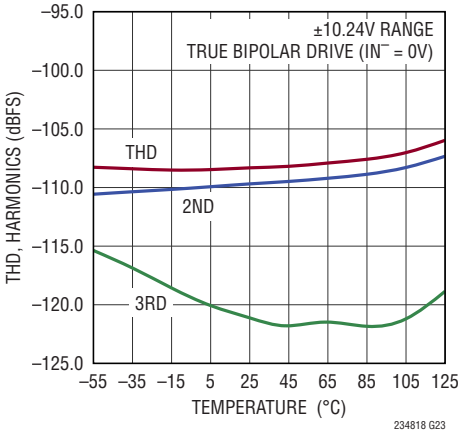
Crosstalk vs Input Frequency and Channel



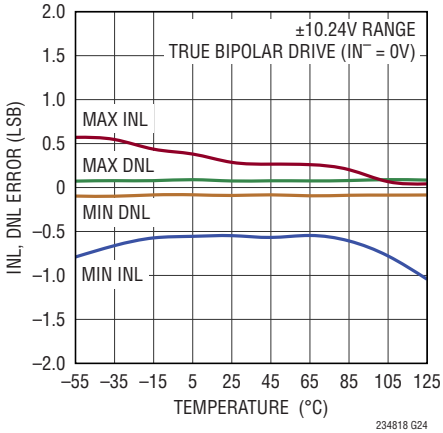
SNR, SINAD vs Temperature, f_{IN} = 2kHz



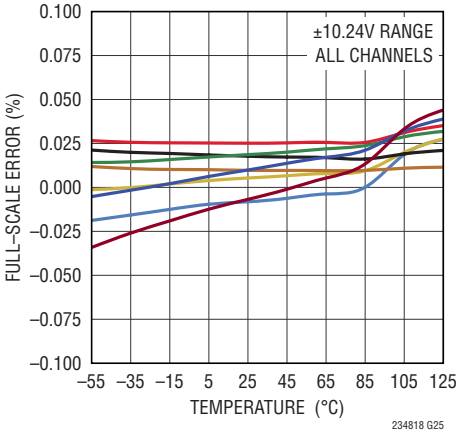
THD, Harmonics vs Temperature, f_{IN} = 2kHz



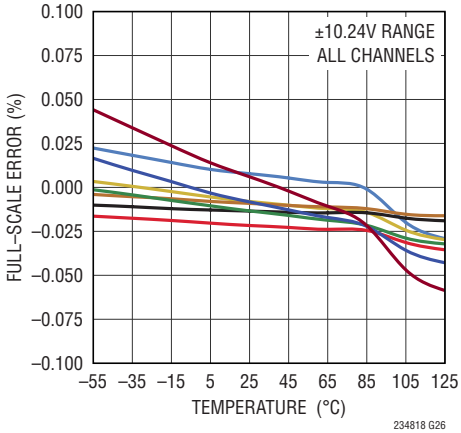
INL, DNL vs Temperature



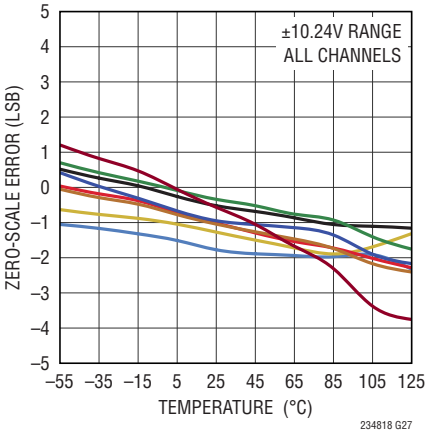
Positive Full-Scale Error vs Temperature and Channel



Negative Full-Scale Error vs Temperature and Channel



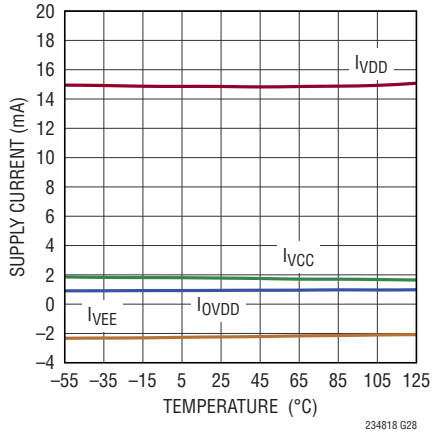
Zero-Scale Error vs Temperature and Channel



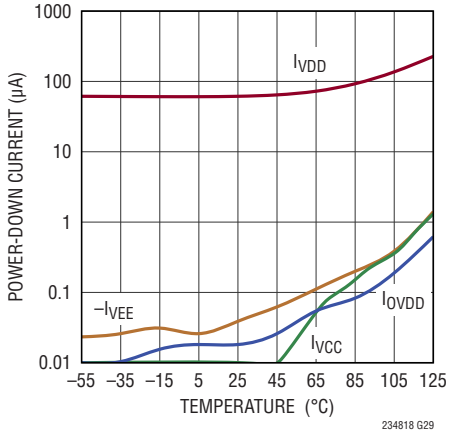
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{CC} = +15V, V_{EE} = –15V, V_{DD} = 5V, OV_{DD} = 2.5V, Internal Reference and Buffer (V_{REFBUF} = 4.096V), f_{SMPL} = 200ksps, unless otherwise noted.

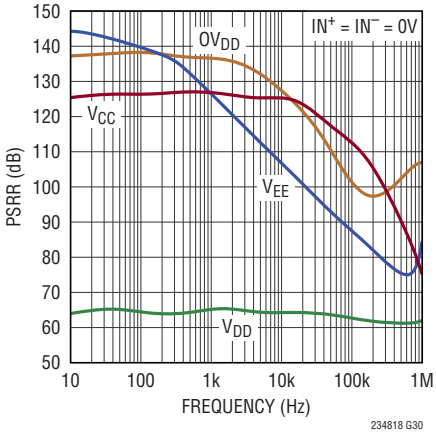
Supply Current vs Temperature



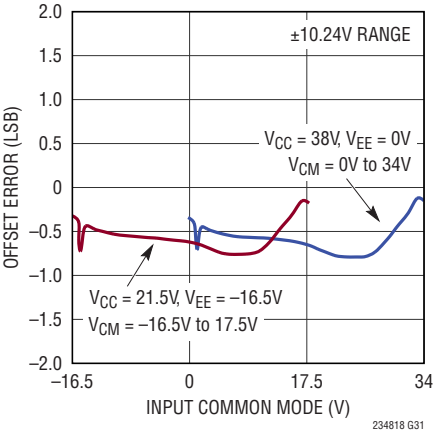
Power-Down Current vs Temperature



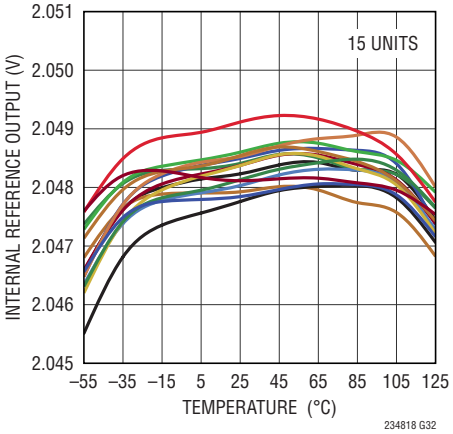
PSRR vs Frequency



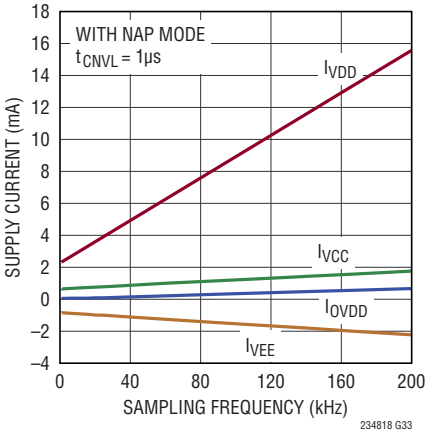
Offset Error vs Input Common Mode



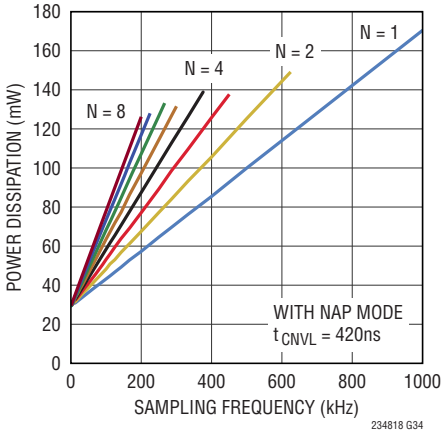
Internal Reference Output vs Temperature



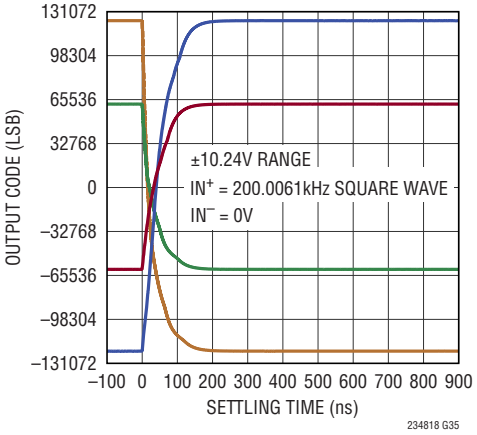
Supply Current vs Sampling Rate



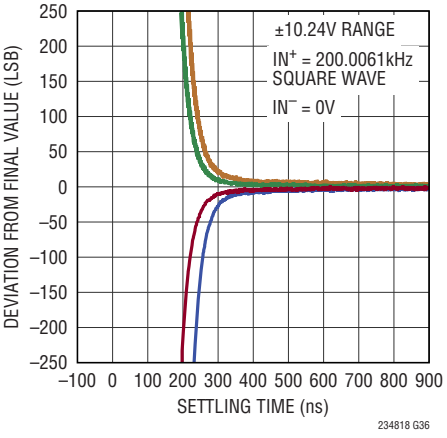
Power Dissipation vs Sampling Rate, N-Channels Enabled



Step Response (Large-Signal Settling)



Step Response (Fine Settling)



PIN FUNCTIONS

Pins that are the Same for All Digital I/O Modes

IN0+ to IN7+, IN0– to IN7– (Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 47, and 48): Positive and Negative Analog Inputs, Channels 0 to 7. The converter simultaneously samples and digitizes ($V_{IN+} – V_{IN–}$) for all channels. Wide input common mode range ($V_{EE} \leq V_{CM} \leq V_{CC} – 4V$) and high common mode rejection allow the inputs to accept a wide variety of signal swings. Full-scale input range is determined by the channel's SoftSpan configuration.

GND (Pins 15, 18, 20, 30, 41, 44, 46): Ground. Solder all GND pins to a solid ground plane.

V_{CC} (Pin 16): Positive High Voltage Power Supply. The range of V_{CC} is 0V to 38V with respect to GND and 10V to 38V with respect to V_{EE}. Bypass V_{CC} to GND close to the pin with a 0.1µF ceramic capacitor. In applications where V_{CC} is shorted to GND this capacitor may be omitted.

V_{EE} (Pins 17, 45): Negative High Voltage Power Supply. The range of V_{EE} is 0V to –16.5V with respect to GND and –10V to –38V with respect to V_{CC}. Connect Pins 17 and 45 together and bypass the V_{EE} network to GND close to Pin 17 with a 0.1µF ceramic capacitor. In applications where V_{EE} is shorted to GND this capacitor may be omitted.

REFIN (Pin 19): Bandgap Reference Output/Reference Buffer Input. An internal bandgap reference nominally outputs 2.048V on this pin. An internal reference buffer amplifies V_{REFIN} to create the converter master reference voltage $V_{REFBUF} = 2 \bullet V_{REFIN}$ on the REFBUF pin. When using the internal reference, bypass REFIN to GND (Pin 20) close to the pin with a 0.1µF ceramic capacitor to filter the bandgap output noise. If more accuracy is desired, overdrive REFIN with an external reference in the range of 1.25V to 2.2V.

REFBUF (Pin 21): Internal Reference Buffer Output. An internal reference buffer amplifies V_{REFIN} to create the converter master reference voltage $V_{REFBUF} = 2 \bullet V_{REFIN}$ on this pin, nominally 4.096V when using the internal bandgap reference. Bypass REFBUF to GND (Pin 20) close to the pin with a 47µF ceramic capacitor. The internal reference buffer may be disabled by grounding its input at REFIN. With the buffer disabled, overdrive REFBUF with an external reference voltage in the range of 2.5V to 5V. When using the internal reference buffer, limit the loading of any external circuitry connected to REFBUF to less than 10µA. Using a high input impedance amplifier to buffer V_{REFBUF} to any external circuits is recommended.

PD (Pin 22): Power Down Input. When this pin is brought high, the LTC2348-18 is powered down and subsequent conversion requests are ignored. If this occurs during a conversion, the device powers down once the conversion completes. If this pin is brought high twice without an intervening conversion, an internal global reset is initiated, equivalent to a power-on-reset event. Logic levels are determined by OV_{DD}.

LVDS/$\overline{\text{CMOS}}$ (Pin 23): I/O Mode Select. Tie this pin to OV_{DD} to select LVDS I/O mode, or to ground to select CMOS I/O mode. Logic levels are determined by OV_{DD}.

CNV (Pin 24): Conversion Start Input. A rising edge on this pin puts the internal sample-and-holds into the hold mode and initiates a new conversion. CNV is not gated by $\overline{CS}$, allowing conversions to be initiated independent of the state of the serial I/O bus.

BUSY (Pin 38): Busy Output. The BUSY signal indicates that a conversion is in progress. This pin transitions low-to-high at the start of each conversion and stays high until the conversion is complete. Logic levels are determined by OV_{DD}.

V_{DDLBYP} (Pin 40): Internal 2.5V Regulator Bypass Pin. The voltage on this pin is generated via an internal regulator operating off of V_{DD}. This pin must be bypassed to GND close to the pin with a 2.2µF ceramic capacitor. Do not connect this pin to any external circuitry.

V_{DD} (Pins 42, 43): 5V Power Supply. The range of V_{DD} is 4.75V to 5.25V. Connect Pins 42 and 43 together and bypass the V_{DD} network to GND with a shared 0.1µF ceramic capacitor close to the pins.

PIN FUNCTIONS

CMOS I/O Mode

SDO0 to SDO7 (Pins 25, 26, 27, 28, 33, 34, 35, and 36): CMOS Serial Data Outputs, Channels 0 to 7. The most recent conversion result along with channel configuration information is clocked out onto the SDO pins on each rising edge of SCKI. Output data formatting is described in the Digital Interface section. Leave unused SDO outputs unconnected. Logic levels are determined by OV_{DD}.

SCKI (Pin 29): CMOS Serial Clock Input. Drive SCKI with the serial I/O clock. SCKI rising edges latch serial data in on SDI and clock serial data out on SDO0 to SDO7. For standard SPI bus operation, capture output data at the receiver on rising edges of SCKI. SCKI is allowed to idle either high or low. Logic levels are determined by OV_{DD}.

OV_{DD} (Pin 31): I/O Interface Power Supply. In CMOS I/O mode, the range of OV_{DD} is 1.71V to 5.25V. Bypass OV_{DD} to GND (Pin 30) close to the pin with a 0.1µF ceramic capacitor.

SCKO (Pin 32): CMOS Serial Clock Output. SCKI rising edges trigger transitions on SCKO that are skew-matched to the serial output data streams on SDO0 to SDO7. The resulting SCKO frequency is half that of SCKI. Rising and falling edges of SCKO may be used to capture SDO data at the receiver (FPGA) in double data rate (DDR) fashion. For standard SPI bus operation, SCKO is not used and should be left unconnected. SCKO is forced low at the falling edge of BUSY. Logic levels are determined by OV_{DD}.

SDI (Pin 37): CMOS Serial Data Input. Drive this pin with the desired 24-bit SoftSpan configuration word (see Table 1a), latched on the rising edges of SCKI. If all channels will be configured to operate only in SoftSpan 7, tie SDI to OV_{DD}. Logic levels are determined by OV_{DD}.

$\overline{CS}$ (Pin 39): Chip Select Input. The serial data I/O bus is enabled when $\overline{CS}$ is low and is disabled and Hi-Z when $\overline{CS}$ is high. $\overline{CS}$ also gates the external shift clock, SCKI. Logic levels are determined by OV_{DD}.

LVDS I/O Mode

SDO0, SDO7, SDI (Pins 25, 36, and 37): CMOS Serial Data I/O. In LVDS I/O mode, these pins are Hi-Z.

SDI^+, SDI^- (Pins 26 and 27): LVDS Positive and Negative Serial Data Input. Differentially drive SDI^+/SDI^- with the desired 24-bit SoftSpan configuration word (see Table 1a), latched on both the rising and falling edges of $SCKI^+/SCKI^-$. The SDI^+/SDI^- input pair is internally terminated with a 100Ω differential resistor when $\overline{CS}$ is low.

$SCKI^+$, $SCKI^-$ (Pins 28 and 29): LVDS Positive and Negative Serial Clock Input. Differentially drive $SCKI^+/SCKI^-$ with the serial I/O clock. $SCKI^+/SCKI^-$ rising and falling edges latch serial data in on SDI^+/SDI^- and clock serial data out on SDO^+/SDO^-. Idle $SCKI^+/SCKI^-$ low, including when transitioning $\overline{CS}$. The $SCKI^+/SCKI^-$ input pair is internally terminated with a 100Ω differential resistor when $\overline{CS}$ = 0.

OV_{DD} (Pin 31): I/O Interface Power Supply. In LVDS I/O mode, the range of OV_{DD} is 2.375V to 5.25V. Bypass OV_{DD} to GND (Pin 30) close to the pin with a 0.1µF ceramic capacitor.

$SCKO^+$, $SCKO^-$ (Pins 32 and 33): LVDS Positive and Negative Serial Clock Output. $SCKO^+/SCKO^-$ outputs a copy of the input serial I/O clock received on $SCKI^+/SCKI^-$, skew-matched with the serial output data stream on SDO^+/SDO^-. Use the rising and falling edges of $SCKO^+/SCKO^-$ to capture SDO^+/SDO^- data at the receiver (FPGA). The $SCKO^+/SCKO^-$ output pair must be differentially terminated with a 100Ω resistor at the receiver (FPGA).

SDO^+, SDO^- (Pins 34 and 35): LVDS Positive and Negative Serial Data Output. The most recent conversion result along with channel configuration information is clocked out onto SDO^+/SDO^- on both rising and falling edges of $SCKI^+/SCKI^-$, beginning with channel 0. The SDO^+/SDO^- output pair must be differentially terminated with a 100Ω resistor at the receiver (FPGA).

$\overline{CS}$ (Pin 39): Chip Select Input. The serial data I/O bus is enabled when $\overline{CS}$ is low, and is disabled and Hi-Z when $\overline{CS}$ is high. $\overline{CS}$ also gates the external shift clock, $SCKI^+/SCKI^-$. The internal 100Ω differential termination resistors on the $SCKI^+/SCKI^-$ and SDI^+/SDI^- input pairs are disabled when $\overline{CS}$ is high. Logic levels are determined by OV_{DD}.

CONFIGURATION TABLES

Table 1a. SoftSpan Configuration Table. Use This Table with Table 1b to Choose Independent Binary SoftSpan Codes SS[2:0] for Each Channel Based on Desired Analog Input Range. Combine SoftSpan Codes to Form 24-Bit SoftSpan Configuration Word S[23:0]. Use Serial Interface to Write SoftSpan Configuration Word to LTC2348-18, as shown in Figure 19

BINARY SoftSpan CODE SS[2:0]	ANALOG INPUT RANGE	FULL SCALE RANGE	BINARY FORMAT OF CONVERSION RESULT
111	$\pm 2.5 \cdot V_{REFBUF}$	$5 \cdot V_{REFBUF}$	Two's Complement
110	$\pm 2.5 \cdot V_{REFBUF}/1.024$	$5 \cdot V_{REFBUF}/1.024$	Two's Complement
101	$0V$ to $2.5 \cdot V_{REFBUF}$	$2.5 \cdot V_{REFBUF}$	Straight Binary
100	$0V$ to $2.5 \cdot V_{REFBUF}/1.024$	$2.5 \cdot V_{REFBUF}/1.024$	Straight Binary
011	$\pm 1.25 \cdot V_{REFBUF}$	$2.5 \cdot V_{REFBUF}$	Two's Complement
010	$\pm 1.25 \cdot V_{REFBUF}/1.024$	$2.5 \cdot V_{REFBUF}/1.024$	Two's Complement
001	$0V$ to $1.25 \cdot V_{REFBUF}$	$1.25 \cdot V_{REFBUF}$	Straight Binary
000	Channel Disabled	Channel Disabled	All Zeros

Table 1b. Reference Configuration Table. The LTC2348-18 Supports Three Reference Configurations. Analog Input Range Scales with the Converter Master Reference Voltage, V_{REFBUF}

REFERENCE CONFIGURATION	V_{REFIN}	V_{REFBUF}	BINARY SoftSpan CODE SS[2:0]	ANALOG INPUT RANGE
Internal Reference with Internal Buffer	2.048V	4.096V	111	±10.24V
			110	±10V
			101	0V to 10.24V
			100	0V to 10V
			011	±5.12V
			010	±5V
			001	0V to 5.12V
External Reference with Internal Buffer (REFIN Pin Externally Overdriven)	1.25V (Min Value)	2.5V	111	±6.25V
			110	±6.104V
			101	0V to 6.25V
			100	0V to 6.104V
			011	±3.125V
			010	±3.052V
			001	0V to 3.125V
	2.2V (Max Value)	4.4V	111	±11V
			110	±10.742V
			101	0V to 11V
			100	0V to 10.742V
			011	±5.5V
			010	±5.371V
			001	0V to 5.5V

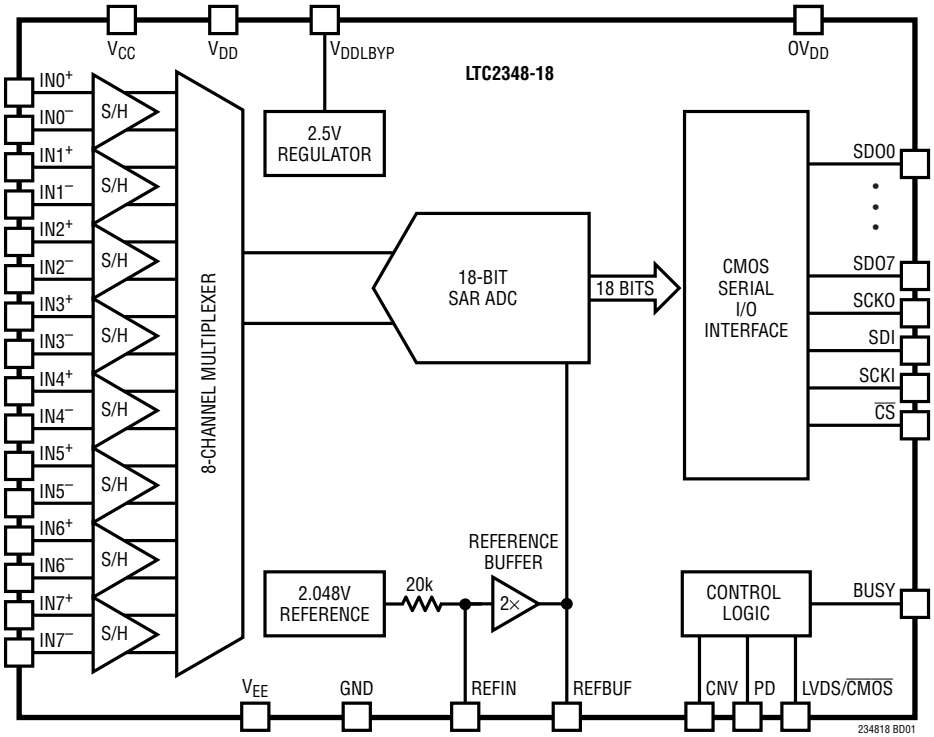
CONFIGURATION TABLES

Table 1b. Reference Configuration Table (Continued). The LTC2348-18 Supports Three Reference Configurations. Analog Input Range Scales with the Converter Master Reference Voltage, V_{REFBUF}

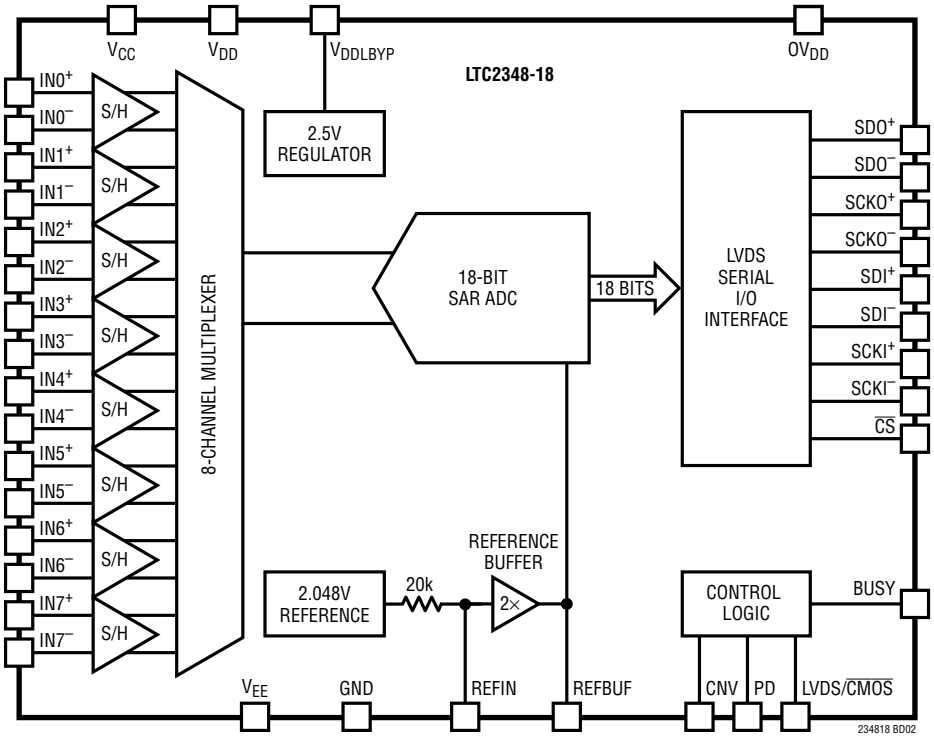
REFERENCE CONFIGURATION	V_{REFIN}	V_{REFBUF}	BINARY SoftSpan CODE SS[2:0]	ANALOG INPUT RANGE
External Reference Unbuffered (REFBUF Pin Externally Overdriven, REFIN Pin Grounded)	0V	2.5V (Min Value)	111	±6.25V
			110	±6.104V
			101	0V to 6.25V
			100	0V to 6.104V
			011	±3.125V
			010	±3.052V
			001	0V to 3.125V
	0V	5V (Max Value)	111	±12.5V
			110	±12.207V
			101	0V to 12.5V
			100	0V to 12.207V
			011	±6.25V
			010	±6.104V
			001	0V to 6.25V

FUNCTIONAL BLOCK DIAGRAM

CMOS I/O Mode

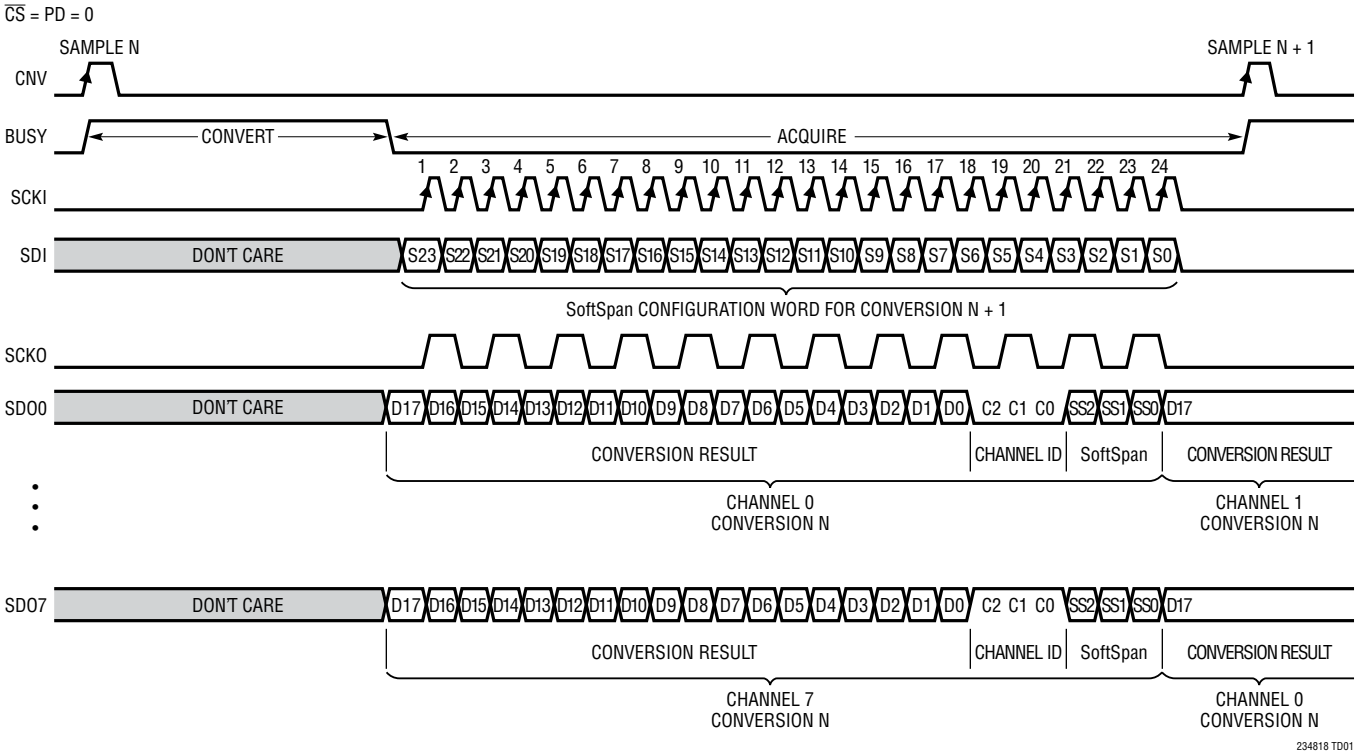


LVDS I/O Mode

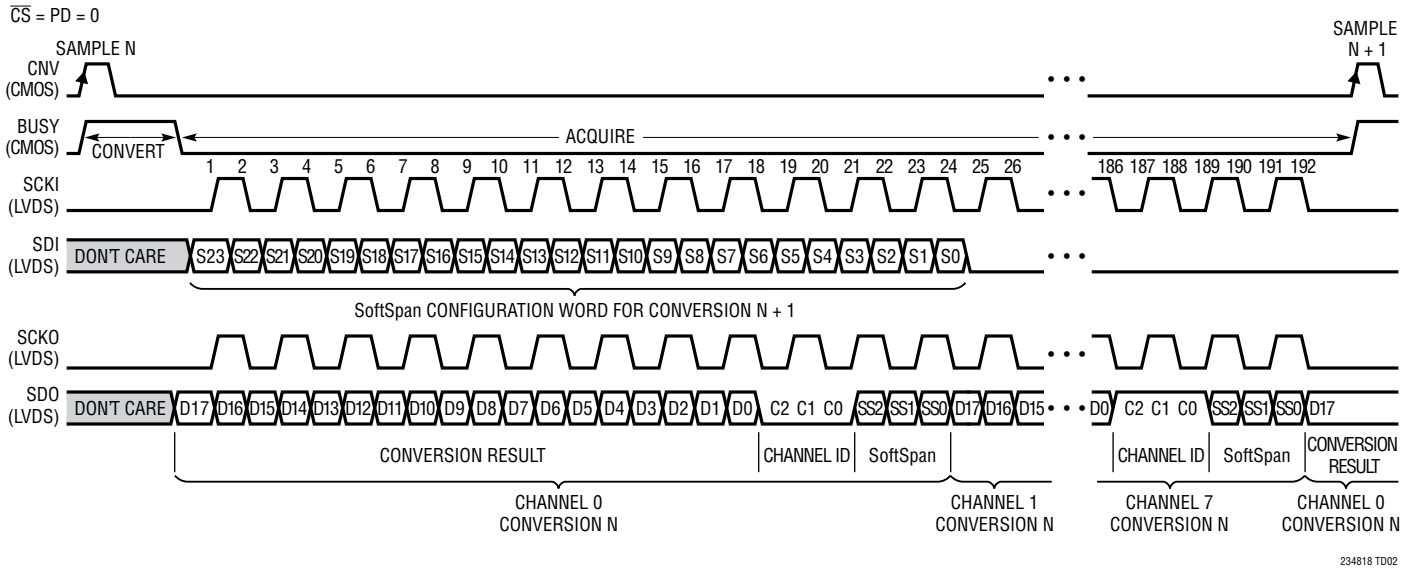


TIMING DIAGRAM

CMOS I/O Mode



LVDS I/O Mode



APPLICATIONS INFORMATION

OVERVIEW

The LTC2348-18 is an 18-bit, low noise 8-channel simultaneous sampling successive approximation register (SAR) ADC with differential, wide common mode range inputs. The ADC operates from a 5V low voltage supply and flexible high voltage supplies, nominally ±15V. Using the integrated low-drift reference and buffer (V_{REFBUF} = 4.096V nominal), each channel of this SoftSpan ADC can be independently configured on a conversion-by-conversion basis to accept ±10.24V, 0V to 10.24V, ±5.12V, or 0V to 5.12V signals. The input signal range may be expanded up to ±12.5V using an external 5V reference. Individual channels may also be disabled to increase throughput on the remaining channels.

The wide input common mode range and high CMRR (118dB typical, $V_{IN}+ = V_{IN}– = 18V_{P-P}$ 200Hz Sine) of the LTC2348-18 analog inputs allow the ADC to directly digitize a variety of signals, simplifying signal chain design. The absolute common mode input range is determined by the choice of high voltage supplies, which may be biased asymmetrically around ground and include the ability for either the positive or negative supply to be tied directly to ground. This input signal flexibility, combined with ±3LSB INL, no missing codes at 18-bits, and 96.7dB SNR, makes the LTC2348-18 an ideal choice for many high voltage applications requiring wide dynamic range.

The LTC2348-18 supports pin-selectable SPI CMOS (1.8V to 5V) and LVDS serial interfaces, enabling it to communicate equally well with legacy microcontrollers and modern FPGAs. In CMOS mode, applications may employ between one and eight lanes of serial output data, allowing the user to optimize bus width and data throughput. The LTC2348-18 typically dissipates 140mW when converting eight analog input channels simultaneously at 200ksps per channel throughput. Optional nap and power down modes may be employed to further reduce power consumption during inactive periods.

CONVERTER OPERATION

The LTC2348-18 operates in two phases. During the acquisition phase, the sampling capacitors in each channel's sample-and-hold (S/H) circuit connect to their respective analog input pins and track the differential analog input voltage ($V_{IN}+ – V_{IN}–$). A rising edge on the CNV pin transitions all channels' S/H circuits from track mode to hold mode, simultaneously sampling the input signals on all channels and initiating a conversion. During the conversion phase, each channel's sampling capacitors are connected, one channel at a time, to an 18-bit charge redistribution capacitor D/A converter (CDAC). The CDAC is sequenced through a successive approximation algorithm, effectively comparing the sampled input voltage with binary-weighted fractions of the channel's SoftSpan full-scale range (e.g., $V_{FSR}/2$, $V_{FSR}/4$ … $V_{FSR}/262144$) using a differential comparator. At the end of this process, the CDAC output approximates the channel's sampled analog input. Once all channels have been converted in this manner, the ADC control logic prepares the 18-bit digital output codes from each channel for serial transfer.

TRANSFER FUNCTION

The LTC2348-18 digitizes each channel's full-scale voltage range into 2^{18} levels. In conjunction with the ADC master reference voltage, V_{REFBUF}, a channel's SoftSpan configuration determines its input voltage range, full-scale range, LSB size, and the binary format of its conversion result, as shown in Tables 1a and 1b. For example, employing the internal reference and buffer (V_{REFBUF} = 4.096V nominal), SoftSpan 7 configures a channel to accept a ±10.24V bipolar analog input voltage range, which corresponds to a 20.48V full-scale range with a 78.125µV LSB. Other SoftSpan configurations and reference voltages may be employed to convert both larger and smaller bipolar and unipolar input ranges. Conversion results are output in two's complement binary format for all bipolar SoftSpan ranges, and in straight binary format for all unipolar SoftSpan ranges. The ideal two's complement transfer function is shown in Figure 2, while the ideal straight binary transfer function is shown in Figure 3.

APPLICATIONS INFORMATION

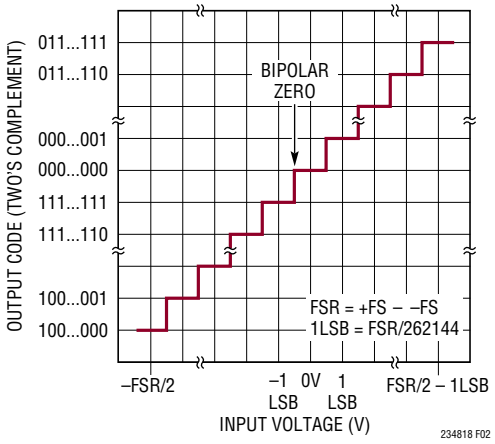


Figure 2. LTC2348-18 Two's Complement Transfer Function

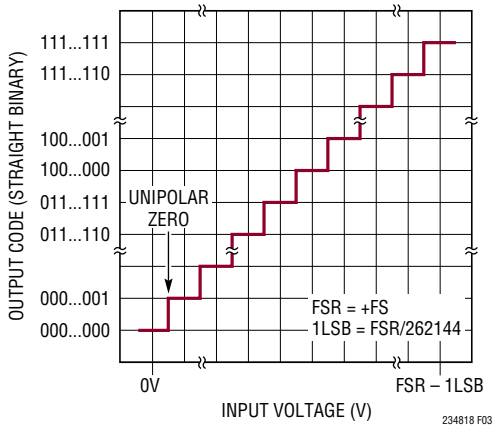


Figure 3. LTC2348-18 Straight Binary Transfer Function

ANALOG INPUTS

Each channel of the LTC2348-18 simultaneously samples the voltage difference (V_{IN}+ – V_{IN}–) between its analog input pins over a wide common mode input range while attenuating unwanted signals common to both input pins by the common-mode rejection ratio (CMRR) of the ADC. Wide common mode input range coupled with high CMRR allows the IN^+/IN^- analog inputs to swing with an arbitrary relationship to each other, provided each pin remains between (V_{CC} – 4V) and V_{EE}. This unique feature of the LTC2348-18 enables it to accept a wide variety of signal swings, including traditional classes of analog input signals such as pseudo-differential unipolar, pseudo-differential true bipolar, and fully differential, simplifying signal chain design.

The wide operating range of the high voltage supplies offers further input common mode flexibility. As long as the voltage difference limits of $10V \le V_{CC} - V_{EE} \le 38V$ are observed, V_{CC} and V_{EE} may be independently biased anywhere within their own individual allowed operating ranges, including the ability for either of the supplies to be tied directly to ground. This feature enables the common mode input range of the LTC2348-18 to be tailored to the specific application's requirements.

In all SoftSpan ranges, each channel's analog inputs can be modeled by the equivalent circuit shown in Figure 4. At the start of acquisition, the 40pF sampling capacitors (C_{IN}) connect to the analog input pins IN^+/IN^- through the sampling switches, each of which has approximately 600Ω (R_{IN}) of on-resistance. The initial voltage on both sampling capacitors at the start of acquisition is approximately equal to the sampled common-mode voltage (V_{IN}+ + V_{IN}–)/2 from the prior conversion. The external circuitry connected to IN^+ and IN^- must source or sink the charge that flows through R_{IN} as the sampling capacitors settle from their initial voltages to the new input pin voltages over the course of the acquisition interval. During conversion, nap, and power down modes, the analog inputs draw only a small leakage current. The diodes at the inputs provide ESD protection.

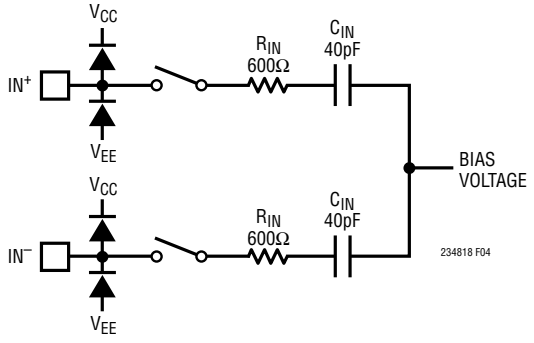


Figure 4. Equivalent Circuit for Differential Analog Inputs, Single Channel Shown

APPLICATIONS INFORMATION

Bipolar SoftSpan Input Ranges

For channels configured in SoftSpan ranges 7, 6, 3, or 2, the LTC2348-18 digitizes the differential analog input voltage ($V_{IN}+ – V_{IN}–$) over a bipolar span of $\pm2.5 \cdot V_{REFBUF}$, $\pm2.5 \cdot V_{REFBUF}/1.024$, $\pm1.25 \cdot V_{REFBUF}$, or $\pm1.25 \cdot V_{REFBUF}/1.024$, respectively, as shown in Table 1a. These SoftSpan ranges are useful for digitizing input signals where IN^+ and $IN^–$ swing above and below each other. Traditional examples include fully differential input signals, where IN^+ and $IN^–$ are driven 180 degrees out-of-phase with respect to each other centered around a common mode voltage $(V_{IN}+ + V_{IN}–)/2$, and pseudo-differential true bipolar input signals, where IN^+ swings above and below a ground reference level, driven on $IN^–$. Regardless of the chosen SoftSpan range, the wide common mode input range and high CMRR of the $IN^+/IN^–$ analog inputs allow them to swing with an arbitrary relationship to each other, provided each pin remains between (V_{CC} – 4V) and V_{EE}. The output data format for all bipolar SoftSpan ranges is two's complement.

Unipolar SoftSpan Input Ranges

For channels configured in SoftSpan ranges 5, 4, or 1, the LTC2348-18 digitizes the differential analog input voltage ($V_{IN}+ – V_{IN}–$) over a unipolar span of 0V to $2.5 \cdot V_{REFBUF}$, 0V to $2.5 \cdot V_{REFBUF}/1.024$, or 0V to $1.25 \cdot V_{REFBUF}$, respectively, as shown in Table 1a. These SoftSpan ranges are useful for digitizing input signals where IN^+ remains above $IN^–$. A traditional example includes pseudo-differential unipolar input signals, where IN^+ swings above a ground reference level, driven on $IN^–$. Regardless of the chosen SoftSpan range, the wide common mode input range and high CMRR of the $IN^+/IN^–$ analog inputs allow them to swing with an arbitrary relationship to each other, provided each pin remains between (V_{CC} – 4V) and V_{EE}. The output data format for all unipolar SoftSpan ranges is straight binary.

INPUT DRIVE CIRCUITS

The initial voltage on each channel's sampling capacitors at the start of acquisition must settle to the new input pin voltages during the acquisition interval. The external circuitry connected to IN^+ and $IN^–$ must source or sink the charge that flows through R_{IN} as this settling occurs. The LTC2348-18 sampling network RC time constant of 24ns implies an 18-bit settling time to a full-scale step of approximately $13 \cdot (R_{IN} \cdot C_{IN}) = 312$ns. The impedance and self-settling of external circuitry connected to the analog input pins will increase the overall settling time required. Low impedance sources can directly drive the inputs of the LTC2348-18 without gain error, but high impedance sources should be buffered to ensure sufficient settling during acquisition and to optimize the linearity and distortion performance of the ADC. Settling time is an important consideration even for DC input signals, as the voltages on the sampling capacitors will differ from the analog input pin voltages at the start of acquisition.

Most applications should use a buffer amplifier to drive the analog inputs of the LTC2348-18. The amplifier provides low output impedance, enabling fast settling of the analog signal during the acquisition phase. It also provides isolation between the signal source and the charge flow at the analog inputs when entering acquisition.

Input Filtering

The noise and distortion of an input buffer amplifier and other supporting circuitry must be considered since they add to the ADC noise and distortion. Noisy input signals should be filtered prior to the buffer amplifier with a low-bandwidth filter to minimize noise. The simple one-pole RC lowpass filter shown in Figure 5 is sufficient for many applications.

At the output of the buffer, a lowpass RC filter network formed by the 600Ω sampling switch on-resistance (R_{IN}) and the 40pF sampling capacitance (C_{IN}) limits the input bandwidth on each channel to 7MHz, which is fast enough to allow for sufficient transient settling during acquisition

APPLICATIONS INFORMATION

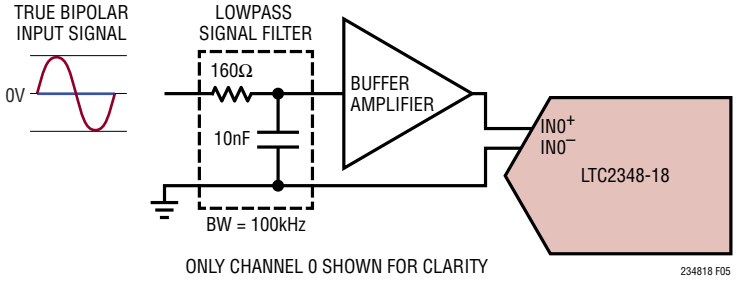


Figure 5. True Bipolar Signal Chain with Input Filtering

while simultaneously filtering driver wideband noise. A buffer amplifier with low noise density should be selected to minimize SNR degradation over this bandwidth. An additional filter network may be placed between the buffer output and ADC input to further minimize the noise contribution of the buffer and reduce disturbances to the buffer from ADC acquisition transients. A simple one-pole lowpass RC filter is sufficient for many applications. It is important that the RC time constant of this filter be small enough to allow the analog inputs to completely settle to 18-bit resolution within the ADC acquisition time (t_{ACQ}), as insufficient settling can limit INL and THD performance. Also note that the minimum acquisition time varies with sampling frequency (f_{SMPL}) and the number of enabled channels.

High quality capacitors and resistors should be used in the RC filters since these components can add distortion. NPO/COG and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self-heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

Buffering Arbitrary and Fully Differential Analog Input Signals

The wide common mode input range and high CMRR of the LTC2348-18 allow each channel's IN^+ and IN^- pins to swing with an arbitrary relationship to each other, provided each pin remains between (V_{CC} – 4V) and V_{EE}. This unique feature of the LTC2348-18 enables it to accept a wide variety of signal swings, simplifying signal chain design. In many applications, connecting a channel's IN^+ and IN^- pins directly to the existing signal chain circuitry will not allow the channel's sampling network to settle to 18-bit resolution within the ADC acquisition time (t_{ACQ}). In these cases, it is recommended that two unity-gain buffers be inserted between the signal source and the ADC input pins, as shown in Figure 6a. Table 2 lists several amplifier and lowpass filter combinations recommended for use in this circuit. The LT1469 combines fast settling, high linearity, and low offset with 5nV/$\sqrt{Hz}$ input-referred noise density, enabling it to achieve the full ADC data sheet SNR and THD specifications, as shown in the FFT plots in Figures 6b to 6e. In applications where slightly degraded

Table 2. Recommended Amplifier and Filter Combinations for the Buffer Circuits in Figures 6a and 9. AC Performance Measured Using Circuit in Figure 6a, ±10.24V Range

AMPLIFIER	R_{FILT} (Ω)	C_{FILT} (pF)	INPUT SIGNAL DRIVE	SNR (dB)	THD (dB)	SINAD (dB)	SFDR (dB)
½ LT1469	49.9	1000	FULLY DIFFERENTIAL	96.7	–119	96.6	120
½ LT1355	100	270	FULLY DIFFERENTIAL	96.5	–119	96.4	120
½ LT1469	49.9	1000	TRUE BIPOLAR	96.7	–109	96.5	110
½ LT1355	100	270	TRUE BIPOLAR	96.5	–106	96.1	108
½ LT1469	0	0	TRUE BIPOLAR	95.7	–109	95.5	110
½ LT1355	0	0	TRUE BIPOLAR	95.9	–106	95.5	108
½ LT1358	100	270	TRUE BIPOLAR	96.7	–108	96.5	110

APPLICATIONS INFORMATION

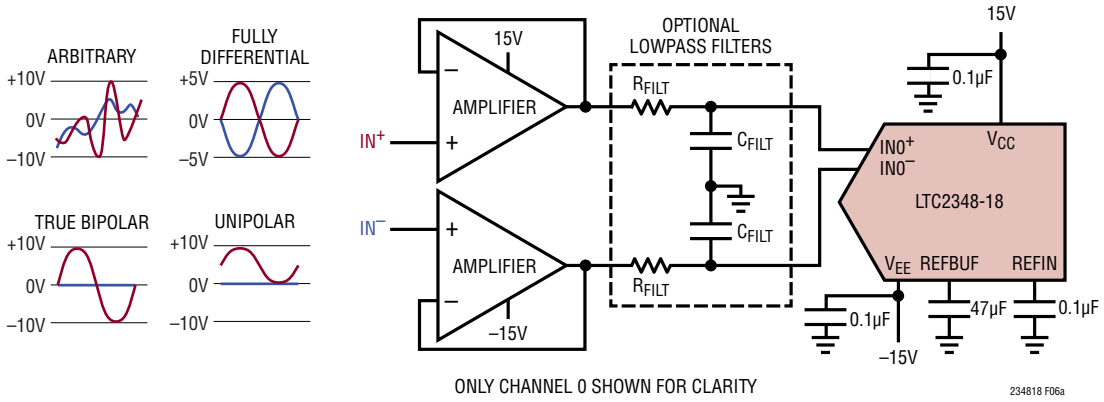


Figure 6a. Buffering Arbitrary, Fully Differential, True Bipolar, and Unipolar Signals. See Table 2 For Recommended Amplifier and Filter Combinations

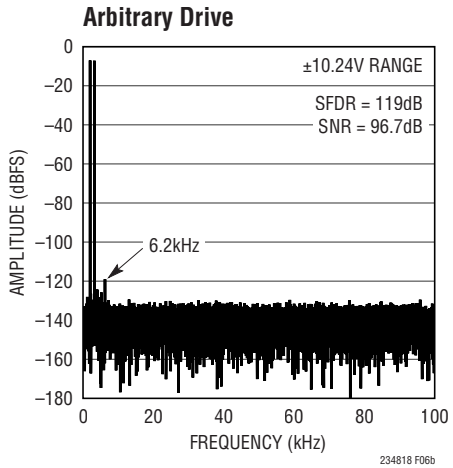


Figure 6b. Two-Tone Test. IN⁺ = –7dBFS 2kHz Sine, IN⁻ = –7dBFS 3.1kHz Sine, 32k Point FFT, f_{SMPL} = 200ksps. Circuit Shown in Figure 6a with LT1469 Amplifiers, R_{FILT} = 49.9Ω, C_{FILT} = 1000pF

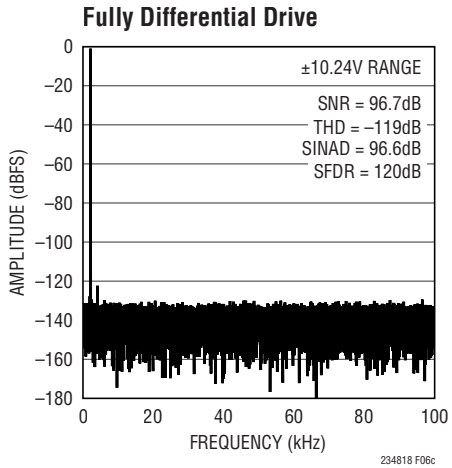


Figure 6c. IN⁺/IN⁻ = –1dBFS 2kHz Fully Differential Sine, V_{CM} = 0V, 32k Point FFT, f_{SMPL} = 200ksps. Circuit Shown in Figure 6a with LT1469 Amplifiers, R_{FILT} = 49.9Ω, C_{FILT} = 1000pF

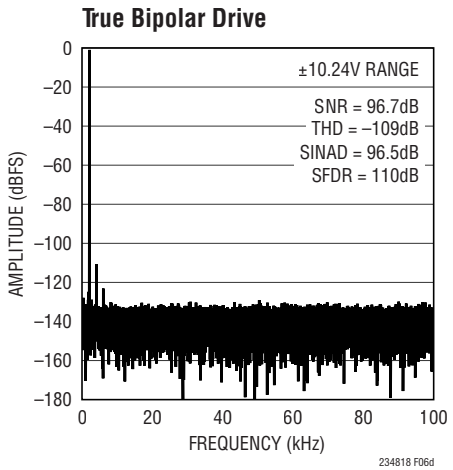


Figure 6d. IN⁺ = –1dBFS 2kHz True Bipolar Sine, IN⁻ = 0V, 32k Point FFT, f_{SMPL} = 200ksps. Circuit Shown in Figure 6a with LT1469 Amplifiers, R_{FILT} = 49.9Ω, C_{FILT} = 1000pF

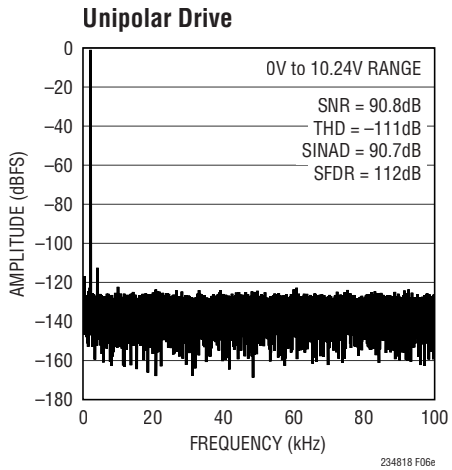


Figure 6e. IN⁺ = –1dBFS 2kHz Unipolar Sine, IN⁻ = 0V, 32k Point FFT, f_{SMPL} = 200ksps. Circuit Shown in Figure 6a with LT1469 Amplifiers, R_{FILT} = 49.9Ω, C_{FILT} = 1000pF

APPLICATIONS INFORMATION

SNR and THD performance is acceptable, it is possible to drive the LTC2348-18 using the lower-power LT1355. The LT1355 combines fast settling, good linearity, and moderate offset with 10nV/√Hz input-referred noise density, enabling it to drive the LTC2348-18 with only 0.2dB SNR loss and 3dB THD loss compared with the LT1469. As shown in Table 2, both the LT1469 and LT1355 may be used without a lowpass filter at a loss of ≤1dB SNR due to increased wideband noise. For sampling frequencies with minimum acquisition times (t_{ACQ}) under 500ns, use either the LT1469 or LT1355 without lowpass filtering, or the LT1358 with lowpass filtering, for the best settling, linearity, and THD performance.

The two-tone test shown in Figure 6b demonstrates the arbitrary input drive capability of the LTC2348-18. This test simultaneously drives IN⁺ with a –7dBFS 2kHz single-ended sine wave and IN⁻ with a –7dBFS 3.1kHz single-ended sine wave. Together, these signals sweep the analog inputs across a wide range of common mode and differential mode voltage combinations, similar to the more general arbitrary input signal case. They also have a simple spectral representation. An ideal differential converter with no common-mode sensitivity will digitize this signal as two –7dBFS spectral tones, one at each sine wave frequency. The FFT plot in Figure 6b demonstrates the LTC2348-18 response approaches this ideal, with 119dB of SFDR limited by the converter's second harmonic distortion response to the 3.1kHz sine wave on IN⁻.

The ability of the LTC2348-18 to accept arbitrary signal swings over a wide input common mode range with high CMRR can simplify application solutions. In practice, many sensors produce a differential sensor voltage riding on top of a large common mode signal. Figure 7a depicts one way of using the LTC2348-18 to digitize signals of this type. The amplifier stage provides a differential gain of approximately 10V/V to the desired sensor signal while the unwanted common mode signal is attenuated by the ADC CMRR. The circuit employs the ±5V SoftSpan range of the ADC. Figure 7b shows measured CMRR performance of this solution, which is competitive with the best commercially available instrumentation amplifiers. Figure 7c shows measured AC performance of this solution.

In Figure 8, another application circuit is shown which uses two channels of the LTC2348-18 to simultaneously sense the voltage on and bidirectional current through a sense resistor over a wide common mode range. In many applications of this type, the impedance of the external circuitry is low enough that the ADC sampling network can fully settle without buffering.

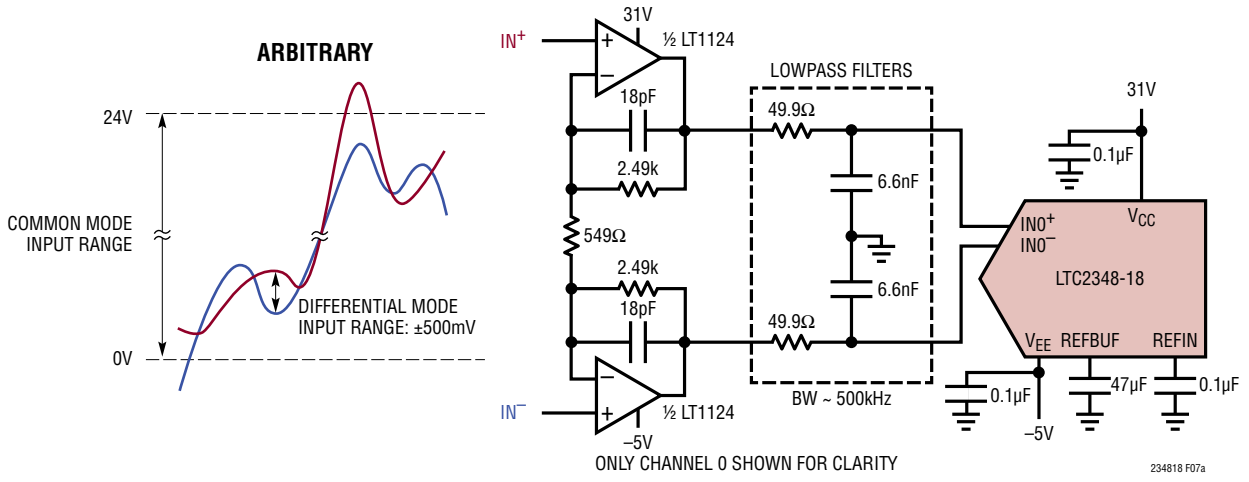


Figure 7a. Digitize Differential Signals Over a Wide Common Mode Range

APPLICATIONS INFORMATION

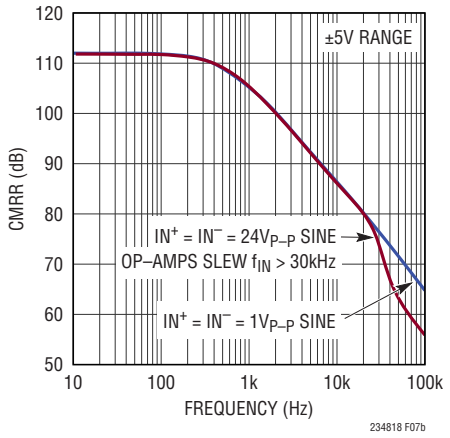


Figure 7b. CMRR vs Input Frequency. Circuit Shown in Figure 7a

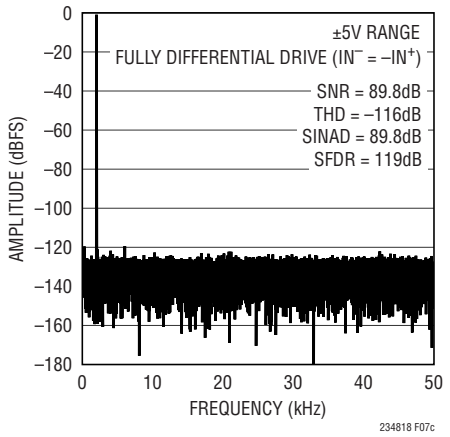
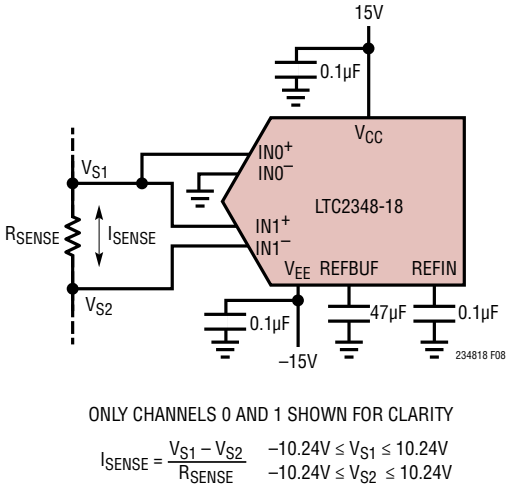


Figure 7c. IN^+/IN^- = 450mV 2kHz Fully Differential Sine, 0V ≤ V_{CM} ≤ 24V, 32k Point FFT, f_{SMPL} = 100ksps. Circuit Shown in Figure 7a



ONLY CHANNELS 0 AND 1 SHOWN FOR CLARITY

$$I_{SENSE} = \frac{V_{S1} - V_{S2}}{R_{SENSE}} \quad \begin{matrix} -10.24V \le V_{S1} \le 10.24V \\ -10.24V \le V_{S2} \le 10.24V \end{matrix}$$

Figure 8. Simultaneously Sense Voltage (CH0) and Current (CH1) Over a Wide Common Mode Range

Buffering Single-Ended Analog Input Signals

While the circuit shown in Figure 6a is capable of buffering single-ended input signals, the circuit shown in Figure 9 is preferable when the single-ended signal reference level is inherently low impedance and doesn't require buffering. This circuit eliminates one driver and lowpass filter, reducing part count, power dissipation, and SNR degradation due to driver noise. Using the recommended driver and filter combinations in Table 2, the performance of this circuit with single-ended input signals is on par with the performance of the circuit in Figure 6a.

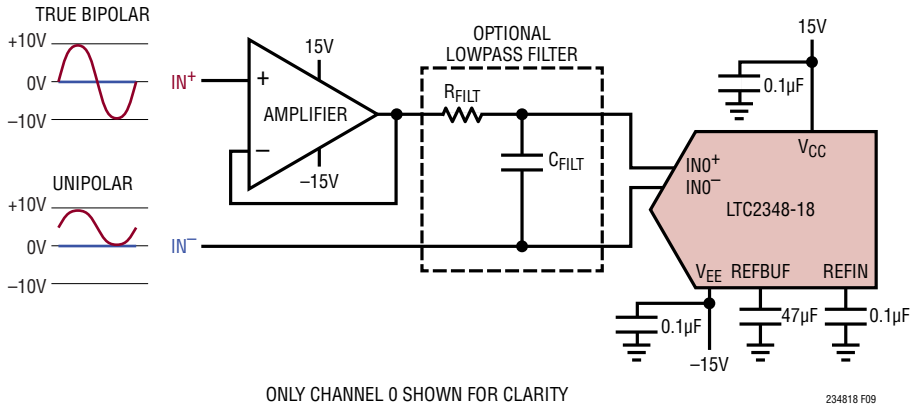


Figure 9. Buffering Single-Ended Input Signals. See Table 2 For Recommended Amplifier and Filter Combinations

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ADC REFERENCE

As shown previously in Table 1b, the LTC2348-18 supports three reference configurations. The first uses both the internal bandgap reference and reference buffer. The second externally overdrives the internal reference but retains the internal buffer, which isolates the external reference from ADC conversion transients. This configuration is ideal for sharing a single precision external reference across multiple ADCs. The third disables the internal buffer and overdrives the REFBUF pin externally.

Internal Reference with Internal Buffer

The LTC2348-18 has an on-chip, low noise, low drift (20ppm/°C maximum), temperature compensated bandgap reference that is factory trimmed to 2.048V. The reference output connects through a 20kΩ resistor to the REFIN pin, which serves as the input to the on-chip reference buffer, as shown in Figure 10a. When employing the internal bandgap reference, the REFIN pin should be bypassed to GND (Pin 20) close to the pin with a 0.1µF ceramic capacitor to filter wideband noise. The reference buffer amplifies V_{REFIN} to create the converter master reference voltage $V_{REFBUF} = 2 \cdot V_{REFIN}$ on the REFBUF pin, nominally 4.096V when using the internal bandgap reference. Bypass REFBUF to GND (Pin 20) close to the pin with at least a 47µF ceramic capacitor (X7R, 10V, 1210 size or X5R, 10V, 0805 size) to compensate the reference buffer, absorb transient conversion currents, and minimize noise.

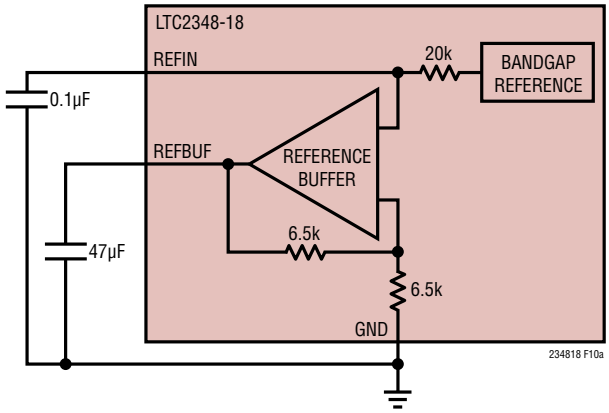

Figure 10a. Internal Reference with Internal Buffer Configuration

External Reference with Internal Buffer

If more accuracy and/or lower drift is desired, REFIN can be easily overdriven by an external reference since 20kΩ of resistance separates the internal bandgap reference output from the REFIN pin, as shown in Figure 10b. The valid range of external reference voltage overdrive on the REFIN pin is 1.25V to 2.2V, resulting in converter master reference voltages V_{REFBUF} between 2.5V and 4.4V, respectively. Linear Technology offers a portfolio of high performance references designed to meet the needs of many applications. With its small size, low power, and high accuracy, the LTC6655-2.048 is well suited for use with the LTC2348-18 when overdriving the internal reference. The LTC6655-2.048 offers 0.025% (maximum) initial accuracy

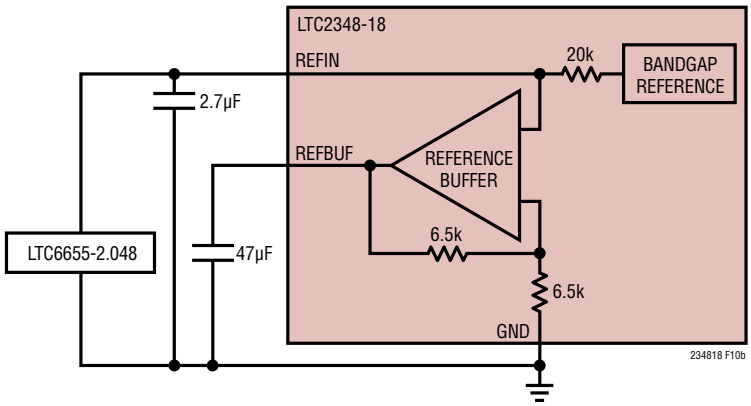

Figure 10b. External Reference with Internal Buffer Configuration

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and 2ppm/°C (maximum) temperature coefficient for high precision applications. The LTC6655-2.048 is fully specified over the H-grade temperature range, complementing the extended temperature range of the LTC2348-18 up to 125°C. Bypassing the LTC6655-2.048 with a 2.7µF to 100µF ceramic capacitor close to the REFIN pin is recommended.

External Reference with Disabled Internal Buffer

The internal reference buffer supports V_{REFBUF} = 4.4V maximum. By grounding REFIN, the internal buffer may be disabled allowing REFBUF to be overdriven with an external reference voltage between 2.5V and 5V, as shown in Figure 10c. Maximum input signal swing and SNR are achieved by overdriving REFBUF using an external 5V reference. The buffer feedback resistors load the REFBUF pin with 13kΩ even when the reference buffer is disabled. The LTC6655-5 offers the same small size, accuracy, drift, and extended temperature range as the LTC6655-2.048, and achieves a typical SNR of 97.5dB when paired with the LTC2348-18. Bypass the LTC6655-5 to GND (Pin 20) close to the REFBUF pin with at least a 47µF ceramic capacitor (X7R, 10V, 1210 size or X5R, 10V, 0805 size) to absorb transient conversion currents and minimize noise.

The LTC2348-18 converter draws a charge (Q_{CONV}) from the REFBUF pin during each conversion cycle. On short time scales most of this charge is supplied by the external REFBUF bypass capacitor, but on longer time scales all of the charge is supplied by either the reference buffer, or when the internal reference buffer is disabled, the external reference. This charge draw corresponds to a DC current equivalent of $I_{REFBUF} = Q_{CONV} \bullet f_{SMPL}$, which is proportional

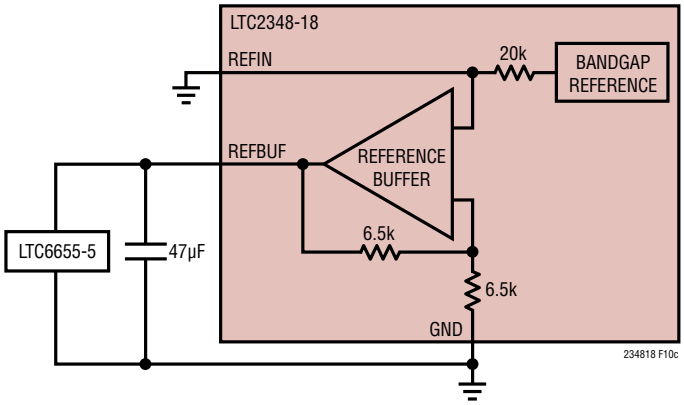

Figure 10c. External Reference with Disabled Internal Buffer Configuration

to sample rate. In applications where a burst of samples is taken after idling for long periods of time, as shown in Figure 11, I_{REFBUF} quickly transitions from approximately 0.4mA to 1.5mA (V_{REFBUF} = 5V, f_{SMPL} = 200kHz). This current step triggers a transient response in the external reference that must be considered, since any deviation in V_{REFBUF} affects converter accuracy. If an external reference is used to overdrive REFBUF, the fast settling LTC6655 family of references is recommended.

Internal Reference Buffer Transient Response

For optimum performance in applications employing burst sampling, the external reference with internal reference buffer configuration should be used. The internal reference buffer incorporates a proprietary design that minimizes movements in V_{REFBUF} when responding to a burst of conversions following an idle period. Figure 12 compares

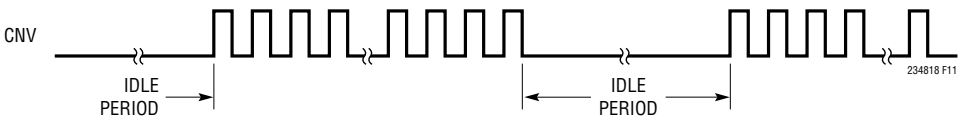

Figure 11. CNV Waveform Showing Burst Sampling

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the burst conversion response of the LTC2348-18 with an input near full scale for two reference configurations. The first configuration employs the internal reference buffer with REFIN externally overdriven by an LTC6655-2.048, while the second configuration disables the internal reference buffer and overdrives REFBUF with an external LTC6655-4.096. In both cases REFBUF is bypassed to GND with a 47µF ceramic capacitor.

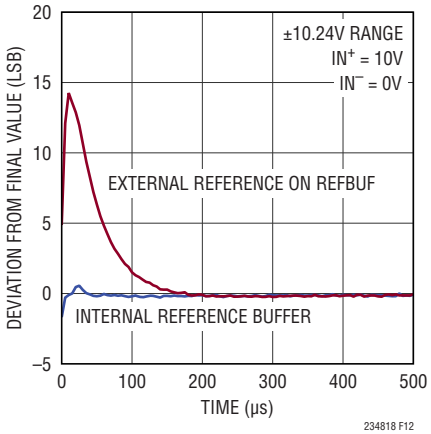

Figure 12. Burst Conversion Response of the LTC2348-18, f_{SMPL} = 200ksps

DYNAMIC PERFORMANCE

Fast Fourier transform (FFT) techniques are used to test the ADC's frequency response, distortion, and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. The LTC2348-18 provides guaranteed tested limits for both AC distortion and noise measurements.

Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the A/D output. The output is band-limited to frequencies below half the sampling frequency, excluding DC. Figure 13 shows that the LTC2348-18 achieves a typical SINAD of 96.5dB in the ±10.24V range at a 200kHz sampling rate with a true bipolar 2kHz input signal.

Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC. Figure 13 shows that the LTC2348-18 achieves a typical SNR of 96.7dB in the ±10.24V range at a 200kHz sampling rate with a true bipolar 2kHz input signal.

Total Harmonic Distortion (THD)

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ($f_{SMPL}/2$). THD is expressed as:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 ... V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through Nth harmonics, respectively. Figure 13 shows that the LTC2348-18 achieves a typical THD of –109dB (N = 6) in the ±10.24V range at a 200kHz sampling rate with a true bipolar 2kHz input signal.

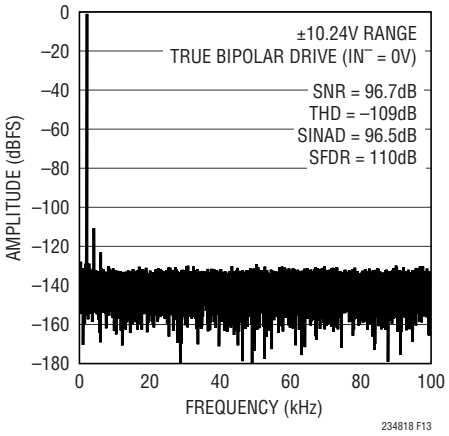

Figure 13. 32k Point FFT f_{SMPL} = 200ksps, f_{IN} = 2kHz

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POWER CONSIDERATIONS

The LTC2348-18 requires four power supplies: the positive and negative high voltage power supplies (V_{CC} and V_{EE}), the 5V core power supply (V_{DD}) and the digital input/output (I/O) interface power supply (OV_{DD}). As long as the voltage difference limits of $10V \leq V_{CC} - V_{EE} \leq 38V$ are observed, V_{CC} and V_{EE} may be independently biased anywhere within their own individual allowed operating ranges, including the ability for either of the supplies to be tied directly to ground. This feature enables the common mode input range of the LTC2348-18 to be tailored to the specific application's requirements. The flexible OV_{DD} supply allows the LTC2348-18 to communicate with CMOS logic operating between 1.8V and 5V, including 2.5V and 3.3V systems. When using LVDS I/O mode, the range of OV_{DD} is 2.375V to 5.25V.

Power Supply Sequencing

The LTC2348-18 does not have any specific power supply sequencing requirements. Care should be taken to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section. The LTC2348-18 has an internal power-on-reset (POR) circuit which resets the converter on initial power-up and whenever V_{DD} drops below 2V. Once the supply voltage re-enters the nominal supply voltage range, the POR reinitializes the ADC. No conversions should be initiated until at least 10ms after a POR event to ensure the initialization period has ended. When employing the internal reference buffer, allow 200ms for the buffer to power up and recharge the REFBUF bypass capacitor. Any conversion initiated before these times will produce invalid results.

TIMING AND CONTROL

CNV Timing

The LTC2348-18 sampling and conversion is controlled by CNV. A rising edge on CNV transitions all channels' S/H circuits from track mode to hold mode, simultaneously sampling the input signals on all channels and initiating a conversion. Once a conversion has been started, it cannot be terminated early except by resetting the ADC, as discussed in the Reset Timing section. For optimum performance, drive CNV with a clean, low jitter signal and avoid transitions on data I/O lines leading up to the rising edge of CNV. Additionally, to minimize channel-to-channel crosstalk, avoid high slew rates on the analog inputs for 100ns before and after the rising edge of CNV. Converter status is indicated by the BUSY output, which transitions low-to-high at the start of each conversion and stays high until the conversion is complete. Once CNV is brought high to begin a conversion, it should be returned low between 40ns and 60ns later or after the falling edge of BUSY to minimize external disturbances during the internal conversion process. The CNV timing required to take advantage of the reduced power nap mode of operation is described in the Nap Mode section.

Internal Conversion Clock

The LTC2348-18 has an internal clock that is trimmed to achieve a maximum conversion time of 550•N ns with N channels enabled. With a minimum acquisition time of 570ns when converting eight channels simultaneously, throughput performance of 200ksps is guaranteed without any external adjustments.

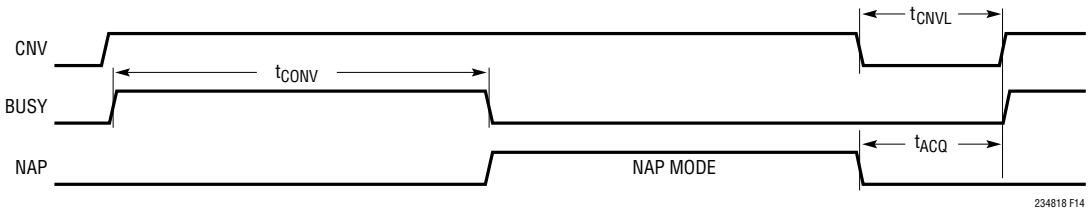

Figure 14. Nap Mode Timing for the LTC2348-18

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Nap Mode

The LTC2348-18 can be placed into nap mode after a conversion has been completed to reduce power consumption between conversions. In this mode a portion of the device circuitry is turned off, including circuits associated with sampling the analog input signals. Nap mode is enabled by keeping CNV high between conversions, as shown in Figure 14. To initiate a new conversion after entering nap mode, bring CNV low and hold for at least 420ns before bringing it high again. The converter acquisition time (t_{ACQ}) is set by the CNV low time (t_{CNVL}) when using nap mode.

Power Down Mode

When PD is brought high, the LTC2348-18 is powered down and subsequent conversion requests are ignored. If this occurs during a conversion, the device powers down once the conversion completes. In this mode, the device draws only a small regulator standby current resulting in a typical power dissipation of 0.36mW. To exit power down mode, bring the PD pin low and wait at least 10ms before initiating a conversion. When employing the internal reference buffer, allow 200ms for the buffer to power up and recharge the REFBUF bypass capacitor. Any conversion initiated before these times will produce invalid results.

Reset Timing

A global reset of the LTC2348-18, equivalent to a power-on-reset event, may be executed without needing to cycle the supplies. This feature is useful when recovering from system-level events that require the state of the entire system to be reset to a known synchronized value. To initiate a global reset, bring PD high twice without an intervening conversion, as shown in Figure 15. The reset event is triggered on the second rising edge of PD, and asynchronously ends based on an internal timer. Reset clears all serial data output registers and restores the internal SoftSpan configuration register default state of all channels in SoftSpan 7. If reset is triggered during a conversion, the conversion is immediately halted. The normal power down behavior associated with PD going high is not affected by reset. Once PD is brought low, wait at least 10ms before initiating a conversion. When employing the internal reference buffer, allow 200ms for the buffer to power up and recharge the REFBUF bypass capacitor. Any conversion initiated before these times will produce invalid results.

Power Dissipation vs Sampling Frequency

When nap mode is employed, the power dissipation of the LTC2348-18 decreases as the sampling frequency is reduced, as shown in Figure 16. This decrease in average power dissipation occurs because a portion of the LTC2348-18 circuitry is turned off during nap mode, and the fraction of the conversion cycle (t_{CYC}) spent napping increases as the sampling frequency (f_{SMPL}) is decreased.

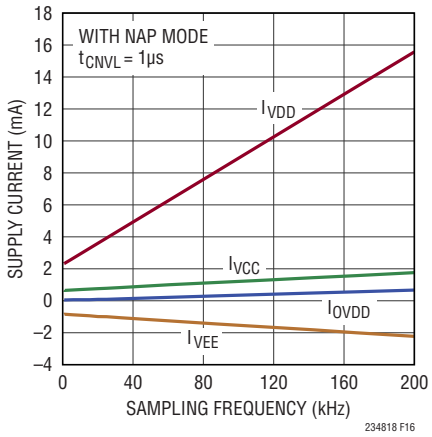

Figure 16. Power Dissipation of the LTC2348-18 Decreases with Decreasing Sampling Frequency

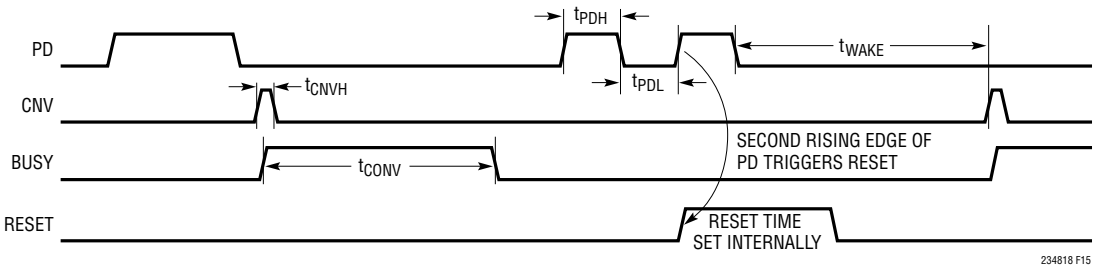

Figure 15. Reset Timing for the LTC2348-18

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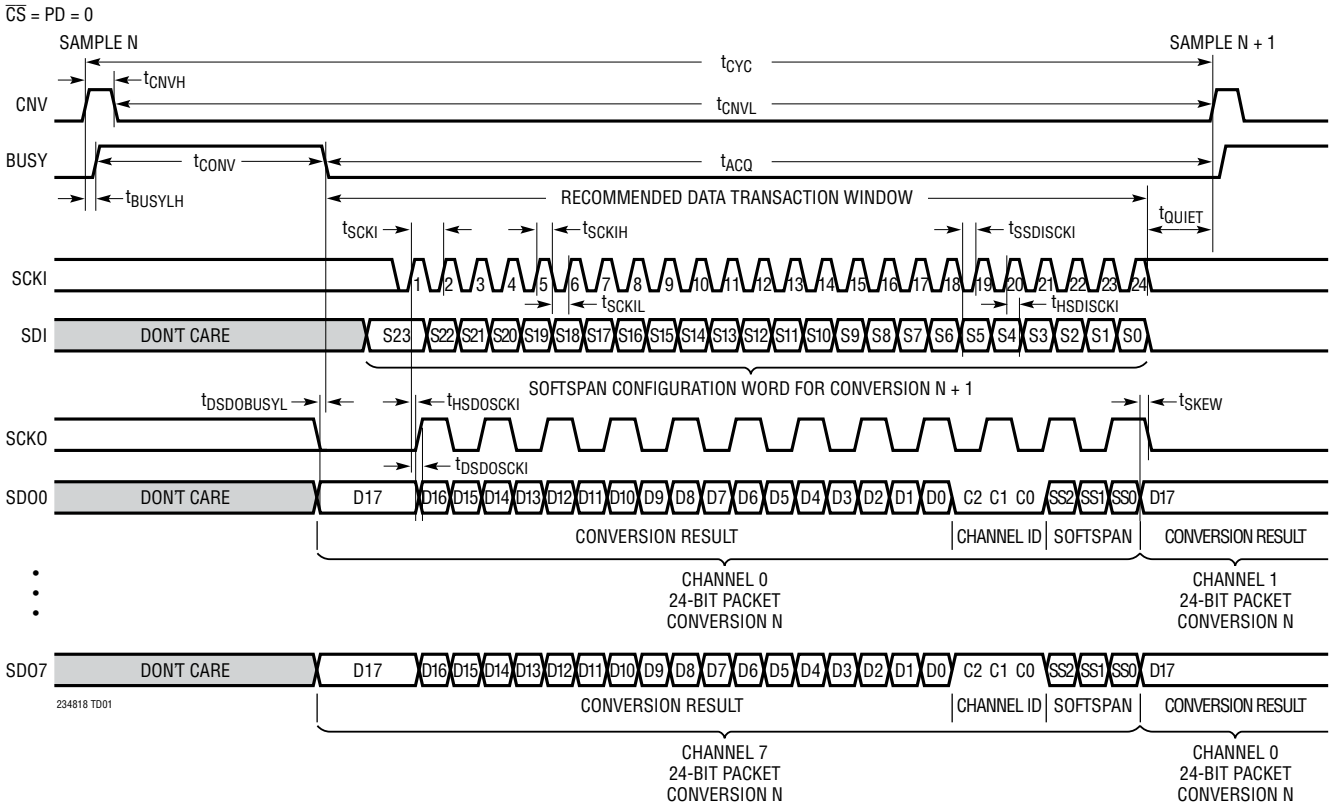

Figure 17. Serial CMOS I/O Mode

DIGITAL INTERFACE

The LTC2348-18 features CMOS and LVDS serial interfaces, selectable using the LVDS/$\overline{CMOS}$ pin. The flexible OV_{DD} supply allows the LTC2348-18 to communicate with any CMOS logic operating between 1.8V and 5V, including 2.5V and 3.3V systems, while the LVDS interface supports low noise digital designs. In CMOS mode, applications may employ between one and eight lanes of serial data output, allowing the user to optimize bus width and data throughput. Together, these I/O interface options enable the LTC2348-18 to communicate equally well with legacy microcontrollers and modern FPGAs.

Serial CMOS I/O Mode

As shown in Figure 17, in CMOS I/O mode the serial data bus consists of a serial clock input, SCKI, serial data input, SDI, serial clock output, SCKO, and eight lanes of serial data output, SDO0 to SDO7. Communication with the LTC2348-18 across this bus occurs during predefined data transaction windows. Within a window, the device accepts 24-bit SoftSpan configuration words for the next conversion on SDI and outputs 24-bit packets containing conversion results and channel configuration information from the previous conversion on SDO0 to SDO7. New data transaction windows open 10ms after powering up or resetting the LTC2348-18, and at the end of each conversion on the falling edge of BUSY. In the recommended use case, the data transaction should be completed with a minimum t_{QUIET} time of 20ns prior to the start of the next conversion, as shown in Figure 17. New SoftSpan configuration words are only accepted within this recommended data transaction window, but SoftSpan changes take effect immediately with no additional analog input settling time required before starting the next conversion. It is still possible to read conversion data after starting the next conversion, but this will degrade conversion accuracy and therefore is not recommended.

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Just prior to the falling edge of BUSY and the opening of a new data transaction window, SCKO is forced low and SDO0 to SDO7 are updated with the latest conversion results from analog input channels 0 to 7, respectively. Rising edges on SCKI serially clock conversion results and analog input channel configuration information out on SDO0 to SDO7 and trigger transitions on SCKO that are skew-matched to the data on SDO0 to SDO7. The resulting SCKO frequency is half that of SCKI. SCKI rising edges also latch SoftSpan configuration words provided on SDI, which are used to program the internal 24-bit SoftSpan configuration register. See the section Programming the SoftSpan Configuration Register in CMOS I/O Mode for further details. SCKI is allowed to idle either high or low in CMOS I/O mode. As shown in Figure 18, the CMOS bus is enabled when $\overline{CS}$ is low and is disabled and Hi-Z when $\overline{CS}$ is high, allowing the bus to be shared across multiple devices.

The data on SDO0 to SDO7 are grouped into 24-bit packets consisting of an 18-bit conversion result, 3-bit analog channel ID, and 3-bit SoftSpan code, all presented MSB first. As suggested in Figures 17 and 18, each SDO lane outputs these packets for all analog input channels in a sequential, circular manner. For example, the first 24-bit packet output on SDO0 corresponds to analog input channel 0, followed by the packets for channels 1 through 7. The data output on SDO0 then wraps back to channel 0, and this pattern repeats indefinitely. Other SDO lanes follow a similar circular pattern, except the first packet presented on each lane corresponds to its associated analog input channel.

When interfacing the LTC2348-18 with a standard SPI bus, capture output data at the receiver on rising edges of SCKI. SCKO is not used in this case. Multiple SDO lanes are also usually not useful in this case. In other applications, such as interfacing the LTC2348-18 with an FPGA or CPLD, rising and falling edges of SCKO may be used to capture serial output data on SDO0 to SDO7 in double data rate (DDR) fashion. Capturing data using SCKO adds robustness to delay variations over temperature and supply.

Full Eight Lane Serial CMOS Output Data Capture

As shown in Table 3, full 200ksps per channel throughput can be achieved with a 45MHz SCKI frequency by capturing the first packet (24 SCKI cycles total) from all eight serial data output lanes SDO0 to SDO7. This configuration also allows conversion results from all channels to be captured using as few as 18 SCKI cycles if the 3-bit analog channel ID and 3-bit SoftSpan code are not needed and the device SoftSpan configuration is not being changed. Multi-lane data capture is usually best suited for use with FPGA or CPLD capture hardware, but may be useful in other application-specific cases.

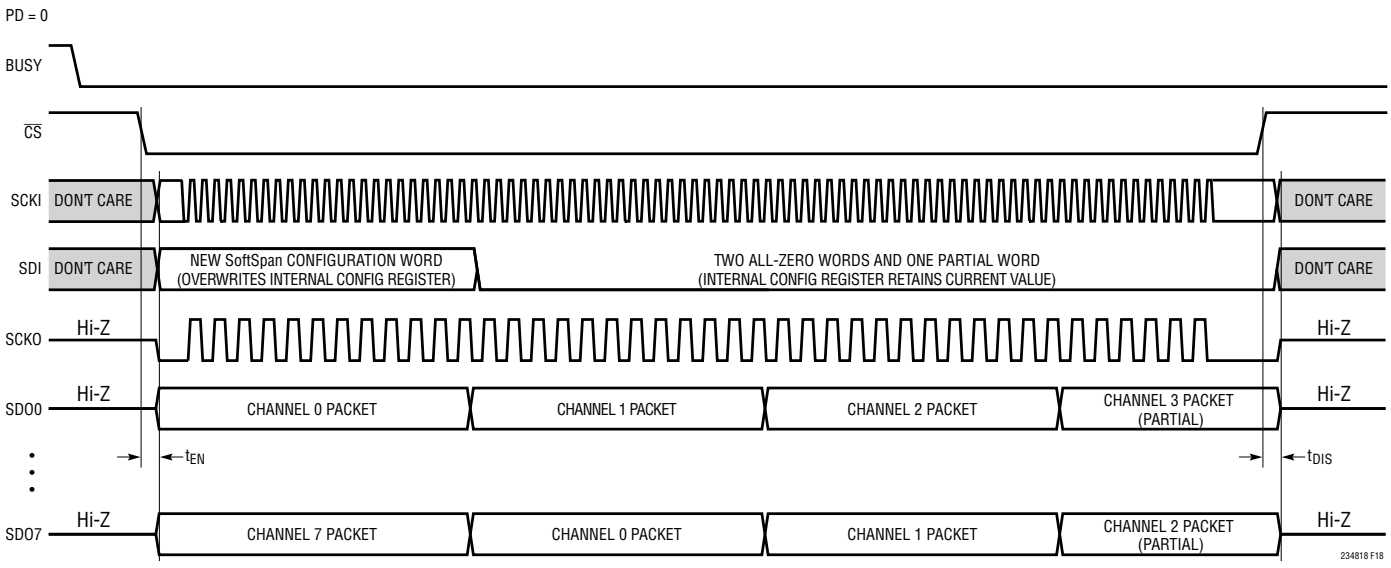

Figure 18. Internal SoftSpan Configuration Register Behavior. Serial CMOS Bus Response to $\overline{CS}$

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Fewer Than Eight Lane Serial CMOS Output Data Capture

Applications that cannot accommodate the full eight lanes of serial data capture may employ fewer lanes without reconfiguring the LTC2348-18. For example, capturing the first two packets (48 SCKI cycles total) from SDO0, SDO2, SDO4, and SDO6 provides data for analog input channels 0 and 1, 2 and 3, 4 and 5, and 6 and 7, respectively, using four output lanes. Similarly, capturing the first four packets (96 SCKI cycles total) from SDO0 and SDO4 provides data for analog input channels 0 to 3 and 4 to 7, respectively, using two output lanes. If only one lane can be accommodated, capturing the first eight packets (192 SCKI cycles total) from SDO0 provides data for all analog input channels. As shown in Table 3, full 200ksps per channel throughput can be achieved with a 90MHz SCKI frequency in the four lane case, but the maximum CMOS SCKI frequency of 100MHz limits the throughput to less than 200ksps per channel in the two lane and one lane cases. Finally, note that in choosing the number of lanes and which lanes to use for data capture, the user is not restricted to the specific cases mentioned above. Other choices may be more optimal in particular applications.

Programming the SoftSpan Configuration Register in CMOS I/O Mode

The internal 24-bit SoftSpan configuration register controls the SoftSpan range for all analog input channels of the LTC2348-18. The default state of this register after power-up or resetting the device is all ones, configuring each channel to convert in SoftSpan 7, the $\pm 2.5 \cdot V_{REFBUF}$ range (see Table 1a). The state of this register may be modified by providing a new 24-bit SoftSpan configuration word on SDI during the data transaction window shown in Figure 17. New SoftSpan configuration words are only accepted within this recommended data transaction window, but SoftSpan changes take effect immediately with no additional analog input settling time required before starting the next conversion. Setting a channel's SoftSpan code to SS[2:0] = 000 immediately disables the channel, resulting in a corresponding reduction in t_{CONV} on the next conversion. Similarly, enabling a previously disabled channel requires no additional analog input settling time before starting the next conversion. The mapping between the serial SoftSpan configuration word, the internal SoftSpan configuration register, and each channel's 3-bit SoftSpan code is illustrated in Figure 19.

If fewer than 24 SCKI rising edges are provided during a data transaction window, the partial word received on SDI will be ignored and the SoftSpan configuration register will not be updated. If exactly 24 SCKI rising edges are provided, the SoftSpan configuration register will be updated to match the received SoftSpan configuration word, S[23:0]. The one exception to this behavior occurs when S[23:0] is all zeros. In this case, the SoftSpan configuration register will not be updated, allowing applications to retain the current SoftSpan configuration state by idling SDI low. If more than 24 SCKI rising edges are provided during a data transaction window, each complete 24-bit word received on SDI will be interpreted as a new SoftSpan configuration word and applied to the SoftSpan configuration register as described above. Any partial words are ignored.

Table 3. Required SCKI Frequency to Achieve Various Throughputs in Common Output Bus Configurations with Eight Channels Enabled. Shaded Entries Denote Throughputs That Are Not Achievable In a Given Configuration. Calculated Using f_{SCKI} = (Number of SCKI Cycles)/($t_{ACQ(MIN)} - t_{QUIET}$)

I/O MODE	NUMBER OF SDO LANES	NUMBER OF SCKI CYCLES	REQUIRED f_{SCKI} (MHz) TO ACHIEVE THROUGHPUT OF 200ksps/CHANNEL (t_{ACQ} = 570ns)	100ksps/CHANNEL (t_{ACQ} = 5570ns)	50ksps/CHANNEL (t_{ACQ} = 15570ns)
CMOS	8	18	35	4	2
	8	24	45	5	2
	4	48	90	9	4
	2	96	Not Achievable	18	7
	1	192	Not Achievable	35	13
LVDS	1	96	180 (360Mbps)	18 (36Mbps)	7 (14Mbps)

APPLICATIONS INFORMATION

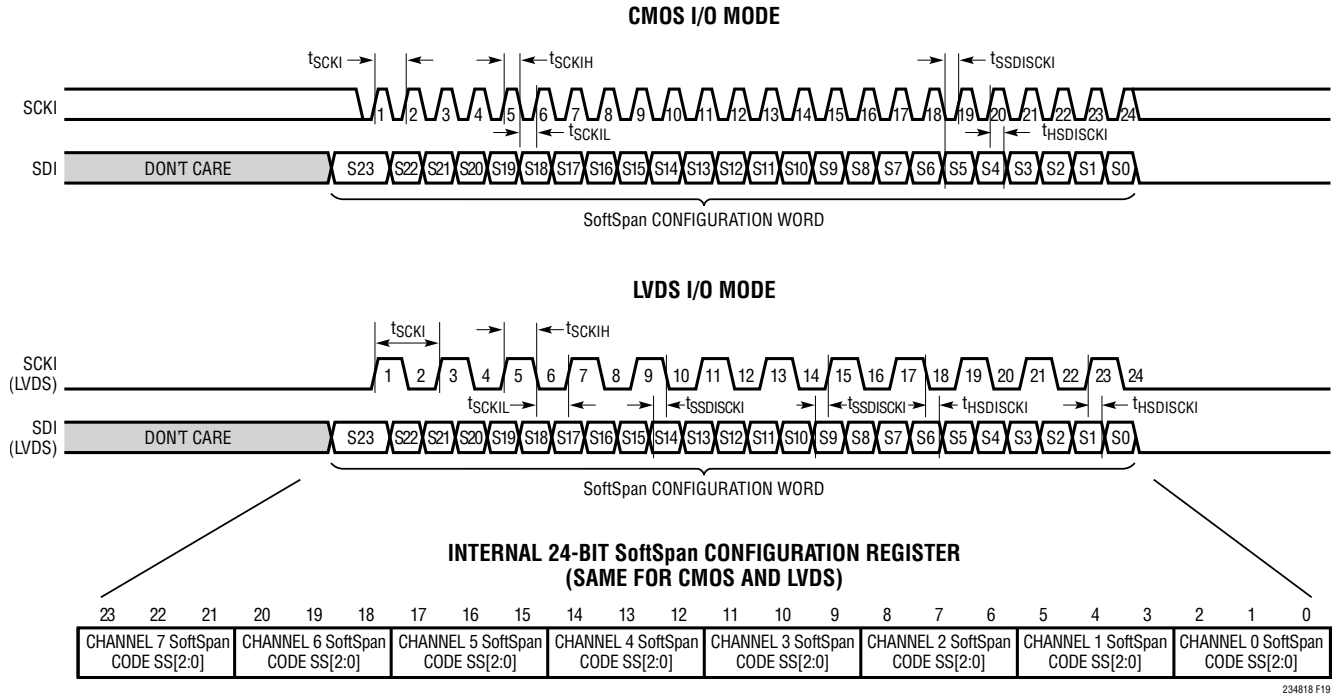


Figure 19. Mapping Between Serial SoftSpan Configuration Word, Internal SoftSpan Configuration Register, and SoftSpan Code for Each Analog Input Channel

Typically, applications will update the SoftSpan configuration register in the manner shown in Figures 17 and 18. After the opening of a new data transaction window at the falling edge of BUSY, the user supplies a 24-bit SoftSpan configuration word on SDI during the first 24 SCKI cycles. This new word overwrites the internal configuration register contents following the 24th SCKI rising edge. The user then holds SDI low for the remainder of the data transaction window causing the register to retain its contents regardless of the number of additional SCKI cycles applied. SoftSpan settings may be retained across multiple conversions by holding SDI low for the entire data transaction window, regardless of the number of SCKI cycles applied.

Serial LVDS I/O Mode

In LVDS I/O mode, information is transmitted using positive and negative signal pairs ($LVDS^+/LVDS^-$) with bits differentially encoded as ($LVDS^+ – LVDS^-$). These signals are typically routed using differential transmission lines with 100Ω characteristic impedance. Logical 1's and 0's are nominally represented by differential +350mV and –350mV, respectively. For clarity, all LVDS timing diagrams and interface discussions adopt the logical rather than physical convention.

As shown in Figure 20, in LVDS I/O mode the serial data bus consists of a serial clock differential input, SCKI, serial data differential input, SDI, serial clock differential output, SCKO, and serial data differential output, SDO. Communication with the LTC2348-18 across this bus occurs during predefined data transaction windows. Within a window, the device accepts 24-bit SoftSpan configuration words for the next conversion on SDI and outputs 24-bit packets containing conversion results and channel configuration information from the previous conversion on SDO. New data transaction windows open 10ms after powering up or resetting the LTC2348-18, and at the end of each conversion on the falling edge of BUSY. In the recommended use case, the data transaction should be completed with a minimum t_{QUIET} time of 20ns prior to the start of the next conversion, as shown in Figure 20. New SoftSpan configuration words are only accepted within this recommended data transaction window, but SoftSpan changes

APPLICATIONS INFORMATION

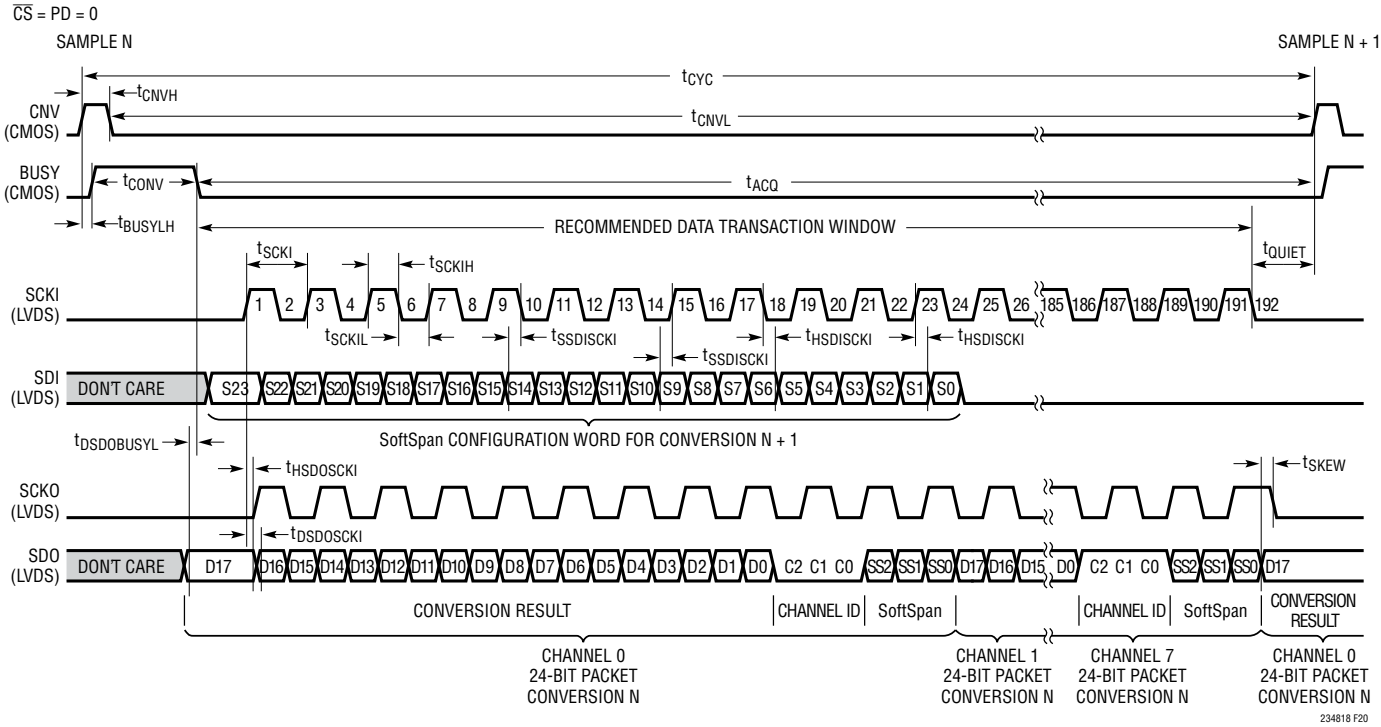


Figure 20. Serial LVDS I/O Mode

take effect immediately with no additional analog input settling time required before starting the next conversion. It is still possible to read conversion data after starting the next conversion, but this will degrade conversion accuracy and therefore is not recommended.

Just prior to the falling edge of BUSY and the opening of a new data transaction window, SDO is updated with the latest conversion results from analog input channel 0. Both rising and falling edges on SCKI serially clock conversion results and analog input channel configuration information out on SDO. SCKI is also echoed on SCKO, skew-matched to the data on SDO. Whenever possible, it is recommended that rising and falling edges of SCKO be used to capture DDR serial output data on SDO, as this will yield the best robustness to delay variations over supply and temperature. SCKI rising and falling edges also latch SoftSpan configuration words provided on SDI, which are used to program the internal 24-bit SoftSpan configuration register. See the section Programming the SoftSpan Configuration Register in LVDS I/O Mode for further details. As shown in Figure 21, the LVDS bus is enabled when $\overline{CS}$ is low and is disabled and Hi-Z when $\overline{CS}$ is high, allowing the bus to be shared across multiple devices. Due to the high speeds involved in LVDS signaling, LVDS bus sharing must be carefully considered. Transmission line limitations imposed by the shared bus may limit the maximum achievable bus clock speed. LVDS inputs are internally terminated with a 100Ω differential resistor when $\overline{CS}$ is low, while outputs must be differentially terminated with a 100Ω resistor at the receiver (FPGA). SCKI must idle in the low state in LVDS I/O mode, including when transitioning $\overline{CS}$.

The data on SDO are grouped into 24-bit packets consisting of an 18-bit conversion result, 3-bit analog channel ID, and 3-bit SoftSpan code, all presented MSB first. As suggested in Figures 20 and 21, SDO outputs these packets for all analog input channels in a sequential, circular manner. For example, the first 24-bit packet output on SDO corresponds to analog input channel 0, followed by the packets for channels 1 through 7. The data output on SDO then wraps back to channel 0, and this pattern repeats indefinitely.

APPLICATIONS INFORMATION

Serial LVDS Output Data Capture

As shown in Table 3, full 200ksps per channel throughput can be achieved with a 180MHz SCKI frequency by capturing eight packets (96 SCKI cycles total) of DDR data from SDO. The LTC2348-18 supports LVDS SCKI frequencies up to 250MHz.

Programming the SoftSpan Configuration Register in LVDS I/O Mode

The internal 24-bit SoftSpan configuration register controls the SoftSpan range for all analog input channels of the LTC2348-18. The default state of this register after power-up or resetting the device is all ones, configuring each channel to convert in SoftSpan 7, the ±2.5 • V_{REFBUF} range (see Table 1a). The state of this register may be modified by providing a new 24-bit SoftSpan configuration word on SDI during the data transaction window shown in Figure 20. New SoftSpan configuration words are only accepted within this recommended data transaction window, but SoftSpan changes take effect immediately with no additional analog input settling time required before starting the next conversion. Setting a channel's SoftSpan code to SS[2:0] = 000 immediately disables the channel, resulting in a corresponding reduction in t_{CONV} on the next conversion. Similarly, enabling a previously disabled channel requires no additional analog input settling time before starting the next conversion. The mapping between the serial SoftSpan configuration word, the internal SoftSpan configuration register, and each channel's 3-bit SoftSpan code is illustrated in Figure 19.

If fewer than 24 SCKI edges (rising plus falling) are provided during a data transaction window, the partial word received on SDI will be ignored and the SoftSpan configuration register will not be updated. If exactly 24 SCKI edges are provided, the SoftSpan configuration register will be updated to match the received SoftSpan configuration word, S[23:0]. The one exception to this behavior occurs when S[23:0] is all zeros. In this case, the SoftSpan configuration register will not be updated, allowing applications to retain the current SoftSpan configuration state by idling SDI low. If more than 24 SCKI edges are provided during a data transaction window, each complete 24-bit word received on SDI will be interpreted as a new SoftSpan configuration word and applied to the SoftSpan configuration register as described above. Any partial words are ignored.

Typically, applications will update the SoftSpan configuration register in the manner shown in Figures 20 and 21. After the opening of a new data transaction window at the falling edge of BUSY, the user supplies a 24-bit DDR SoftSpan configuration word on SDI during the first 12 SCKI cycles. This new word overwrites the internal configuration register contents following the 12th SCKI falling edge. The user then holds SDI low for the remainder of the data transaction window causing the register to retain its contents regardless of the number of additional SCKI cycles applied. SoftSpan settings may be retained across multiple conversions by holding SDI low for the entire data transaction window, regardless of the number of SCKI cycles applied.

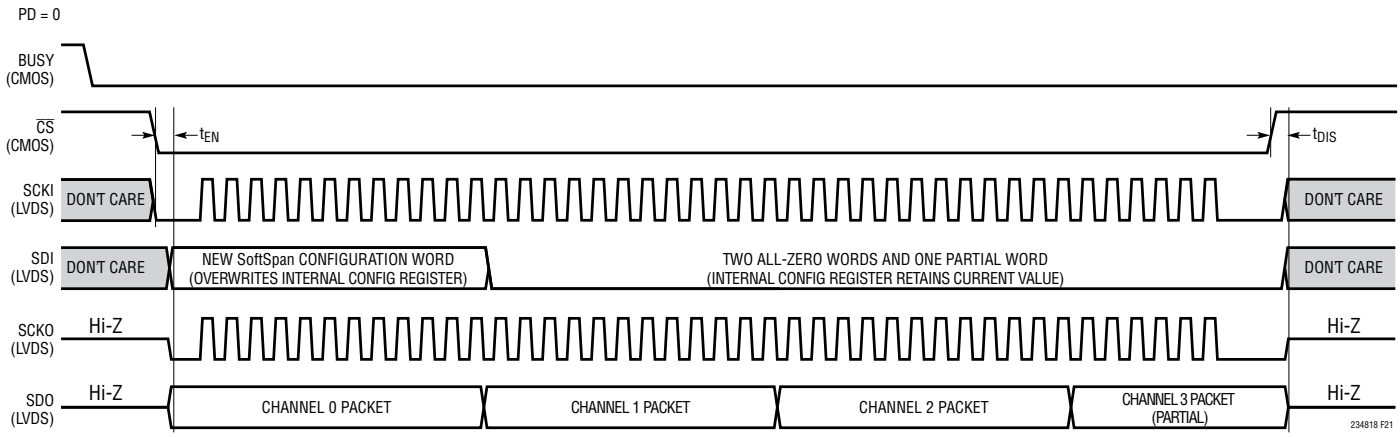


Figure 21. Internal SoftSpan Configuration Register Behavior. Serial LVDS Bus Response to $\overline{CS}$

BOARD LAYOUT

To obtain the best performance from the LTC2348-18, a four-layer printed circuit board (PCB) is recommended. Layout for the PCB should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital clocks or signals alongside analog signals or underneath the ADC. Also minimize the length of the REFBUF to GND (Pin 20) bypass capacitor return loop, and avoid routing CNV near signals which could potentially disturb its rising edge.

Supply bypass capacitors should be placed as close as possible to the supply pins. Low impedance common returns for these bypass capacitors are essential to the low noise operation of the ADC. A single solid ground plane is recommended for this purpose. When possible, screen the analog input traces using ground.

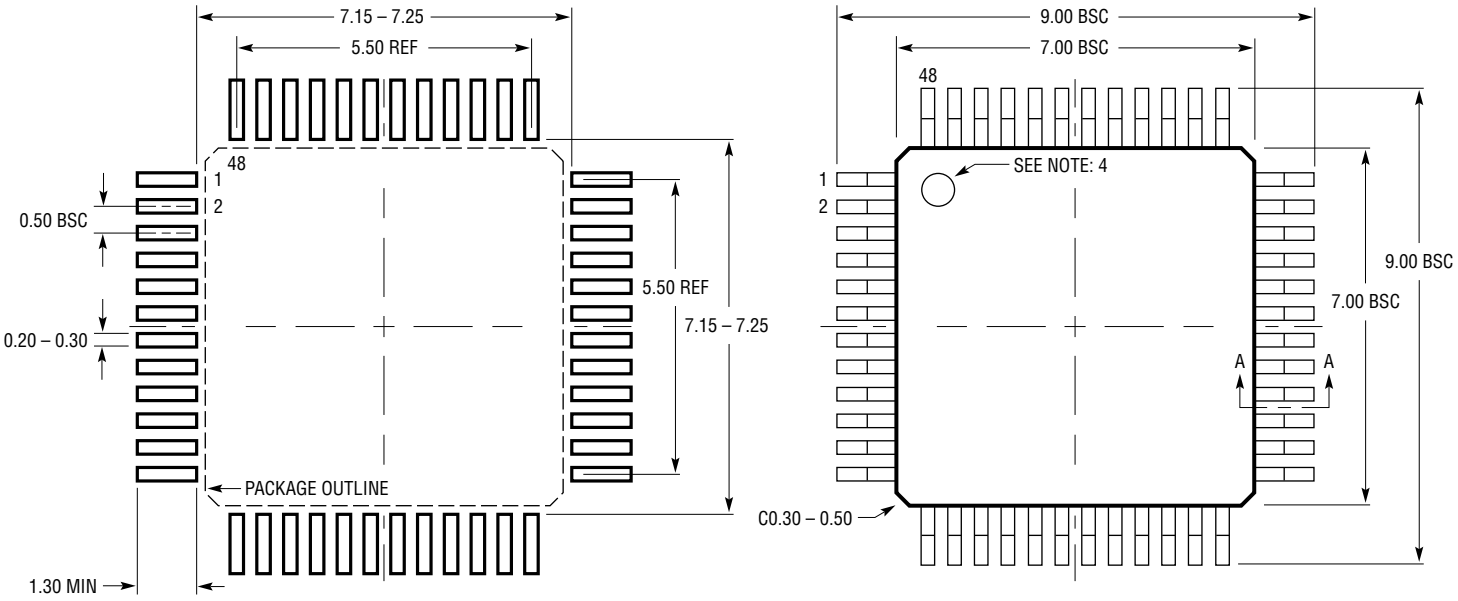
Reference Design

For a detailed look at the reference design for this converter, including schematics and PCB layout, please refer to DC2094A, the evaluation kit for the LTC2348-18.

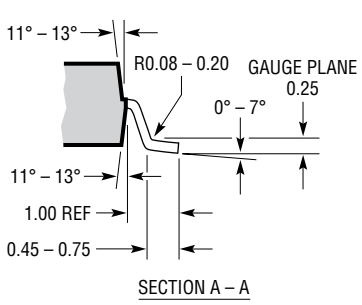
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC2348-18#packaging for the most recent package drawings.

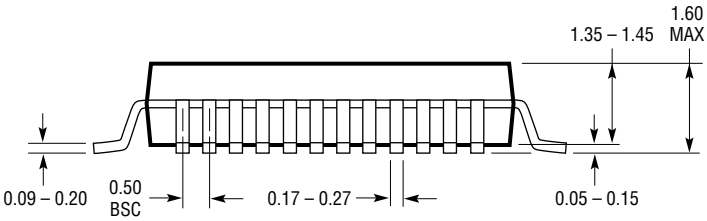
LX Package
48-Lead Plastic LQFP (7mm × 7mm)
(Reference LTC DWG # 05-08-1760 Rev A)

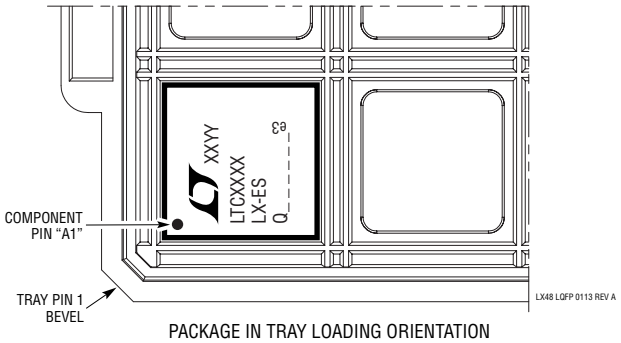


RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



SECTION A – A





PACKAGE IN TRAY LOADING ORIENTATION

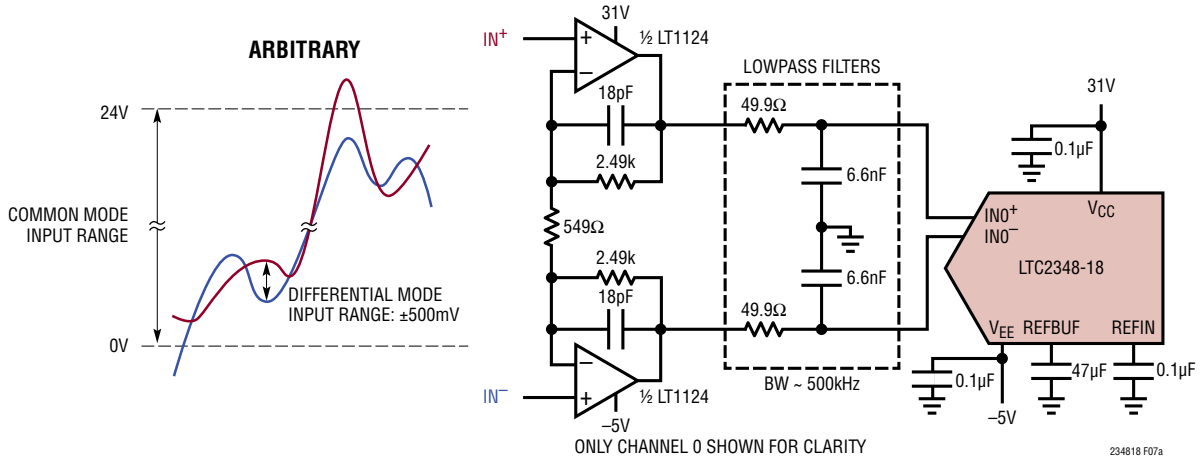
NOTE:
1. PACKAGE DIMENSIONS CONFORM TO JEDEC #MS-026 PACKAGE OUTLINE
2. DIMENSIONS ARE IN MILLIMETERS
3. DIMENSIONS OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.25mm ON ANY SIDE, IF PRESENT
4. PIN-1 INDENTIFIER IS A MOLDED INDENTATION, 0.50mm DIAMETER
5. DRAWING IS NOT TO SCALE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	02/16	Updated the ADC Timing Characteristics section	6
		Inserted new graphs: PSRR vs Frequency and Power Dissipation vs Sampling Rate	12
		Updated Table 2	22
		Updated the Application Information section	24
		Updated Figure 16	30
		Updated Table 3	33
		Updated the Board Layout section	37

TYPICAL APPLICATION

Digitize Differential Signals Over a Wide Common Mode Range



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC2348-16	16-Bit, 200ksps, 8-Channel Simultaneous Sampling, ±1LSB INL, Serial ADC	±10.24V SoftSpan Inputs with Wide Common Mode Range, 94db SNR, Serial CMOS and LVDS I/O, 7mm × 7mm LQFP-48 Package
LTC2378-20/LTC2377-20/ LTC2376-20	20-Bit, 1Msps/500ksps/250ksps, ±0.5ppm INL Serial, Low Power ADC	2.5V Supply, ±5V Fully Differential Input, 104dB SNR, MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2338-18/LTC2337-18/ LTC2336-18	18-Bit, 1Msps/500ksps/250ksps, Serial, Low Power ADC	5V Supply, ±10.24V Fully Differential Input, 100dB SNR, MSOP-16 Package
LTC2328-18/LTC2327-18/ LTC2326-18	18-Bit, 1Msps/500ksps/250ksps, Serial, Low Power ADC	5V Supply, ±10.24V Pseudo-Differential Input, 95dB SNR, MSOP-16 Package
LTC2373-18/LTC2372-18	18-Bit, 1Msps/500ksps, 8-Channel, Serial ADC	5V Supply, 8 Channel Multiplexed, Configurable Input Range, 100dB SNR, DGC, 5mm × 5mm QFN-32 Package
LTC2379-18/LTC2378-18/ LTC2377-18/LTC2376-18	18-Bit,1.6Msps/1Msps/500ksps/250ksps, Serial, Low Power ADC	2.5V Supply, Differential Input, 101.2dB SNR, ±5V Input Range, DGC, Pin Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2380-16/LTC2378-16/ LTC2377-16/LTC2376-16	16-Bit, 2Msps/1Msps/500ksps/250ksps, Serial, Low Power ADC	2.5V Supply, Differential Input, 96.2dB SNR, ±5V Input Range, DGC, Pin Compatible Family in MSOP-16 and 4mm × 3mm DFN-16 Packages
LTC2389-18/LTC2389-16	18-Bit/16-Bit, 2.5Msps, Parallel/Serial ADC	5V Supply, Pin-Configurable Input Range, 99.8dB/96dB SNR, Parallel or Serial I/O 7mm × 7mm LQFP-48 and QFN-48 Packages
LTC1859/LTC1858/ LTC1857	16-/14-/12-Bit, 8-Channel, 100ksps, Serial ADC	±10V, SoftSpan, Single-Ended or Differential Inputs, Single 5V Supply, SSOP-28 Package
LTC1609	16-Bit, 200ksps Serial ADC	±10V, Configurable Unipolar/Bipolar Input, Single 5V Supply, SSOP-28 and SO-20 Packages
DACs		
LTC2756/LTC2757	18-Bit, Serial/Parallel I_{OUT} SoftSpan DAC	±1LSB INL/DNL, Software-Selectable Ranges, SSOP-28/7mm × 7mm LQFP-48 Package
LTC2668	16-Channel 16-/12-Bit ±10V V_{OUT} SoftSpan DACs	±4LSB INL, Precision Reference 10ppm/°C Max, 6mm × 6mm QFN-40 Package
References		
LTC6655	Precision Low Drift Low Noise Buffered Reference	5V/2.5V/2.048V/1.25V, 2ppm/°C, 0.25ppm Peak-to-Peak Noise, MSOP-8 Package
LTC6652	Precision Low Drift Low Noise Buffered Reference	5V/2.5V/2.048V/1.25V, 5ppm/°C, 2.1ppm Peak-to-Peak Noise, MSOP-8 Package
Amplifiers		
LT1468/LT1469	Single/Dual 90MHz, 22V/µs, 16-Bit Accurate Op Amp	Low Input Offset: 75µV/125µV
LT1354/LT1355/LT1356	Single/Dual/Quad 1mA, 12MHz, 400V/µs Op Amp	Good DC Precision, Stable with All Capacitive Loads
LT1357/LT1358/LT1359	Single/Dual/Quad 2mA, 25MHz, 800V/µs Op Amp	Good DC Precision, Stable with All Capacitive Loads

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