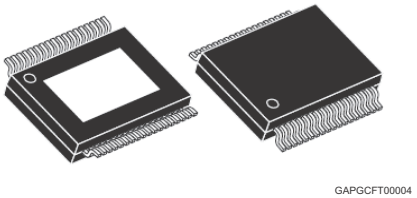
L99CL01XP

8 channel high-side LED driver for automotive applications

Datasheet - production data



PowerSSO-36

Applications

- Automotive interior lighting
- Automotive exterior lighting

Description

The L99CL01XP is designed to provide a cost effective solution for exterior and interior automotive lighting applications with LEDs.

Features

- Octal fully protected high-side switches with programmable overcurrent threshold and RDSON
- Split supply for flexible application assignment (6 V to 24V)
- SPI communication interface with daisy chain capability
- Digital diagnosis individually for each switch
- Analogue current sense output with SPI programmable multiplexer
- Integrated synchronous PWM module with programmable phase shift, pulse skipping feature and quick access via direct drive pins
- Improved EMC behavior by phase shift control and output edge shaping
- Limp home function with 6 independent direct drive pins
- Integrated fail mode handling
- Ultra low power mode (< 5 µA max at 25°C)

Table 1. Device summary

Package	Order code	
	Tube	Tape and real
PowerSSO-36	Root part number 1	L99CL01XPTR

Contents

List of tables

List of figures

1 Block diagram and pin description

Figure 1. Application block diagram

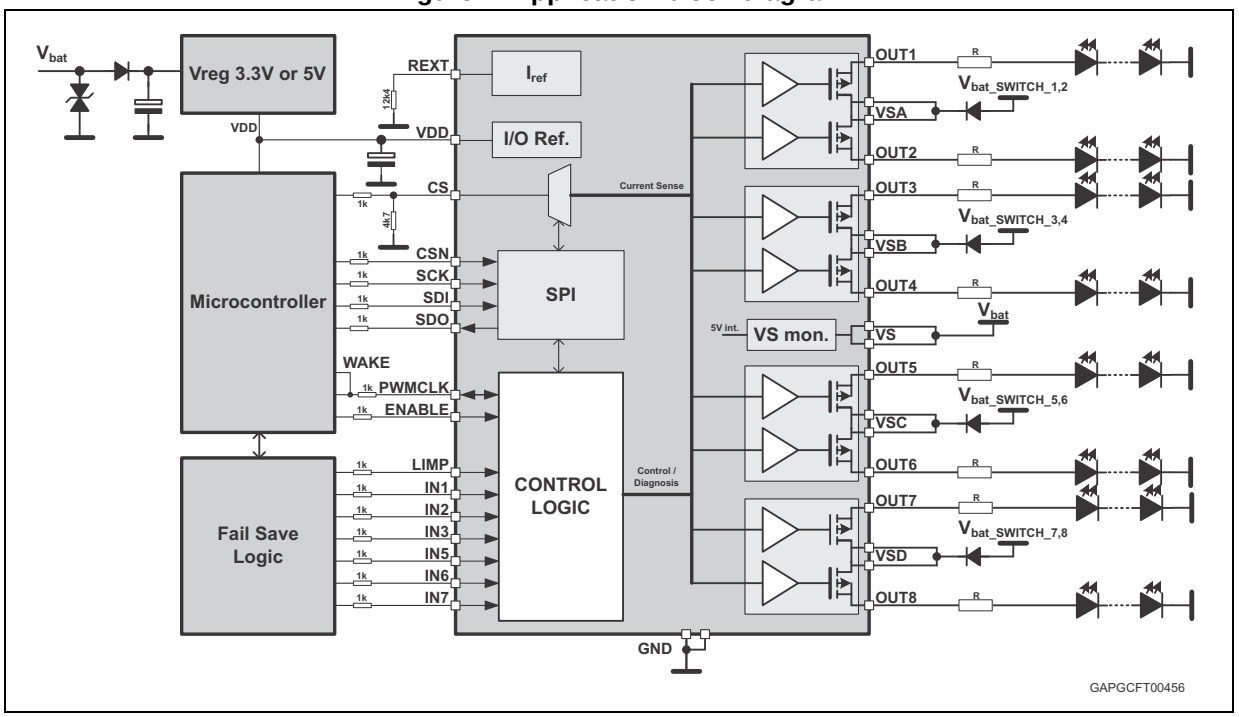


Figure 2. Device block diagram

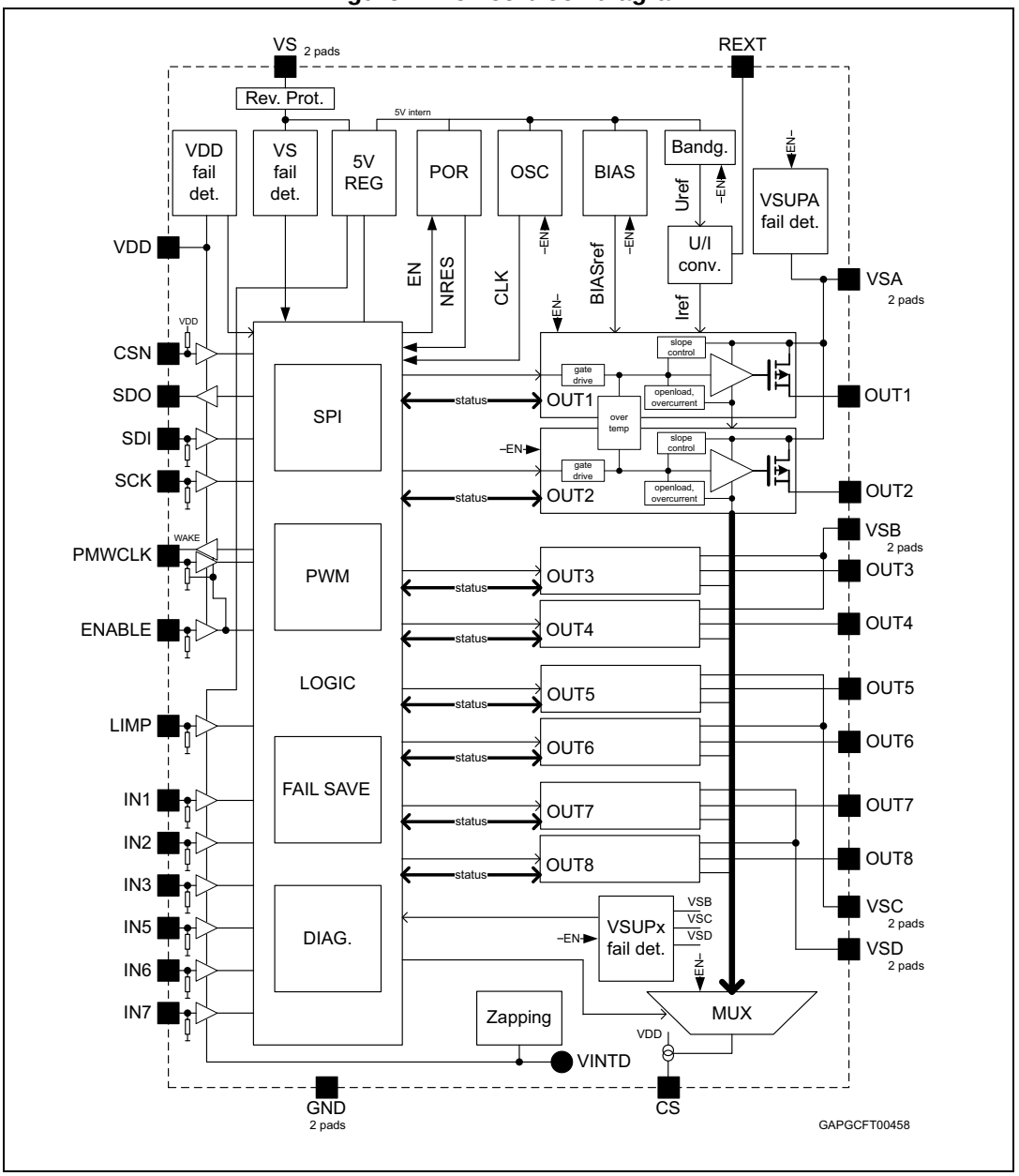


Figure 3. Configuration diagram (top view)

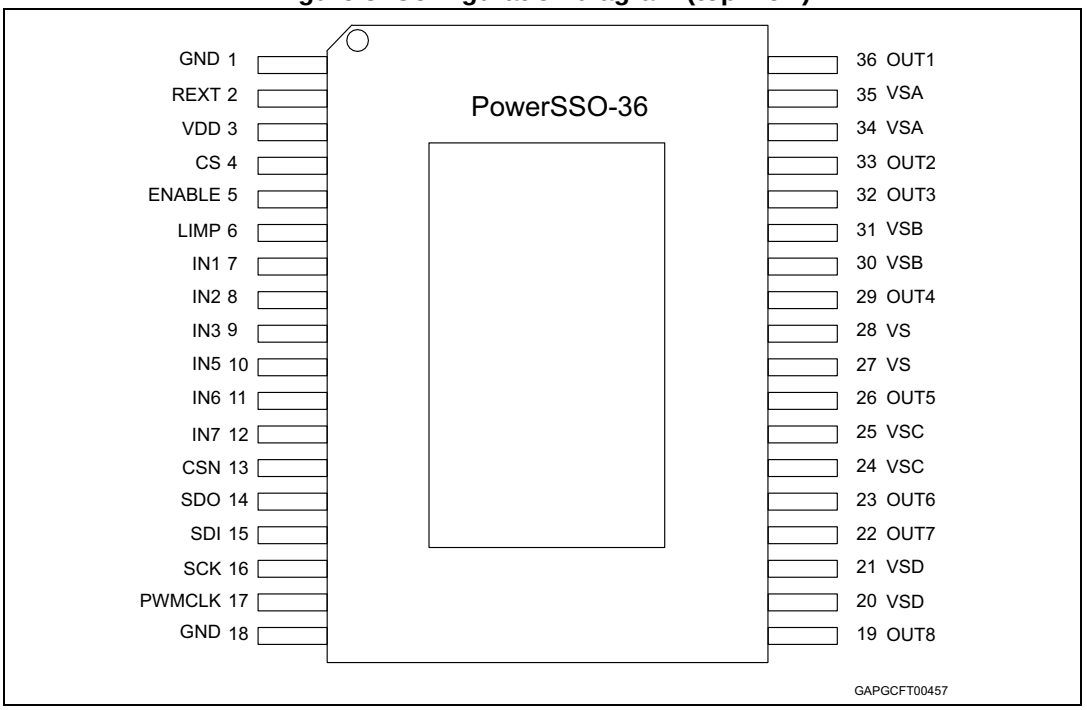


Table 2. Pin function

Pin	Symbol	Function
1,18	GND	Ground: This terminal is the ground for the logic and analogue circuitry of the device.
2	REXT	External Resistor: The Resistor is used to improve internal current precision.
3	VDD	Logic supply voltage: SPI and logic I/O structure power supply.
4	CS	Current sense output: This terminal is used to supply a current proportional to the output current in the power output stages. The selection of the output is SPI programmable.
5	ENABLE	Enable (active high): This input enables the device. After wakeup the internal configuration is in default state. The terminal has an internal pull down resistor.
6	LIMP	Limp home input (active high): The fail mode of the component can be activated by logic [1] at this input. The LIMP state is internally filtered by a 10ms digital filter. This terminal has an internal pull down resistor.
7,8, 9,10, 11,12	IN1, IN2, IN3, IN5, IN6, IN7	Direct Drive input 1,2,3,5,6,7: These inputs enable the device and are used to control the corresponding power outputs 1,2,3,5,6,7 in case of fail mode (direct drive). During normal mode the control of the outputs is SPI programmable. All input terminals have an internal pull down resistor.

Table 2. Pin function (continued)

Pin	Symbol	Function
13	CSN	SPI chip select input (active low): When this digital signal is logical [1], SPI signals are ignored. Asserting this terminal [0] an SPI transaction starts. The transaction is indicated as complete when this signal returns to [1]. This terminal has an internal pull up resistor.
14	SDO	SPI data-out: SPI data is sent to the microcontroller by this terminal. This data output changes on the positive edge of SCLK. When CSN is [1], this terminal is at high impedance.
15	SDI	SPI data-in: This data input is sampled on the negative edge of the SCK. The terminal has an internal pull down resistor.
16	SCK	SPI clock input: This digital input terminal is connected to the controller providing the clock (up to 4MHz) for SPI communication. The terminal has an internal pull down resistor.
17	PWMCLK	PWM clock input, (WAKE output if ENABLE low): This clock defines the frequency of the internal generated PWM. The terminal has an internal pull down resistor. If ENABLE is low, this pin is used as a WAKE output. This output indicates if another wakeup source, beside ENABLED, is active.
19, 22, 23, 26, 29, 32, 33, 36	OUT1 ~ OUT8	Power output 1~8: Fully protected high-side switches with individually programmable R_{DSON} and over current shutdown threshold. The output current is up to 1A per channel. However the total current of the device is limited due to the max power dissipation of the component and the total thermal resistance/capacitances of the PCB. The outputs OUT1~OUT3 and OUT5~OUT7 are controlled by the corresponding inputs IN1, IN2, IN3, IN5, IN6, IN7 during fail mode (OUT4 and OUT8 are off). During normal mode the outputs are controlled by the internal PWM generator or the selected direct drive input.
20, 21	VSD	Supply voltage pins for outputs 7 and 8. Pins must be tied together on PCB.
24, 25	VSC	Supply voltage pins for outputs 5 and 6. Pins must be tied together on PCB.
27, 28	VS	Battery supply voltage: Power supply terminal.
30, 31	VSB	Supply voltage pins for outputs 3 and 4. Pins must be tied together on PCB.
34, 35	VSA	Supply voltage pins for outputs 1 and 2. Pins must be tied together on PCB.

Note: The Heat Slug is internally connected to GND.

1.1 Power supply (VS, GND)

The VS terminal is the power supply pin of the device and it is also used to supply the internal logic of the device. This pin is protected against reverse battery conditions without any external components, down to -24 V.

Overvoltage and undervoltage events on the VS pin are reported by the OVF, respectively the UVF status bits (refer to Device Status #2). Once one of these events has occurred, the corresponding status bit is latched.

The GND is the signal ground and power ground terminal of the device.

1.2 VDD (logic interface supply voltage)

The VDD is the logic interface supply voltage terminal, used to supply the SPI communication interface and logic I/Os of the device.

The VDD is monitored by an internal circuitry. In case an under voltage condition is detected, the L99CL01XP enters the Fail Mode after the filter time t_{VDD_UV}.

1.3 ENABLE (active high)

The ENABLE is used to enable the device by the microcontroller (normal mode).

When the ENABLE input is

- logic [0] the device is in standby mode (WAKE output enabled)
- logic [1] the device is in active mode (PWMCLK input enabled)

ENABLE has an internal pull down resistor.

Please check for other wakeup sources the *Section 2.4: Control inputs (IN1, IN2, IN3, IN5, IN6, IN7)*.

2 Functional description

2.1 Switch supply terminals (VSA, VSB, VSC and VSD)

The device has four groups of output supplies in order to achieve flexible application fuse assignment. The VSA terminal is the drain (power supply pin) of the output switches 1 and 2, while VSB is the supply of switches 3 and 4, VSC is the supply of switches 5 and 6 and VSD is the supply of switches 7 and 8. The supply pins belonging to the same supply group must be connected together in order to ensure proper current capability for PowerMOS devices.

Overvoltage and undervoltage events on the VSX pins are reported by the corresponding OVF_X, respectively the UVF_X status bits (refer to Device Status #3). Once one of these events has occurred, the corresponding status bit is latched, the corresponding outputs are latched off and the OUTENx (see control register OUT enable, #10) is set to 0.

The device is fully protected against loss of any supply terminal.

2.2 Power Outputs [OUT1 ~ OUT8]

The power outputs are used to control LED arrays with either integrated current source or series resistors.

Each output offers a fully protected p-channel MOSFET (programmable Ron) driver with digital switch diagnosis and analogue current sense circuitry. Paralleling of two or more outputs is possible in order to reduce power dissipation without restriction in performance.

The outputs are protected against:

- output over load and short circuit (incl. very low resistive short circuit and shorts with line inductance)
- overtemperature
- overvoltage/undervoltage

The digital switch diagnosis by SPI communication (see *Section 3.1.6: Status Data Registers*) contains reporting of

- overcurrent shutdown status
- overtemperature shutdown status incl. over temperature warning status
- undervoltage/overvoltage status

In case of undervoltage, thermal shutdown or overcurrent the corresponding OUT is switched off with edge shaping to reduce internal power dissipation in case of hard short.

In normal mode, after a thermal shutdown, an overcurrent, an undervoltage or overvoltage at VSA, VSB, VSC or VSD, the corresponding outputs are latched off until a read and clear command of the corresponding status register is sent.

In fail mode, an overtemperature of an output leads to a latch off, whereas, an auto restart strategy is implemented after an overcurrent, an undervoltage or overvoltage at VSA, VSB, VSC or VSD.

2.3 Current Sense (CS) – analog diagnosis

The current sense terminal delivers a current which is proportional to the output current. Depending on the programmed R_{DSON} [#9] (see *Section 3.1.5: Control Data Registers (CDR)*) the ratio is defined to I_{OUT}/1000 for 1 Ω and I_{OUT}/2000 for 600mΩ.

The MUX[2:0] bits select which output channel is connected to the CS pin [#0:D7~D4] (see *Section 3.1.5: Control Data Registers (CDR)*).

Fast output settling is provided in order to enable processing with synchronous sampling and peak detector as well as diagnosis at very small duty cycle.

2.4 Control inputs (IN1, IN2, IN3, IN5, IN6, IN7)

The control inputs are used to

- provide wakeup capability (see *Section 3.2.2: Wake up and operating modes*).
- directly control the corresponding outputs during fail mode (see *Section 3.2.5: Fail Mode*).
- control the outputs during normal mode, when the output control is enabled by SPI register [#11, #12 and #13]. By default, the Control Inputs (INx) are disabled. For more detail see *Section 2.7.2: PWM module*.

The inputs have internal pull down resistors.

2.5 PWMCLK input / wake output pin

2.5.1 PWMCLK input

When the device is enabled with the ENABLE pin to logic ‘1’, the pin acts as an input with which the PWM frequency is generated from PWMCLK terminal by the integrated PWM module (see *Section 2.7.2: PWM module*).

The clock input frequency is the factor 256 of the PWM switching frequency. (f_{PWM}=100Hz…400Hz=>f_{CLK}=25.6kHz…102.4kHz). Therefore the internal PWM module provides an 8-bit resolution PWM.

The PWM module is disabled in case of PWMCLK failure and the outputs are set according to the OUTxEN control bits (control register #10). The status bit PCLKF is set (Status register #3, bit3). This bit is latched until a Read and Clear command is sent to this register.

A PWMCLK failure is detected when the frequency at the PWMCLK input is lower than 5kHz ($t_{pos\_lock\_edge}$+1 - $t_{pos\_lock\_edge}$ > 1/5kHz => failure). This failure is reported in the SPI register [#1:D3] (see *Section 3.1.6: Status Data Registers*).

The input terminal has an internal pull down resistor.

2.5.2 WAKE output

When the device is not enabled via the ENABLE, this pin is used as an output to indicate the wake state of the device which is related to the INx pins.

[0] no wakeup source detected

[1] INx wakeup source detected or 2sec wake timer running

2.6 Limp input

The fail mode (limp home mode) of the component is activated by this digital input port in addition to the internal fail mode detection circuit of the device (see *Section 3.2.5: Fail Mode*).

The limp home mode is activated by a logic [1] signal at the input. During limp home mode the outputs are directly controlled by the inputs IN1, IN2, IN3, IN5, IN6, IN7. and the PWM module is disabled.

The limp input has an internal pull down resistor.

2.7 Control, protection and diagnosis

2.7.1 Smart switches and gate drivers

The smart switches are controlled by dedicated gate driver including:

- Output pulse shaping
- Overload protection incl. protection against low resistive short circuit and shorts with line inductance
- Over temperature protection incl. over temperature warning signals

The outputs are switched with active pulse shaping to provide an excellent EMC performance of the system.

Therefore the output current of each driver is monitored by a feedback loop in order to control the switching speed of the output. Thereby a compromise between edge shaping and propagation delay of the switch is necessary to achieve low duty cycle values (3% < dc < 97% @ 250Hz).

2.7.2 PWM module

PWM control

In order to minimize the microcontroller's work load, a synchronous PWM module is integrated. The frequency and timing is derived from the PWMclock input (see *Section 2.5.1: PWMCLK input*), the control of the PWM module is provided by SPI and INx (see *Section : PWM control*)

The smart switches can be controlled in the range of 0%...100% with a resolution of 1/256%. The value 00h in the Individual and Global PWM registers refers to OFF state, the value FFh refers to 255/256 ON state of the switches. The PWM timing includes 4 programmable switching phases (0°, 90°, 180° and 270°). The phase can be controlled individually for each channel depending on the channel control registers [#1~#8 D10~D9]

The synchronization of the switching phases between different devices is provided by the PWMsync bit in Initialisation register [#0:D8].

To guarantee a proper generation and smooth PWM duty cycle change via SPI the duty cycle start point is defined by the internal PWM counter zero crossing. Therefore every SPI programmed duty cycle change and duty cycle source change will not take effect till the PWM counter zero crossing is reached (this strategy is also known as buffered PWM). Setting the output to OFF or 100% ON, the setting will occur immediately and independently from PWM counter.

For generation of output duty cycles close to 100% the pulse skipping feature is integrated (see *Pulse skipping feature*).

The PWM module is disabled in case of

- fail mode (direct drive)
- clock input signal failure (controlled by PWMxEN register)

PWM module in normal mode with OUTENx bit = 1

This section describes the PWM control modes for OUT1-8, provided that the corresponding OUTENx bit is set (OUTx is enabled).

If OUTENx bit = 0, the corresponding output is disabled.

PWM control modes in normal mode for OUTx (x = 1, 2, 3, 5, 6 or 7)

In normal mode, the state of the OUTx, x=1,2,3,5,6 or 7 is determined by the combinations between INSELx[1:0], PWMSELx[1:0] and the state of INx, provided that OUTENx bit is set to 1.

3 cases must be considered:

- Case 1: direct input INx is disabled (INSELx[1:0] = [0,0])
- Case 2: direct input INx is enabled (INSELx[1:0] ≠ [0,0]) and INx = Low
- Case 3: direct input INx is enabled (INSELx[1:0] ≠ [0,0]) and INx = High

Case 1: INx is disabled: The output behaves according to the *Table 3*.

Table 3. PWM mode selection for OUTx (x = 1, 2, 3, 5, 6 or 7) when INx is disabled

OUTENx	INx	INSELx1	INSELx0	PWMSELx1	PWMSELx0	State of OUTx x = 1, 2, 3, 5, 6 or 7
1	X(1)	0	0	0	0	Individual PWM
1	X	0	0	0	1	GPWM1
1	X	0	0	1	0	GPWM2
1	X	0	0	1	1	100% ON

1. X: do not care.

- Individual PWM selected:

  In this mode the PWM control of the channels is provided individually for each channel by the corresponding channel control register [#1~#8:D7~D0].
- GPWM1 selected:

  in this mode the PWM control of the switches is provided by the global PWM1 value [#14:D7~D0].
- GPWM2 selected:

  in this mode the PWM control of the switches is provided by the global PWM2 value [#15:D7~D0].
- 100% ON selected:

  In this mode the output is fully on.
- OFF selected:

  In this mode the output is OFF.

Case 2: direct input INx is enabled (INSELx[1:0] ≠ [0,0]) and INx = Low

In this case, the state of the output is independent from the settings of PWMSELx[1:0]. It is determined only by setting of INSELx[1:0] according to the *Table 4*.

Table 4. PWM mode selection for OUTx (x = 1, 2, 3, 5, 6 or 7) when INx is enabled and INx = 0

INx	INSELx1	INSELx0	PWMSELx1	PWMSELx0	State of OUTx x = 1, 2, 3, 5, 6 or 7
Low	0	1	X(1)	X	GPWM1
Low	1	0	X	X	GPWM2
Low	1	1	X	X	OFF

1. X: do not care.

Case 3: direct input INx is enabled (INSELx[1:0] ≠ [0,0]) and INx = High

If the direct input INx is High, the state of the output is independent from the settings of INSELx[1:0]. It is determined only by the setting of PWMSELx[1:0] according to the *Table 5*.

Table 5. PWM mode selection for OUTx (x = 1, 2, 3, 5, 6 or 7) when INx is enabled and INx = 1

OUTxEN	INx	INSELx1	INSELx0	PWMSELx1	PWMSELx0	State of OUTx x = 1, 2, 3, 5, 6 or 7
1	High	X(1)	X	0	0	Individual PWM
1	High	X	X	0	1	GPWM1
1	High	X	X	1	0	GPWM2
1	High	X	X	1	1	100% ON

1. X: do not care, provided that INSELx[1:0] is different from [0,0]

Table 6 and *Table 7* show some examples of SPI settings resulting in states of OUTx, which are independent (*Table 6*) or dependent (*Table 7*) from the levels at INx. Other settings are possible.

Table 6. Examples of settings for INSELx[1:0] and PWMSELx[1:0] resulting in OUTx states, which are independent from INx

OUTxEN	INx	INSELx1	INSELx0	PWMSELx1	PWMSELx0	State of OUTx x = 1, 2, 3, 5, 6 or 7
0	X(1)	X	X	X	X	OFF
1	X	0	0	1	1	100% ON
1	X	0	0	0	0	Individual PWM
1	X	0	1	0	1	GPWM1
1	X	1	0	1	0	GPWM2

1. X: do not care.

Table 7. Examples of settings for INSELx[1:0] and PWMSELx[1:0] resulting in OUTx states, which are dependent from INx.

OUTxEN	INSELx1	INSELx0	PWMSELx1	PWMSELx0	State of OUTx x = 1, 2, 3, 5, 6 or 7
1	1	1	0	0	(Individual PWM) AND (INx)
1	1	1	0	1	(GPWM1) AND (INx)
1	1	1	1	0	(GPWM2) AND (INx)
1	1	1	1	1	According to INx

PWM control modes in normal mode for OUTx, x = 4 or 8, if OUTENx = 1

OUT4 and OUT8 do not have any direct input or INSELx[1:0] control bits. In normal mode, their behaviour is only determined by the control registers PWMSEL4[1:0] and PWMSEL8[1:0], according to the following table:

Table 8. PWM mode selection for OUT4 and OUT8

PWMSELx1	PWMSELx0	State of OUTx x = 4 or 8
0	0	Individual PWM
0	1	GPWM1
1	0	GPWM2
1	1	100% ON

Pulse skipping feature

Due to the output pulse shaping feature and the thereof resulting propagation delay time of the smart switches, the duty cycle range close to 100% can not be generated by the device. Therefore the pulse skipping feature (PSF) is integrated to generate this output duty cycle range in normal mode.

The pulse skipping consists of fixed duty cycle patterns with 8 PWM cycles.

When the corresponding PSF bit [#1~#8:D8] is set, the PWM values 97.25%...99.61% (C3h…C7h) are generated individually for each channel by modulation of the duty cycle in discrete steps by the pulse skipping logic according to the following table:

Table 9. Duty cycle selection (PSF enabled)

Duty Cycle (%)	HEX (9bit)	#1	#2	#3	#4	#5	#6	#7	#8
100.00%	0x100	256	256	256	256	256	256	256	256
99.61%	0x0FF	248	256	256	256	256	256	256	256
99.22%	0x0FE	248	256	256	256	248	256	256	256
98.82%	0x0FD	248	248	256	256	256	248	256	256
98.43%	0x0FC	248	248	256	256	248	248	256	256
98.04%	0x0FB	248	248	248	256	256	248	248	256

Table 9. Duty cycle selection (PSF enabled) (continued)

Duty Cycle (%)	HEX (9bit)	#1	#2	#3	#4	#5	#6	#7	#8
97.65%	0x0FA	248	248	248	256	248	248	248	256
97,25%	0x0F9	248	248	248	248	248	248	248	256

The PSF is started with the next PWM cycle after SPI communication. The start step number can not be guaranteed. In reset condition PSFx = [0], the pulse skipping feature is disabled.

The PSF is not available in Fail Mode.

2.7.3 Overcurrent detection

The over current shutdown threshold (I_{OC}) combined with the R_{DSON} can be programmed individually for each switch in two different levels by SPI command Mode Control [#9: D7~D0] (see *Section 3.1.5: Control Data Registers (CDR)*):

- when RON bit is [0] the over current shutdown threshold is 1.5 A and the R_{DSON} is 600 mΩ
- when RON bit is [1] the over current shutdown threshold is 750 mA and the R_{DSON} is 1 Ω

The setting of the RON bits can be monitored by SDO register Mode Control [#9:D7~D0] (see *Section 3.1.6: Status Data Registers*).

In case of overcurrent failure the corresponding OUTxEN bit is automatically reset and the corresponding OCx status bit is set. This bit is latched once an OC event is detected.

To reset the diagnosis register, the condition has to be removed and an SPI read and clear operation of the corresponding register has to be performed.

2.7.4 External resistor

To achieve the precise internal slope control and timings, an accurate external resistor is needed.

The resistance has to be 12.4 kΩ (1% tolerance) connected to GND.

If the resistor is removed or shorted, an RFAIL failure is reported via SPI [#1:D2] (see *Section 3.1.6: Status Data Registers*).

2.7.5 Channel voltage level comparator

In addition to the digital diagnosis a multiplexed channel OUT voltage comparator is implemented. The compared threshold is 5 V.

The channel is selected via the MUXEN and the MUX2:1 bits in the Control Data Register [#0:D7:4]. The OUTL bit can be found in the Status Data Registers [#5,#6,#7,#8:D7].

2.7.6 Device protection

A protection strategy enables light functionality even in case of failures inside the component of the light module.

Therefore the component is protected against

- loss of any supply line
- loss of communication interface and PWMCLK fail

Reverse polarity protection

VS has an integrated active reverse polarity protection. VSA, VSB, VSC and VSD have to be protected against reverse polarity by using external protection devices (i.e. series diodes) in the battery supply lines.

Loss of supply lines

The device is protected against loss of any supply line.

During loss of

- VS: the device can not drive any loads, and no communication via SPI is possible. The Device is in Power Down Mode (refer to *Figure 4: State diagram*). When a valid VS voltage is applied again, the content of the registers are set to their default value. This event is reflected in the Reset bit, at the first SPI access.
- VSA, VSB, VSC or VSD: the device can not drive the corresponding load group, but sends UVF_A / UVF_B / UVF_C or UVF_D flag via SPI to the microcontroller.
- VDD: if the condition VDD < VDDUV is present for more than t_{VDDUV}, the device enters in Fail Mode. The refreshing of the WD is disabled as long as VDD < VDDUV.

All I/O lines have to be protected by external series resistors.

Loss of communication interface

The following failures are considered as a loss of SPI communication: loss of SCK or CSN, or CSN is stuck to High or Low. These failures are detected by the monitoring of the WD bit. In case of WD time-out, the device enters Fail Mode and the failure is reported by the status bit WDCERR (#1,bit 1).

Note: A short circuit of CSN to Low for a duration exceeding CSN time-out, additionally causes SDO to go in tri-state, in order to avoid a blocking of the whole SPI bus.

If SDI stuck to High of Low, or if the number of SCK cycles is not a multiple of 16, during a SPI transaction, the device directly enters Fail Mode. Moreover the status register SPIF is set (#1, bit 5).

Logic Input supervision

The logic inputs are supervised by the device with different check strategies and consequential failures:

Table 10. Error handling

Input/Output	Signal check strategy	System failure reaction
PWM Clock	frequency too low	No PWM feature a PWMCLK Fail is reported
SPI	WD bit time-out	Fail Mode
SPI	SDI, SCK, CSN stuck at High or Low	Fail Mode
SPI	SCK fail	Fail Mode

3 SPI interface

A 16 bit SPI interface (f_{max} = 2 MHz) is used for control and diagnosis of the component.

The SPI offers daisy-chain-capability to provide high data rate, minimum circuit overheads and overall synchronization of multiple PWM modules.

During each SPI cycle a 16 bit word is transferred into the control register of each device and a 16 bit word is received from each device.

The data includes the toggling of a watchdog bit, which indicates the proper operation of the SPI interface. The watchdog bit has to be toggled by every SPI access starting after reset with ‘0’.

3.1 SPI communication

3.1.1 CSN (chip select (active low))

The CSN terminal enables the SPI communication with the microcontroller:

- the SDO output driver is enabled
- the device status data is latched to the output shift registers on the falling edge of the CSN
- the input shift register data is latched into the addressed registers on the rising edge of CSN

CSN has an internal pull up resistor and a CSN timeout is implemented. If CSN is kept low for a duration, which is longer than t_{CSN} time-out, the incoming frame is considered as invalid and the SDO goes to tri-state. The CSN time-out avoids that a short circuit of CSN to GND blocks the SPI bus.

3.1.2 SCK (serial input clock)

The SCK terminal clocks the internal shift registers of the device.

The SDI terminal accepts data into the input shift register on the falling edge of the SCK signal, while the SDO terminal shifts output data to the SDO line driver on the rising edge of the SCK signal (MCU setting: CPHA = 1; CPOL = 0).

The SCK terminal has to be in logic [0] state whenever CSN makes any transition.

When CSN is logic [1] state, signals at the SCK and SDI inputs are ignored and SDO driver output is in tri-state condition (high impedance). The L99CL01XP requires a number of SCK cycles, which is a multiple of 16, during an SPI transaction. If this condition is not met, the device enters Fail Mode.

SCK has an internal pull down resistor.

3.1.3 SDI (serial data input)

The SDI pin is the data input terminal of the SPI communication interface.

The input has an internal pull down resistor. Writing all [0] or all [1] to SDI within one SPI frame will generate an SPI fail (stuck @ error).

The implemented SPI requires a 16 bit stream of serial data, starting with D15 and ending with D0.

3.1.4 SDO (serial data output)

The SDO pin is the data output terminal of the SPI communication interface.

The SDO terminal is in tri-state condition unless CSN input is in logic [0] state. When CSN is in logic [0] state, the data from the output shift registers is sent via the SDO pin.

The SDO terminal changes the state at the rising edge of the SCK input and reads out on the falling edge of SCLK.

3.1.5 Control Data Registers (CDR)

The data sent to the device will be latched into the internal Control Registers with the rising edge of CSN after a valid SPI cycle is performed.

The written data can be read back by setting the RAMREAD bit D9 in the Initialization register #0. After Reset all registers are by default [0] (except SDOA0 is [1]).

CDR base address = 0x00h

The CDR register are shown in *Table 11: CDR registers*

Table 11. CDR registers

Register	Address offset	Reset value
Initialization Register	0x00h	0x0001h
Address #1-#8 CHx control		
Address #1 CHx control	0x01h	0x1000h
Address #2 CHx control	0x02h	0x2000h
Address #3 CHx control	0x03h	0x3000h
Address #4 CHx control	0x04h	0x4000h
Address #5 CHx control	0x05h	0x5000h
Address #6 CHx control	0x06h	0x6000h
Address #7 CHx control	0x07h	0x7000h
Address #8 CHx control	0x08h	0x8000h
Address #9 mode control	0x09h	0x9000h
Address #10 OUT enable	0x0Ah	0xA001h
Address #11 PWMSEL / INSEL CH1 + CH2	0x0Bh	0xB000h
Address #12 PWMSEL / INSEL CH3 + CH4 + CH5	0x0Ch	0xC001h
Address #13 PWMSEL / INSEL CH6 + CH7 + CH8	0x0Dh	0xD000h
Address #14 Global PWM1	0x0Eh	0xE000h
Address #15 Global PWM2	0x0Fh	0xF000h

Initialization Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address				WD	NO CLEAR	RAM READ	PWMsync	MUXEN	MUX2	MUX1	MUX0	SOA3	SOA2	SOA1	SOA0
R				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: Base address + 0x00h

Type: R, R/W

Reset: 0x0001h

Note: Writing all [0] to this register will generate a SPI fail (stuck @ '0').

Bit 15:12 Address

Bit 11 WD: Watchdog toggle bit (75ms, start with [0] after Reset, toggled with every SPI access)

Bit 10 NOCLEAR: With this bit set to:

0: every read access clears the read out status bits

1: any reported status from the read and clear flags are not cleared by a read

The clear of the read and clear flags will be re-enabled by writing a [0] to this bit.

Bit 9 READRAM: With this bit set to:

0: the addressed status data register (see *Section 3.1.4: SDO (serial data output)*) is sent back via SDO

1: the addressed control data register is sent back via SDO. This is to verify the written data in the device.

Note: The read back of the Status Data Registers will be re-enabled by writing a [0] to this bit.

Bit 8 PWMsync: internal PWM counter reset. Writing a '1' to this Register will reset the internal PWM counter after valid SPI command and CSN high. This bit is automatically reset after synchronization.

Bit 7 MUXEN: Enable current sense output and the OUT voltage level comparator

0: CS pin disabled / OUT voltage comparator disabled (default)

1: CS pin enable / OUT voltage comparator enabled (see MUX[2:0]) setting

Bit 6:4 MUX[2:0]: Binary decoded selection of current sense output and the OUT voltage level comparator
000: Channel 1 selected (default
001: Channel 2 selected
010: Channel 3 selected
011: Channel 4 selected
100: Channel 5 selected
101: Channel 6 selected
110: Channel 7 selected
111: Channel 8 selected

Bit 3:0 SDOA[3:0]: Address of next SDO data word (also see READRAM bit)
0000: READRAM = 0: Address #1 selected, else Address #0
0001: Address #1 selected (default)
0010: Address #2 selected
0011: Address #3 selected
0100: Address #4 selected
0101: Address #5 selected
0110: Address #6 selected
0111: Address #7 selected
1000: Address #8 selected
1001: Address #9 selected
1010: Address #10 selected
1011: Address #11 selected
1100: Address #12 selected
1101: Address #13 selected
1110: Address #14 selected
1111: Address #15 selected

Address #1-#8 CHx control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address				WD	PHx1	PHx0	PSFx	IxDC7	IxDC6	IxDC5	IxDC4	IxDC3	IxDC2	IxDC1	IxDC0
R				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: Base address + 0x0Yh (Y = 0x01h to 0x08h)

Type: R, R/W

Reset: 0xY000h

Bit 15:12 Address

Bit 11 WD: Watchdog toggle bit (75ms, start with [0] after Reset, toggled with every SPI access)

Bit 10:9 PHx[1:0]: Binary decoded PWM phase shift selection (0°, 90°, 180°, 270°)
00: 0° Phase (default)
01: 90° Phase
10: 180° Phase
11: 270° Phase

Bit 8 PSFx: Pulse skipping enable
0: disabled
1: enabled

Bit 7:0 DCx7:0: Channel individual duty cycle programmable from 0x00 to 0xFF
DutyCycle value in % DC[%] = value*100/256
0x00h: 0%
0x01h: 0.39%
0x02h: 0.78%
....
0xFFh: 99.61%

Address #9 mode control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address				WD	res	0	OCBLN	RON8	RON7	RON6	RON5	RON4	RON3	RON2	RON1
R				R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: Base address + 0x09h

Type: R, R/W

Reset: 0x9000h

Bit 15:12 Address

Bit 11 WD: Watchdog toggle bit (75ms, start with [0] after Reset, toggled with every SPI access)

Bit 10 Reserved bits have to be written with 0

Bit 9 0

Bit 8 OCBLN: OC Blanking disable
0: OC blanking = 150us blanking after OUTx on enabled (default)
1: OC blanking = 150us blanking after OUTx on disabled

Bit 7:0 RON8:1: Defines over current threshold and R_{DSON} value
0: OC threshold = 1.5A and R_{DSON} = 600mΩ (OL high threshold) (default)
1: OC threshold = 750mA and R_{DSON} = 1Ω (OL low threshold)

Address #10 OUT enable

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address				WD	res	res	res	OUT8EN	OUT7EN	OUT6EN	OUT5EN	OUT4EN	OUT3EN	OUT2EN	OUT1EN
R				R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: Base address + 0x0Ah

Type: R, R/W

Reset: 0xA001h

Bit 15:12 Address

Bit 11 WD: Watchdog toggle bit (75ms, start with [0] after Reset, toggled with every SPI access)

Bit 10:8 Reserved bits have to be written with 0

Bit 7:0 OUTEN8:1: Enables the Output in Normal Mode. In case of OVx, UVx, TSDx or OCx the corresponding bits are cleared and therefore the OUTx is switched off.

0: disabled (default)

1: enabled (OUT corresponding INSELx, PWMSELx and INx)

Address #11 PWMSEL / INSEL CH1 + CH2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address				WD	res	res	res	INSEL21	INSEL20	PWMSEL21	PWMSEL20	INSEL11	INSEL10	PWMSEL11	PWMSEL10
R				R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: Base address + 0x0Bh

Type: R, R/W

Reset: 0xB000h

Bit 15:12 Address

Bit 11 WD: Watchdog toggle bit (75ms, start with [0] after Reset, toggled with every SPI access)

Bit 10:8 Reserved bits have to be written with 0

Bit 7:6 - Bit 3:2 INSELx[1:0]: INx function selector see *Section 2.7.2: PWM module*

Bit 5:4 - Bit 1:0 PWMSELx[1:0]: PWM function selector see *Section 2.7.2: PWM module*

Address #12 PWMSEL / INSEL CH3 + CH4 + CH5

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address				WD	res	INSEL51	INSEL50	PWMSEL51	PWMSEL50	PWMSEL41	PWMSEL40	INSEL31	INSEL30	PWMSEL31	PWMSEL30
R				R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: Base address + 0x0Ch

Type: R, R/W

Reset: 0xC001h

Bit 15:12 Address

Bit 11 WD: Watchdog toggle bit (75ms, start with [0] after Reset, toggled with every SPI access)

Bit 10 Reserved bits have to be written with 0

Bit 9:8 - Bit 3:2 INSELx[1:0]: INx function selector see *Section 2.7.2: PWM module*

Bit 7:4 - Bit 1:0 PWMSELx[1:0]: PWM function selector see *Section 2.7.2: PWM module*

Address #13 PWMSEL / INSEL CH6 + CH7 + CH8

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address				WD	res	PWMSEL81	PWMSEL80	INSEL71	INSEL70	PWMSEL71	PWMSEL70	INSEL61	INSEL60	PWMSEL61	PWMSEL60
R				R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: Base address + 0x0Dh

Type: R, R/W

Reset: 0xD000h

Bit 15:12 Address

Bit 11 WD: Watchdog toggle bit (75ms, start with [0] after Reset, toggled with every SPI access)

Bit 10 Reserved bits have to be written with 0

Bit 7:6 - Bit 3:2 See *Section 2.7.2: PWM module*

Bit 5:4 - Bit 1:0 See *Section 2.7.2: PWM module*

Address #14 Global PWM1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address				WD	0	0	0	G1DC7	G1DC6	G1DC5	G1DC4	G1DC3	G1DC2	G1DC1	G1DC0
R				R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: Base address + 0x0Eh

Type: R, R/W

Reset: 0xE000h

Bit 15:12 Address

Bit 11 Watchdog toggle bit (75ms, start with [0] after Reset, toggled with every SPI access)

Bit 10:8 0

Bit 7:0 G1DCx: Global 1 duty cycle programmable from 0x00 to 0xFF:
DutyCycle value in %; DC[%] = value * 100/256
0x00h: 0%
0x01h: 0.39%
0x02h: 0.78%
....
0xFFh: 99.61%

Address #15 Global PWM2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address				WD	0	0	0	G2DC7	G2DC6	G2DC5	G2DC4	G2DC3	G2DC2	G2DC1	G2DC0
R				R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Note: Writing all [1] to this register will generate a SPI fail (stuck @ '1').

Address: Base address + 0x0Fh

Type: R, R/W

Reset: 0xF000h

Bit 15:12 Address

Bit 11 WD: Watchdog toggle bit (75ms, start with [0] after Reset, toggled with every SPI access)

Bit 10:8 0

Bit 7:0 G2DCx: Global 2 duty cycle programmable from 0x00 to 0xFF
DutyCycle value in %; DC[%] = value * 100/256
0x00h: 0%
0x01h: 0.39%
0x02h: 0.78%
....
0xFFh: 99.61%

All SDI input data values, are latched into the registers at the rising edge of CSN if the communication is valid (multiple of 16 SCKs and data consistency check).

Table 12. Control Data Register

Register	Address					Control data												
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Initialization	0	0	0	0	0	WD	NO CLEAR	RAM READ	PWMsync	MUXEN	MUX2	MUX1	MUX0	SOA3	SOA2	SOA1	SOA0
CH1 control	1	0	0	0	1	WD	PH11	PH10	PSF1	I1DC7	I1DC6	I1DC5	I1DC4	I1DC3	I1DC2	I1DC1	I1DC0
CH2 control	2	0	0	1	0	WD	PH21	PH20	PSF2	I2DC7	I2DC6	I2DC5	I2DC4	I2DC3	I2DC2	I2DC1	I2DC0
CH3 control	3	0	0	1	1	WD	PH31	PH30	PSF3	I3DC7	I3DC6	I3DC5	I3DC4	I3DC3	I3DC2	I3DC1	I3DC0
CH4 control	4	0	1	0	0	WD	PH41	PH40	PSF4	I4DC7	I4DC6	I4DC5	I4DC4	I4DC3	I4DC2	I4DC1	I4DC0
CH5 control	5	0	1	0	1	WD	PH51	PH50	PSF5	I5DC7	I5DC6	I5DC5	I5DC4	I5DC3	I5DC2	I5DC1	I5DC0
CH6 control	6	0	1	1	0	WD	PH61	PH60	PSF6	I6DC7	I6DC6	I6DC5	I6DC4	I6DC3	I6DC2	I6DC1	I6DC0
CH7 control	7	0	1	1	1	WD	PH71	PH70	PSF7	I7DC7	I7DC6	I7DC5	I7DC4	I7DC3	I7DC2	I7DC1	I7DC0
CH8 control	8	1	0	0	0	WD	PH81	PH80	PSF8	I8DC7	I8DC6	I8DC5	I8DC4	I8DC3	I8DC2	I8DC1	I8DC0
Mode control	9	1	0	0	1	WD	res	0	OCBLN	RON8	RON7	RON6	RON5	RON4	RON3	RON2	RON1
OUT enable	10	1	0	1	0	WD	res	res	res	OUT8EN	OUT7EN	OUT6EN	OUT5EN	OUT4EN	OUT3EN	OUT2EN	OUT1EN
PWMSEL / INSEL CH1 + CH2	11	1	0	1	1	WD	res	res	res	INSEL21	INSEL20	PWMSEL21	PWM SEL20	INSEL11	INSEL10	PWMSEL11	PWMSEL10
PWMSEL / INSEL CH3 + CH4 + CH5	12	1	1	0	0	WD	res	INSEL51	INSEL50	PWM SEL51	PWM SEL50	PWMSEL41	PWMSEL40	INSEL31	INSEL30	PWMSEL31	PWMSEL30
PWMSEL / INSEL CH6 + CH7 + CH8	13	1	1	0	1	WD	res	PWMSEL81	PWMSEL80	INSEL71	INSEL70	PWMSEL71	PWMSEL70	INSEL61	INSEL60	PWMSEL61	PWMSEL60
Global PWM1	14	1	1	1	0	WD	0	0	0	G1DC7	G1DC6	G1DC5	G1DC4	G1DC3	G1DC2	G1DC1	G1DC0
Global PWM2	15	1	1	1	1	WD	0	0	0	G2DC7	G2DC6	G2DC5	G2DC4	G2DC3	G2DC2	G2DC1	G2DC0

3.1.6 Status Data Registers

By accessing the Status Registers, the read and clear flags are cleared after rising CSN edge. All read and clear flags are latched and keep the status till read out. All other flags report the actual status and are therefore not clearable. By setting the NOCLEAR flag D10 in Initialisation register #0, this automatic clear is prohibited.

If a flag is set during read out phase the flag is latched and will be reported with the next read.

The SPI output delivers the data set programmed by the bits D9 (READRAM option) and D3:0 (SDOA3:0) inside the control data register [#0] of the SPI:

SDR base address = 0x00h

The SDR register are shown in *Table 13: SDR registers*

Table 13. SDR registers

Register	Address offset	Reset value
Address #0	0x00h	0x00h
Address #1 Device Status 1	0x01h	0x00h
Address #2 Device Status 2	0x02h	0x00h
Address #3 Device Status 3	0x03h	0x00h
Address #4 Quick Status	0x04h	0x00h
Address #5-#8 Status CHx+CHy		
Address #5 Status CH1+CH2	0x05h	0x00h
Address #6 Status CH31+CH4	0x06h	0x00h
Address #7 Status CH5+CH6	0x07h	0x00h
Address #8 Status CH7+CH8	0x08h	0x00h
Address #9 Mode Control	0x09h	0x00h
Address #10 OUT enable	0x0Ah	0x00h
Address #11 INx Status	0x0Bh	0x00h
Address #12 Silicon Version	0x0Ch	0x01h

Address #0

A read access to Status Register #0 is not allowed. It is interpreted as SDO is shorted to "0" and lead the device to enter Fail Mode

Address #1 Device Status 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address				FAILSAFE	SVF	X(1)	DSF	CHIP RESET	VDDF	SPIF	LIMP	PCLKF	RFAIL	WDC ERR	WDC0
R				R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

1. X: do not care

Address: Base address + 0x01h

Type: R, R/W

Reset: 0x00h

Bit 15:12 Address

Bit 11 FAILSAFE:
0: Device is in Normal Mode
1: Device is in Fail Mode (DirectDrive enabled)

Bit 10 SVF: logical OR combination of all OV, UV, OVx, UVx
0: supply voltage in operating range
1: supply voltage failure

Bit 9 X: do not care

Bit 8 DSF: logical OR combination of VDDF or SPIF or LIMP or PCLKF or RFAIL or WDCERR
0: no fail detected
1: fail detected

Bit 7 CHIP RESET: indicates if all registers are previously reset, cleared with the first SPI read (by default #1)
0: device has not been previously reset
1: all registers are in reset state (cleared with first valid SPI command after reset)

Bit 6 VDDF: VDD fail occurred
0: no VDD fail detected
1: VDD fail detected

Bit 5 SPIF: SPI clock fail or SDI stuck @ detected
0: no SPI fail detected
1: SPI fail detected (SPI clock cycles during a transaction is not a multiple of 16, stuck @ 0 or 1 at SDI detected)

Bit 4 LIMP: LIMP pin high detected
0: no LIMP high detected
1: LIMP high detected

Bit 3 PCLKF: PWMCLK fail detected
0: no PWMCLK fail detected
1: PWMCLK fail detected

Bit 2 RFAIL: External R failure detected
0: R external connected correctly
1: R external fail detected

Bit 1 WDCERR: WDC time-out or WD toggle bit fail detected
0: no watchdog failure
1: watchdog fail detected

Bit 0 WDC0: WDC 50% flag
0: watchdog 50% time-out not reached
1: watchdog 50% time-out reached

Address #2 Device Status 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address				FAILSAFE	SVF	X(1)	DSF	0	0	0	0	TSD	TW	OVF	UVF
R				R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

1. X: do not care

Address: Base address + 0x02h

Type: R, R/W

Reset: 0x00h

Bit 15:12 Address

Bit 11 FAILSAFE:
0: Device is in Normal Mode
1: Device is in Fail Mode (DirectDrive enabled)

Bit 10 SVF: Logical OR combination of all OV, UV, OVx, UVx
0: supply voltage in operating range
1: supply voltage failure

Bit 9 X: do not care

Bit 8 DSF: Logical OR combination of VDDF or SPIF or LIMP or PCLKF or RFAIL or WDCERR
0: no fail detected
1: fail detected

Bit 7:4 0

Bit 2 TW: Logical OR combination of all TWx
0: no thermal warning detected
1: thermal warning detected

Bit 1 OVF: OverVoltage at VS detected
0: no over voltage detected
1: over voltage detected (OVF is latched once an overvoltage on VS is detected)

Bit 0 UVF: UnderVoltage at VS detected
0: no under voltage detected
1: under voltage detected (UVF is latched once an undervoltage on VS is detected)

Address #3 Device Status 3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address				FAILSAFE	SVF	X(1)	DSF	OVF_A	UVF_A	OVF_B	UVF_B	OVF_C	UVF_C	OVF_D	UVF_D
R				R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

1. X: do not care

Address: Base address + 0x03h

Type: R, R/W

Reset: 0x00h

Bit 15:12 Address

Bit 11 FAILSAFE:
0: Device is in Normal Mode
1: Device is in Fail Mode (DirectDrive enabled)

Bit 10 SVF: Logical OR combination of all OVx, UVx
0: supply voltage in operating range
1: supply voltage failure

Bit 9 X: do not care

Bit 8 DSF: Logical OR combination of VDDF or SPIF or LIMP or PCLKF or RFAIL or WDCERR
0: no fail detected
1: fail detected

Bit 7 OVF_A(1): OverVoltage at VSA detected
0: no over voltage detected
1: over voltage detected, OUT1EN and OUT2EN are cleared automatically (channel OFF)

Bit 6 UVF_A(1): UnderVoltage at VSA detected
0: no under voltage detected
1: under voltage detected, OUT1EN and OUT2EN are cleared automatically (channel OFF)

Bit 5 OVF_B(1): OverVoltage at VSB detected
0: no over voltage detected
1: over voltage detected, OUT3EN and OUT4EN are cleared automatically (channel OFF)

Bit 4 UVF_B(1): UnderVoltage at VSB detected
0: no under voltage detected
1: under voltage detected, OUT3EN and OUT4EN are cleared automatically (channel OFF)

Bit 3 OVF_C(1): OverVoltage at VSC detected
0: no over voltage detected
1: over voltage detected, OUT5EN and OUT6EN are cleared automatically (channel OFF)

Bit 2 UVF_C(1): UnderVoltage at VSC detected
0: no under voltage detected
1: under voltage detected, OUT5EN and OUT6EN are cleared automatically (channel OFF)

Bit 1 OVF_D(1): OverVoltage at VSD detected
0: no over voltage detected
1: over voltage detected, OUT7EN and OUT8EN are cleared automatically (channel OFF)

Bit 0 UVF_D(1): UnderVoltage at VSD detected
0: no under voltage detected
1: under voltage detected, OUT7EN and OUT8EN are cleared automatically (channel OFF)

1. OVF_X and UVF_X are latched, once an overvoltage, respectively, and undervoltage is detected on VS_X.

Address #4 Quick Status

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address				FAILSAFE	SVF	X(1)	DSF	QSF8	QSF7	QSF6	QSF5	QSF4	QSF3	QSF2	QSF1
R				R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

1. X: do not care

Address: Base address + 0x04h

Type: R, R/W

Reset: 0x00h

Bit 15:12 Address

Bit 11 FAILSAFE:
0: Device is in Normal Mode
1: Device is in Fail Mode (DirectDrive enabled)

Bit 10 SVF: Logical OR combination of all OVx, UVx
0: supply voltage in operating range
1: supply voltage failure

Bit 9 X: do not care

Bit 8 DSF: logical OR combination of VDDF or SPIF or LIMP or PCLKF or RFAIL or WDCERR
0: no fail detected
1: fail detected

Bit 7:0 QSFx[7:0]: channel specific logical OR combination of TSDx or TWx_th2 or TWx_th1 or OCx or OLx
0: no fail detected
1: fail detected

Address #5-#8 Status CHx+CHy

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address				FAILSAFE	SVF	X(1)	DSF	OUTL	TSDxy	TWxyth2	TWxyth1	OCy	X(1)	OCx	X(1)
R				R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

1. X: do not care

Address: Base address + 0x0Yh (Y = 0x05 to 0x08h)

Type: R, R/W

Reset: 0x00h

Bit 15:12 Address

Bit 11 FAILSAFE:
0: Device is in Normal Mode
1: Device is in Fail Mode (DirectDrive enabled)

Bit 10 SVF: Logical OR combination of all OVx, UVx
0: supply voltage in operating range
1: supply voltage failure

Bit 9 X: do not care

Bit 8 DSF: logical OR combination of VDDF or SPIF or LIMP or PCLKF or RFAIL or WDCERR
0: no fail detected
1: fail detected

Bit 7 OUTL: logical read back value of selected [#0:D7~D4] OUTx channel. This information can be used to distinguish between open load and short to VSx in OFF state.
0: OUTx is low
1: OUTx is high

Bit 6 TSDxy: thermal shutdown flag of channel x or y
0: no thermal shutdown detected
1: thermal shutdown detected, the corresponding OUTxEN are cleared automatically (channel OFF). TSDxy is latched off once an thermal shutdown occured.

Bit 5 TWxy_th2: thermal warning threshold2 flag of channel x or y
0: no thermal warning detected
1: thermal warning detected. This bit is not latched. Once the temperature on outputs x/y is below TjTW2, this status bit is reset.

Bit 4 TWxy_th1: thermal warning threshold1 flag of channel x or y
0: no thermal warning detected
1: thermal warning detected

Bit 3, 1 OCx/y: channel specific over current flag
1: overcurrent detected, the corresponding OUTxEN is cleared automatically (channel OFF)

Bit 2, 0 X: do not care

Address #9 Mode Control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address				FAILSAFE	SVF	X(1)	DSF	RON8	RON7	RON6	RON5	RON4	RON3	RON2	RON1
R				R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

1. X: do not care

Address: Base address + 0x09h

Type: R, R/W

Reset: 0x00h

Bit 15:12 Address

Bit 11 FAILSAFE:
0: Device is in Normal Mode
1: Device is in Fail Mode (DirectDrive enabled)

Bit 10 SVF: Logical OR combination of all OVx, UVx
0: supply voltage in operating range
1: supply voltage failure

Bit 9 X: do not care

Bit 8 DSF: logical OR combination of VDDF or SPIF or LIMP or PCLKF or RFAIL or WDCERR
0: no fail detected
1: fail detected

Bit 7:0 RON8:1: Copy of over current threshold and R_{DSON} value defined in input register #9
0: OC threshold = 1.5A and R_{DSON} = 500mΩ (OL high threshold)
1: OC threshold = 750mA and R_{DSON} = 1Ω (OL low threshold)

Address #10 OUT enable

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address				FAILSAFE	SVF	X(1)	DSF	OUT8EN	OUT7EN	OUT6EN	OUT5EN	OUT4EN	OUT3EN	OUT2EN	OUT1EN
R				R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

1. X: do not care

Address: Base address + 0x0Ah

Type: R, R/W

Reset: 0x00h

Bit 15:12 Address

Bit 11 FAILSAFE:
0: Device is in Normal Mode
1: Device is in Fail Mode (DirectDrive enabled)

Bit 10 SVF: Logical OR combination of all OVx, UVx
0: supply voltage in operating range
1: supply voltage failure

Bit 9 X: do not care

Bit 8 DSF: logical OR combination of VDDF or SPIF or LIMP or PCLKF or RFAIL or WDCERR
0: no fail detected
1: fail detected

Bit 7:0 OUTEN8:1: Copy of output enable in Normal Mode status defined in input register #10
0: disabled
1: enabled (OUT corresponding INSELx and PWMSELx)

Address #11 INx Status

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address				FAILSAFE	SVF	X(1)	DSF	0	IN7	IN6	IN5	0	IN3	IN2	IN1
R				R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

1. X: do not care

Address: Base address + 0x0Bh

Type: R, R/W

Reset: 0x00h

Bit 15:12 Address

Bit 11 FAILSAFE:
0: Device is in Normal Mode
1: Device is in Fail Mode (DirectDrive enabled)

Bit 10 SVF: Logical OR combination of all OVx, UVx
0: supply voltage in operating range
1: supply voltage failure

Bit 9 X: do not care

Bit 8 DSF: logical OR combination of VDDF or SPIF or LIMP or PCLKF or RFAIL or WDCERR
0: no fail detected
1: fail detected

Bit 7:4 - Bit 2:0 IN7, IN6, IN5, IN3, IN2, IN1: corresponding INx pin value
0: input logical [0] detected
1: input logical [1] detected

Bit 3 0

Address #12 Silicon Version

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address				FAILSAFE	SVF	X(1)	DSF	0	0	0	0	SV3	SV2	SV1	SV0
R				R/W	R/W	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W

1. X: do not care

Address: Base address + 0x0Ch

Type: R, R/W

Reset: 0x01h

Bit 15:12 Address

Bit 11 FAILSAFE:
0: Device is in Normal Mode
1: Device is in Fail Mode (DirectDrive enabled)

Bit 10 SVF: Logical OR combination of all OVx, UVx
0: supply voltage in operating range
1: supply voltage failure

Bit 9 X: do not care

Bit 8 DSF: logical OR combination of VDDF or SPIF or LIMP or PCLKF or RFAIL or WDCERR
0: no fail detected
1: fail detected

Bit 7:4 0

Bit 3:0 SV3:0: Binary coded version of Silicon
0001: Silicon version

Table 14. Status Data Register(1)

Register	Address					Control data											
	#	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NA	0	0	0	0	0	X(2)	X	X	X	X	X	X	X	X	X	X	X
Device status 1	1	0	0	0	1	FAIL SAFE	SVF	X	DSF	CHIP RESET	VDDF	SPIF	LIMP	PCLKF	RFAIL	WDC ERR	WDC0
Device status 2	2	0	0	1	0	FAIL SAFE	SVF	X	DSF	0	0	0	0	TSD	TW	OVF	UVF
Device status 3	3	0	0	1	1	FAIL SAFE	SVF	X	DSF	OVF_A	UVF_A	OVF_B	UVF_B	OVF_C	UVF_C	OVF_D	UVF_D
Quick status	4	0	1	0	0	FAIL SAFE	SVF	X	DSF	X	X	X	X	X	X	X	X
Diag CH1 + 2	5	0	1	0	1	FAIL SAFE	SVF	X	DSF	OUTL	TSD12	TW12th2	TW12th1	OC2	X	OC1	X
Diag CH3 + 4	6	0	1	1	0	FAIL SAFE	SVF	X	DSF	OUTL	TSD34	TW34th2	TW34th1	OC4	X	OC3	X
Diag CH5 +6	7	0	1	1	1	FAIL SAFE	SVF	X	DSF	OUTL	TSD56	TW56th2	TW56th1	OC6	X	OC5	X
Diag CH7 + 8	8	1	0	0	0	FAIL SAFE	SVF	X	DSF	OUTL	TSD78	TW78th2	TW78th1	OC8	X	OC7	X
Mode control	9	1	0	0	1	FAIL SAFE	SVF	X	DSF	RON8	RON7	RON6	RON5	RON4	RON3	RON2	RON1
OUT enable	10	1	0	1	0	FAIL SAFE	SVF	X	DSF	OUT8EN	OUT7EN	OUT6EN	OUT5EN	OUT4EN	OUT3EN	OUT2EN	OUT1EN
INx status	11	1	0	1	1	FAIL SAFE	SVF	X	DSF	0	IN7	IN6	IN5	IN4	IN3	IN2	IN1
Silicon version	12	1	1	0	0	FAIL SAFE	SVF	X	DSF	0	0	0	0	SV3	SV2	SV1	SV0

1. Grey cells: read and clear flags.
2. X: do not care.

3.2 Operating modes

3.2.1 Standby mode

The standby mode is the default mode of the device after power on ($VS > VS_{UV}$) without applying any wake up signals (High signal on one of the INx pins or on EN pin).

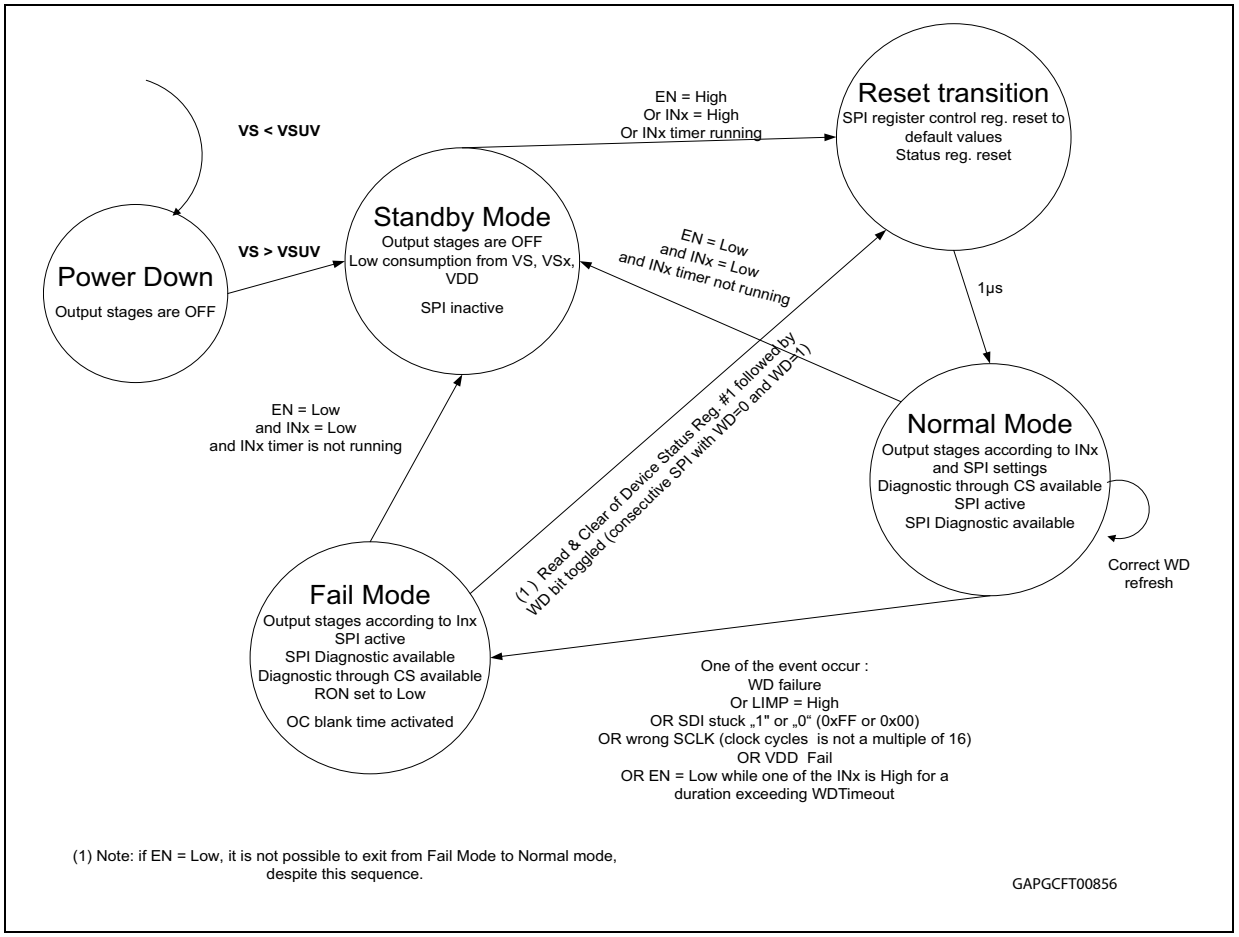
During standby mode

- The current consumption of the device is minimized (VDD, VS, VSx)
- The internal circuitry is deactivated
- All outputs are OFF and protected against mistreatment

3.2.2 Wake up and operating modes

The device leaves the standby mode if one of the following wake-up events occurs. Refer to *Figure 4*:

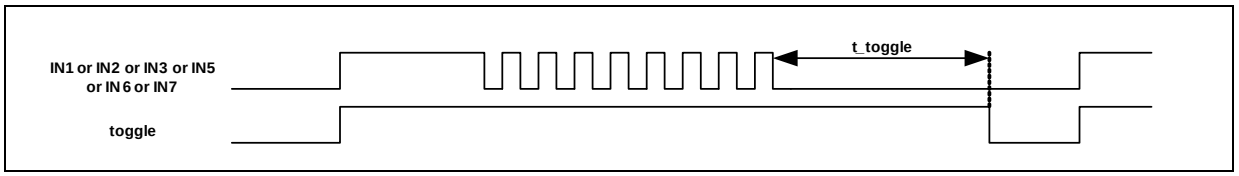
Figure 4. State diagram



Wakeup sources are as follows:

- ENABLE
- input signals IN1, IN2, IN3, IN5, IN6, IN7
- toggle signal: this signal is an OR combination from all input signals by a retriggerable mono stable. It keeps the device active for a dedicated time (t_{toggle}) after the last negative edge at any input signal IN1, IN2, IN3, IN5, IN6, IN7:

Figure 5. Toggle signal



When ENABLE is off but another wakeup source is still active this can be monitored by the PWMCLK(WAKE) pin which is an active high output during pending WAKE.

By leaving the FailMode all internal registers will be reset to default state.

3.2.3 Cold start – power up reset

The cold start sequence describes the power up and the startup of the device. When VS is in the specified ranges and the INx or the ENABLE pin are on a logical [0] level the device is in STANDBY. When INx or ENABLE change their levels to logical [1] the internal EN for the power on reset circuit (POR) and the oscillator (OSC) will be set to [1] and the two blocks will be enabled. The device is started. The internal POR is released and the oscillator is running. The internal registers are reset. to their default value and the device enter NORMAL MODE

3.2.4 Normal Mode

The device enters Normal mode:

- either from Standby Mode if VDD > VDDUV, LIMP =Low, and EN goes from Low to High. Refer to *Section 3.2.3: Cold start – power up reset*
- or from Fail Mode, refer to *Section 3.2.6: Warm start – (Transition from FailMode to Normal over Internal Reset)*

In Normal mode, the SPI is active and the output stages are controlled by the SPI and the INx settings. The SPI diagnostics and the CurrentSense pin are both available. The protections are fully functional.

Normal mode is left with the following conditions:

- VDD falls below VDDUV
- A watchdog failure occurs: wrong toggling of WD Bit or No toggling of the WD bit for a duration exceeding TWD
- EN goes Low
- An SPI failure occurs
- LIMP goes to Low

3.2.5 Fail Mode

The L99CL01XP offers the possibility to control OUT1-3 and OUT5-7 in case of fail safe event by the corresponding INx pins (refer to *Table 15*)

Table 15. Mapping between the input pins and the outputs in Fail Mode

Pin	Corresponding output
IN1	OUT1
IN2	OUT2
IN3	OUT3
IN5	OUT5
IN6	OUT6
IN7	OUT7

The Fail Mode is activated if one of the conditions listed in the following table occurs. The operation in Fail Mode is reported by the status bit Fail Safe (any Status Register, bit11) and by one of the status bits: VDDUV, SPIF, WDCERR, LIMP, depending on the cause of the activation of the Fail Mode.

Table 16. Events leading to Fail Mode

Event	Related status bit	Delay to Fail Mode
VDD undervoltage	VDDUV	After t_{VDD_UV}
SPI Failure	SPIF	Immediate
Watchdog check error	WDCERR	After WDTimeout
LIMP = High	LIMP	After t_{LIMP}
During Active Mode, EN goes from High to Low while one of the $INx_{,x= 1-3, 5-6}$ is High (1)	WDCERR	After WDTimeout

1. When this condition occurs, the device prevents the refresh of the WD toggle bit, leading to a Watchdog timeout failure. As long as EN = Low, the refresh of the WD is blocked and the device cannot go to Normal Mode.

In this mode, the device's SPI is active unless a VDD undervoltage occurs.

The control registers behaves as described in the *Table 17*. The content of the status registers are kept during the transition to Fail Mode.

Table 17. Control registers in Fail Mode

Control registers	Content during transition to Fail Mode	Write protection	Valid content
Initialization, #0	As before Fail mode	No	Yes
CHx Control, #1-8	As before Fail mode	No	No(1)
Mode Control, #9	Reset to default value	Yes(2)	Yes
OUT enable, #10	As before Fail mode	No	No(2)

Table 17. Control registers in Fail Mode

Control registers	Content during transition to Fail Mode	Write protection	Valid content
PWMEN/INSEL, #11-13	As before Fail mode	No	No(2)
Global PWMx, #1-2	As before Fail mode	No	No(2)

1. The PWM unit is disabled and the state of OUTx is according to the corresponding INx,x=1-3,5-7 regardless to the content of these registers. OUT4 and OUT8 are OFF.
2. While entering the Fail Mode, the content of the Mode Control register is reset to its default value and the device behaves accordingly: the Rdson of the Output is set to the low value and the overcurrent blank time is enabled. This control register is write-protected in Fail Mode.

The current sense is active and the Kfactor is the one, which corresponds to the Low Ron setting.

Auto restart feature

The auto restart feature is used to control the smart switches in case of overcurrent, under or over voltage failure conditions to provide a high availability of the outputs even when no supervising intelligence of the microcontroller is available (Fail Mode).

Auto restart is enabled in case of

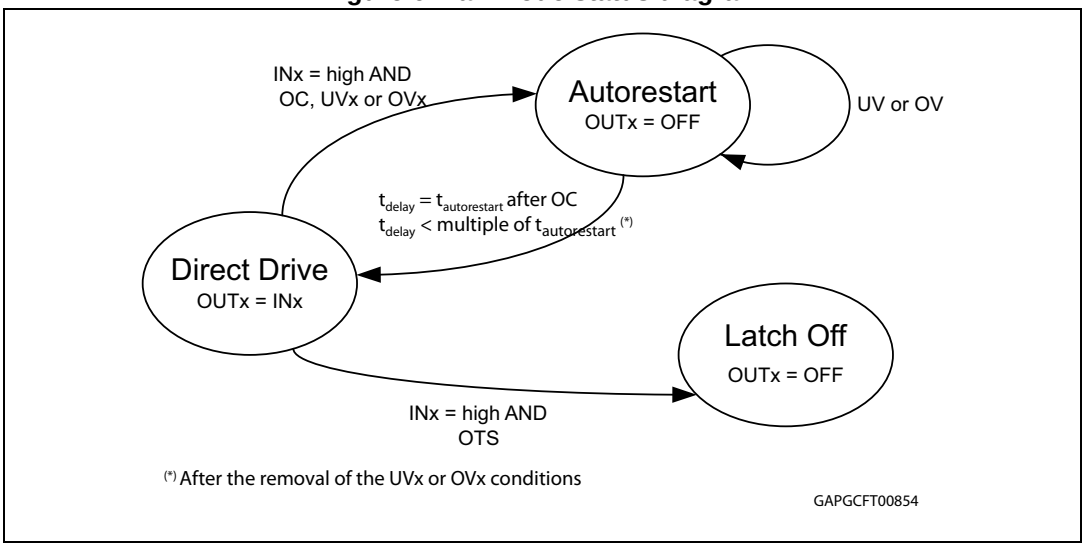
- Overcurrent condition (OCx) of the corresponding channel
- Under or over voltage condition (UVx or OVx) on the corresponding supply line

In case of OC, UV or OV the corresponding output or outputs are deactivated. In case of OC failure the output returns to Fail Mode direct drive after a dedicated time ($t_{autorestart}$ = 100 ms). During this ON phase the diagnosis is restarted. When the failure is still present and the channel is turned off again. Therefore the output stays in this cyclic loop as long as the failure is present.

In case of UV or OV the diagnosis is continuously running. After removing the failure condition (UV or OV) the switch returns to Fail Mode direct drive after a dedicated time within $t_{autorestart}$.

In case of over temperature shutdown (OTS) the switch enters “Latch OFF” state which can only be removed by a mode change to “Normal Mode” or “Standby” (see*Chapter 3.2: Operating modes*).

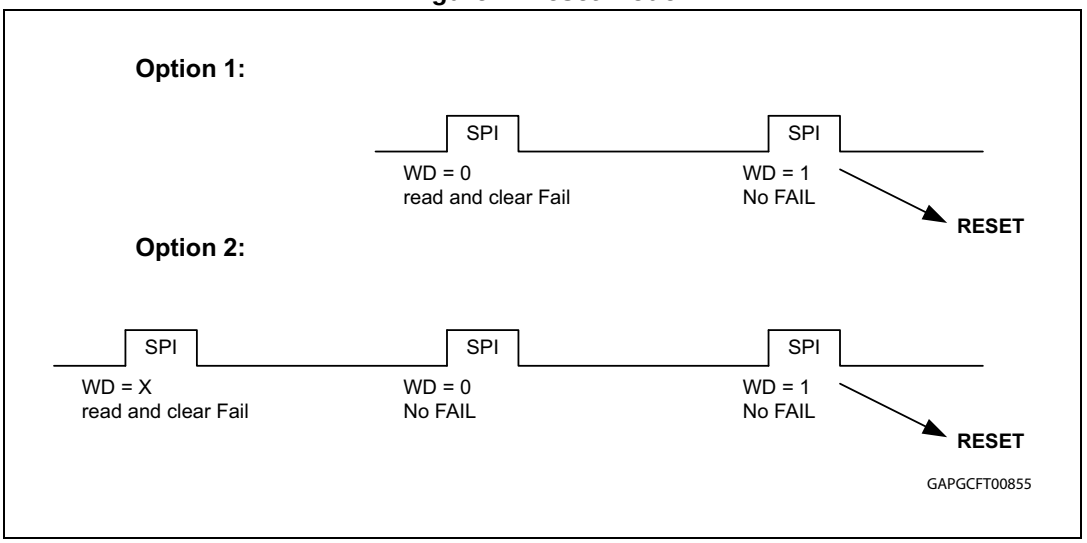
Figure 6. Fail mode status diagram



3.2.6 Warm start – (Transition from FailMode to Normal over Internal Reset)

Due to a possible unknown state of the internal registers a reset of the device is necessary by leaving FAIL mode. Therefore a reset is generated when the device leaves FAIL mode with two consecutive valid SPI commands with WD ‘0’ and WD ‘1’. This is only possible when ENABLE is logical [1] and the failure is removed (read and clear) before the two consecutive SPI commands are sent. This kind of reset has no impact on the POR and the OSC.

Figure 7. Reset mode



4 Electrical specifications

4.1 Absolute maximum rating

Stressing the device above the rating listed in *Table 18* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other condition above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 18. Absolute maximum rating

Symbol	Parameter	Test condition	Value	Unit
VSA, VSB, VSC, VSD	Supply voltage range for channel couples A, B, C and D	Short circuit; single pulse; T_j = 25°C(1)	6 to 24	V
		Short circuit; repetitive pulse; -40°C < T_j < 150°C(1)	6 to 20	V
		load dump (400 ms)	40	V
VS_{REV}	reverse polarity voltage range(2)		-24	V
V_{IO}	logic input voltage range		-0.3 to V_{DD}+0.3	V
$I_{in\ clamp}$	input clamping current	Maximum value of each pin	5	mA
V_{OUT}	Output voltage range		-1.5 to V_S+0.3	V
V_{CLAMP_high}	OUTx, INx, LIMP, CSN, ENABLE, VS, VSA, VSB, VSC, VSD		42	V
V_{CLAMP_low}	SDO, SDI, SCK, PWMCLK, CS, VDD, REXT		7	V
T_j	Junction operating temperature		-40 to 150	°C
T_{stg}	Storage temperature		-55 to 150	°C
V_{ESD}	Electrostatic discharge (Human Body Model, 100pF/1,5k)	VS(3), GND, OUT1 ~ OUT8	±4	kV
		All other pins	±2	kV
	Charge device model (CDM-AEC-Q100-011)		1000	V

1. Also valid for VSA, VSB, VSC, VSD < 6 V
2. Valid for VS.
3. Valid for VSA, VSB, VSC, VSD.

4.2 Thermal data

Table 19. Temperature warning and thermal shutdown

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{jTW1}(1)	Temperature warning threshold junction temperature	125		165	°C
T_{jTW2}(1)	Temperature warning threshold junction temperature	135		175	°C
T_{jTSD}(1)	Thermal shutdown threshold junction temperature	155		195	°C

1. Parameter guaranteed by design and characterization; not subject to production test.

Table 20. Thermal data

Symbol	Parameter	Typ. value	Unit
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-5)(1)(2)	48.5	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (JEDEC JESD 51-7)(2)(3)	19.5	°C/W

1. Device mounted on two-layers 2s0p PCB with 2 cm^2 heatsink copper trace
2. One channel ON.
3. Device mounted on four-layers 2s2p PCB

Table 21. Digital timings

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{INT}	Internal oscillator clock frequency	1.75	2	2.25	MHz
t_{TSD}(1)	Internal TWx and TSD filter time	20	25	30	µs
t_{VDD_UV}(1)	VDD_{UV} detection time	20	25	30	µs
$t_{VS\_OV/UV}$(1)	VS UV/OV detection time	20	25	30	µs
t_{LIMP}(1)	Limp mode settling time	0.9	1.15	1.4	ms
t_{REXTF}(1)	R extern fail deglitch time	20	25	30	µs
t_{TOGGLE}(1)	Input toggle time	1.65	2.1	2.55	s
$t_{AUTORESTART}$(1)	Auto restart delay time	100	130	160	ms
t_{WD}(1)	Watchdog timeout	60	75	90	ms
t_{OC}(1)	Overcurrent shutdown delay time	40	50	60	µs
$t_{OCBLANK}$(1)	OC blanking time	160	200	240	µs
$t_{CSN\ timeout}$(1)	CSN timeout	100	130	160	ms

1. Parameter guaranteed by design and characterization; not subject to production test.

4.3 Electrical characteristics

V_S = 6 V to 24 V, V_{DD} = 4.5 V to 5.5 V, T_j = -40°C to 150°C, unless otherwise specified.

The voltages are referred to GND and currents are assumed positive, when the current flows into the pin.

Table 22. Electrical characteristics (logic + inputs)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
VDD	Digital I/O supply voltage range		3.0		5.5	V
VDD_{UV}	Digital I/O supply undervoltage threshold at T_j = 25°C		2.0	2.5	3.0	V
VDD_{UVHyst}	Digital I/O supply undervoltage threshold hysteresis at T_j = 25°C				0.4	V
I_{DD}	Supply current in ON-state from V_{DD}				500	µA
I_{QDD}	Standby current consumption from V_{DD} at T_j = 25°C				5	µA
VS_{UV}	Battery supply under voltage flag at T_j = 25°C(1)		5.0	5.5	6.0	V
VS_{UVHyst}	Battery supply undervoltage flag hysteresis at T_j = 25°C				0.4	V
VS_{OV}	Battery supply overvoltage flag		30	32	34	V
VS_{OVHyst}	Battery supply overvoltage flag hysteresis		1	1.5	2	V
I_S	Supply current in ON-state from V_S at V_S = 12 V	I_{OUTx} = 0 A			10	mA
I_{QS}	Standby current consumption from V_S at T_j = 25°C, V_S = 12 V				5	µA
V_{VDDH}	Logic input high level(2)	All digital inputs connected to V_{DD}	0.56 V_{DD}	0.66 V_{DD}	0.76 V_{DD}	V
	Logic input high level(3)	All digital inputs connected to V_{DD}	0.52 V_{DD}	0.58 V_{DD}	0.64 V_{DD}	V
$V_{VDDHyst}$	Input hysteresis(4)	All digital inputs connected to V_{DD}	0.16 V_{DD}	0.22 V_{DD}	0.26 V_{DD}	V
V_{intH}	Logic input high level(5)	All digital inputs connected to internal 5V	1.4	1.7	2.0	V
$V_{intHyst}$	Logic input hysteresis(5)	All digital inputs connected to internal 5V	0.4	0.6	0.8	V
$I_{L(off)}$	Off-state output current at V_S = V_{Sx} = 12 V	Channel OFF; V_{OUT} = 0 V			1	µA
V_{OL}	Output low voltage(6)	I_{out} = 5mA			0.5	V
V_{OH}	Output high voltage(6)	I_{out} = -5mA	V_{DD} – 1.3			V

Table 22. Electrical characteristics (logic + inputs) (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{PORH}	Power on reset high threshold for V_S at V_{DD} = 5 V		2	2.8	4	V
V_{PORL}	Power on reset high threshold for V_S at V_{DD} = 5 V		2	2.9	4	V
R_{up}(3)	Pull up resistor for logic pin		9	20	44	kΩ
R_{down}(7)	Pull down resistor for logic pin		36	100	250	kΩ
f_{PWM}	PWM frequency range		100		400	Hz
f_{CLK}	Clock input frequency range		25.6		102.4	kHz
δ_{PWM}	PWM duty cycle resolution			1/256		%
R_{EXT}	External resistor range for REXT pin		10	12.4	15	kΩ
R_{failH}			15			kΩ
R_{failL}					10	kΩ
V_{REXT}	REXT output voltage	I_{out} = 200 µA	2.4	2.5	2.6	V
$f_{CLK\ fail\ low}$(8)	Clock frequency fail detection range	Low frequency			10	kHz

1. Valid for VS, VSA, VSB, VSC, VSD.
2. Valid for ENABLE, SDI, SCK, PWMCLK
3. Valid for CSN
4. Valid for ENABLE, SDI, SCK, PWMCLK, CSN.
5. Valid for IN1, IN2, IN3, IN5, IN6, IN7, LIMP
6. Valid for SDO
7. Valid for ENABLE, SDI, SCK, INx, PWMCLK, LIMP.
8. Parameter guaranteed by design and characterization; not subject to production test.

Table 23. Dynamic characteristics (SPI)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SPI_{clk}(1)	SPI clock frequency				2	MHz
t_{CSNQV}(1)	CSN falling until SDO valid	C_{out} = 100pF			120	ns
t_{CSNQT}(1)	CSN rising until SDO tristate	C_{out} = 100pF			4	s
t_{SCKQV}(1)	SCK rising until SDO valid	C_{out} = 100pF			20	ns
t_{SCSN}(1)	CSN setup time before SCK rising		20			ns
t_{SSDI}(1)	SDI setup time before SCK falling		20			ns
t_{HSCK}(1)	minimum SCK high time		125			ns
t_{LSCK}(1)	minimum SCK low time		125			ns
t_{HCSN}(1)	minimum CSN high time		5			µs
t_{SSCK}(1)	SCK setup time before CSN rising		50			ns

1. Parameter guaranteed by design and characterization; not subject to production test.

Table 24. Switching (V_S = 12 V; T_j = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time $R_{ON}[x]$ = 0	R_{LOAD} = 32 Ω	—		25	µs
$t_{d(on)}$	Turn-on delay time $R_{ON}[x]$ = 1	R_{LOAD} = 16 Ω	—		25	µs
$t_{d(off)}$	Turn-off delay time $R_{ON}[x]$ = 0	R_{LOAD} = 32 Ω	—		25	µs
$t_{d(off)}$	Turn-off delay time $R_{ON}[x]$ = 1	R_{LOAD} = 16 Ω	—		25	µs
$(dV_{OUt}/dt)_{on}$	Turn-on voltage slope		—	0.14		V/µs
$(dV_{OUt}/dt)_{off}$	Turn-off voltage slope		—	0.32		V/µs
t_{SKEW}	Differential pulse skew		—		-200	µs

Figure 8. SPI timing

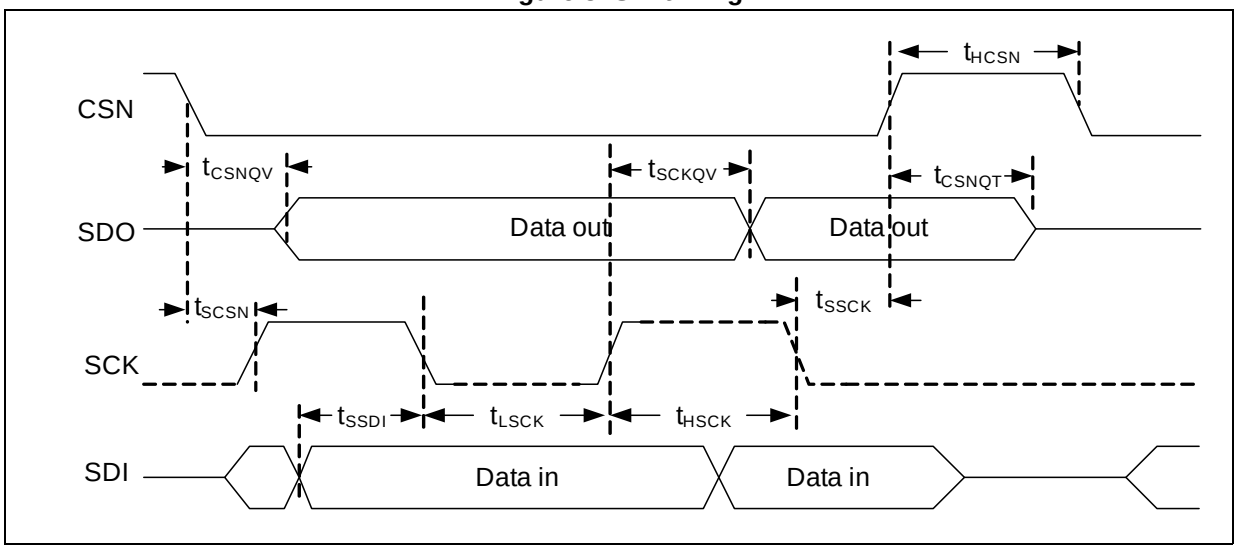


Table 25. Electrical characteristics (OUT1 - OUT8)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{DSon}	output resistance	RONx = [1]; I = 800 mA	0.35	0.6	1	Ω
		RONx = [0]; I = 400 mA	0.65	1	1.7	Ω
I_{OC}	Overcurrent shutdown threshold	OC high range; ON state(1)	1.2	1.5	1.8	A
		OC low range; ON state(1)	0.6	0.75	0.9	A
V_{OUTL}	Selected OUTx voltage threshold		4.5	5	5.5	V

Table 25. Electrical characteristics (OUT1 - OUT8) (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{SENSE0}	Analog sense	I_{OUT} = 0 A; V_{CS} = 0 V; Channels in OFF-state; Current sense multiplexer enabled on one of the outputs			0.5	µA
		I_{OUT} = 0 A; V_{CS} = 0 V; Channels in ON-state; Current sense multiplexer disabled			0.5	µA
$t_{DSENSE1H}$	Current sense settling time from rising edge of CS pin	Maximum value for setting to 90%	5	130	250	µs
K_1	Current sense ratio at different currents	I_{OUT}/I_{CS}; RON[x] = 0; I_{OUT} = 50 mA	450	1450	3500	
		I_{OUT}/I_{CS}; RON[x] = 1; I_{OUT} = 30 mA	300	725	1500	
dK_1/K_1 (2)	Current sense ratio drift with temperature	I_{OUT}/I_{CS}; RON[x] = 0; I_{OUT} = 50 mA	-40		40	%
		I_{OUT}/I_{CS}; RON[x] = 1; I_{OUT} = 30 mA	-35		35	%
K_2	Current sense ratio at different currents	I_{OUT}/I_{CS}; RON[x] = 0; I_{OUT} = 100 mA	1000	1650	2500	
		I_{OUT}/I_{CS}; RON[x] = 1; I_{OUT} = 50 mA	500	825	1250	
dK_2/K_2 (2)	Current sense ratio drift with temperature	I_{OUT}/I_{CS}; RON[x] = 0; I_{OUT} = 100 mA	-25		25	%
		I_{OUT}/I_{CS}; RON[x] = 1; I_{OUT} = 50 mA	-25		25	%
K_3	Current sense ratio at different currents	I_{OUT}/I_{CS}; RON[x] = 0; I_{OUT} = 300 mA	1500	1900	2200	
		I_{OUT}/I_{CS}; RON[x] = 1; I_{OUT} = 100 mA	650	900	1100	
dK_3/K_3 (2)	Current sense ratio drift with temperature	I_{OUT}/I_{CS}; RON[x] = 0; I_{OUT} = 300 mA	-10		10	%
		I_{OUT}/I_{CS}; RON[x] = 1; I_{OUT} = 100 mA	-15		15	%
K_4	Current sense ratio at different currents	I_{OUT}/I_{CS}; RON[x] = 0; I_{OUT} = 800 mA	1800	2000	2200	
		I_{OUT}/I_{CS}; RON[x] = 1; I_{OUT} = 400 mA	900	1000	1100	
dK_4/K_4 (2)	Current sense ratio drift with temperature	I_{OUT}/I_{CS}; RON[x] = 0; I_{OUT} = 800 mA	-7.5		7.5	%
		I_{OUT}/I_{CS}; RON[x] = 1; I_{OUT} = 400 mA	-7.5		7.5	%

Table 25. Electrical characteristics (OUT1 - OUT8) (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{CS_offset}	I_{CS} offset current @25°C	I_{CS} @ I_{OUT} = 0 A	0	9	25	µA
$I_{CS\_drift\_ratio}$(2)	I_{CS_offset} variation between I_{CS} at 25°C and I_{CS} at 150°C or I_{CS} at -40°C		-60		60	%
ΔK_{LRON}	Offset compensated K-factor at low R_{ON}	I_{OUT} = 50 mA	1725		2090	
ΔK_{HRON}	Offset compensated K-factor at high R_{ON}	I_{OUT} = 30 mA	850		1040	
I_{CS_max}	Current sense full scale range	Typical value for OC at 25°C			850	µA
V_{CS}	Current sense output voltage	Nominal voltage range	0		V_{DD} - 1	V

1. Value can be higher and vary during active pulse shaping
2. Parameter guaranteed by design and characterization; not subject to production test.

Table 26. Electrical transient requirements (part 1/3)

ISO 7637-2: 2004(E) test pulse	Test levels (1)		Number of pulses or test times	Burst cycle / pulse repetition time		Delays and impedance
	III	IV		Min.	Max.	
1	-75V	-100V	5000 pulses	0.5s	5s	2 ms, 10Ω
2a	+37V	+50V	5000 pulses	0.2s	5s	50µs, 2Ω
3a	-100V	-150V	1h	90ms	100ms	0.1µs, 50Ω
3b	+75V	+100V	1h	90ms	100ms	0.1µs, 50Ω
4	-6V	-7V	1 pulse			100ms, 0.01Ω
5b(2)	+65V	+87V	1 pulse			400ms, 2Ω

1. The above test levels must be considered referred to V_S = 13.5 V except for pulse 5b.
2. Valid in case of external load dump clamp: 40V maximum referred to ground (-40°C < T_j < 150°C).

Table 27. Electrical transient requirements (part 2/3)

ISO 7637-2: 2004E test pulse	Test level results	
	III	VI
1	E	E
2a	C	C
3a	C	C
3b	C	C

Table 27. Electrical transient requirements (part 2/3) (continued)

ISO 7637-2: 2004E test pulse	Test level results	
	III	VI
4	C	C
5b(1)	C	C

1. Valid in case of external load dump clamp: 40V maximum referred to ground (-40°C < T_j < 150°C).

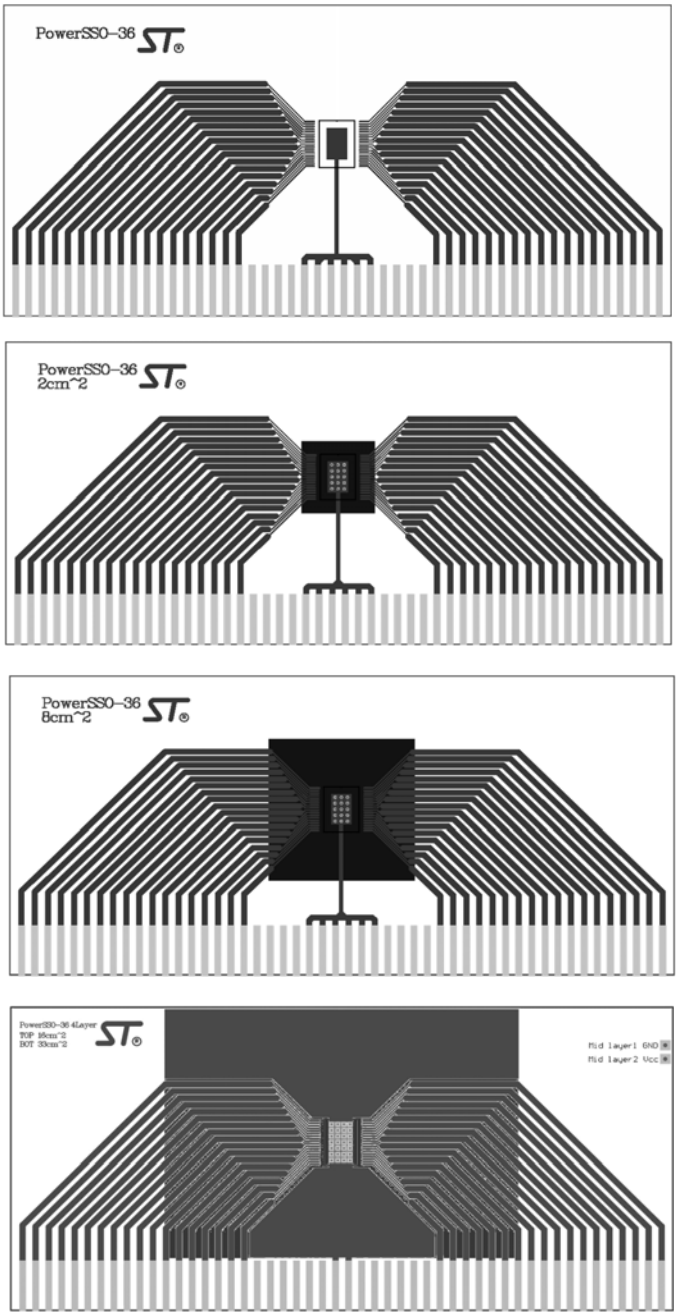
Table 28. Electrical transient requirements (part 3/3)

Class	Contents
C	All functions of the device performed as designed after exposure to disturbance.
E	One or more functions of the device did not perform as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

5 Package and PCB thermal data

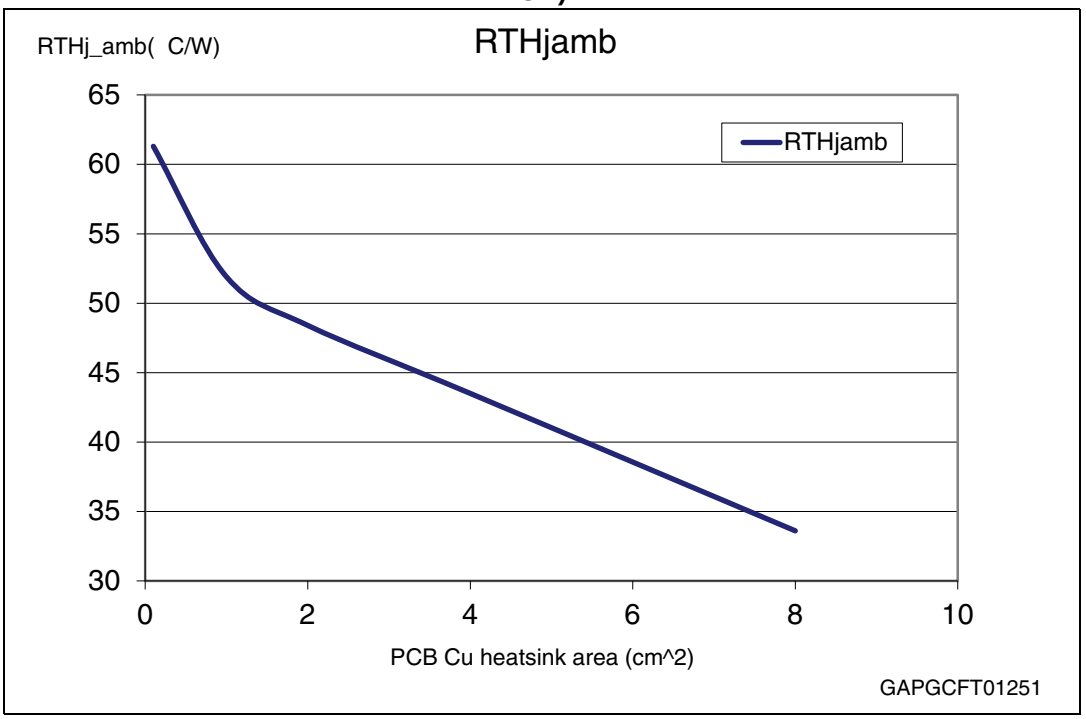
5.1 PowerSSO-36 thermal data

Figure 9. PowerSSO-36 PC board



Note:
Board finish thickness 1.6 mm +/- 10%; Board double layer and four layers; Board dimension 129x60; Board Material FR4; Cu thickness 0.070 mm (outer layers); Cu thickness 0.035 mm (inner layers); Thermal vias separation 1.2 mm; Thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias 0.025 mm; Footprint dimension 4.1 mm x 6.5 mm

Figure 10. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition (one channel ON)



6 Package information

6.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com.

ECOPACK® is an ST trademark.

6.2 PowerSSO-36™ mechanical data

Figure 11. PowerSSO-36™ package dimensions

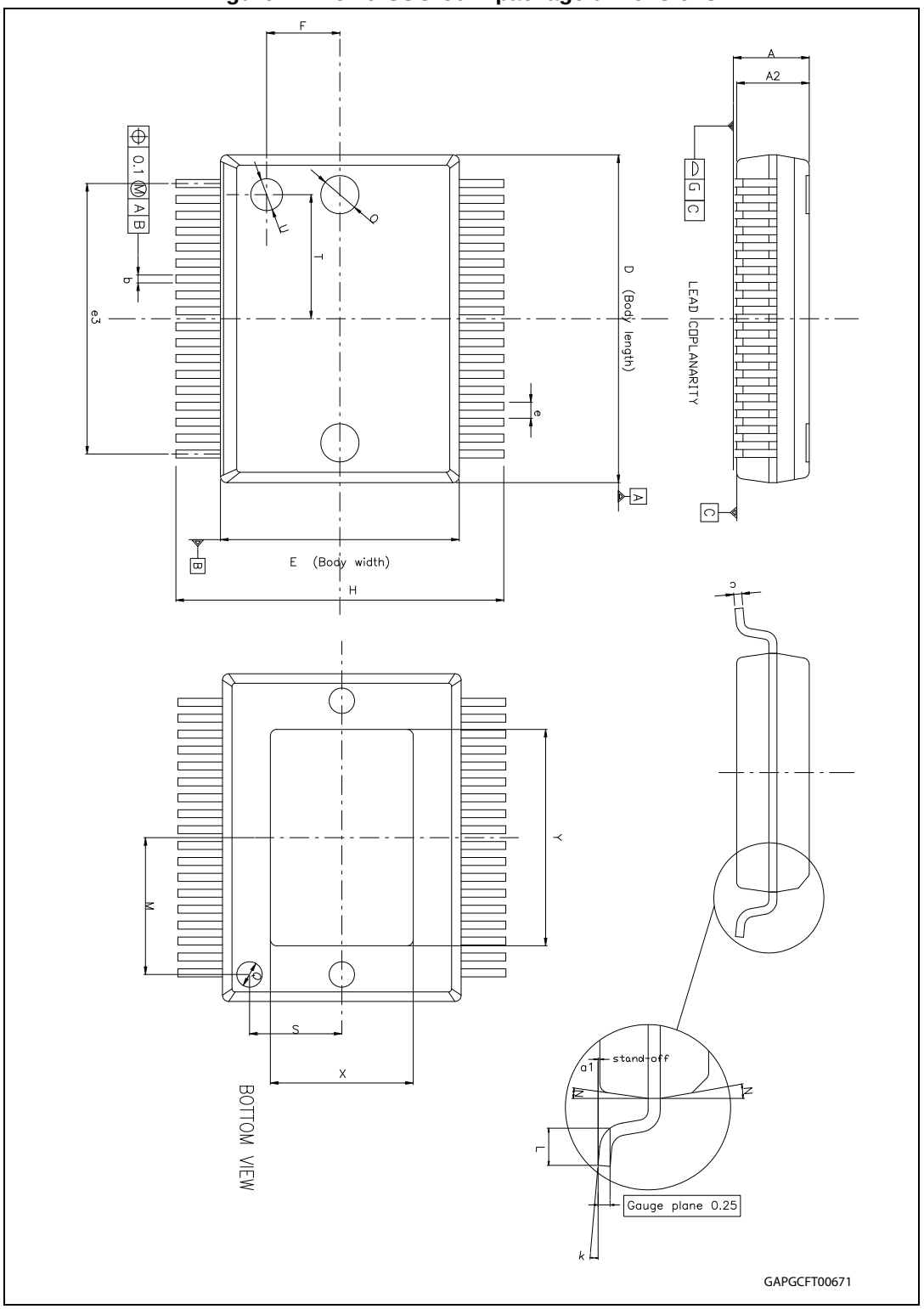


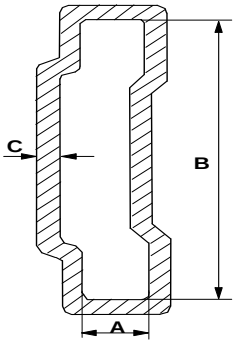
Table 29. PowerSSO-36™ mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	2.15	—	2.45
A2	2.15	—	2.35
a1	0	—	0.1
b	0.18	—	0.36
c	0.23	—	0.32
D	10.10	—	10.50
E	7.4	—	7.6
e	—	0.5	—
e3	—	8.5	—
F	—	2.3	—
G	—	—	0.1
H	10.1	—	10.5
h	—	—	0.4
k	0°	—	8°
L	0.55	—	0.85
M	—	4.3	—
N	—	-	10°
O	—	1.2	—
Q	—	0.8	—
S	—	2.9	—
T	—	3.65	—
U	—	1.0	—
X(1)	4.3	—	5.2
Y(1)	6.9	—	7.5

1. Corresponding to internal variation C.

6.3 Packing information

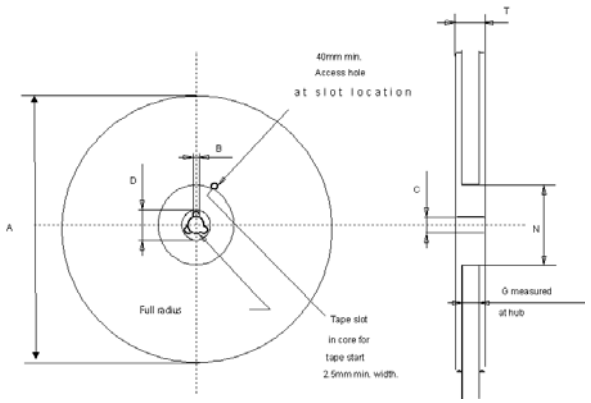
Figure 12. PowerSSO-36 tube shipment (no suffix)



Base Q.ty	49
Bulk Q.ty	1225
Tube length (± 0.5)	532
A	3.5
B	13.8
C (± 0.1)	0.6

All dimensions are in mm.

Figure 13. PowerSSO-36 tape and reel shipment (suffix "TR")



REEL DIMENSIONS

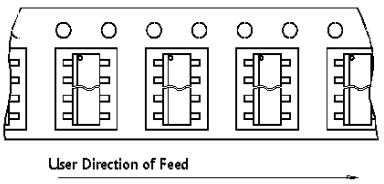
Base Q.ty	1000
Bulk Q.ty	1000
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	100
T (max)	30.4

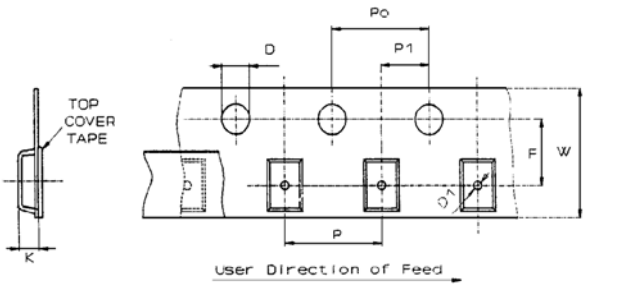
TAPE DIMENSIONS

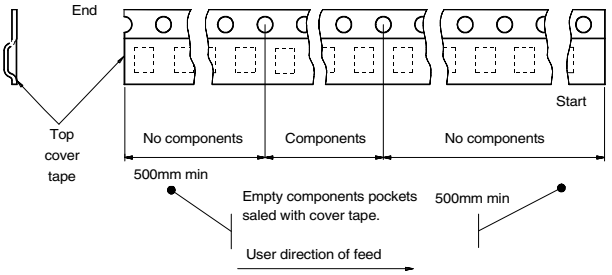
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	12
Hole Diameter	**D (± 0.05)**	1.55
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.1)**	11.5
Compartment Depth	**K (max)**	2.85
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







7 Revision history

Table 30. Document revision history

Date	Revision	Changes
08-Nov-2012	1	Initial release.
03-Dec-2012	2	*Table 19: Temperature warning and thermal shutdown*: – added note *Table 21: Digital timings*: – added note *Table 22: Electrical characteristics (logic + inputs)*: – $f_{CLK\ fail\ low}$: added note *Table 23: Dynamic characteristics (SPI)*: – added note *Table 24: Switching (V_S = 12 V; T_j = 25°C)*: – $t_{d(on)}$, $t_{d(off)}$, t_{SKEW}: updated max. value *Table 25: Electrical characteristics (OUT1 - OUT8)*: – I_{CS_offset}, $I_{CS\_drift\_ratio}$: updated values – ΔK_{LRON}, ΔK_{HRON}: added rows
24-Apr-2013	3	Updated *Features* list Updated *Section 1.1: Power supply (VS, GND)* and *Section 2.3: Current Sense (CS) – analog diagnosis* Removed *Figure 4: Typical output voltage waveforms (rising/falling edge)* Updated introduction of *Chapter 3: SPI interface* Updated *Table 13: SDR registers* Updated *Section : Address #12 Silicon Version* Updated *Table 20: Thermal data* *Table 22: Electrical characteristics (logic + inputs)*: – V_{PORH}, V_{PORL}: updated parameter and values – $t_{DSENSE1H}$, ΔK_{LRON}, ΔK_{HRON}: updated values – K_0, dK_0/K_0: removed rows Added *Figure 10: $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition (one channel ON)*
19-Sep-2013	4	Updated Disclaimer.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR “AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL” INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.
Information in this document supersedes and replaces all information previously supplied.
The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com