ILLUMINANT 北極光企業有限公司

PRODUCT SPECIFICATION FOR TFT LCM

CUSTOMER:	
MODEL NO:	I3504-6HMT3224B
ACCEPTED BY:	

APPROVED BY:	CHECKED BY:	ORGANIZED BY:
LCM產品部 2008.01.23 隆茂生	LCM產品部 2008.01.23 贺秋芳	LCM產品部 2008.01.23 贺秋芳

■Approval for Specifications Only

□Approval for Specifications and Sample

Note: 1. Version of Specifications : 1

2. Others: Rohs Compliment

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Version	Date	Contents
1	08/01/23	Initial Release

CONTENTS

1. Mechanical Specification

Item	Standard Value	Unit
Display Size	3.5	inch
Module Dimension	77.3(W)*64.1(H)*4.10(D)	mm
Active Area	70.08(W)*52.56(H)	mm
Number of Dots	320RGB*240Dots	Dot
Pixel Arrangement	RGB Vertical Stripe	-
Pixel Pitch	0.219(W)mm*0.219(H)mm	mm
LCD Type	Normal White / Transmissive	-
Viewing Direction	6H	-
Driver	HX8238-A	-
Approx. Weight	-	g
Various Color Display	262	K
Backlight Color	White	
Chip Connection	3-LED Serial *2	

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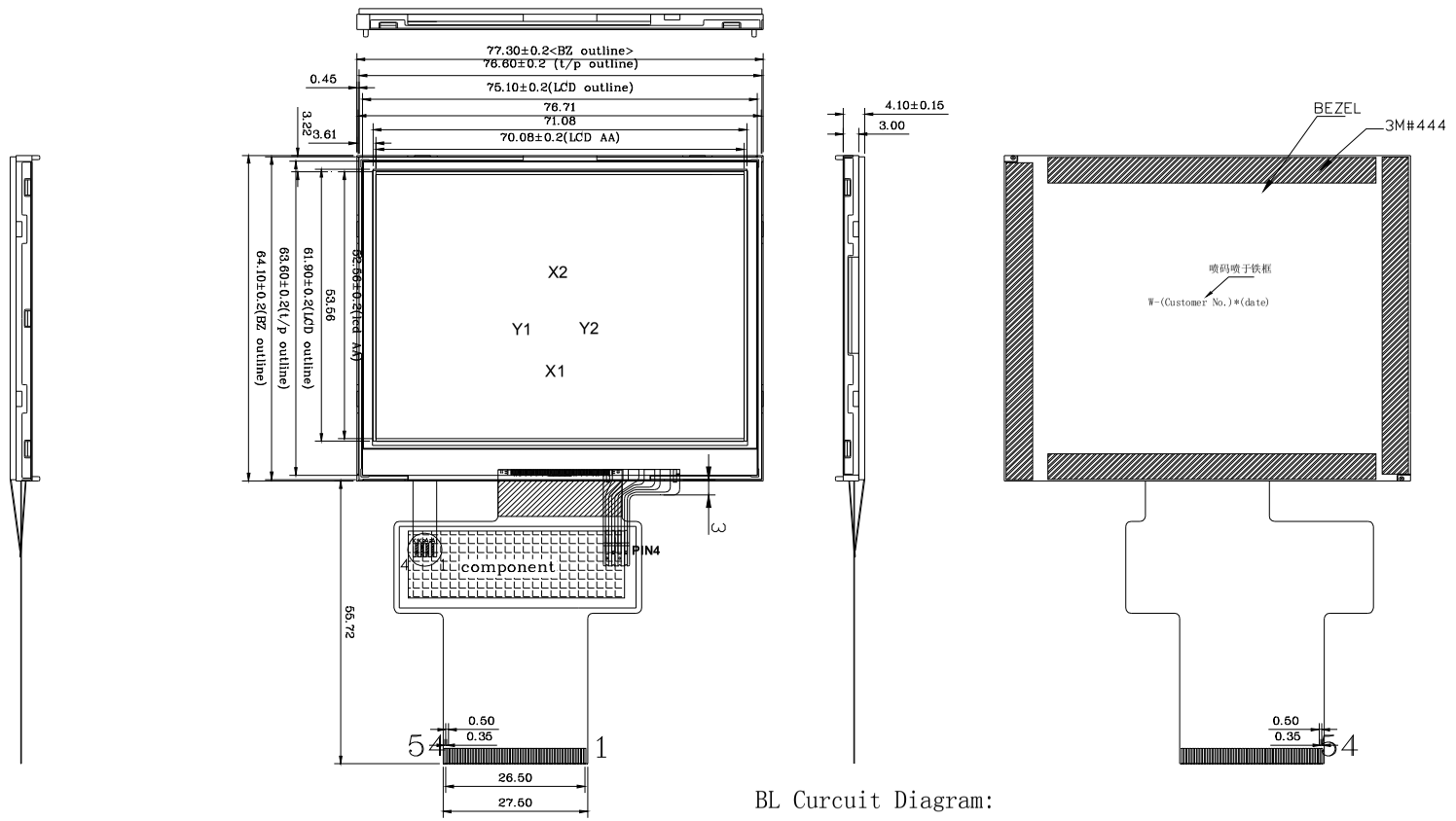
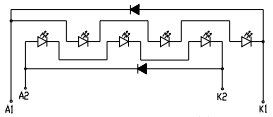


BL Curcuit Diagram:



CIRCUIT DIAGRAM
LED: 3 X 2=6 DIES

FPC INTERFACE

1	VBL−	11	SPDI	21	G1	31	R3	41	VCC	51	NC
2	VBL−	12	B0	22	G2	32	R4	42	VCC	52	ENB
3	VBL+	13	B1	23	G3	33	R5	43	Y2	53	GND
4	VBL+	14	B2	24	G4	34	R6	44	X2	54	GND
5	Y1	15	B3	25	G5	35	R7	45	NC		
6	X1	16	B4	26	G6	36	HSYNC	46	NC		
7	SPDO	17	B5	27	G7	37	VSYNC	47	NC		
8	/RESET	18	B6	28	R0	38	DCLK	48	IF2		
9	SPENA	19	B7	29	R1	39	NC	49	IF1		
10	SPCLK	20	G0	30	R2	40	NC	50	IF0		

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					1	New Drawing			
					REVISION	CONTENT			DATE
TOLERANCE	0~15	±0.2	61~150	±0.2	DRAWING		DATE	TITLE	
	16~60	±0.2	151~		CHECK		DATE	TYPE	ASSEMBLY
	UNIT	mm	SCALE	None	APPROVE		DATE	PAGE	1 OF 1

2. Absolute Maximum Ratings

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Supply Voltage for Logic	V_{DD}	-0.3		+4.0	V	
Input voltage	Vin	-0.5		V_{DD} +0.5	V	
Operating Temperature	TOP	-20	-	+60	℃	-
Storage Temperature	TST	-30	-	+70	℃	-

*NOTE: Based on Vss=0V.

3. Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage for Logic	V_{CC}	Ta=25℃	2.4	2.8	3.3	V
High-level input voltage	VIHC	Vcc=2.8V	0.8 V_{DD}		V_{DD}	
Low-level input voltage	VILC	Vcc=2.8V	0		0.2 V_{DD}	
TFT Gate ON Voltage	VGH	Vcc=2.8V	--	15	--	-
TFT Gate OFF Voltage	VGL	Vcc=2.8V	--	-10	--	V
VCOM	VCOMH		2.5	3.6	4.5	
	VCOML		-3	-2.4	0	
Power Supply Current for VDD	I_{DD}	V_{DD}=2.8V	-	-	42.24	mA

4. Optical Characteristics

Item		Symbol	Condition	Specifications			Unit	Remark
				Min.	Typ.	Max.		
Contrast Ration		CR	Viewing Normal Angle $\Theta x = \Theta y = 0°$	380	400	-	-	Note 5,6
Response Time		T_R		-	15	20	ms	Note 2
		T_F		-	35	50	ms	Note 2
Chromaticity Coordinates (Without Polarizer)	Red	X_R		(0.5908)	(0.6208)	(0.6508)	-	Note 5,6
		Y_R		(0.334)	(0.364)	(0.394)		
	Green	X_G		(0.3181)	(0.3481)	(0.3781)		
		Y_G		(0.5368)	(0.5668)	(0.5968)		
	Blue	X_B		(0.1034)	(0.1334)	(0.1634)		
		Y_B		(0.0469)	(0.0769)	(0.1069)		
	White	X_W		(0.2676)	(0.2976)	(0.3276)		
		Y_W		(0.2756)	(0.3056)	(0.3356)		
Viewing Angle	Hor.	Θ_{X+}	Center CR≧10		45	-	deg.	Note 3
		Θ_{X-}			45	-		
	Ver.	Θ_{Y+}		-	15	-		
		Θ_{Y-}		-	35	-		
The Brightness of Module		B	$\Theta x = \Theta y = 0°$	300	-	-	cd/m^2	Note 5,6
The Uniformity of Brightness		-	-	75	-	-	%	Note 7

Note (1) Definition of Contrast Ration (CR) :

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

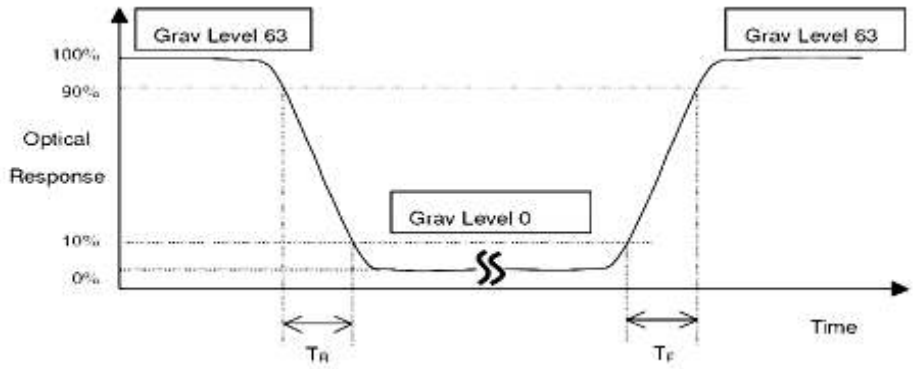
L63 : Luminance of grey level 63

L0 : Luminance of grey level 0

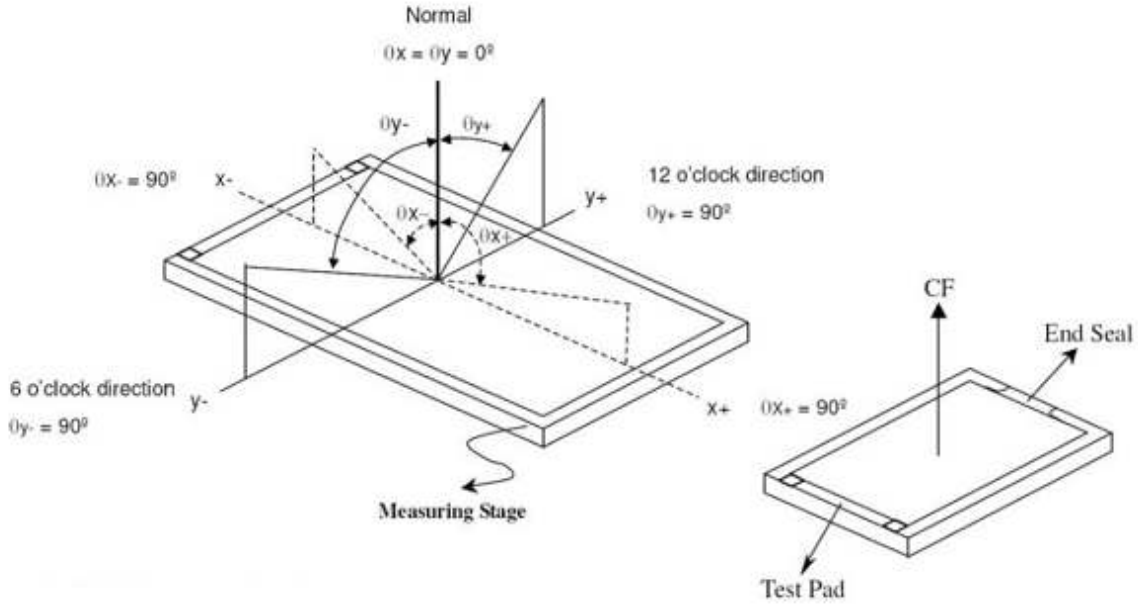
CR = CR (10)

CR (X) is corresponding to the Contrast Ration of the point X at figure in Note (5).

Note (2) Definition of Response Time (T_R, T_F) :

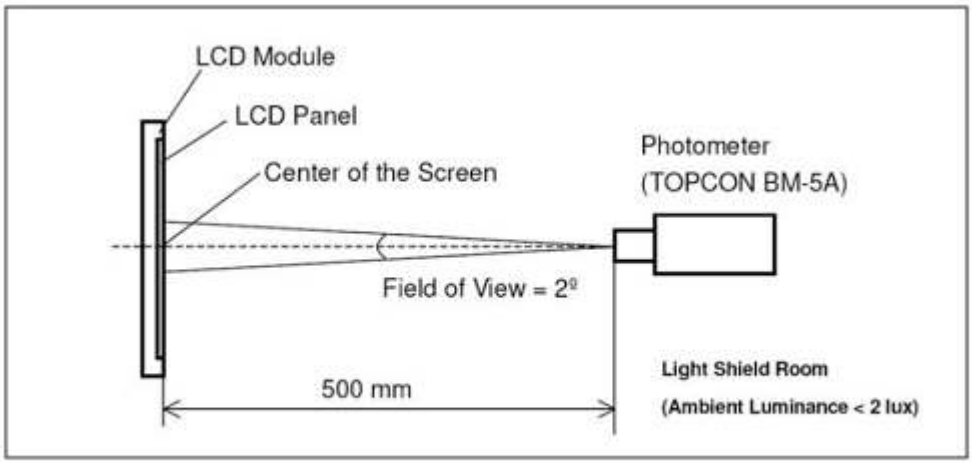


Note (3) Definition of Viewing Angle



Note (4) Measurement Set-Up:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20minutes in a windless room.

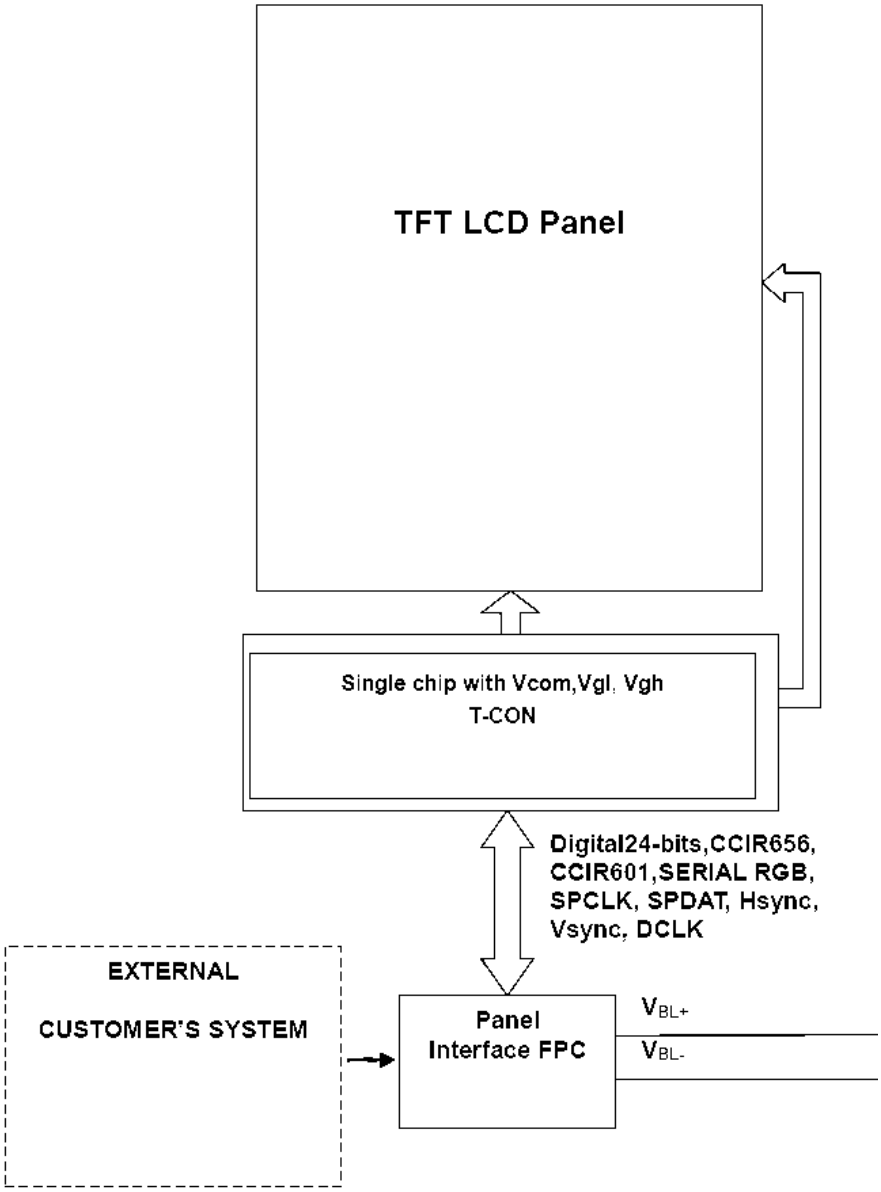


5. Interface

No.	Symbol	I/O	Function
1	VBL-	I	Backlight LED Ground
2	VBL-	I	Backlight LED Ground
3	VBL+	I	Backlight LED Power
4	VBL+	I	Backlight LED Power
5	Y1	I	T/P Top Electrode
6	X1	I	T/P Right Electrode
7	SPDO	O	SPI Output
8	/RESET	-	LCM Reset
9	SPENA	I	SPI interface Data Enable signal
10	SPCLK	I	SPI Clock
11	SPDI	I	SPI Input
12	B0	I	Blue Data Bit
13	B1	I	Blue Data Bit
14	B2	I	Blue Data Bit
15	B3	I	Blue Data Bit
16	B4	I	Blue Data Bit
17	B5	I	Blue Data Bit
18	B6	I	Blue Data Bit
19	B7	I	Blue Data Bit
20	G0	I	Green Data Bit
21	G1	I	Green Data Bit
22	G2	I	Green Data Bit
23	G3	I	Green Data Bit
24	G4	I	Green Data Bit
25	G5	I	Green Data Bit
26	G6	I	Green Data Bit
27	G7	I	Green Data Bit
28	R0	I	Red Data Bit
29	R1	I	Red Data Bit

30	R2	I	Red Data Bit
31	R3	I	Red Data Bit
32	R4	I	Red Data Bit
33	R5	I	Red Data Bit
34	R6	I	Red Data Bit
35	R7	I	Red Data Bit
36	HSYNC	I	Horizontal Sync Input
37	VSYNC	I	Vertical Sync Input
38	DCLK	I	Dot Data Clock
39	NC		Not use
40	NC		Not use
41	VCC	I	Digital Power
42	VCC	I	Digital Power
43	Y2	I	Tp Bottom Electrode
44	X2	I	Tp Left Electrode
45	NC		Not use
46	NC		Not use
47	NC		Not use
48	IF2	I	Control the input data format
49	IF1	I	Control the input data format
50	IF0	I	Control the input data format
51	NC		Not use
52	DE	I	Data Enable Input
53	GND	I	Ground
54	GND		Ground

6. Block Diagram



7. Timing Control

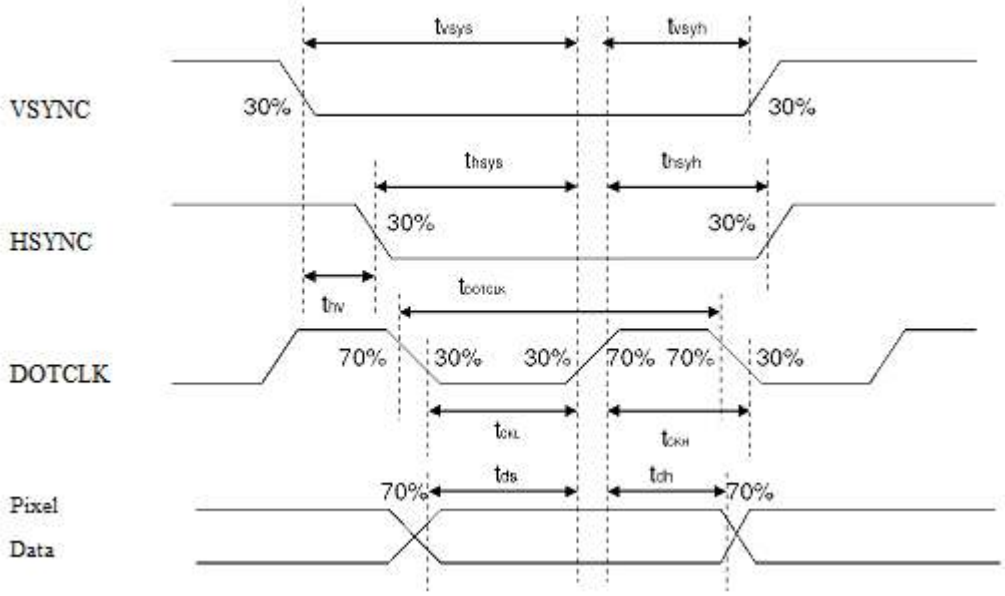
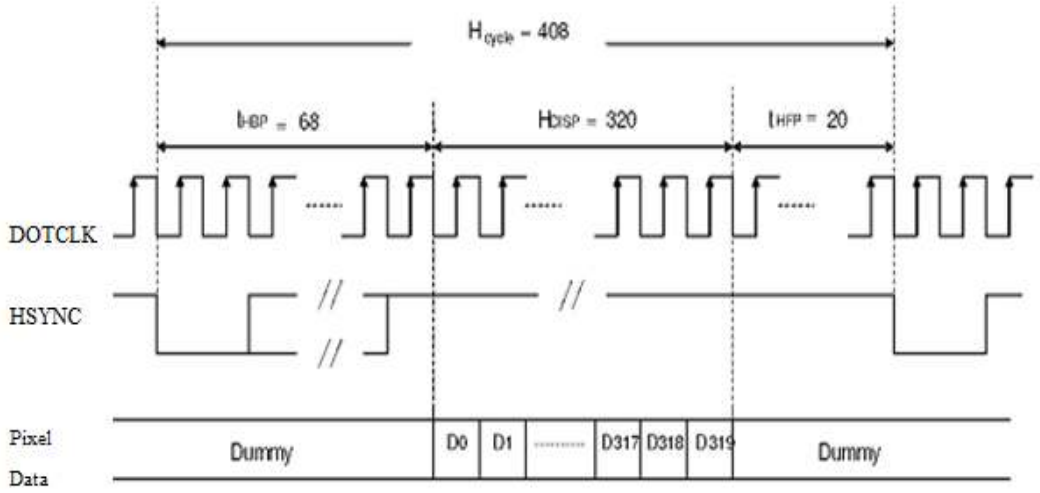


Figure 13. 1 Pixel Timing

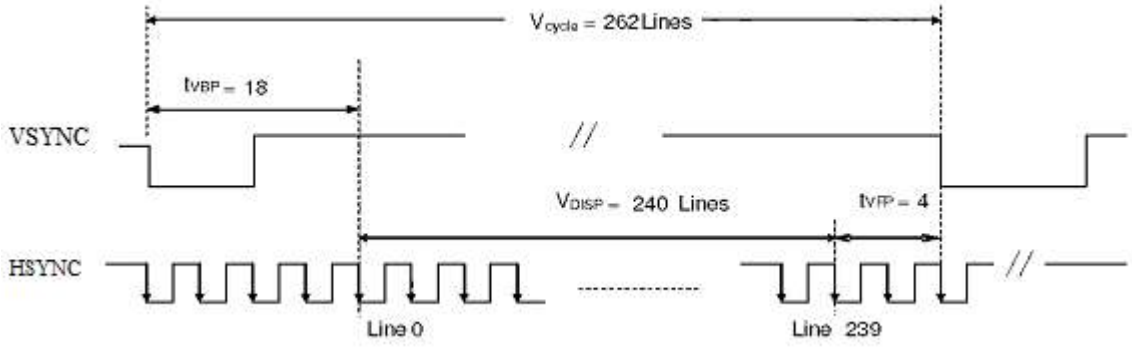
Characteristics	Symbol	Min.		Typ.		Max.		Unit
		24 Bit	8 Bit	24 Bit	8 Bit	24 Bit	8 Bit	
DOTCLK Frequency	fDOTCLK	-	-	6.5	19.5	10	30	MHz
DOTCLK Period	tDOTCLK	100	33.3	154	51.3	-	-	ns
Vertical sync setup time	tvsys	20	10	-	-	-	-	ns
Vertical sync hold time	tvsyh	20	10	-	-	-	-	ns
Horizontal sync setup time	thsys	20	10	-	-	-	-	ns
Horizontal sync hold time	thsyh	20	10	-	-	-	-	ns
Phase difference of sync signal falling edge	thv	1		-		240		tDOTCLK
DOTCLK Low period	tCKL	50	15	-	-	-	-	ns
DOTCLK High period	tCKH	50	15	-	-	-	-	ns
Data setup time	tds	12	10	-	-	-	-	ns
Data hold time	tdh	12	10	-	-	-	-	ns
Reset pulse width	tRES	10		--		-		us

Note : External clock source must be provided to DOTCLK pin of HX8238-A. The driver will not operate if absent of clocking signal.

Table 13. 1 Pixel Timing



a) Horizontal Data Transaction Timing



b) Vertical Data Transaction Timing

Figure 13.2 Data Transaction Timing in Parallel RGB (24bit) Interface (SYNC Mode)

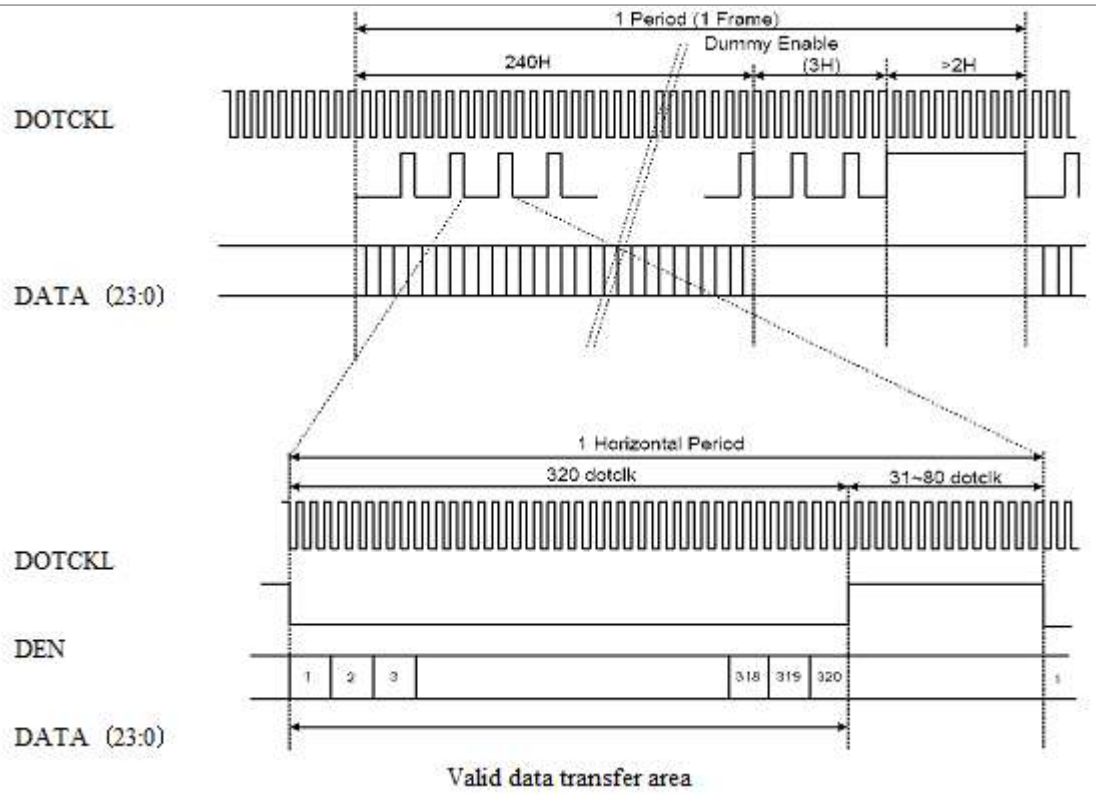
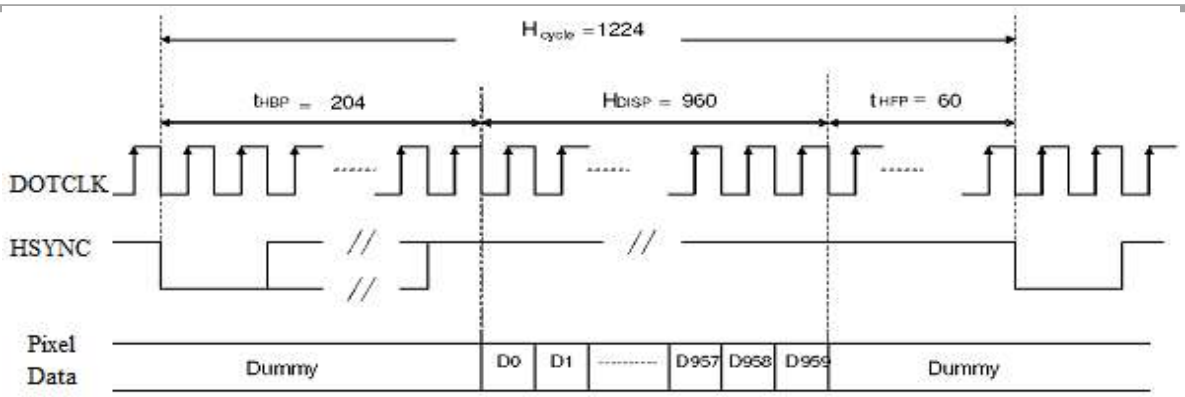


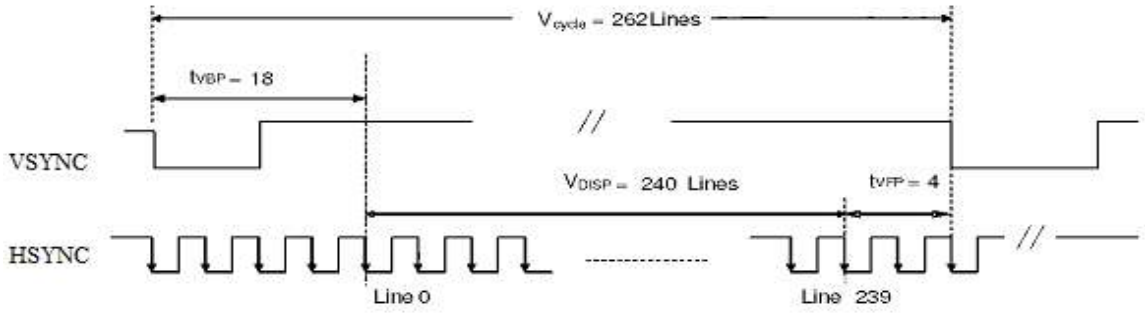
Figure 13.3 Data Transaction Timing in Parallel RGB (24Bit) Interface (DE Mode)

Characteristics		Symbol	Min.		Typ.		Max.		Unit
			24 Bit	8 Bit	24 Bit	8 Bit	24 Bit	8 Bit	
DOTCLK Frequency		fDOTCLK	-	-	6.5	19.5	10	30	MH_Z
DOTCLK Period		tDOTCLK	100	33.3	154	51.3	-	-	ns
Horizontal Frequency (Line)		fH			14.9		22.35		KH_Z
Vertical Frequency (Refresh)		fV			60		90		H_Z
Horizontal Back Porch		tHBP			68	204			tDOTCLK
Horizontal Front Porch		tHFP			20	60			tDOTCLK
Horizontal Data Start Point		tHBP			68	204			tDOTCLK
Horizontal Blanking Period		tHBP + tHFP			88	264			tDOTCLK
Horizontal Display Area		HDISP			320	960			tDOTCLK
Horizontal Cycle		Hcycle			408	1224	450	1350	tDOTCLK
Vertical Back Porch		tVBP			18				Lines
Vertical Front Porch		tVFP			4		-		Lines
Vertical Data Start Point		tVBP			18				Lines
Vertical Blanking Period		tVBP + tVFP			22				Lines
Vertical Display Area	NTSC	VDISP			240				Lines
	PAL				280(PALM=0)				
					288(PALM=1)				
Vertical Cycle	NTSC	Vcycle			262		350		Lines
	PAL				313				

Table 13.2 Data Transaction Timing in Normal Operating Mode



a) Horizontal Data Transaction Timing



b) Vertical Data Transaction Timing

Figure 13.4 Data Transaction Timing in Serial RGB (8Bit) Interface (SYNC Mode)

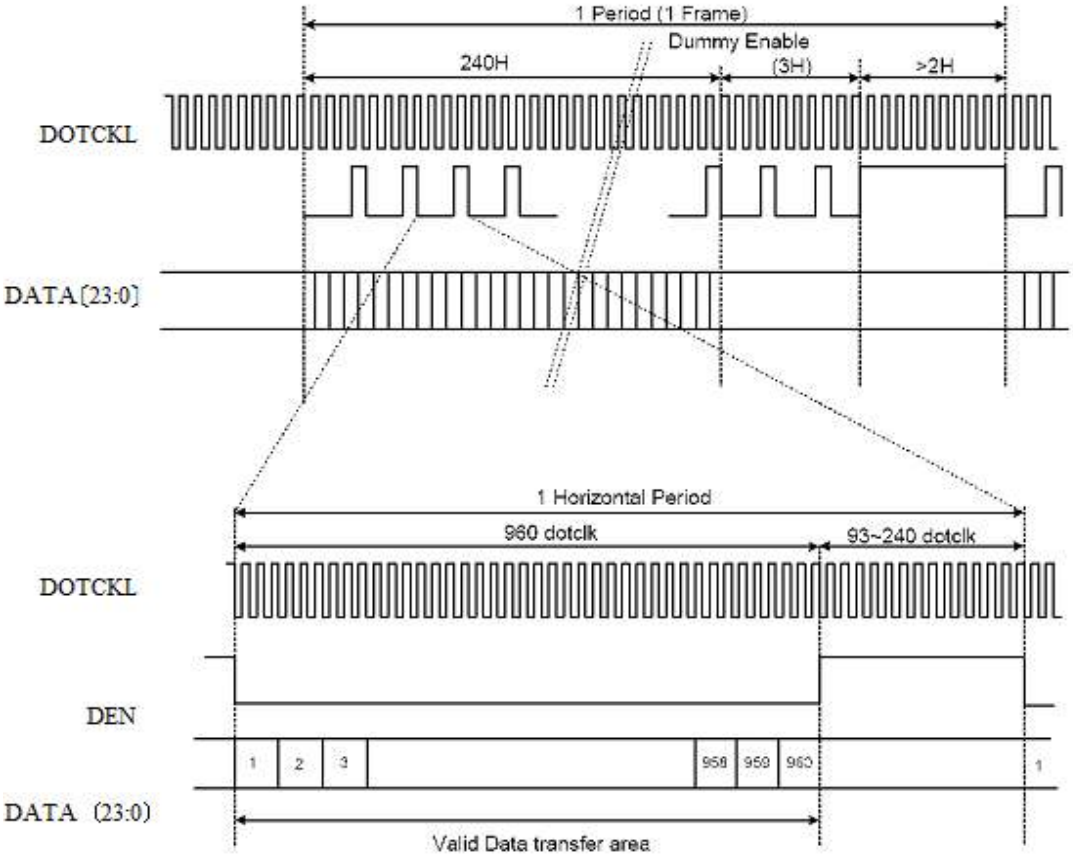
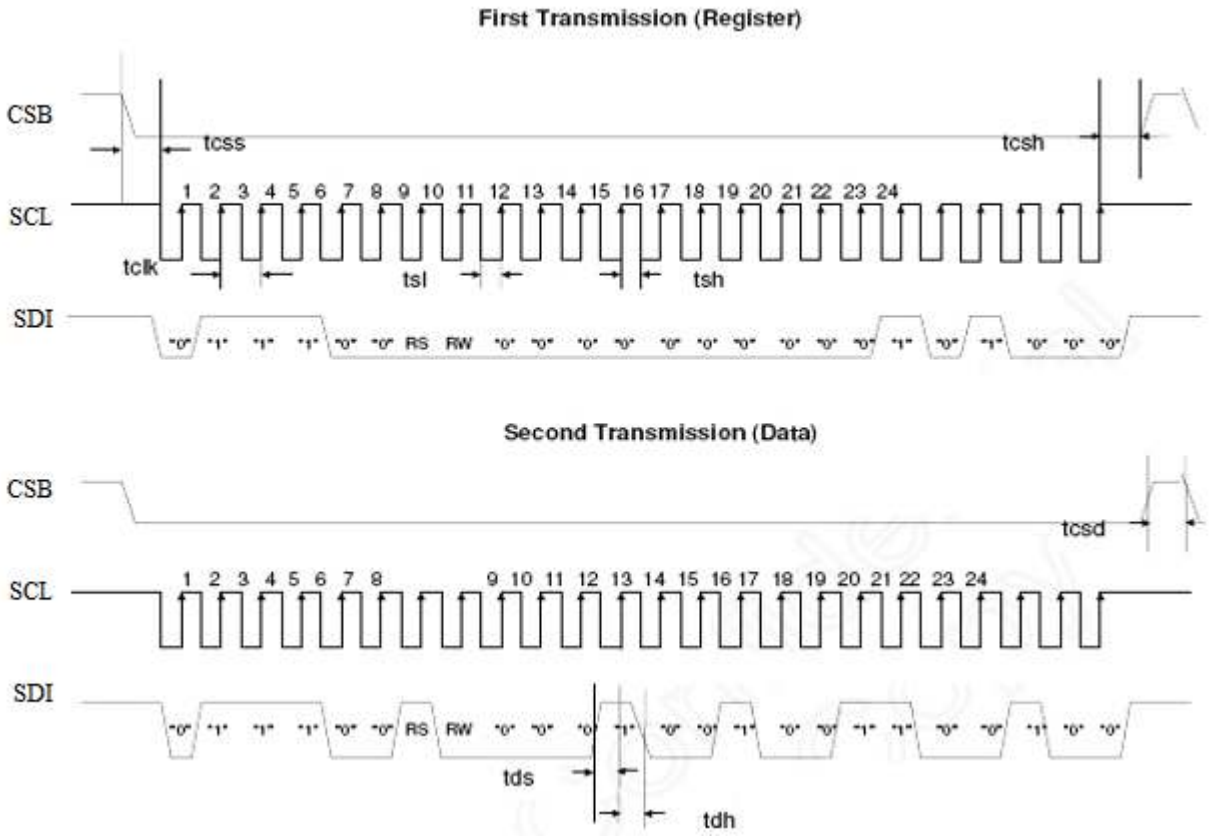


Figure 13.5 Data Transaction Timing in Serial RGB (8Bit) Interface (DE Mode)

SPI interface timing diagram & transaction example



Characteristics	Symbol	Min.	Typ.	Max.	Unit
Serial Clock Frequency	fclk	-	-	20	MH_Z
Serial Clock Cycle Time	tclk	50	-	-	ns
Clock Low Width	tsl	25	-	-	ns
Clock High Width	tsh	25	-	-	ns
Chip Select Set up Time	tcss	0	-	-	ns
Chip Select Hold Time	tcsh	10	-	-	ns
Chip Select High Delay Time	tcsd	20	-	-	ns
Data Setup Time	tds	5	-	-	ns
Data Hold Time	tdh	10	-	-	ns

8. Backlight

8.1 Standard Lamp Styles (Edge Lighting Type):

The LED chips are distributed over the edge light area of the illumination unit, which gives the less power consumption:

8.2 The Main Advantages of the LED Backlight are as Following:

The brightness of the backlight can simply be adjusted by a resistor or a potentiometer.

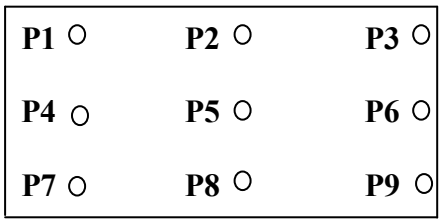
8.3 Data About LED Backlight:

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Forward voltage	**Vf**	**If =40**	**9**	**9.6**	**12**	**V**
Forward current	**If**		**-**	**40**		**mA**
Uniformity	**-**	**If=40**	**75%**	**-**	**-**	**-**
Luminous color	**-**	**White**				
Chip connection	**-**	**3-LED Serial connection *2**				

NOTE:

1.Backlight Only
2.Average Luminous Intensity of P1-P9
3.Uniformity = Min(P1~P9)/Max(P1~P9) * 100%>80%

8.4 Measured Method:



(Effective spatial Distribution)
Hole Diameter±1ø ; 1 to 9per Position Measured Luminous