

# DN8665S

## 8-Bit Shift Register Latch Constant Current Driver IC

### Overview

The DN8665S is a semiconductor integrated circuit which incorporates a 8-bit shift register, a latch driver and a constant current driver to satisfy the demand for equalization of LED panel brightness. It also incorporates the serial-in and serial-out/parallel-out functions. It employs the Bi-CMOS process : The 8-step shift register block and latch block consist of CMOS while the 8-step parallel driver block is bipolar.

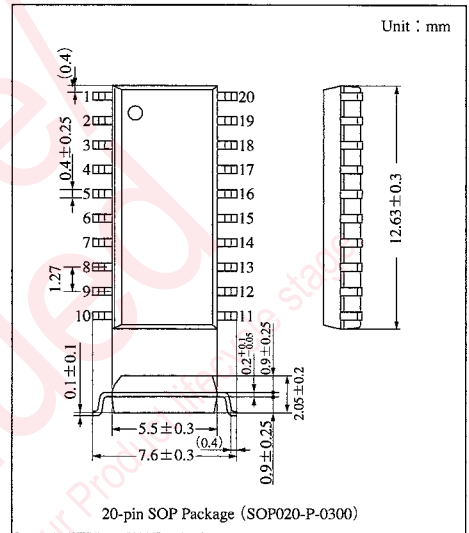
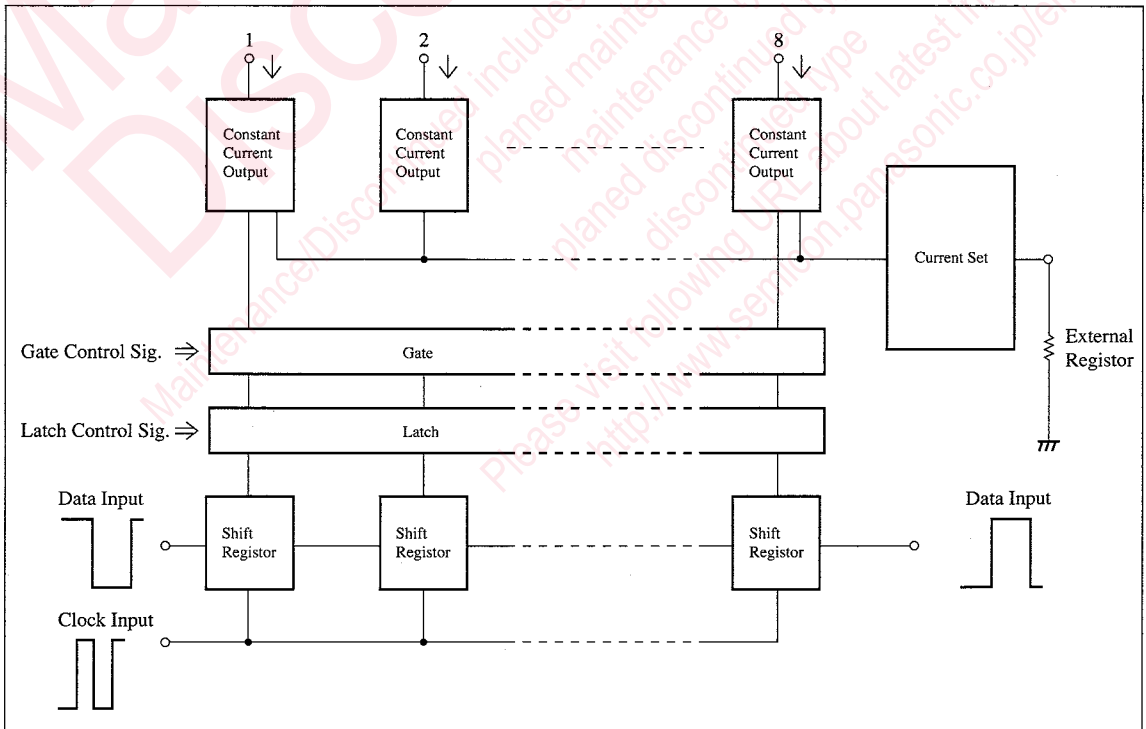
### Features

- Serial-in, serial-out/parallel-out
- Cascade connection possible
- Constant current output (0 to 60 mA able to be set by one external resistor)
- Output-forced ON/OFF pin provided (EN)
- Input/Output CMOS compatible

### Application

- LED panel drive

### Block Diagram



### ■ Absolute Maximum Rating (Ta=25 °C)

Parameter	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	0 to +7.0	V
Input voltage	V <sub>I</sub>	-0.4 to V <sub>CC</sub> +0.4	V
Output voltage <sup>Note 1)</sup>	V <sub>O</sub>	0 to +30	V
Output current	I <sub>O</sub>	80	mA
Single unit IC power dissipation <sup>Note 2)</sup>	P <sub>D</sub>	0.718	W
Reference printed board mounting power dissipation <sup>Note 2)</sup>		1.374	
Operating ambient temperature	T <sub>opr</sub>	-20 to +85	°C
Storage temperature	T <sub>stg</sub>	-55 to +150	°C

Note 1) When output is off

Note 2) It is specified for reference printed board SM (glass epoxy printed board : 50×50×0.8mm) .  
It decreases with rate of 11.0 mW/°C from Ta=25 °C.

### ■ Recommended Operation Range (Ta=25 °C)

Parameter	Symbol	Range
Operating supply voltage	V <sub>CC</sub>	4.5V to 5.5V

### ■ Electrical Characteristics (V<sub>CC</sub>=5V, Ta=25 ± 2°C)

Parameter	Symbol	Condition	min	typ	max	Unit		
Input voltage	Positive direction	$\begin{cases} V_{SOUT}=0.1, V_{CC}-0.1V \\ I_{SOUT}=20\mu A \\ I_O(\overline{Qn})=10\mu, 22mA \\ V_O(\overline{Qn})=1.0V, I_{ref}=-12mA \end{cases}$	0.35V <sub>CC</sub>	—	0.7V <sub>CC</sub>	V		
	Negative direction		0.2V <sub>CC</sub>	—	0.55V <sub>CC</sub>	V		
Input current	I <sub>IH</sub>	V <sub>IH</sub> =5.0V	—	—	25	μA		
	I <sub>IL</sub>	V <sub>IL</sub> =0V	-25	—	—	μA		
Output voltage (SOUT)	V <sub>OH</sub>	V <sub>CC</sub> =5.0V, I <sub>OH</sub> =-0.4mA	4.0	—	—	V		
	V <sub>OL</sub>	V <sub>CC</sub> =5.0V, I <sub>OL</sub> =1.6mA	—	—	0.5	V		
Output current	I <sub>O</sub>	V <sub>O</sub> ( $\overline{Qn}$ )=0.8V	—	—	60	mA		
Output current error between bits	ΔI <sub>O</sub>	V <sub>CC</sub> =5.0V, I <sub>ref</sub> =-12mA V <sub>O</sub> ( $\overline{Qn}$ )=1.0V	—	—	±6	%		
Output leak current	I <sub>OLK</sub>	V <sub>O</sub> =30V (Output OFF)	—	—	50	μA		
	I <sub>OLK</sub>	V <sub>O</sub> =15V (Output OFF)	—	—	25	μA		
Supply current	I <sub>CC1</sub>	Total Driver Output OFF ON V <sub>CC</sub> =5.5V	I <sub>ref</sub> =0mA	—	—	6	mA	
	I <sub>CC2</sub>		I <sub>ref</sub> =-12mA	—	—	45	mA	
	I <sub>CC3</sub>		I <sub>ref</sub> =-12mA	—	—	55	mA	
Maximum clock frequency	f <sub>max</sub>	CLK	12	—	—	MHz		
Transmission delay time	t <sub>PLH</sub>	CLK	SOUT	V <sub>CC</sub> =5.0V R <sub>L</sub> =50Ω C <sub>L</sub> =15pF	—	—	100	ns
	t <sub>PHL</sub>				—	—	100	ns
	t <sub>PLH</sub>	CLK	$\overline{Qn}$		—	—	350	ns
	t <sub>PHL</sub>				—	—	350	ns
	t <sub>PLH</sub>	EN	$\overline{Qn}$		—	—	350	ns
	t <sub>PHL</sub>				—	—	350	ns
	t <sub>PLH</sub>	STB	$\overline{Qn}$		—	—	350	ns
	t <sub>PHL</sub>				—	—	350	ns

■ Recommended Operation Conditions (Ta = -20 ~ +85°C)

Parameter		Symbol	Condition	min	typ	max	Unit
Supply voltage		V <sub>CC</sub>		4.5	5.0	5.5	V
Output voltage		V <sub>O</sub>		—	—	30	V
Input voltage		V <sub>I</sub>		0	—	V <sub>CC</sub>	V
Clock frequency		f <sub>CLK</sub>	Input Duty 40 to 60%	—	—	12	MHz
Input pulse width	CLK	t <sub>w</sub>		33	—	—	ns
	STB			33	—	—	ns
Setting-up time	SIN	t <sub>su</sub>		25	—	—	ns
	STB			33	—	—	ns
Holding time	SIN	t <sub>h</sub>		20	—	—	ns
	STB			10	—	—	ns
Clock pulse rise time		t <sub>r</sub>		—	—	500	ns
Clock pulse fall time		t <sub>f</sub>		—	—	500	ns
Output current <sup>Note)</sup>	$\overline{Q_n}$	I <sub>OUT</sub>		—	—	60	mA
	SOUT	I <sub>OH</sub>		—	—	-0.4	mA
		I <sub>OL</sub>		—	—	1.6	mA

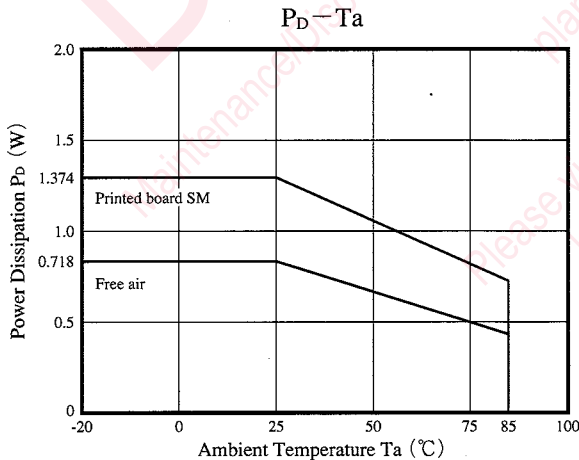
Note) Allowable value is changed, depending on the number of simultaneous ON circuits and duty.  
The power dissipation should be reviewed enough for use of DN8665S.

■ Function Table (Note)

Input				Output			
CLK	STB	EN	SIN	$\overline{Q_0}$	$\overline{Q_m}$	$\overline{Q_7}$	SOUT
↑	H	L	Q <sub>n</sub>	$\overline{Q_n}$	$\overline{Q_{m-1}}$	$\overline{Q_6}$	Q <sub>6</sub>
↑	L	L	Q <sub>n</sub>	nc	nc	nc	Q <sub>6</sub>
↑	×	H	Q <sub>n</sub>	H	H	H	Q <sub>6</sub>
↓	×	×	Q <sub>n</sub>	nc	nc	nc	nc

(Note)  
 H : High level,  
 L : Low level,  
 × : H or L  
 Q<sub>m</sub>, Q<sub>n</sub> : H or L.  
 However, for  $\overline{Q_n}$ , "H" = OFF, "L" = ON.  
 ↑ : Shift from L to H,  
 ↓ : Shift from H to L  
 nc : No change

■ Package Power Dissipation



Note) For SM to printed board (glass epoxy printed board : 50×50×0.8mm).  
 it decreases with rate of 11.0mW/°C from Ta=25 °C.  
 For free air, it decreases with rate of 5.74mW/°C from Ta=25 °C.



**Pin Descriptions**

Pin No.	Symbol	Pin name	Description
1	DGND	Digital ground	Digital ground
2	SIN	Serial data input	It is the serial data input terminal for shift register.
3	CLK	Clock input	The value of shift register shifts at the rising edge of clock input.
4	STB	Strobe input	Setting the STB input to "H" forwards the data of shift register to the latch. When the STB input is set to "L", even if the value of shift register changes, the value of latch is not changed.
5, 7, 8, 10, 11, 13, 14, 16	$\overline{Q_n}$	Driver output	It outputs signals by using the polarity opposite to that of data taken into the latch. For example, when the value of serial input is "H", the output becomes "L" level and the output is turned on. The output takes open collector form of NPN transistor.
6, 9, 12, 15	PGND	Output ground	Output ground
17	EN	Enabling input	When the EN input is set to "H", all the outputs are turned off, independent of condition of shift register and latch driver.
18	SOUT	Serial data output	It is the terminal which performs the serial-output of data inputted from the SIN.
19	RC	Constant current setting input	It connects the external resistor between RC and GND and sets the current of output block. * Output current calculation : $I_o (\overline{Q_n}) \cong \frac{5 \times V_{CC} (V)}{2 \times R_{RC} + 50 (\Omega)}$ ** RC terminal setting calculation : $I_{RC} \cong \frac{V_{CC} (V)}{2 \times R_{RC} + 50 (\Omega)} \quad \text{or} \quad R_{RC} \cong \frac{1}{2} \left( \frac{V_{CC} (V)}{I_{RC} (A)} - 50 \right)$
20	V <sub>CC</sub>	V <sub>CC</sub>	Supply terminal

\* Calculation example

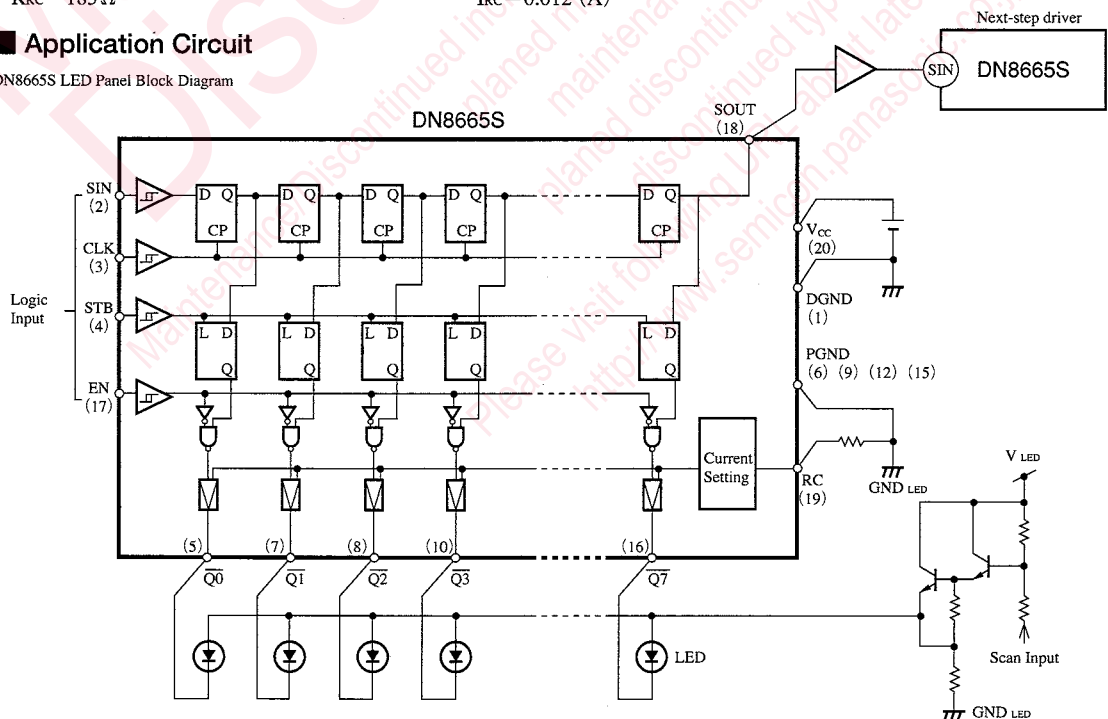
$V_{CC}=5V \quad I_o (\overline{Q_n}) \cong \frac{5 \times 5}{2 \times 183 + 50} \cong 60mA$   
 $R_{RC}=183 \Omega$

\*\* Calculation example

$V_{CC}=5V \quad R_{RC} \cong \frac{1}{2} \left( \frac{5}{0.012} - 50 \right) \cong 183 (\Omega)$   
 $I_{RC}=0.012 (A)$

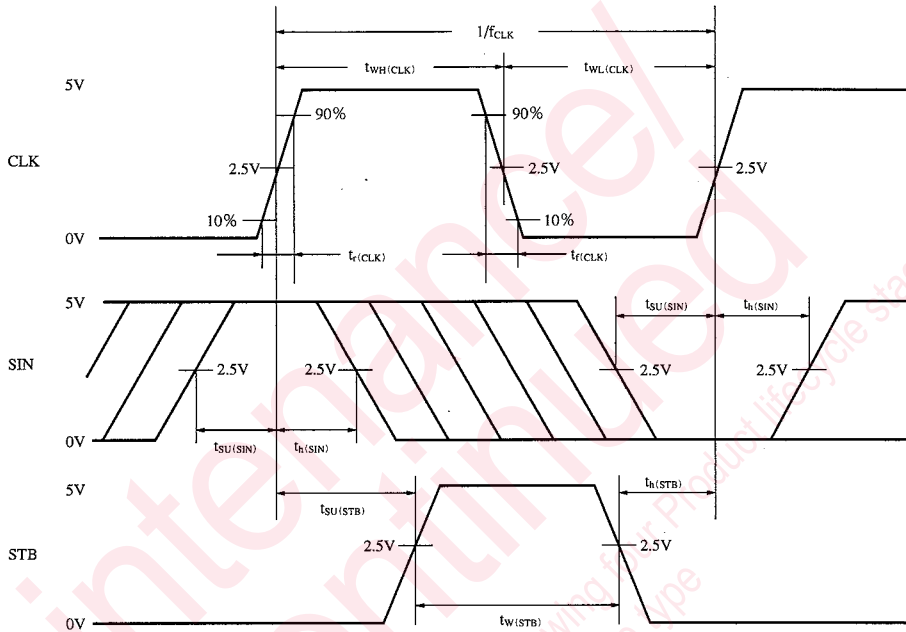
**Application Circuit**

DN8665S LED Panel Block Diagram

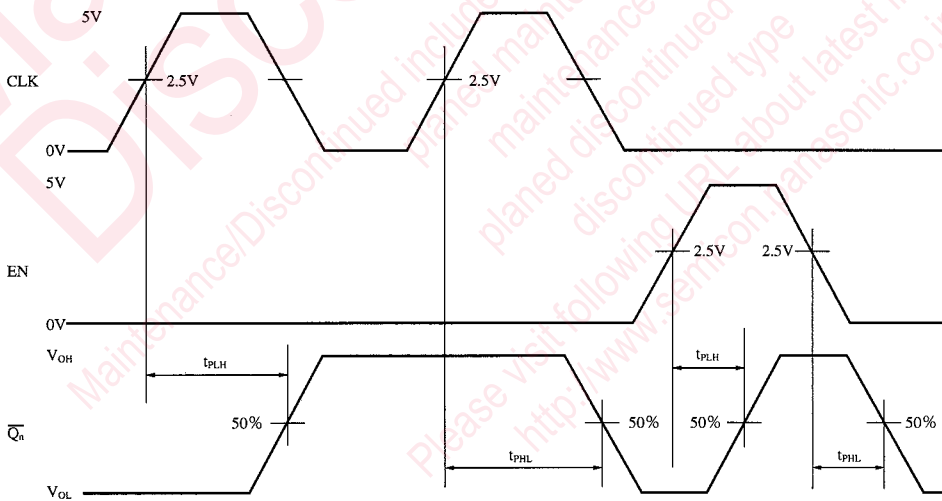


■ Timing Chart

1. Input timing ( $V_{IL}=0V, V_{IH}=5.0V$ )



2. Transmission delay time ( $V_{IL}=0V, V_{IH}=5.0V$ )



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