

# DN8648FBP

## 32-bit Shift Register Latch Driver IC

### ■ Overview

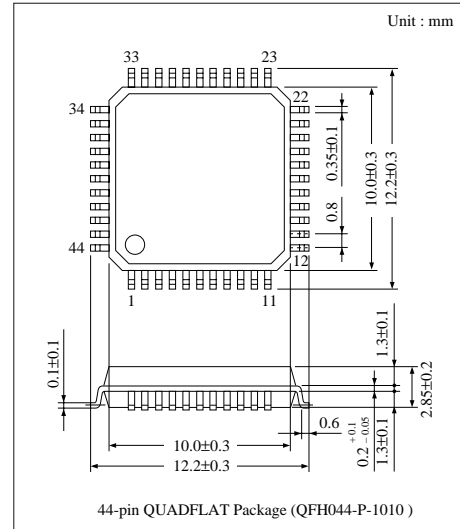
The DN8648FBP is an IC which incorporates a 32-bit shift register and a latch driver to meet high-speed operation low power consumption and high-density printout of the thermal printers for the work processors, and so on. It employs the Bi-CMOS process in which the serial-in and serial-out/parallel-out functions are incorporated, the 32-step shift register block and latch block are composed of CMOS, and the 32-step parallel driver block is bipolar.

### ■ Features

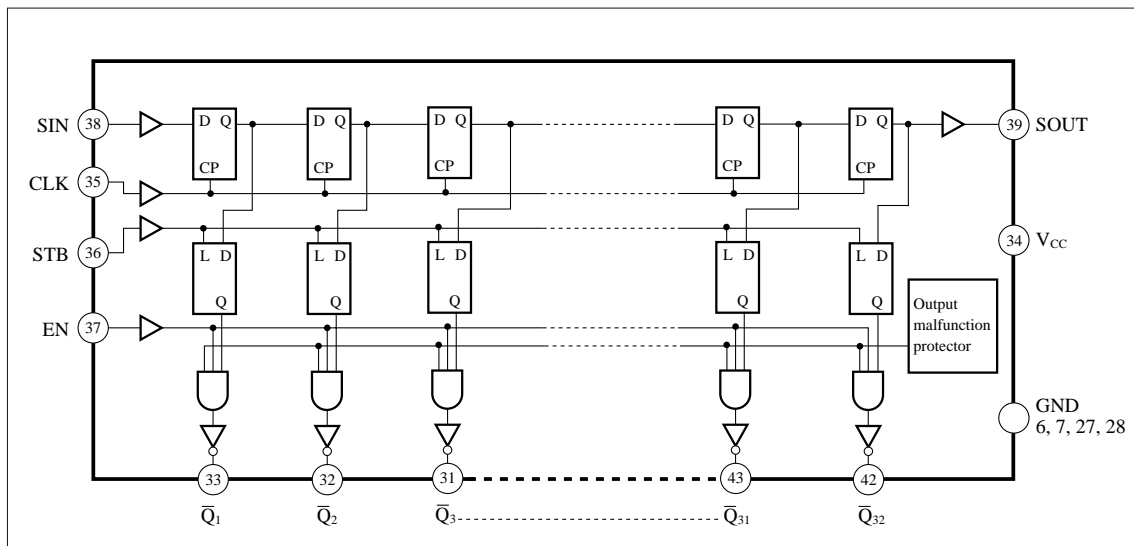
- Serial-in and serial-out/parallel-out
- Cascade connection allowed
- Built-in output malfunctioning preventive circuit
- Low current consumption at standby  $I_{CC} \leq 100\mu A$
- High-breakdown, large current drive type output steps  
Breakdown voltage : 30V  
Output current : 120mA (per pin)
- Surface mountable 44-pin flat package (pin pitch : 0.8mm)

### ■ Applications

- Driving of the thermal heads
- Driving of the relays, LEDs, solenoids, etc.



### ■ Block Diagram



### ■ Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit
Supply voltage	V <sub>CC</sub>	0 to 7	V
Output voltage	V <sub>O</sub>	0 to 30	V
Output current	I <sub>O</sub>	120 (Per one circuit)	mA
Power dissipation	P <sub>D</sub>	1.8 *	W
Operating ambient temperature	T <sub>opr</sub>	- 20 to + 75	°C
Storage temperature	T <sub>stg</sub>	- 55 to + 125	°C

\* When mounting onto the PCB, power dissipation is reduced at a rate of 15mW/°C from Ta= 25°C.

### ■ Recommended Operating Range (Ta=25°C)

Parameter	Symbol	Range	
Operating supply voltage	V <sub>CC</sub>	4 to 6V	
Output voltage	V <sub>O</sub>	below 30V	
Output current	I <sub>O</sub>	below 100mA * <sup>1</sup>	
Clock frequency	f <sub>CLK</sub>	below 10MHz * <sup>2</sup>	
Input pulse width	CLK	t <sub>w</sub>	over 40ns
	STB		over 40ns
Setup time	SIN	t <sub>su</sub>	over 30ns
	STB		over 40ns
Hold time	SIN	t <sub>h</sub>	over 20ns
	STB		over 0ns
Clock pulse rise time	t <sub>r</sub>	below 500ns	
Clock pulse fall time	t <sub>f</sub>	below 500ns	

\*<sup>1</sup> An allowable value changes depends on the number of simultaneously turned-on circuits and the duty. Use with power dissipation taken into full account.

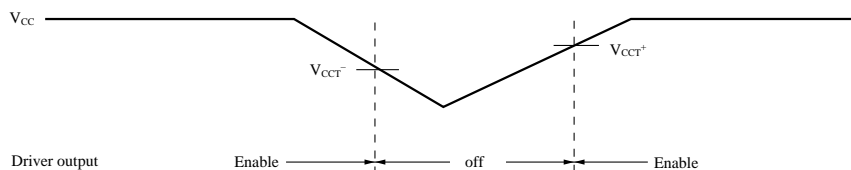
\*<sup>2</sup> Input duty : 40 to 60%

### ■ Electrical Characteristics (Ta=25°C)

Parameter	Symbol	Condition	min	typ	max	Unit
Input voltage	V <sub>IH</sub>	V <sub>CC</sub> = 4 to 6V	0.7V <sub>CC</sub>	—	V <sub>CC</sub>	V
	V <sub>IL</sub>		0	—	0.3V <sub>CC</sub>	V
Input current	I <sub>IH</sub>	V <sub>IH</sub> = 5V	—	—	25	μA
	I <sub>IL</sub>	V <sub>IL</sub> = 0V	—	—	- 25	μA
Output voltage (SOUT)	V <sub>OH</sub>	I <sub>O</sub> = -1μA	4.9	—	—	V
	V <sub>OL</sub>	I <sub>O</sub> = 1μA	—	—	0.1	V
Output current (SOUT)	I <sub>OH</sub>	V <sub>OH</sub> = 4.5V	- 4	—	—	mA
	I <sub>OL</sub>	V <sub>OL</sub> = 0.4V	4	—	—	mA
Output saturation voltage (Q̄n)	V <sub>CE(sat) 1</sub>	I <sub>OL</sub> =100mA	—	—	0.4	V
	V <sub>CE(sat) 2</sub>	I <sub>OL</sub> = 80mA	—	—	0.35	V
Output leakage current	I <sub>OLK1</sub>	V <sub>O</sub> = 30V (output OFF)	—	—	50	μA
	I <sub>OLK2</sub>	V <sub>O</sub> = 15V (output OFF)	—	—	25	μA
Supply current	I <sub>CC1</sub>	Total driver output OFF	—	—	100	μA
	I <sub>CC2</sub>	Driver output 1 circuit ON	—	—	5	mA
Output malfunctioning preventive Circuit operating voltage	V <sub>CCT+</sub>	*	2.9	—	3.9	V
	V <sub>CCT-</sub>	*	2.6	—	3.6	V

\* V<sub>CC</sub>=5V unless otherwise specified

\* Output malfunctioning preventive circuit operating voltage timing chart



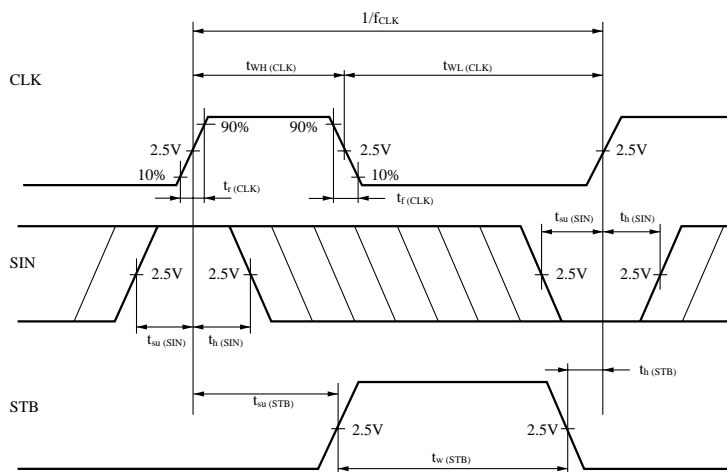
■ Switching Characteristics (Ta = 25°C)

Parameter	Symbol	Input	Output	Condition	min	typ	max	Unit
Maximum clock frequency	$f_{max}$	CLK			10	—	—	MHz
Propagation delay time	$t_{PLH}$	CLK	SOUT	$V_{CC} = 5V$ $C_L = 15pF$	—	—	100	ns
	$t_{PHL}$				—	—	100	ns
	$t_{PLH}$	CLK	$\bar{Q}n$	$V_{CC} = 5V$ $R_L = 100\Omega$	—	—	2	$\mu s$
	$t_{PHL}$				—	—	0.5	$\mu s$
	$t_{PLH}$	EN	$\bar{Q}n$	$C_L = 15pF$	—	—	2	$\mu s$
	$t_{PHL}$				—	—	0.5	$\mu s$

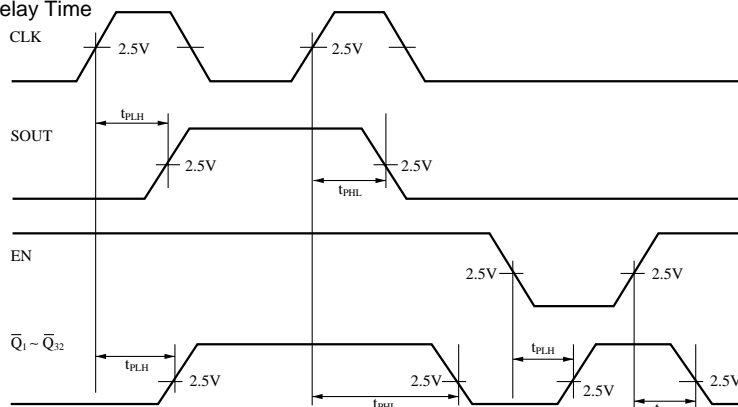
■ Supplementary Descriptions

• Timing Chart

1. Input Timing



2. Propagation Delay Time



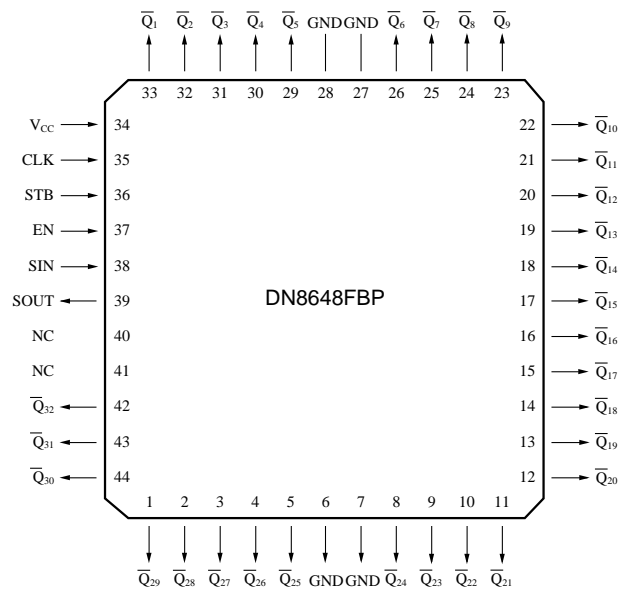
■ Supplementary Descriptions (cont.)

• Function Table

Input				Driver output		SOUT
CLK	EN	STB	SIN	$\bar{Q}_1$	$\bar{Q}_n$	
↑	L	×	×	H	H	$Q'_{31}$
↓	L	×	×	H	H	nc
↑	H	L	×	nc	nc	$Q'_{31}$
↑	H	H	L	H	$\bar{Q}_{n-1}$	$Q'_{31}$
↑	H	H	H	L	$\bar{Q}_{n-1}$	$Q'_{31}$
↓	H	H	×	nc	nc	nc

Note) H = High level, L = Low level, × = Either "H" or "L" will do, ↑ = Transition from "H" to "L",  
 ↓ = Transition from "H" to "L", nc = No change,  $Q'_{31}$  = Status of the 31st shift register

• Pin Assignments



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