CY7C1041BN

256 K × 16 Static RAM

Features

- Temperature range:
  - Commercial: 0 °C to 70 °C
  - Automotive-A: –40 °C to 85 °C
- High speed
  - t_{AA} = 15 ns
- Low active power
  - 1540 mW (max.)
- Low CMOS standby power
  - 2.75 mW (max.)
- 2.0 V data retention (400 µW at 2.0 V retention)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Available in Pb-free and non Pb-free 44-pin TSOP II and molded 44-pin (400-Mil) SOJ packages

Functional Description

The CY7C1041BN is a high-performance CMOS static RAM organized as 262,144 words by 16 bits.

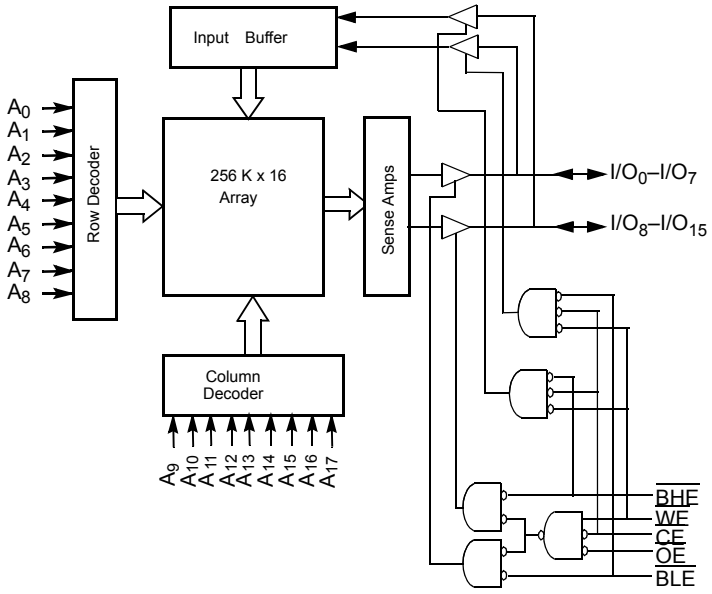
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15}. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

The CY7C1041BN is available in a standard 44-pin 400-mil-wide body width SOJ and 44-pin TSOP II package with center power and ground (revolutionary) pinout.

Logic Block Diagram



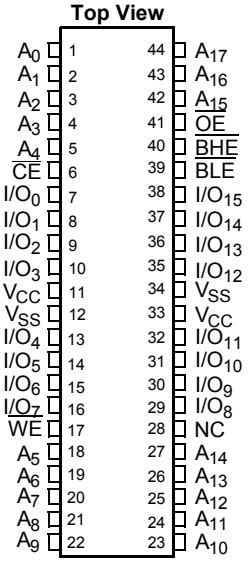
Contents

Selection Guide

Description		-15	-20	Unit
Maximum access time		15	20	ns
Maximum operating current	Commercial	190	170	mA
	Automotive-A	–	190	–
Maximum CMOS standby current	Commercial	0.5	0.5	mA
	Automotive-A	–	6	

Pin Configurations

SOJ
TSOP II
Top View



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on V_{CC} to relative GND[1] .....–0.5 V to +7.0 V

DC voltage applied to outputs in High Z State [1] .....–0.5 V to V_{CC} + 0.5 V

DC input voltage [1] .....–0.5 V to V_{CC} + 0.5 V

Current into outputs (LOW) ..... 20 mA

Operating Range

Range	Ambient Temperature [2]	V_{CC}
Commercial	0 °C to +70 °C	5 V ± 0.5
Automotive-A	–40 °C to +85 °C	

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		-15		-20		Unit
				Min	Max	Min	Max	
V_{OH}	Output HIGH voltage	Min V_{CC}, I_{OH} = –4.0 mA		2.4	–	2.4	–	V
V_{OL}	Output LOW voltage	Min V_{CC}, I_{OL} = 8.0 mA		–	0.4	–	0.4	V
V_{IH}[1]	Input HIGH voltage	–		2.2	V_{CC} + 0.5	2.2	V_{CC} + 0.5	V
V_{IL}[1]	Input LOW voltage	–		–0.5	0.8	–0.5	0.8	V
I_{IX}	Input load current	GND ≤ V_{IN} ≤ V_{CC}		–1	+1	–1	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–1	+1	–1	+1	µA
I_{CC}	V_{CC} operating supply current	Max V_{CC}, f = f_{MAX} = $1/t_{RC}$	Commercial	–	190	–	170	mA
			Automotive-A	–	–	–	190	mA
I_{SB1}	Automatic CE power-down current – TTL inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		–	40	–	40	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V, or V_{IN} ≤ 0.3 V, f = 0	Commercial	–	0.5	–	0.5	mA
			Automotive-A	–	–	–	6	mA

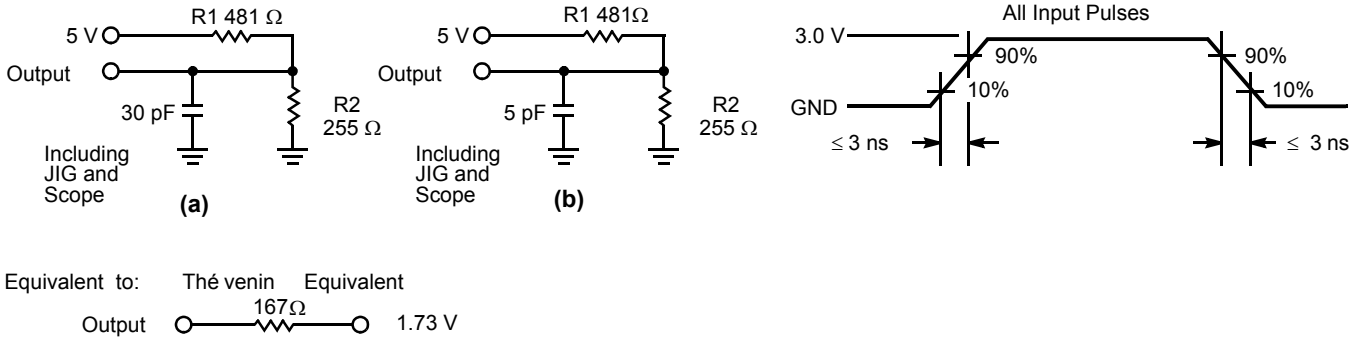
Notes
1. V_{IL} (min.) = –2.0 V for pulse durations of less than 20 ns.
2. T_A is the case temperature.

Capacitance

Parameter [3]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	8	pF
C_{OUT}	I/O capacitance		8	pF

AC Test Loads and Waveforms

Figure 1. AC Test Loads and Waveforms



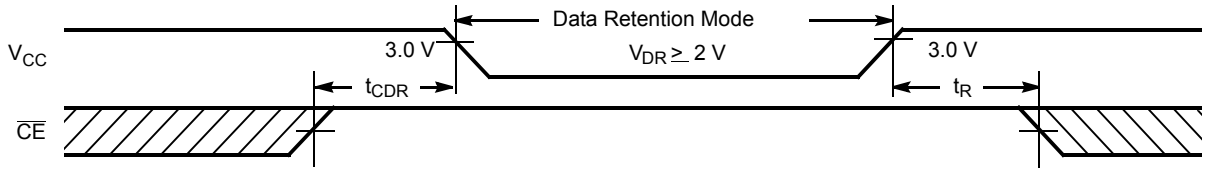
Data Retention Characteristics

Over the Operating Range (Commercial only)

Parameter	Description	Conditions[4]	Min	Max	Unit
V_{DR}	V_{CC} for data retention	–	2.0	–	V
I_{CCDR}	Data retention current	V_{CC} = V_{DR} = 2.0 V, $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V	–	200	µA
t_{CDR}[5]	Chip deselect to data retention time		0	–	ns
t_R[6]	Operation recovery time		t_{RC}	–	ns

Data Retention Waveform

Figure 2. Data Retention Waveform



Notes
3. Tested initially and after any design or process changes that may affect these parameters.
4. No input may exceed V_{CC} + 0.5 V.
5. Tested initially and after any design or process changes that may affect these parameters.
6. $t_r \leq 3$ ns for the –15 speed. $t_r \leq 5$ ns for the -20 and slower speeds.

Switching Characteristics

Over the Operating Range

Parameter [7]	Description	-15		-20		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{power}	V_{CC}(typical) to the first access [8]	1	–	1	–	µs
t_{RC}	Read cycle time	15	–	20	–	ns
t_{AA}	Address to data valid	–	15	–	20	ns
t_{OHA}	Data hold from address change	3	–	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	15	–	20	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	7	–	8	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z	0	–	0	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [9, 10]	–	7	–	8	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z [10]	3	–	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [9, 10]	–	7	–	8	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down	–	15	–	20	ns
t_{DBE}	Byte enable to data valid	–	7	–	8	ns
t_{LZBE}	Byte enable to low Z	0	–	0	–	ns
t_{HZBE}	Byte disable to high Z	–	7	–	8	ns
Write Cycle [11, 12]						
t_{WC}	Write cycle time	15	–	20	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	12	–	13	–	ns
t_{AW}	Address setup to write end	12	–	13	–	ns
t_{HA}	Address hold from write end	0	–	0	–	ns
t_{SA}	Address setup to write start	0	–	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	12	–	13	–	ns
t_{SD}	Data setup to write end	8	–	9	–	ns
t_{HD}	Data hold from write end	0	–	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [13]	3	–	3	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [13, 14]	–	7	–	8	ns
t_{BW}	Byte enable to end of write	12	–	13	–	ns

Notes

7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. This part has a voltage regulator which steps down the voltage from 5 V to 3.3 V internally. t_{power} time has to be provided initially before a read/write operation is started.
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
12. The minimum write cycle time for Write Cycle no. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
13. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
14. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.

Switching Waveforms

Figure 3. Read Cycle No. 1 [15, 16]

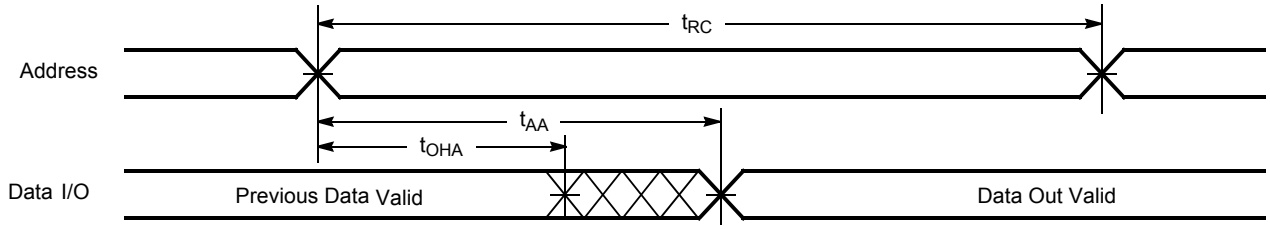
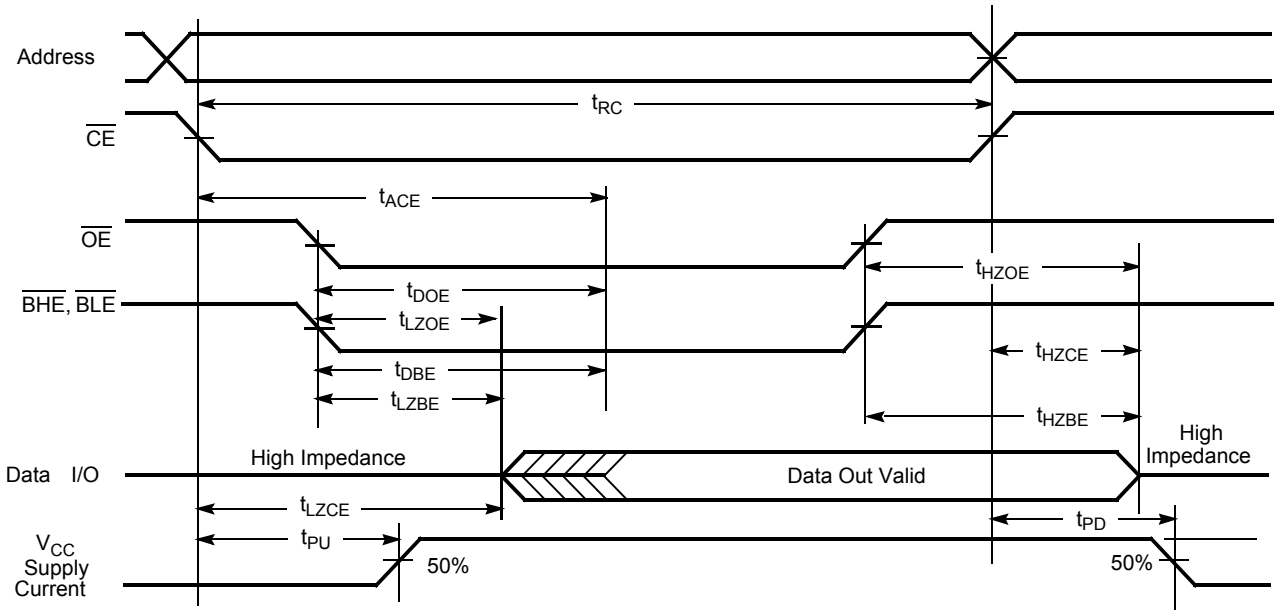


Figure 4. Read Cycle No. 2 ($\overline{OE}$ Controlled) [16, 17]



Notes
15. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$, and/or $\overline{BHE}$ = V_{IL}.
16. $\overline{WE}$ is HIGH for read cycle.
17. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 1 ($\overline{CE}$ Controlled) [18, 19]

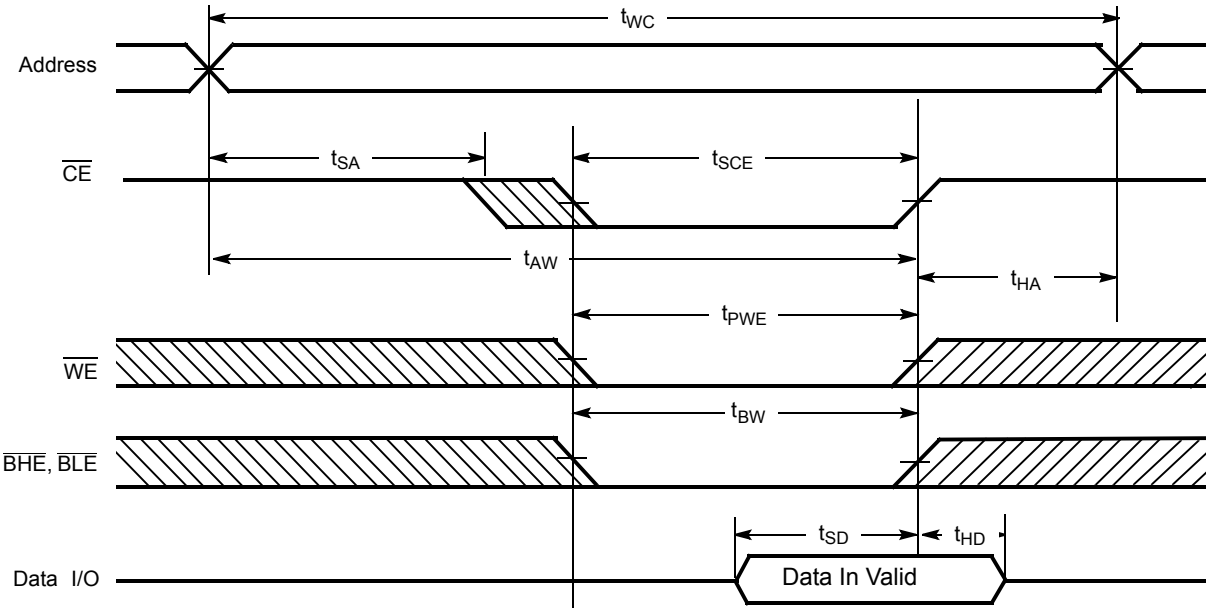
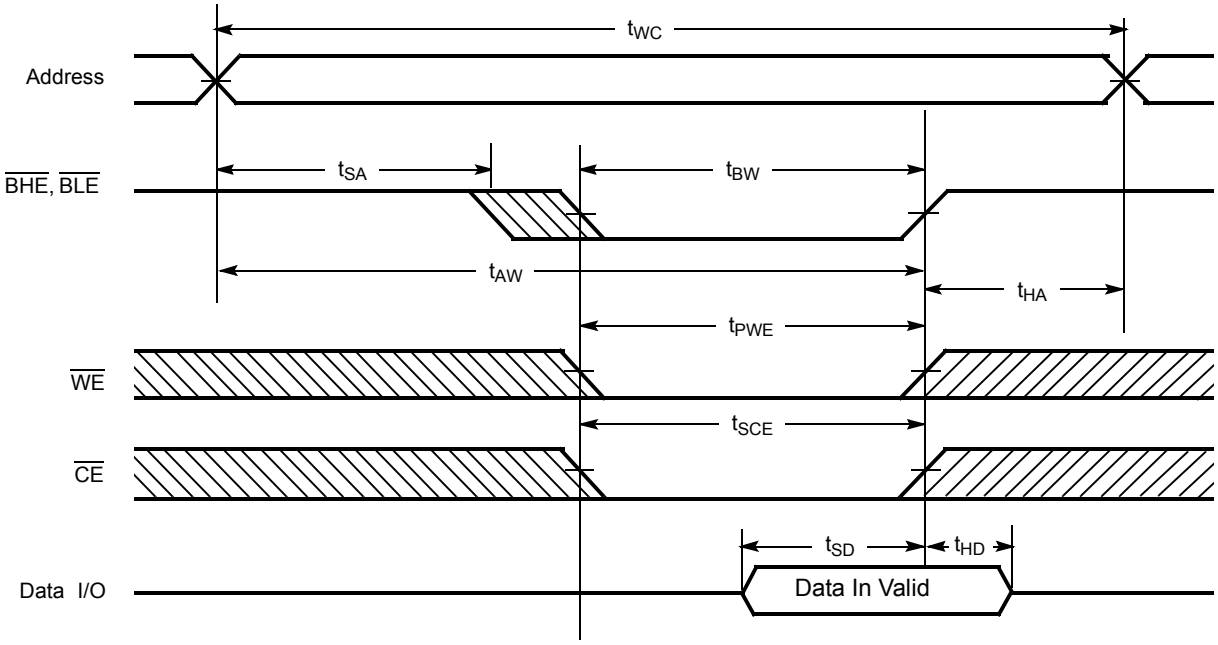


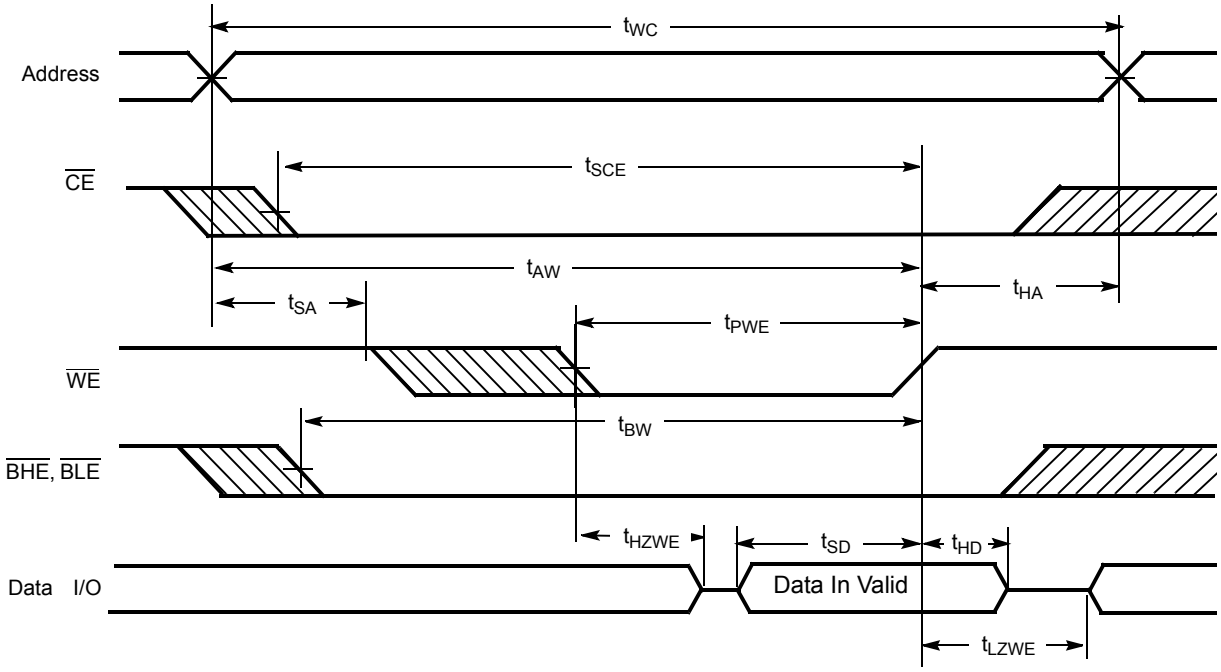
Figure 6. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)



Notes
18. Data I/O is high impedance if $\overline{OE}$ or $\overline{BHE}$ and/or $\overline{BLE}$= V_{IH}.
19. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	$I/O_0–I/O_7$	$I/O_8–I/O_{15}$	Mode	Power
H	X	X	X	X	High Z	High Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data out	Data out	Read all bits	Active (I_{CC})
L	L	H	L	H	Data out	High Z	Read lower bits only	Active (I_{CC})
L	L	H	H	L	High Z	Data out	Read upper bits only	Active (I_{CC})
L	X	L	L	L	Data in	Data in	Write all bits	Active (I_{CC})
L	X	L	L	H	Data in	High Z	Write lower bits only	Active (I_{CC})
L	X	L	H	L	High Z	Data in	Write upper bits only	Active (I_{CC})
L	H	H	X	X	High Z	High Z	Selected, Outputs disabled	Active (I_{CC})

Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at http://www.cypress.com and refer to the product summary page at http://www.cypress.com/products or contact your local sales representative.
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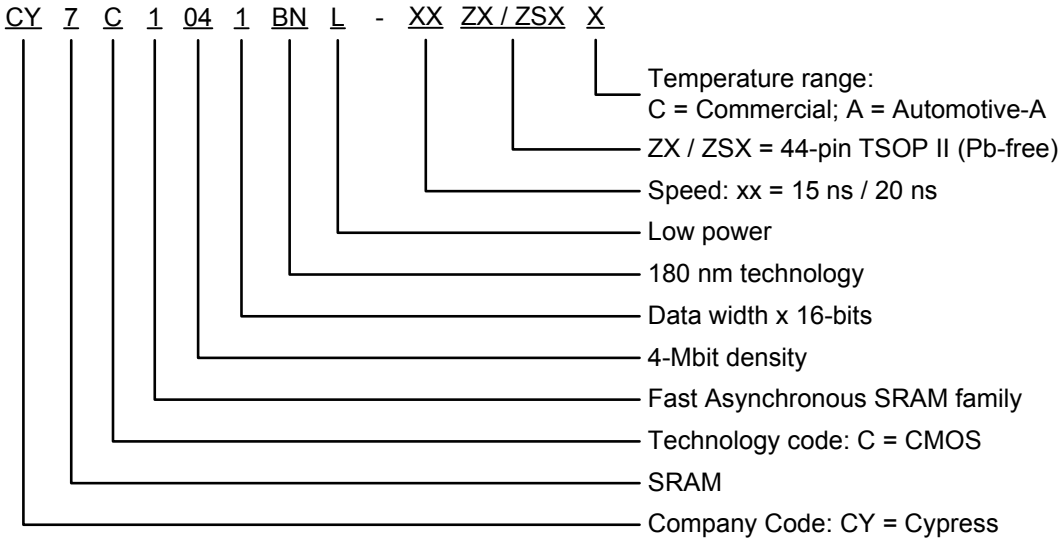
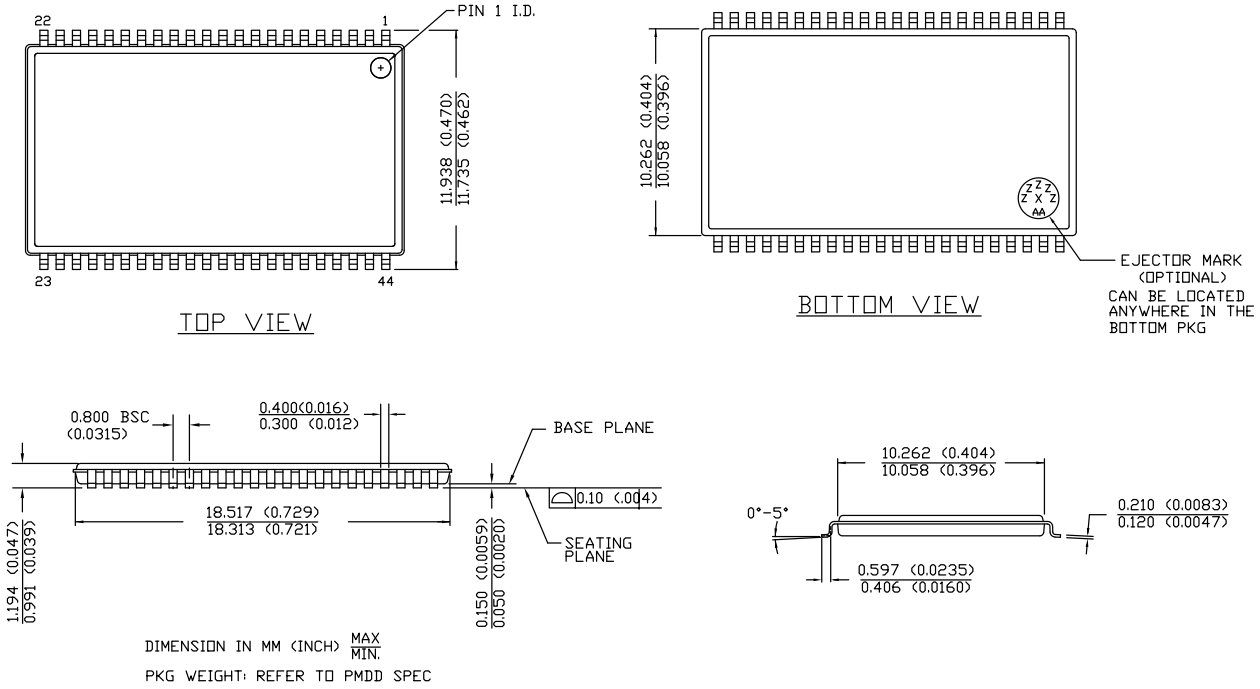
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7C1041BNL-15ZXC	51-85087	44-pin TSOP Type II (Pb-free)	Commercial
20	CY7C1041BN-20ZSXA		44-pin TSOP Type II	Automotive-A

Ordering Code Definitions



Package Diagrams

Figure 8. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 *E

Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
V	volt
MHz	megahertz
µA	microampere
mA	milliampere
mV	millivolt
mW	milliwatt
ns	nanosecond
pF	picofarad
W	watt

Document History Page

Document Title: CY7C1041BN, 256 K × 16 Static RAM Document Number: 001-06496				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	424111	NXR	See ECN	New data sheet.
*A	498575	NXR	See ECN	Added Automotive-A operating range updated Ordering Information Table
*B	2897061	AJU	03/22/10	Removed obsolete parts from ordering information table Updated package diagrams
*C	2906679	NXR	04/07/10	Removed inactive part CY7C1041BNL-20VXCT from the ordering information table.
*D	3086674	PRAS	11/15/10	Removed inactive parts (CY7C1041BN-15ZXI, CY7C1041BN-15VXI). Added Ordering Code Definition.
*E	3232637	PRAS	04/20/2011	Fixed unit for Input Load current and Output Leakage current under Electrical Characteristics table from mA to µA. Updated template. Added Units table.
*F	3383869	TAVA	09/26/2011	Removed all references to Industrial information. All “Commercial-L” changed to “Commercial”. Modified the notes in figures under Read cycle and Write cycle sections. Rearranged sections for better clarity. Revised package diagram.
*G	4113666	VINI	09/04/2013	Updated Package Diagrams: spec 51-85087 – Changed revision from *D to *E. Updated in new template. Completing Sunset Review.

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