



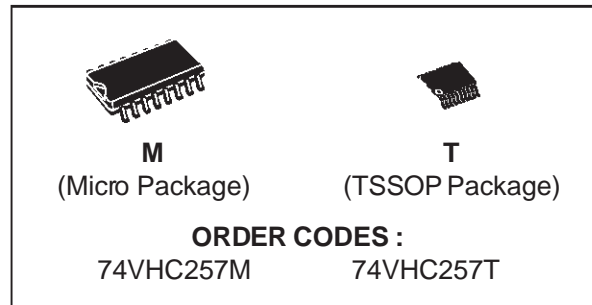
QUAD 2 CHANNEL MULTIPLEXER (3-STATE)

- HIGH SPEED: $t_{PD} = 3.7 \text{ ns}$ (TYP.) at $V_{CC} = 5V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu A$ (MAX.) at $T_A = 25 \text{ }^\circ C$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 8 \text{ mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC} \text{ (OPR)} = 2V \text{ to } 5.5V$
- PIN AND FUNCTION COMPATIBLE WITH
 74 SERIES 257
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE $V_{OLP} = 0.8V$ (Max.)

DESCRIPTION

The 74VHC257 is an advanced high-speed CMOS QUAD 2 CHANNEL MULTIPLEXER (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology.

It is composed of four independent 2 channel multiplexers with common SELECT and ENABLE INPUT.

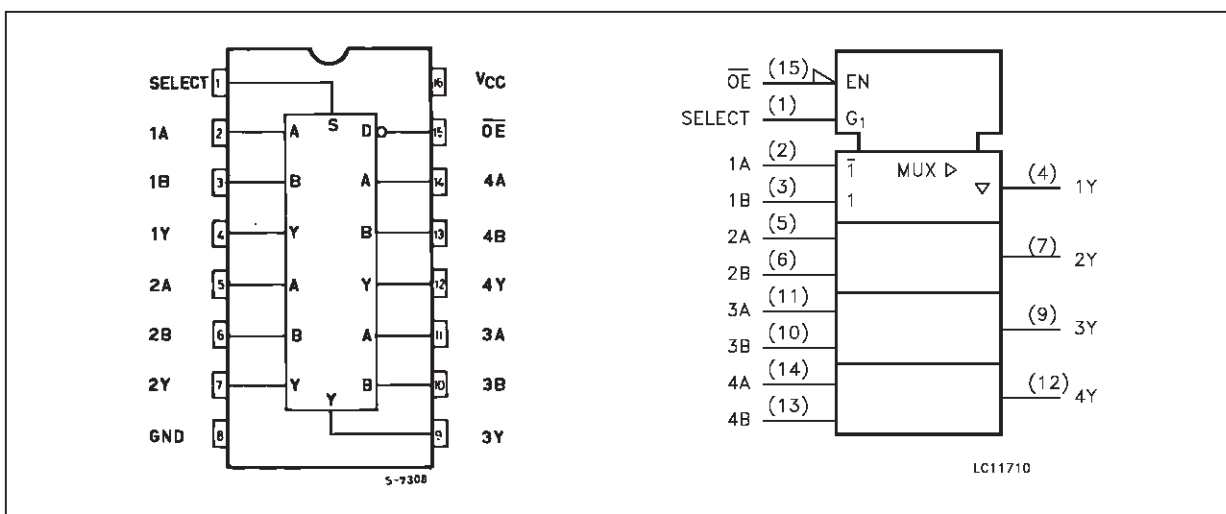


The 74VHC257 is a non inverting multiplexer. When the ENABLE INPUT is held "High", all outputs become high impedance state. If SELECT INPUT is held "Low", "A" data is selected, when SELECT INPUT is "High", "B" data is chosen.

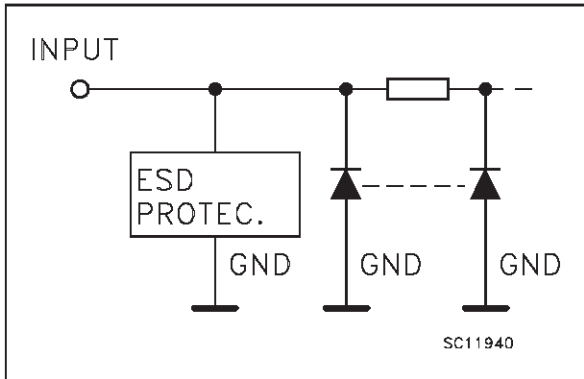
Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

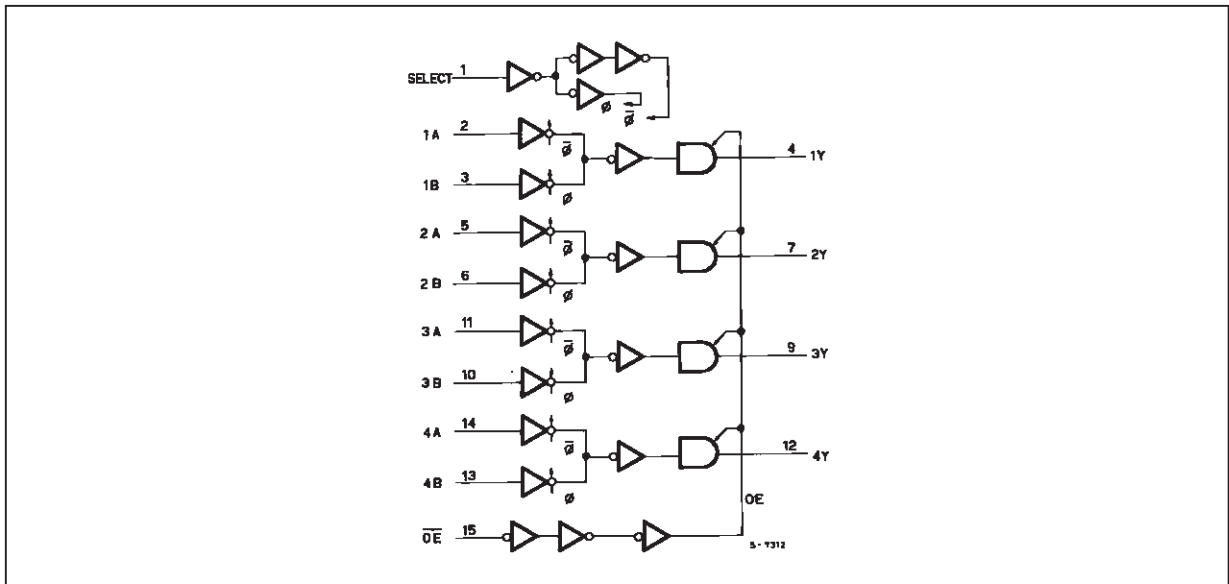
PIN No	SYMBOL	NAME AND FUNCTION
1	SELECT	Common Data Select Input
2, 5, 14, 11	1A to 4A	Data Input From Source A
3, 6, 13, 10	1B to 4B	Data Inputs from Source B
4, 7, 12, 9	1Y to 4Y	3 State Multiplexer Outputs
15	\overline{OE}	3 State Output Enable Inputs (Active LOW)
8	GND	Ground (0V)
16	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS				OUTPUTS
\overline{OE}	SELECT	A	B	Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

X = DON'T CARE Z = HIGH IMPEDANCE

LOGIC DIAGRAM



This logic diagram has not be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7.0	V
V _I	DC Input Voltage	-0.5 to +7.0	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	- 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Current	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 50	mA
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	2.0 to 5.5	V
V _I	Input Voltage	0 to 5.5	V
V _O	Output Voltage	0 to V _{CC}	V
T _{op}	Operating Temperature	-40 to +85	°C
dt/dv	Input Rise and Fall Time (see note 1) (V _{CC} = 3.3 ± 0.3V) (V _{CC} = 5.0 ± 0.5V)	0 to 100 0 to 20	ns/V ns/V

1) V_{IN} from 30% to 70% of V_{CC}

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value					Unit	
				V _{CC} (V)	T _A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		V	
		3.0 to 5.5		0.7V _{CC}			0.7V _{CC}			
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5	V	
		3.0 to 5.5				0.3V _{CC}		0.3V _{CC}		
V _{OH}	High Level Output Voltage	2.0	I _O = -50 μA	1.9	2.0		1.9		V	
		3.0	I _O = -50 μA	2.9	3.0		2.9			
		4.5	I _O = -50 μA	4.4	4.5		4.4			
		3.0	I _O = -4 mA	2.58			2.48			
		4.5	I _O = -8 mA	3.94			3.8			
V _{OL}	Low Level Output Voltage	2.0	I _O = 50 μA		0.0	0.1		0.1	V	
		3.0	I _O = 50 μA		0.0	0.1		0.1		
		4.5	I _O = 50 μA		0.0	0.1		0.1		
		3.0	I _O = 4 mA			0.36		0.44		
		4.5	I _O = 8 mA			0.36		0.44		
I _{OZ}	High Impedance Output Leakage Current	5.5	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			±0.25		±2.5	μA	
I _I	Input Leakage Current	0 to 5.5	V _I = 5.5V or GND			±0.1		±1.0	μA	
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			4		40	μA	

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3$ ns)

Symbol	Parameter	Test Condition			Value					Unit
		V _{CC} (V)	C _L (pF)		T _A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time A, B to Y	3.3 ^(*)	15			5.8	9.3	1.0	11.0	ns
		3.3 ^(*)	50			8.3	12.8	1.0	14.5	
		5.0 ^(**)	15			3.6	5.9	1.0	7.0	
		5.0 ^(**)	50			5.1	7.9	1.0	9.0	
t _{PLH} t _{PHL}	Propagation Delay Time SELECT to Y	3.3 ^(*)	15			7.0	11.0	1.0	13.0	ns
		3.3 ^(*)	50			9.5	14.5	1.0	16.5	
		5.0 ^(**)	15			4.0	6.8	1.0	8.0	
		5.0 ^(**)	50			5.5	8.8	1.0	10.0	
t _{PZL} t _{PZH}	Output Enable Time	3.3 ^(*)	15			6.7	10.5	1.0	12.5	ns
		3.3 ^(*)	50			9.2	14.0	1.0	16.0	
		5.0 ^(**)	15			3.6	6.8	1.0	8.0	
		5.0 ^(**)	50			5.1	8.8	1.0	10.0	
t _{PLZ} t _{PHZ}	Output Disable Time	3.3 ^(*)	50			8.6	12.0	1.0	13.5	ns
		5.0 ^(**)	50			5.7	7.9	1.0	9.0	

(*) Voltage range is 3.3V ± 0.3V

(**) Voltage range is 5V ± 0.5V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions	Value					Unit
			T _A = 25 °C			-40 to 85 °C		
			Min.	Typ.	Max.	Min.	Max.	
C _{IN}	Input Capacitance			4	10		10	pF
C _{OUT}	Output Capacitance			6				pF
C _{PD}	Power Dissipation Capacitance (note 1)			23				pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(oper)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/4$ (per Channel)

DYNAMIC SWITCHING CHARACTERISTICS

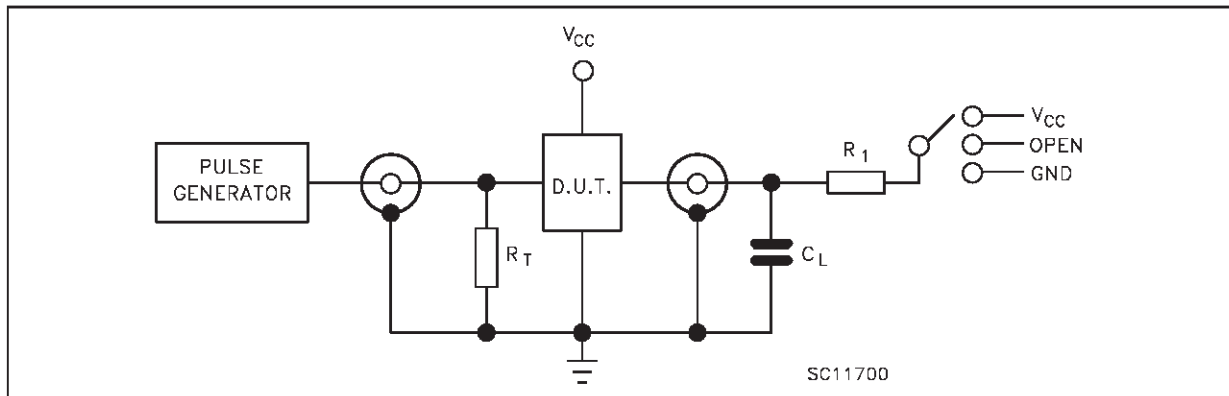
Symbol	Parameter	V _{CC} (V)	Test Conditions	Value					Unit
				T _A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V _{OLP}	Dynamic Low Voltage Quiet Output (note 1, 2)	5.0	C _L = 50 pF		0.3	0.8			V
V _{OLV}				-0.8	-0.3				
V _{IHD}	Dynamic High Voltage Input (note 1, 3)	5.0		3.5					
V _{ILD}	Dynamic Low Voltage Input (note 1, 3)	5.0				1.5			

1) Worst case package.

2) Max number of outputs defined as (n). Data inputs are driven 0V to 5.0V, (n-1) outputs switching and one output at GND.

3) Max number of data inputs (n) switching. (n-1) switching 0V to 5.0V. Inputs under test switching: 5.0V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f=1MHz.

TEST CIRCUIT



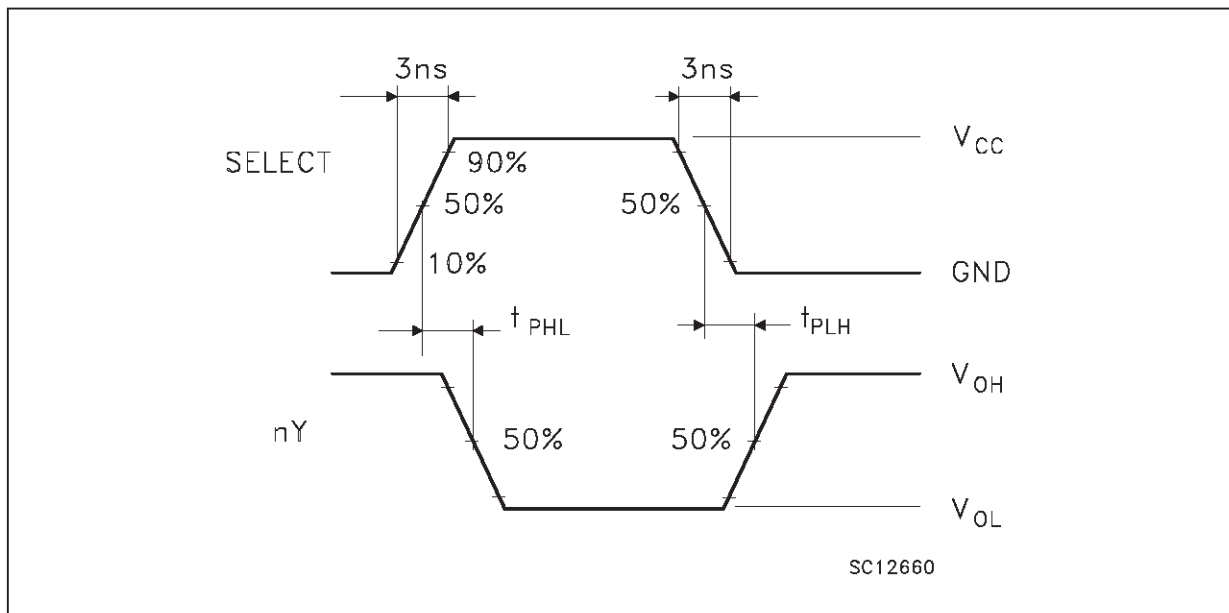
TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	V_{CC}
t_{PZH} , t_{PHZ}	GND

$C_L = 15/50$ pF or equivalent (includes jig and probe capacitance)

$R_L = R_1 = 1K\Omega$ or equivalent

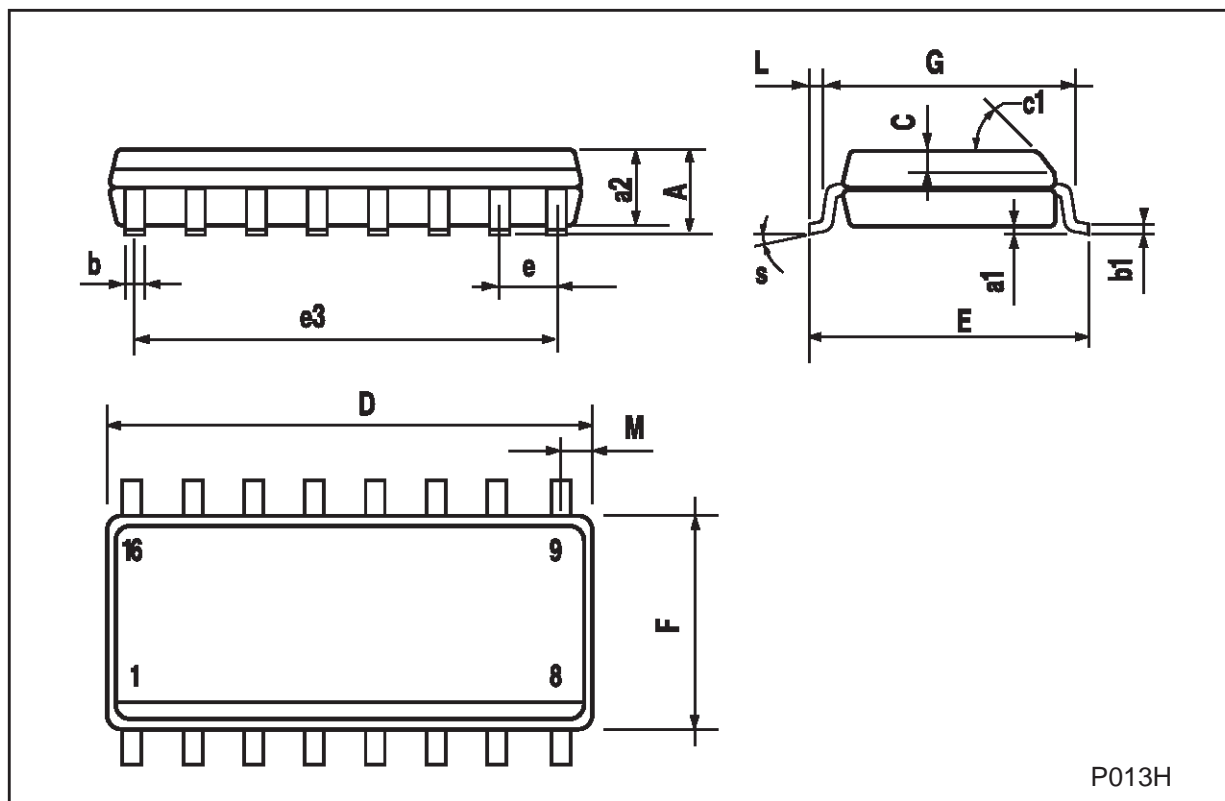
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS FOR INVERTING CONDITIONS ($f=1MHz$; 50% duty cycle)



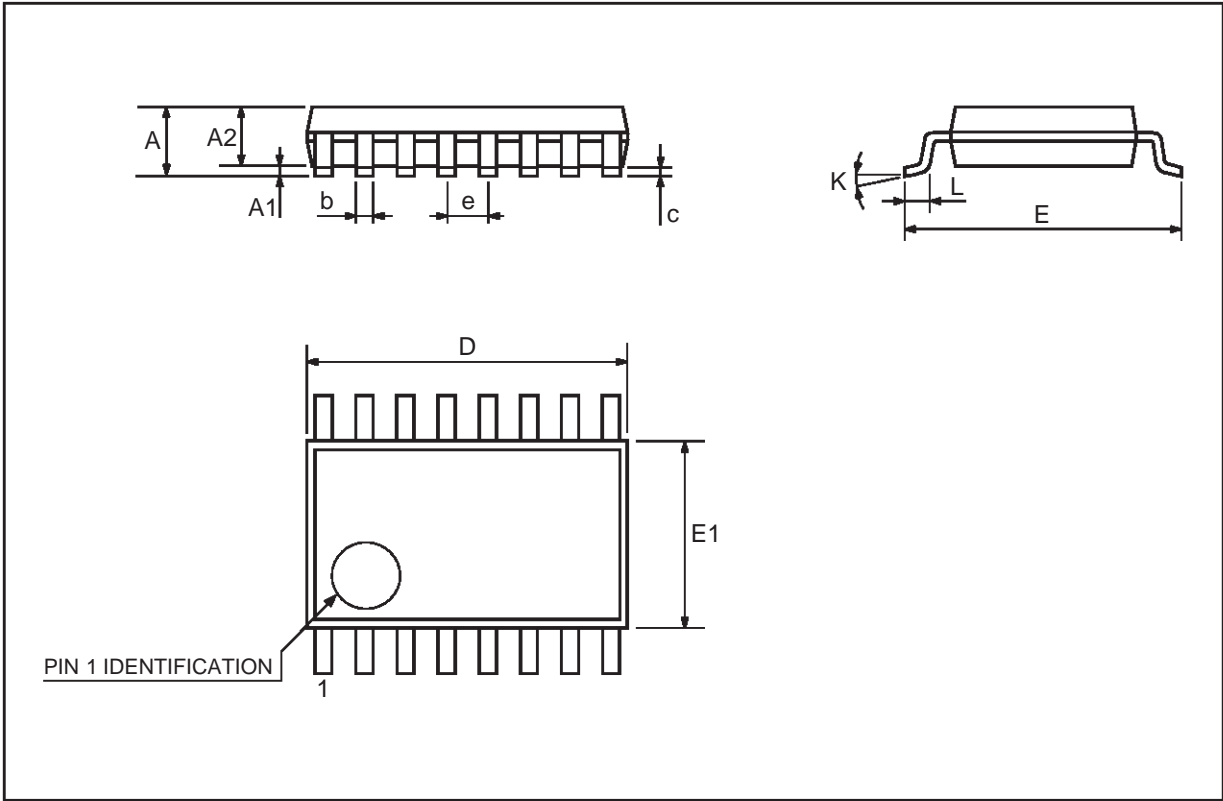
SO-16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8 (max.)					



TSSOP16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



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