TLE84110EL

Deca-Half-Bridge Driver IC

Automotive Power

Never stop thinking

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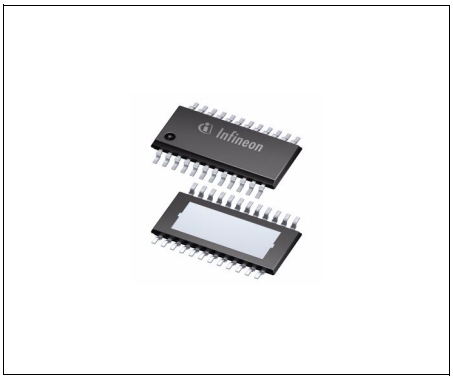
1 Overview



PG-SSOP-24-4

Features

- 10 Half Bridge Power Outputs
- 3.3V / 5V compatible inputs with hysteresis
- Independently Diagnosable Outputs
- 16-bit Standard SPI interface with daisy chain capability for control and diagnosis
- Open load diagnostics in ON-state for all outputs
- All outputs with overload and short circuit protection and diagnosis
- Overtemperature prewarning and protection
- Over- and Undervoltage lockout
- Cross-current protection
- Thermally enhanced exposed pad package
- Green Product (RoHS compliant)
- AEC Qualified

Description

The TLE84110EL is a protected Deca-Half-Bridge-Driver designed especially for automotive motion control applications such as Heating, Ventilation and Air Conditioning (HVAC) flap DC motor control. It is part of the MonolythIC family in Infineon's Smart Power Technology SPT® which combines bipolar and CMOS control circuitry with DMOS power devices.

The 10 half bridge drivers are designed to drive DC motor loads in sequential or parallel operation. Operation modes forward (cw), reverse (ccw), brake and high impedance are controlled from a 16-bit SPI interface. The diagnosis features such as short circuit, open load, power supply failure and overtemperature in combination with its low quiescent current makes this device attractive for automotive applications. The extremely small fine pitch exposed pad PG-SSOP-24-4 package in a SO -14 body provides good thermal performance and reduces PCB-board space and costs.

Table 1 Product Summary

Operating Voltage	V_S	7 ... 18 V
Logic Supply Voltage	V_{DD}	3.0 ... 5.5 V
Maximum Supply Voltage for Load Dump Protection	$V_{S(LD)}$	40 V
Minimum Overcurrent Threshold	$I_{SD1\text{-}10\_MOTOR}$	0.8 A
Maximum On-State Path Resistance at T_j = 150°C	$R_{DSON(total)\_HSx+LSy}$	2 + 2 Ω
Typical Quiescent Current at T_j = 85°C	$I_{S\ (off))}$	1 µA
Maximum SPI Access Frequency	f_{SCLK}	5 MHz

Type	Package	Marking
TLE84110EL	PG-SSOP-24-4	TLE84110EL

2 Block Diagram

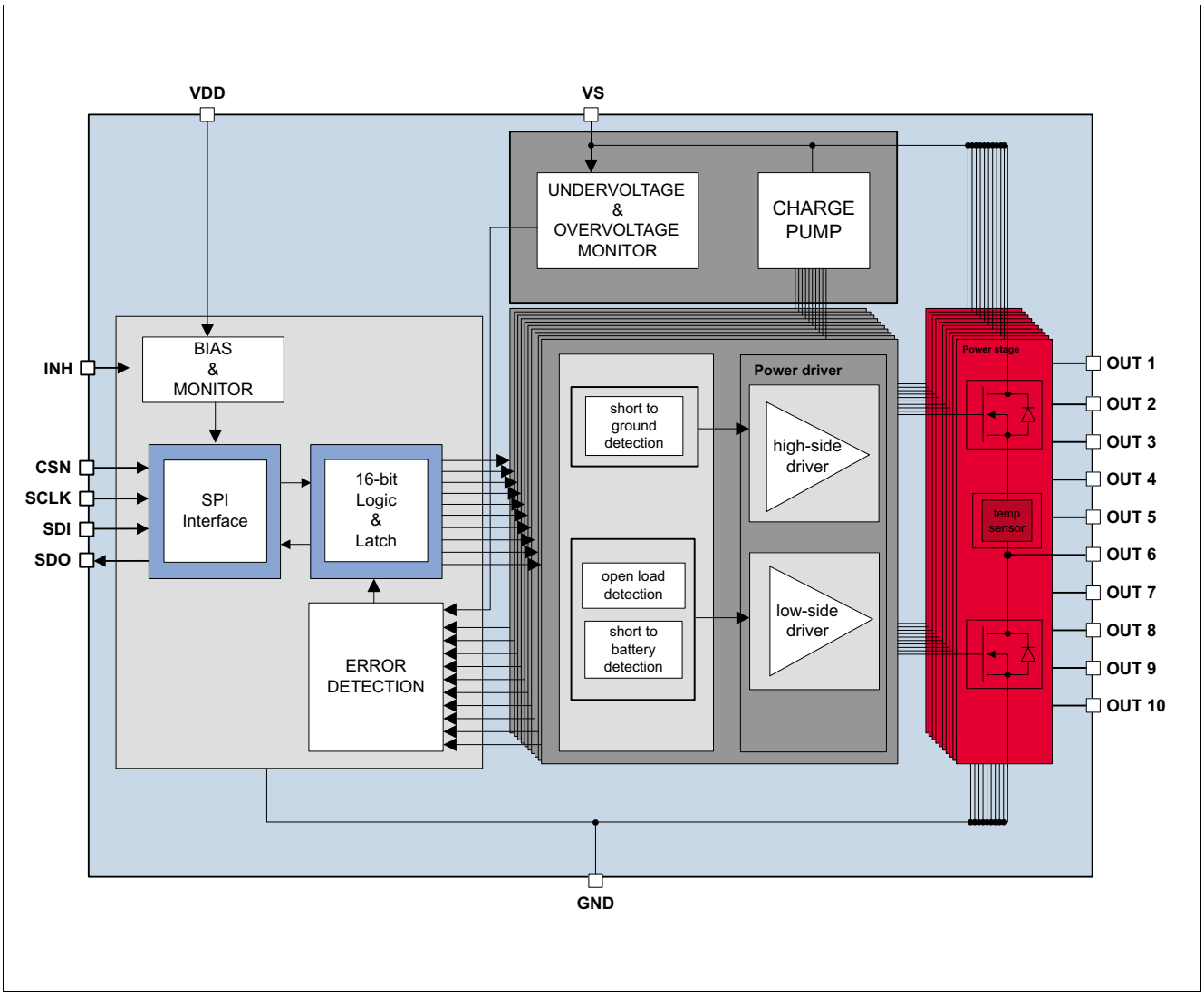


Figure 1 Block Diagram

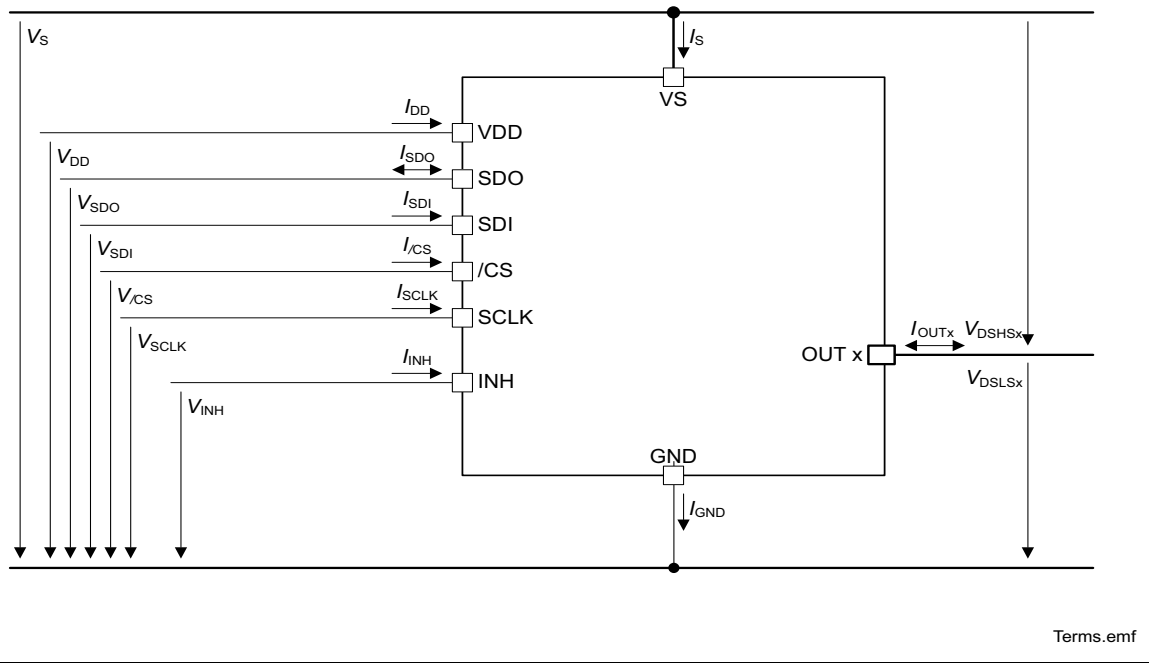


Figure 2 Terms

3 Pin Configuration

3.1 Pin Assignment

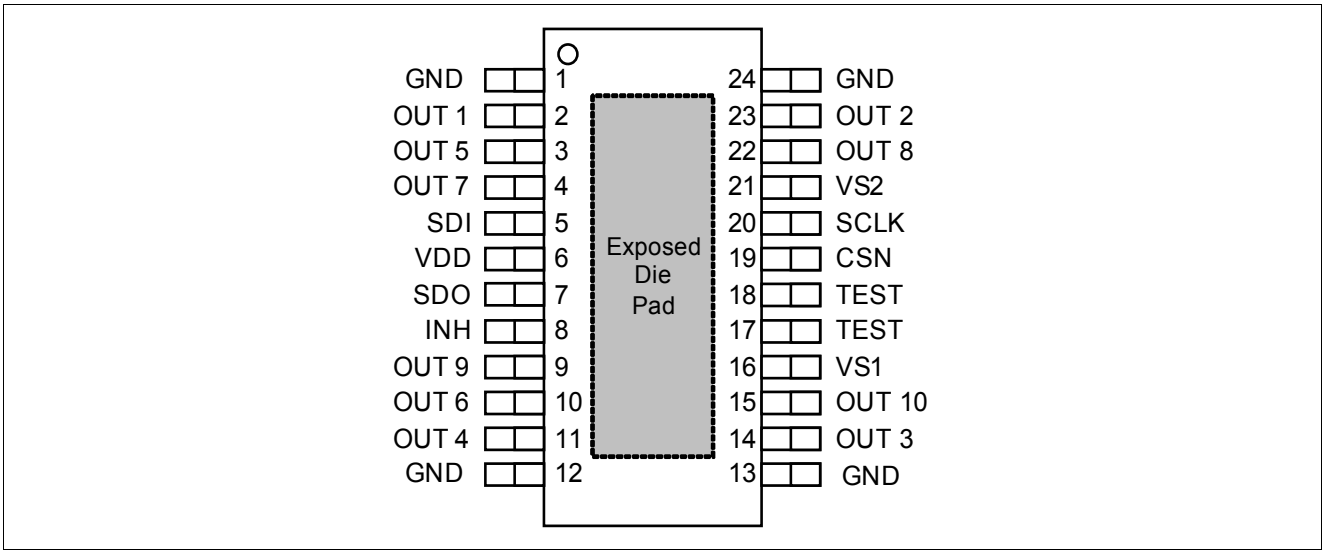


Figure 3 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	GND	Ground
2	OUT 1	Power Half-Bridge 1
3	OUT 5	Power Half-Bridge 5
4	OUT 7	Power Half-Bridge 7
5	SDI	Serial-Data-Input
6	VDD	Logic Supply Voltage
7	SDO	Serial-Data-Output
8	INH	Inhibit input with internal pull-down; Place device in standby mode by pulling the INH line LOW
9	OUT 9	Power Half-Bridge 9
10	OUT 6	Power Half-Bridge 6
11	OUT 4	Power Half-Bridge 4
12	GND	Ground
13	GND	Ground
14	OUT 3	Power Half-Bridge 3
15	OUT 10	Power Half-Bridge 10
16	VS1	Power Supply Voltage for Group 1 supplying current to OUT 3, OUT 4, OUT 6, OUT 9 and OUT 10.
17	TEST	Test input with internal pull down. Used for production test only. This pin should be left open or connected to ground on board.
18	TEST	Test input with internal pull down. Used for production test only. This pin should be left open or connected to ground on board.
19	CSN	Chip-Select-Not-Input
20	SCLK	Serial Clock Input
21	VS2	Power Supply Voltage for Group 2 supplying current to OUT 1, OUT 2, OUT 5, OUT 7 and OUT 8.
22	OUT 8	Power Half-Bridge 8
23	OUT 2	Power Half-Bridge 2
24	GND	Ground
EDP	-	Exposed Die Pad; For cooling purposes only; Do not use as electrical ground.[1)]

1) The exposed die pad at the bottom of the package allows better heat dissipation from the device via the PCB. The exposed die pad is not connected to any active part of the IC. When connecting onto PCB, it can either be left floating or connected to GND for the best EMC and thermal performance.

*Note: All GND pins must be externally connected together to a common GND potential. All VS pins must be externally connected together to a common Vs potential. See **Figure 17** for more Application Information.*

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40 °C to +150 °C

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Supply voltage	V_S	-0.3	40	V	$V_S = V_{S1} = V_{S2}$
4.1.2	Logic supply voltage	V_{DD}	-0.3	5.5	V	0 V < V_S < 40 V
4.1.3	Logic input voltages (SDI, SCLK, CSN; INH)	V_{SDI}, V_{SCLK}, V_{CSN}, V_{INH}	-0.3	5.5	V	0 V < V_S < 40 V 0 V < V_{DD} < 5.5V
4.1.4	Logic output voltage (SDO)	V_{SDO}	-0.3	5.5	V	0 V < V_S < 40 V 0 V < V_{DD} < 5.5V
Currents						
4.1.5	Continuous Supply Current for V_{S1}	I_{S1}	0	2.50	A	–
4.1.6	Continuous Supply Current for V_{S2}	I_{S2}	0	2.50	A	–
Temperatures						
4.1.7	Junction temperature	T_j	-40	150	°C	–
4.1.8	Storage temperature	T_{stg}	-50	150	°C	–
ESD Susceptibility						
4.1.9	ESD capability of OUTx and V_S pin	V_{ESD}	-4	4	kV	[2)]
4.1.10	ESD capability of other pins	V_{ESD}	-2	2	kV	[2)]

1) Not subject to production test, specified by design.

2) Human Body Model according to ANSI EOS\ESD S5.1 standard (eqv. to MIL STD 883D and JEDEC JESD22-A114)

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply voltage range for normal operation	$V_{S(nor)}$	7	18	V	–
4.2.2	Extended Supply Voltage Range for Operation	$V_{S(ext)}$	$V_{UV\ OFF}$	$V_{OV\ OFF}$	V	Limit Values Deviations Possible; After V_S rising above $V_{UV\ ON}$
4.2.3	Supply Voltage Slew Rate	$\lvert dV_S/dt \rvert$	–	10	V/µs	V_S increasing and decreasing [1]
4.2.4	Logic supply voltage range for normal operation	V_{DD}	3.0	5.5	V	–
4.2.5	Logic input voltages (DI, CLK, CSN; INH)	V_{DI}, V_{CLK}, V_{CSN}, V_{INH}	-0.3	5.5	V	–
4.2.6	Junction temperature	T_j	-40	150	°C	–

1) Not subject to production test, specified by design.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case, Ta = -40°C	R_{thjC_cold}	–	3	–	K/W	1)
4.3.2	Junction to Case, Ta = 85°C	R_{thjC_hot}	–	4	–	K/W	1)
4.3.3	Junction to Ambient, Ta = -40°C (1s0p, minimal footprint)	$R_{thjA\_cold\_min}$	–	114	–	K/W	1) 2)
4.3.4	Junction to Ambient, Ta = 85°C (1s0p, minimal footprint)	$R_{thjA\_hot\_min}$	–	96	–	K/W	1) 2)
4.3.5	Junction to Ambient, Ta = -40°C (1s0p, 300mm2 Cu)	$R_{thjA\_cold\_300}$	–	69	–	K/W	1) 3)
4.3.6	Junction to Ambient, Ta = 85°C (1s0p, 300mm2 Cu)	$R_{thjA\_hot\_300}$	–	56	–	K/W	1) 3)
4.3.7	Junction to Ambient, Ta = -40°C (1s0p, 600mm2 Cu)	$R_{thjA\_cold\_600}$	–	62	–	K/W	1) 4)
4.3.8	Junction to Ambient, Ta = 85°C (1s0p, 600mm2 Cu)	$R_{thjA\_hot\_600}$	–	50	–	K/W	1) 4)
4.3.9	Junction to Ambient, Ta = -40°C (2s2p)	$R_{thjA\_cold\_2s2p}$	–	35	–	K/W	1) 5)
4.3.10	Junction to Ambient, Ta = 85°C (2s2p)	$R_{thjA\_hot\_2s2p}$	–	30	–	K/W	1) 5)

1) Not subject to production test, specified by design.

2) Specified RthJA value is according to JEDEC JESD51-2,-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with minimal footprint copper area and 35 µm thickness. Ta = -40°C, Ch 1 to Ch 10 are dissipating a total of 2.5W (0.25W each). Ta = 85°C, Ch 1 to Ch 10 are dissipating a total of 1.8W (0.18W each).

3) Specified RthJA value is according to JEDEC JESD51-2,-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional cooling of 300 mm2 copper area and 35 µm thickness. Ta = -40°C, Ch 1 to Ch 10 are dissipating a total of 2.5W (0.25W each). Ta = 85°C, Ch 1 to Ch 10 are dissipating a total of 1.8W (0.18W each).

4) Specified RthJA value is according to JEDEC JESD51-2,-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with additional cooling of 600 mm2 copper area and 35 µm thickness. Ta = -40°C, Ch 1 to Ch 10 are dissipating a total of 2.5W (0.25W each). Ta = 85°C, Ch 1 to Ch 10 are dissipating a total of 1.8W (0.18W each).

5) Specified RthJA value is according to JEDEC JESD51-2,-3 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (4 x 35µm Cu). Ta = -40°C, Ch 1 to Ch 10 are dissipating a total of 2.5W (0.25W each). Ta = 85°C, Ch 1 to Ch 10 are dissipating a total of 1.8W (0.18W each).

4.4 Electrical Characteristics

Electrical Characteristics

V_S= 7 V to 18 V, V_{DD}= 3.0 V to 5.5 V, T_j = -40 °C to +150 °C, INH = HIGH; $I_{OUT1-10}$ = 0 A; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Current Consumption, INH = GND							
4.4.1	Supply Quiescent current	I_{SQ}	–	1	2.5	µA	V_S = 13.5 V; V_{DD}= 0 V T_j = 85°C
4.4.2	Logic supply quiescent current	I_{DD_Q}	–	0.5	1	µA	T_j = 85°C
4.4.3	Total quiescent current	$I_{SQ}+I_{DD\_Q}$	–	2	4	µA	T_j = 85°C
Current Consumption, INH = HIGH							
4.4.4	Supply current	I_S	–	4.5	10	mA	Power drivers and power stages are off
4.4.5	Logic supply current	I_{DD}	–	1.5	3	mA	SPI not active
4.4.6	Logic supply current	I_{DD_RUN}	–	5	–	mA	V_{DD} = 3.0V; SPI 5MHz
4.4.7	Total supply current	$I_S+I_{DD\_RUN}$	–	9.5	–	mA	–
Over- and Undervoltage Lockout							
4.4.8	UV Switch ON voltage	$V_{UV\ ON}$	–	–	5.2	V	V_S increasing
4.4.9	UV Switch OFF voltage	$V_{UV\ OFF}$	4	–	5.0	V	V_S decreasing
4.4.10	UV ON/OFF hysteresis	$V_{UV\ HY}$	–	0.25	–	V	$V_{UV\ ON}$ - $V_{UV\ OFF}$
4.4.11	OV Switch OFF voltage	$V_{OV\ OFF}$	21	–	25	V	V_S increasing;
4.4.12	OV Switch ON voltage	$V_{OV\ ON}$	20	–	24	V	V_S decreasing;
4.4.13	OV ON/OFF hysteresis	$V_{OV\ HY}$	–	1	–	V	$V_{OV\ OFF}$ - $V_{OV\ ON}$;
4.4.14	V_{DD} Power-On-Reset	$V_{DD\ POR}$	2.60	2.80	3.00	V	V_{DD} increasing
4.4.15	V_{DD} Power-Off-Reset	$V_{DD\ POffR}$	2.50	2.70	2.90	V	V_{DD} decreasing
Static Drain-source ON-Resistance							
4.4.16	High- and Low-side switch	$R_{DSON(1-10)}$	–	0.8	–	Ω	$I_{OUT\ (1-10)}$= ±0.5 A; T_j = 25 °C
			–	1.4	2	Ω	$I_{OUT\ (1-10)}$= ±0.5 A; T_j = 150 °C
Output Protection and Diagnosis							
High-Side Switches							
4.4.17	HS Overcurrent Shutdown Threshold	I_{SD_HS}	-1.6	-1.15	-0.8	A	HS Switch; V_S=13.5V; See **Figure 7**
4.4.18	HS Short Circuit Current Limit	I_{SC_HS}	-2.0	-1.5	-1.0	A	1)
4.4.19	HS_Shutdown Delay Time	t_{dSD}	10	25	50	µs	HS Switch; V_S=13.5V; See **Figure 7**

Electrical Characteristics (cont'd)

V_S= 7 V to 18 V, V_{DD}= 3.0 V to 5.5 V, T_j = -40 °C to +150 °C, INH = HIGH; $I_{OUT1-10}$ = 0 A; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Low-Side Switches							
4.4.20	LS Overcurrent Shutdown Threshold	I_{SD_LS}	0.8	1.15	1.6	A	LS Switch; V_S=13.5V; See **Figure 7**
4.4.21	LS Short Circuit Current Limit	I_{SC_LS}	1.0	1.5	2.0	A	1)
4.4.22	LS_Shutdown Delay Time	t_{dSD}	10	25	50	µs	LS Switch; V_S=13.5V; See **Figure 7**
4.4.23	Open Load Detection Current	I_{OLD}	3	8	15	mA	LS Switch; V_S=13.5V; See **Figure 8**
4.4.24	Open Load Delay Time	t_{dOLD}	200	350	600	µs	
Output Switching Times							
4.4.25	High-Side ON delay-time	t_{dONH}	–	7.5	12	µs	V_S=13.5V, resistive Load = 100Ω, See **Figure 9** and **Figure 10**
4.4.26	High-Side OFF delay-time	t_{dOFFH}	–	3	6	µs	
4.4.27	Low-Side ON delay-time	t_{dONL}	–	6.5	12	µs	
4.4.28	Low-Side OFF delay-time	t_{dOFFL}	–	2	5	µs	
4.4.29	Dead Time H to L	t_{DHL}	1.5	–	–	µs	
4.4.30	Dead Time L to H	t_{DLH}	2.5	–	–	µs	
4.4.31	High-Side RiseTime	t_{ONH}	–	4	–	µs	
4.4.32	High-Side Fall Time	t_{OFFH}	–	2	–	µs	
4.4.33	Low-Side RiseTime	t_{OFFL}	–	1	–	µs	
4.4.34	Low-Side Fall Time	t_{ONL}	–	1	–	µs	
Input Interface, Logic Inputs INH							
4.4.35	High-input voltage	V_{INHH}	70	–	–	% V_{DD}	–
4.4.36	Low-input voltage	V_{INHL}	–	–	30	% V_{DD}	–
4.4.37	Hysteresis of input voltage	V_{INHHY}	50	200	500	mV	–
4.4.38	Pull down resistor	R_{PD_INH}	–	120	–	kΩ	–
SPI INTERFACE							
Delay Time from Sleep mode to first Data in							
4.4.39	Setup time	t_{set}	–	–	100	µs	1)
4.4.40	Time between two consecutive SRR commands	t_{SRR}	100	–	–	µs	1)
Input Interface, Logic Inputs SDI, SCLK, CSN							
4.4.41	High-input voltage	V_{IH}	70	–	–	% V_{DD}	–
4.4.42	Low-input voltage	V_{IL}	–	–	30	% V_{DD}	–
4.4.43	Hysteresis of input voltage	V_{IHY}	50	200	500	mV	–
4.4.44	Pull up resistor at pin CSN	R_{PU_CSN}	–	140	–	kΩ	–
4.4.45	Pull down resistor at pin SDI, SCLK	R_{PD_SDI}, R_{PD_SCLK}	–	120	–	kΩ	–

Electrical Characteristics (cont'd)

V_S= 7 V to 18 V, V_{DD}= 3.0 V to 5.5 V, T_j = -40 °C to +150 °C, INH = HIGH; $I_{OUT1-10}$ = 0 A; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.4.46	Input capacitance at pin CSN, SDI or SCLK	C_I	–	10	15	pF	0V < V_{DD} < 5.25V [1]
Input Interface, Logic Outputs SDO							
4.4.47	High-output voltage	V_{SDOH}	V_{DD} - 1.0	V_{DD} - 0.7	–	V	I_{SDOH} = -1 mA
4.4.48	Low-output voltage	V_{SDOL}	–	0.2	0.4	V	I_{SDOL} = 1.6 mA
4.4.49	Tri-state Leakage Current	I_{SDOLK}	-10	–	10	µA	V_{CSN} = V_{DD} 0V < V_{SDO} < V_{DD}
Data Input Timing. See Figure 12 and Figure 15							
4.4.50	SCLK Frequency	f_{CLK}	–	–	5	MHz	[1]
4.4.51	SCLK Period	t_{pCLK}	500 200	– –	– –	ns ns	V_{DD} = 5.25V V_{DD} = 3.0V [1]
4.4.52	SCLK High Time	t_{SCLKH}	85	–	–	ns	[1]
4.4.53	SCLK Low Time	t_{SCLKL}	85	–	–	ns	[1]
4.4.54	SCLK Setup Time	t_{lag}	85	–	–	ns	[1]
4.4.55	SDI Setup Time	t_{SDI_setup}	50	–	–	ns	[1]
4.4.56	SDI Hold Time	t_{SDI_hold}	50	–	–	ns	[1]
4.4.57	CSN Setup Time	t_{lead}	100	–	–	ns	[1]
4.4.58	CSN High Time	t_{CSNH}	500	–	–	ns	[1] [2]
4.4.59	Input Signal Rise Time at pin SDI, SCLK, CSN	t_{rIN}	–	–	50	ns	[1]
4.4.60	Input Signal Fall Time at pin SDI, SCLK, CSN	t_{fIN}	–	–	50	ns	[1]
Data Output Timing. See Figure 14 and Figure 15							
4.4.61	SDO Rise Time	t_{rSDO}	–	10	25	ns	C_{load} = 40pF [1]
4.4.62	SDO Fall Time	t_{fSDO}	–	10	25	ns	C_{load} = 40pF [1]
4.4.63	SDO Valid Time	t_{VASDO}	–	20	50	ns	V_{SDO} < 0.2V_{DD} V_{SDO} > 0.7V_{DD} C_{load} = 40pF [1]
4.4.64	SDO Enable Time after CSN falling edge	t_{ENSDO}	–	–	50	ns	Low Impedance [1]
4.4.65	SDO Disable Time after CSN rising edge	t_{DISSDO}	–	–	50	ns	High Impedance [1]
4.4.66	Duty cycle of incoming clock at SCLK	$duty_{SCLK}$	40	–	60	%	[1]

Electrical Characteristics (cont'd)

V_S= 7 V to 18 V, V_{DD}= 3.0 V to 5.5 V, T_j = -40 °C to +150 °C, INH = HIGH; $I_{OUT1-10}$ = 0 A; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Thermal Prewarning & Shutdown							
4.4.67	Thermal warning junction temperature	T_{jW_enter}	120	140	170	°C	See **Figure 6** 1)
4.4.68	Thermal warning junction temperature - switch off	T_{jW_exit}	90	–	140	°C	
4.4.69	Temperature warning hysteresis	ΔT_{jW}	–	30	–	K	
4.4.70	Thermal shutdown junction temperature	T_{jSD}	150	175	200	°C	
4.4.71	Thermal switch-on junction temperature	T_{jSO}	130	–	180	°C	
4.4.72	Temperature shutdown hysteresis	ΔT_{jSD}	–	20	–	K	
4.4.73	Ratio of SD to W temperature	T_{jSD} / T_{jW}	1.05	1.20	–	–	

1) Not subject to production test, specified by design

2) CSN High Time : This is the minimum time the user must wait between SPI commands

5 Block Description

5.1 General

5.2 Power Supply

5.2.1 General

The TLE84110EL has two power supply inputs: The half bridge outputs are connected to V_S supply, which is connected to the 12V automotive supply rail. The internal logic part is supplied by a separate voltage V_{DD} = 5 V. V_S and V_{DD} supplies are separated so that information stored in the logic block remains intact in the event of voltage drop outs or disturbances on V_S. The system can therefore continue to operate once V_S has recovered, without having to resend commands to the device.

A rising edge on V_{DD} triggers an internal Power-On Reset (POR) to initialize the IC at power-on. All data stored internally is deleted, and the outputs are switched to high-impedance status (tristate). A 10µF electrolytic and 100nF ceramic capacitor are recommended to be placed as close as possible to the V_S supply pin of the device for improved EMC performance in the high and low frequency band.

5.2.2 Sleep Mode

The TLE84110EL enters low power mode (or sleep mode) by setting the INH input to low. The INH input has an internal pull-down resistor. In sleep-mode, all output transistors are turned off and the SPI register banks are reset.

5.2.3 Reverse Polarity Protection

The TLE84110EL requires an external reverse polarity protection. During reverse polarity, the freewheeling diodes across the half bridge output will begin to conduct, causing an undesired current flow (I_{RB}) from ground potential to battery and excessive power dissipation across the diodes. As such, a reverse polarity protection diode is recommended (see **Figure 4**).

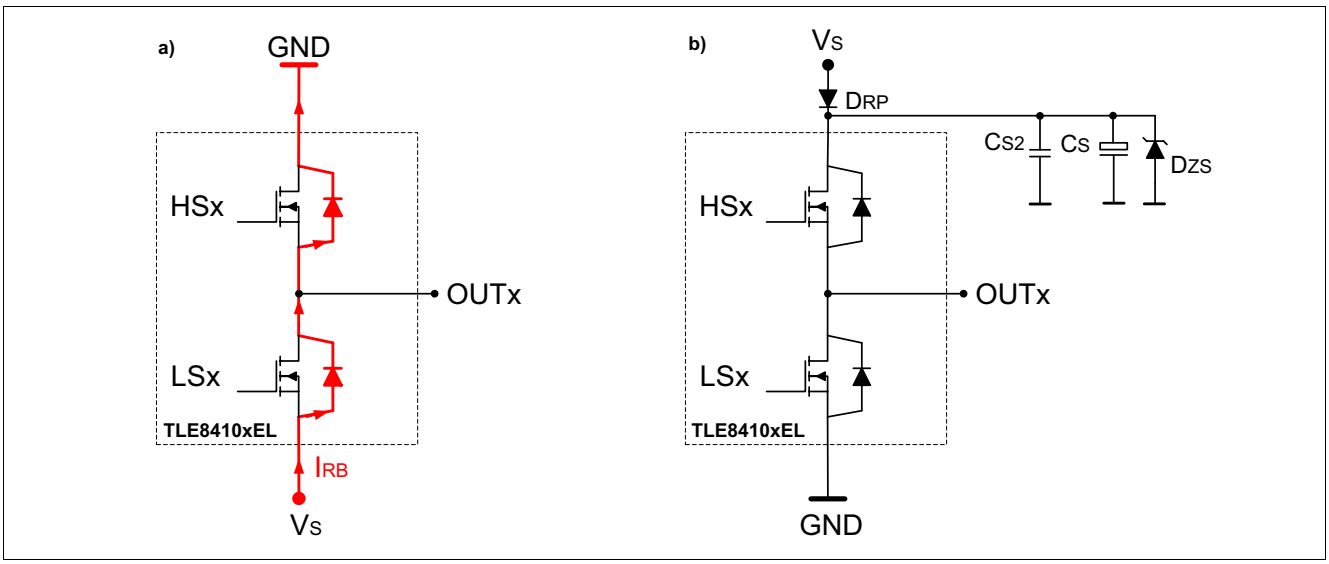


Figure 4 Reverse Polarity Protection

5.2.4 Power Supply Monitoring

The power supply rails V_S and V_{DD} are monitored for over- and undervoltage. See **Figure 5**.

5.2.4.1 V_S Undervoltage

If the supply voltage V_S drops below the switch off voltage V_{UVOFF}, all output transistors are switched off but logic information remains intact and uncorrupted. The “undervoltage” (Power Supply Fail, PSF) error bit is flagged and can be read out via SPI. Once V_S rises again and reaches the threshold switch on voltage V_{UVON}, the power stages are restarted and the PSF error bit is reset.

5.2.4.2 V_S Overvoltage

If the supply voltage V_S rises above the switch off voltage V_{OVOFF}, all output transistors are switched off and the “overvoltage” (PSF) error bit is set. The error is not latched, i.e. if V_S falls again and reaches the switch on voltage V_{OVON}, the power stages are restarted and the Error Flags are reset.

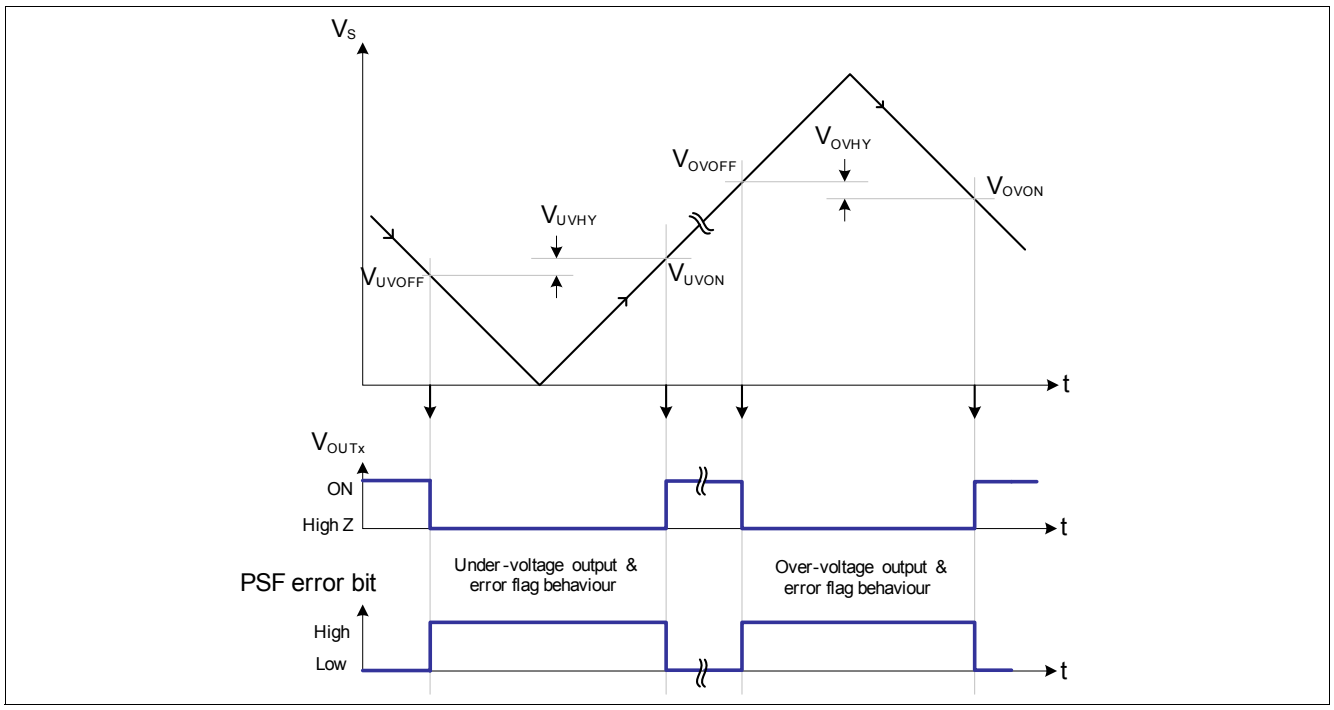


Figure 5 Output behavior during Over- and Undervoltage V_S condition

5.2.5 Reset Behavior

The following reset triggers have been implemented in the TLE84110EL:-

V_{DD} Undervoltage Reset:

The SPI Interface shall not function if V_{DD} is below the undervoltage threshold, $V_{DD\ POffR}$. The digital Block will be initialized. The output stages are switched off to High-Z. The undervoltage reset and SRR is released once V_{DD} voltage levels are above the undervoltage threshold, $V_{DD\ POR}$.

Reset on INH pin:

If the INH pin level is low, the device shall enter reset and the current consumption is reduced to $I_{SQ} + I_{DD\_Q}$.

5.3 Temperature Monitoring

Temperature sensors are integrated in the power stages. The temperature monitoring circuit compares the measured temperature to the warning and shutdown thresholds. If one or more temperature sensors reach the warning temperature, the temperature warning bit, TW is set to HIGH. This bit is not latched (i.e. if the temperature falls below the warning threshold (with hysteresis), the TW bit is reset to LOW again).

If one or more temperature sensors reach the shut-down temperature threshold, all outputs are shut down and latched (i.e. the output stages remain off until an SRR command is sent or a power-on reset is performed). See **Figure 6**.

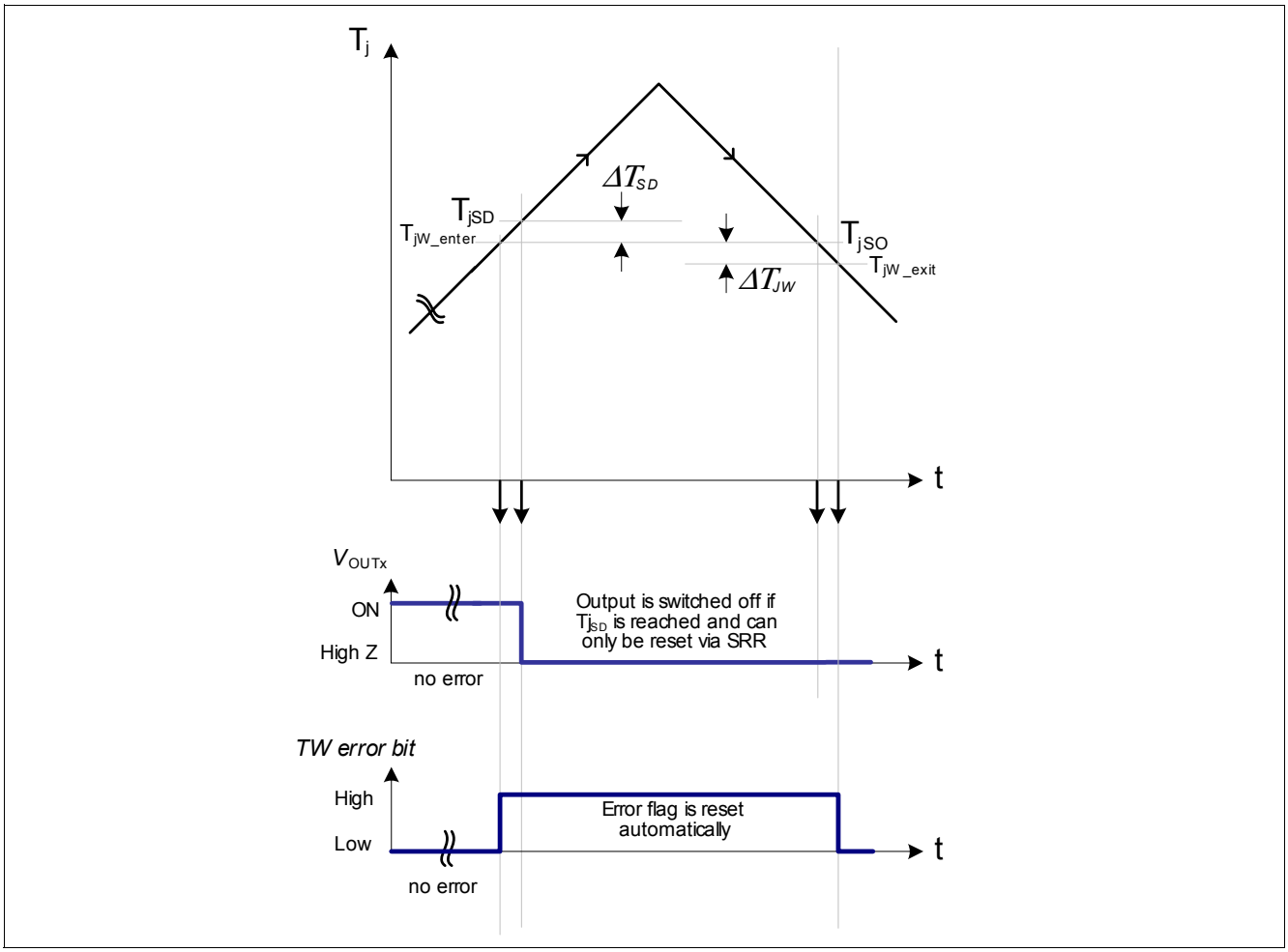


Figure 6 Overtemperature Behavior

5.4 Protection and Diagnosis

This device features embedded protective functions which are designed to prevent IC destruction under fault conditions described in the following sections. Fault conditions are treated as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

5.4.1 Short Circuit of Output to Supply or Ground

The high-side switches are protected against short to ground where as the low-side switches are protected against short to supply.

If a switch is turned on and the current rises above the overcurrent shutdown threshold, I_{SD} for longer than the shutdown delay time t_{dSD}, the output transistor is turned off and the corresponding diagnosis bit, OC, is set. During this delay time, the current is limited to I_{SC} as shown in **Figure 7**. The output stage remains off and the error bit remains set until a status register reset is sent to the SPI or a power-on reset is performed.

..

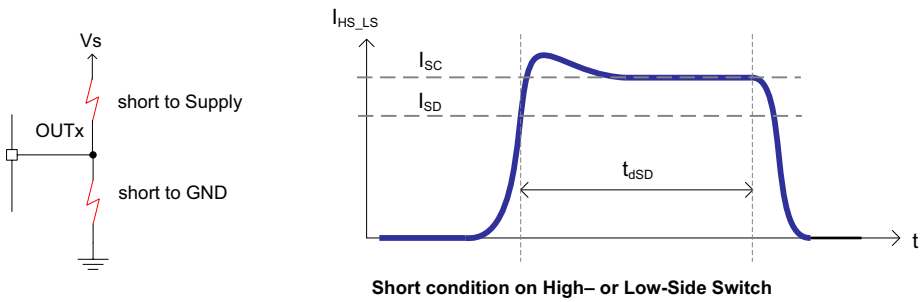


Figure 7 High-Side and Low-Side Switch - Short Circuit and Overcurrent Protection

5.4.2 Open Load

Open-load detection in ON-state is implemented in the Low-Side switches of the bridge outputs: If the current through the low side transistor is lower than the reference current I_{OLD} in ON-state for longer than the open-load detection delay time t_{dOLD}, the corresponding open-load, OL diagnosis bit is set. The output transistor, however, remains ON. The open load error bit is latched and can be reset by the SPI status register reset or by a power-on reset.

As an example, if a motor is connected between outputs OUT 1 and OUT 2 with a broken wire as shown in **Figure 8**, the resulting diagnostic information is shown in **Table 2**.

Open Load Detection Shutdown (OL SD EN) Bit via the Control Register can be activated or deactivated as required. If the OL SD EN bit is set and an open load on the Low-Side Switch is detected, the respective output is disabled. The error remains latched and output is off until an SRR or power on reset is performed. This has the added advantage of independently diagnosing and isolating error flags to the corresponding failed output.

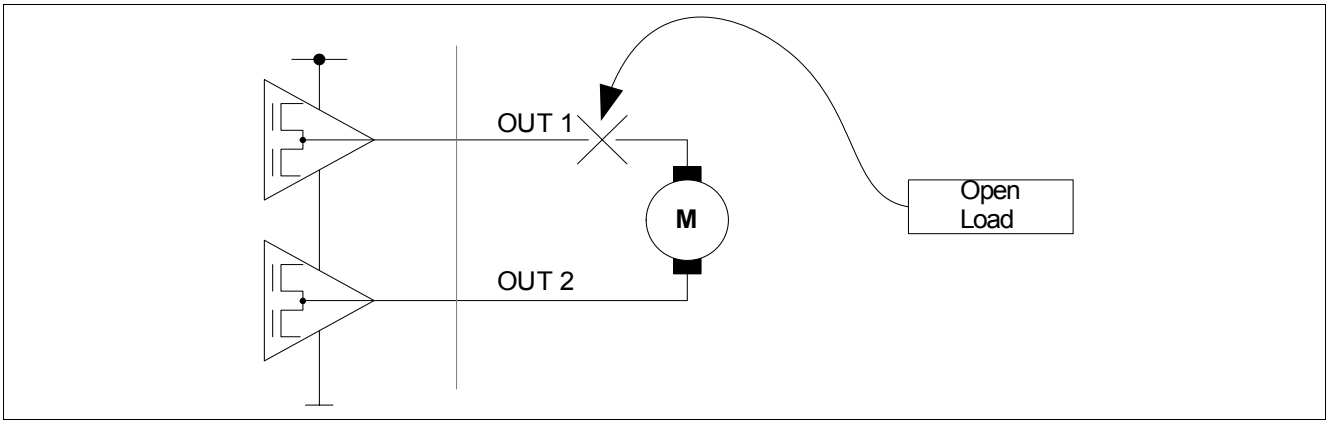


Figure 8 Open Load Example

Table 2 Open Load Diagnosis Example

Control					Diagnostic Information				
					Motor Connected		Motor Disconnected		Open Load Detection (OPLD) Error Flag
LS1 ON	HS1 ON	LS2 ON	HS2 ON	Motor Rotation	LS1 OpL	LS2 OpL	LS1 OpL	LS2 OpL	
0	0	0	0	motor off	0	0	0	0	de-activated
1	0	0	1	clock-wise	0	0	1	0	activated
0	1	1	0	counter clock-wise	0	0	0	1	activated
0	1	0	1	brake high	0	0	0	0	de-activated
1	0	1	0	brake low	1	1	1	1	activated

5.4.3 Cross-Current

In bridge configurations the high-side and low-side power transistors are ensured never to be simultaneously “ON” to avoid cross currents. This is realized by integrating delays in the driver stage of the power outputs, intended to create a dead-time between switching off one Power Transistor and switching on of the other Power Transistor of the same half-bridge. To ensure that there is no overlap of the switching slopes that would lead to a cross current, the dead-times, t_{DHL} and t_{DLH} are specified.

In the event a cross-current has occurred, the device shall turn off both switches and the Overcurrent bit is set High.

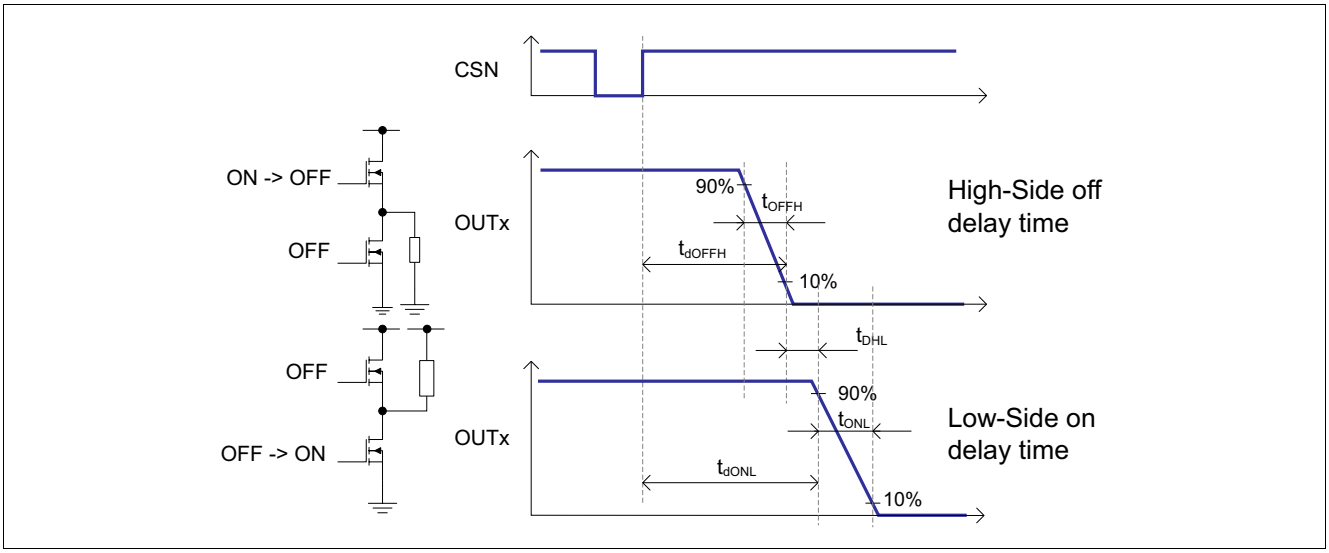


Figure 9 Timing Bridge Outputs High to Low

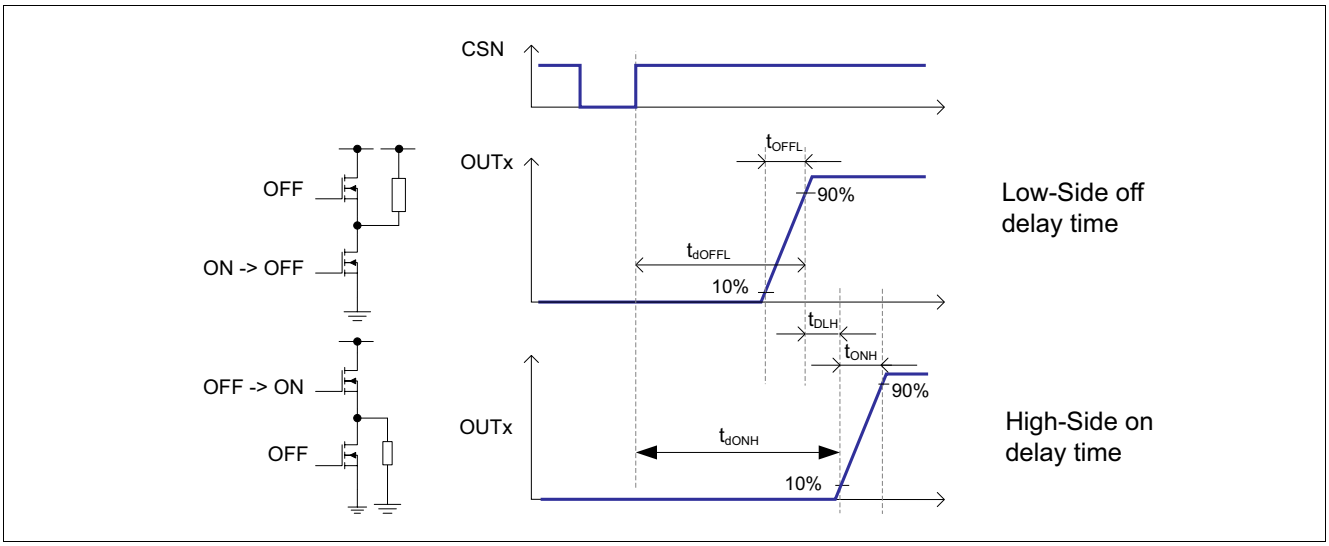


Figure 10 Timing Bridge Outputs Low to High

6 SPI

6.1 General

The SPI is used for bidirectional communication with a control unit. The TLE84110EL acts as SPI-slave and the control unit acts as SPI-master. The 16-bit control word is read via the SDI serial data input. The status word appears synchronously at the SDO serial data output. The communication is synchronized by the serial clock input SCLK.

Standard data transfer timing is shown in **Figure 11**. The clock polarity is data valid on falling edge. SCLK must be low during CSN transition. The transfer is MSB first.

The transmission cycle begins when the chip is selected with the chip-select-not (CSN) input (H to L). Then the data is clocked through the shift register. The transmission ends when the CSN input changes from L to H and the word which has been read into the shift register becomes the control word. The SDO output switches then to tristate status, thereby releasing the SDO bus circuit for other uses. The SPI allows to parallel multiple SPI devices by using multiple CSN lines. The SPI can also be used with other SPI-devices in a daisy-chain configuration.

The control word transmitted from the master to the TLE84110EL is executed at the end of the SPI transmission (CSN L -> H) and remains valid until a different control word is transmitted or a power on reset occurs. At the beginning of the SPI transmission (CSN H -> L), the diagnostic data currently valid are latched into the SPI and transferred to the master.

Data integrity is maintained by polling multiples of 8 data bits to ensure that a valid command has been received.

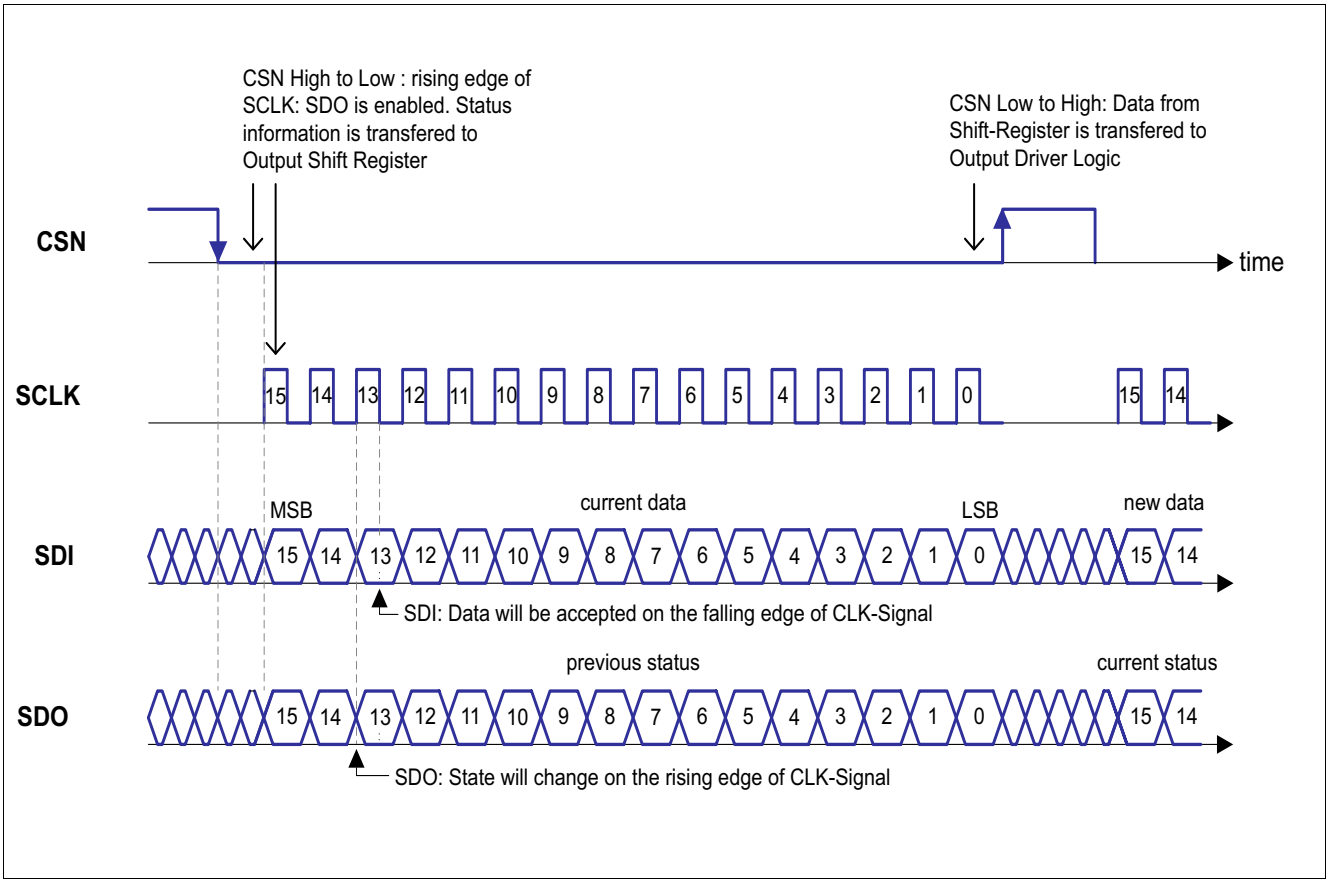


Figure 11 SPI Data Transfer Protocol

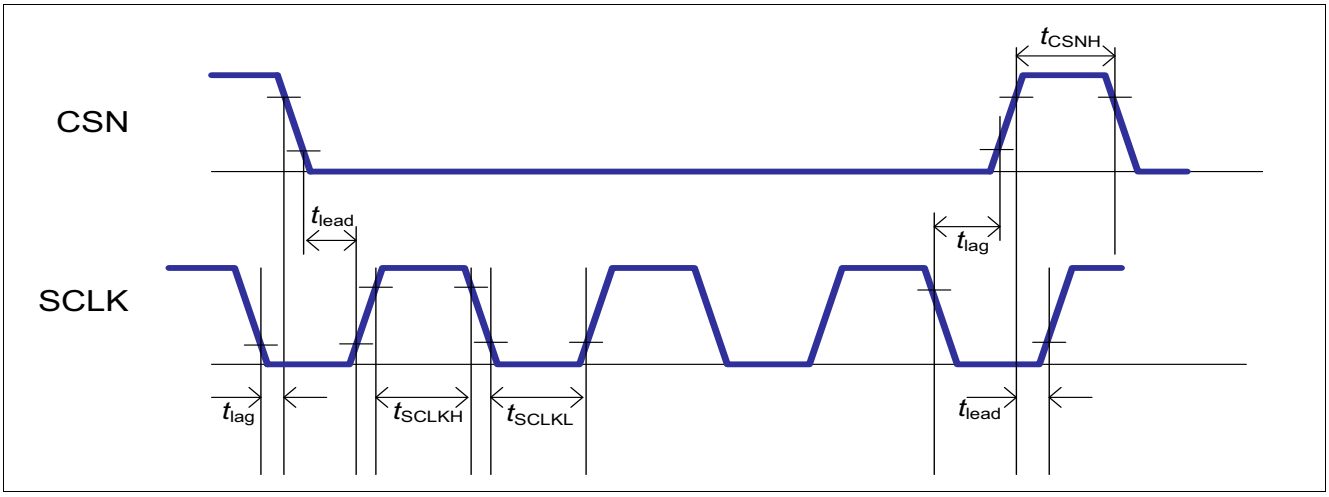


Figure 12 SPI SCLK and CSN

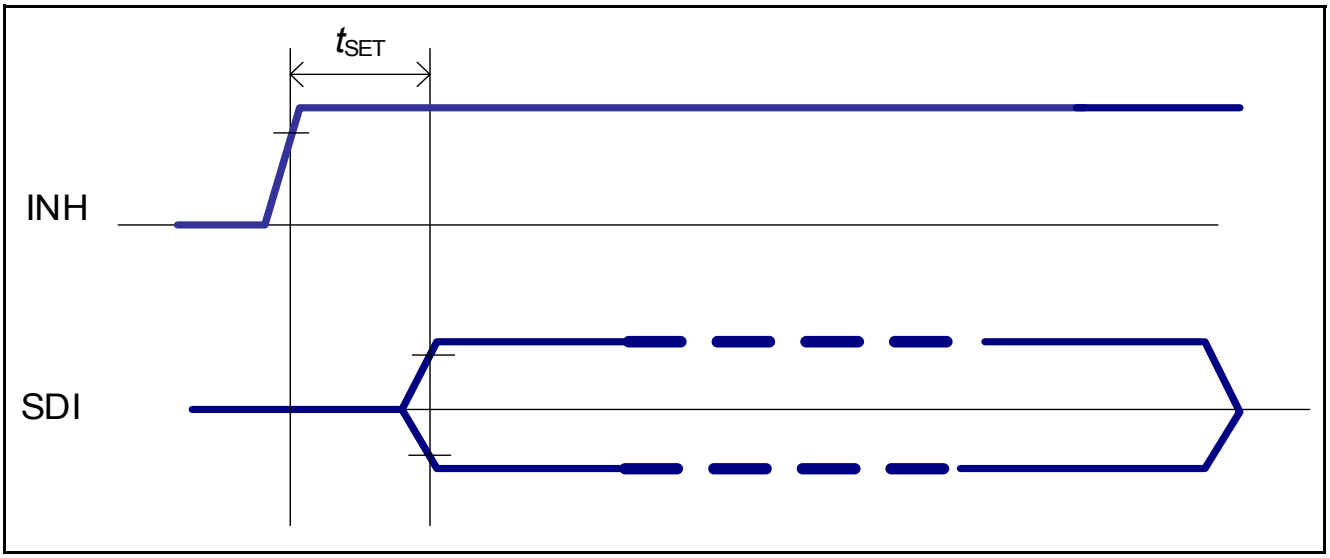


Figure 13 INH and SDI

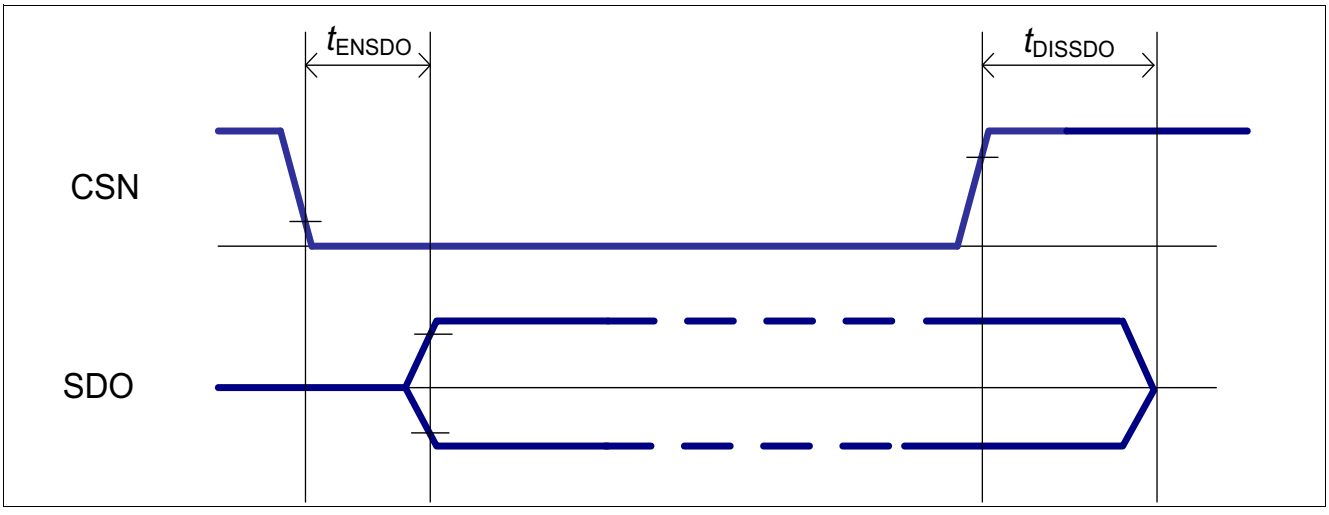


Figure 14 SPI SDO and CSN

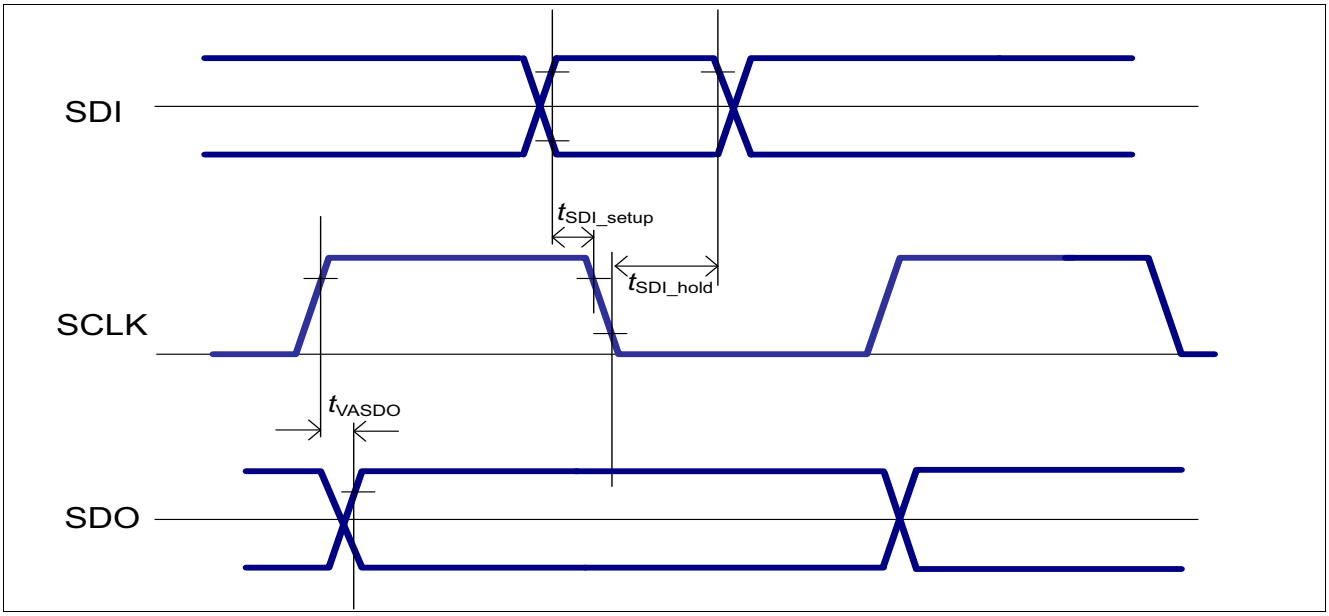


Figure 15 SPI SDI, SDO and SCLK

6.2 Status Register Reset

The SPI is using a standard shift-register concept with daisy-chain capability. Any data transmitted to the SPI will be available to the internal logic part at the end of the SPI transmission (CSN L -> H). To read a specific register, the address of the register is sent by the master to the SPI in a first SPI frame. The data that corresponds to this address is transmitted by the SDO during the following (second) SPI frame to the master. The default address for Status Register transmission after Power-ON Reset is 0.

The Status-Register-Reset command-bit is executed after the next SPI transmission. The two bits, Address Register and SRR act as command to read and reset (or not reset) the addressed Status-Register. The request and response behaviour of the SPI is further illustrated in **Figure 16** below.

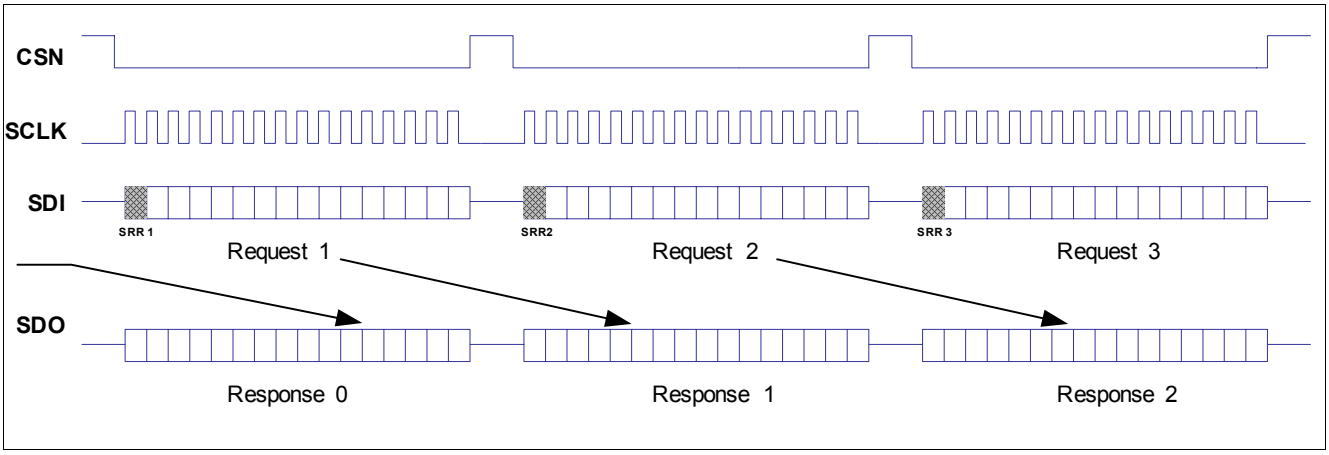


Figure 16 Status Register Reset

6.3 SPI Bit Definitions

6.3.1 Control - Word

Control Register Overview

Control Register 0 for HB 1 : HB 6

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRR	0	OL_SD _EN	ACT_ HB6	ACT_ HB5	ACT_ HB4	ACT_ HB3	ACT_ HB2	ACT_ HB1	CONF_ HB6	CONF_ HB5	CONF_ HB4	CONF_ HB3	CONF_ HB2	CONF_ HB1	0

Control Register 1 for HB 7 : HB 10

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SRR	1	OL_SD _EN	X	X	ACT_ HB10	ACT_ HB9	ACT_ HB8	ACT_ HB7	X	X	CONF_ HB10	CONF_ HB9	CONF_ HB8	CONF_ HB7	0

Table 3 Input (Control) Data Register

Bit	Control Register - 0 HB 1:6	Control Register - 1 HB 7:10	Control Register - 0 HB 1:6 DESCRIPTION	Control Register - 1 HB 7:10 DESCRIPTION
Diagnosis & Register Control				
15	SRR (HB1:6)	SRR (HB7:10)	Status Register Reset (SRR) for HB1 to HB 6. If set to high, the errors bits of the coresponding status register are reset on the rising edge of CSN if sent to the uC. Low indicates no reset.	Status Register Reset (SRR) for HB7 to HB 10. If set to high, the errors bits of the coresponding status register are reset on the rising edge of CSN if sent to the uC. Low indicates no reset.
14	0	1	Address Register	
13	OL SD EN (HB1:6)	OL SD EN (HB7:10)	Open Load Detection Shutdown Enable (OL SD EN) for HB1 to HB 6. This feature allows the affected output stage to be switched off if a true open load or underload condition has been detected. It can be activated or deactivated by bit 13.	Open Load Detection Shutdown Enable (OL SD EN) for HB7 to HB 10. This feature allows the affected output stage to be switched off if a true open load or underload condition has been detected. It can be activated or deactivated by bit 13.
Activate Half-Bridge X				
12	ACT_HB 6	X	H => Half Bridge 6 is active L => Half Bridge 6 is in Hi-Z	X => Don't Care
11	ACT_HB 5	X	H => Half Bridge 5 is active L => Half Bridge 5 is in Hi-Z	X => Don't Care
10	ACT_HB 4	ACT_HB 10	H => Half Bridge 4 is active L => Half Bridge 4 is in Hi-Z	H => Half Bridge 10 is active L => Half Bridge 10 is in Hi-Z

Table 3 Input (Control) Data Register

Bit	Control Register - 0 HB 1:6	Control Register - 1 HB 7:10	Control Register - 0 HB 1:6 DESCRIPTION	Control Register - 1 HB 7:10 DESCRIPTION
9	ACT_HB 3	ACT_HB 9	H => Half Bridge 3 is active L => Half Bridge 3 is in Hi-Z	H => Half Bridge 9 is active L => Half Bridge 9 is in Hi-Z
8	ACT_HB 2	ACT_HB 8	H => Half Bridge 2 is active L => Half Bridge 2 is in Hi-Z	H => Half Bridge 8 is active L => Half Bridge 8 is in Hi-Z
7	ACT_HB 1	ACT_HB 7	H => Half Bridge 1 is active L => Half Bridge 1 is in Hi-Z	H => Half Bridge 7 is active L => Half Bridge 7 is in Hi-Z
Configure Half-Bridge X				
6	CONF_HB 6	X	H => HSD6 = ON & LSD6 = OFF L => HSD6 = OFF & LSD6 = ON	X => Don't Care
5	CONF_HB 5	X	H => HSD5 = ON & LSD5 = OFF L => HSD5 = OFF & LSD5 = ON	X => Don't Care
4	CONF_HB 4	CONF_HB 10	H => HSD4 = ON & LSD4 = OFF L => HSD4 = OFF & LSD4 = ON	H => HSD10 = ON & LSD10 = OFF L => HSD10 = OFF & LSD10 = ON
3	CONF_HB 3	CONF_HB 9	H => HSD3 = ON & LSD3 = OFF L => HSD3 = OFF & LSD3 = ON	H => HSD9 = ON & LSD9 = OFF L => HSD9 = OFF & LSD9 = ON
2	CONF_HB 2	CONF_HB 8	H => HSD2 = ON & LSD2 = OFF L => HSD2 = OFF & LSD2 = ON	H => HSD8 = ON & LSD8 = OFF L => HSD8 = OFF & LSD8 = ON
1	CONF_HB 1	CONF_HB 7	H => HSD1 = ON & LSD1 = OFF L => HSD1 = OFF & LSD1 = ON	H => HSD7 = ON & LSD7 = OFF L => HSD7 = OFF & LSD7 = ON
0	**0**		**Least Significant Bit (LSB) is set to Low**	

6.3.2 Diagnosis - Word

Diagnosis Register Overview

Diagnosis Register 0 for HB 1 : HB 6

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC	PSF	OL	SACT_HB6	SACT_HB5	SACT_HB4	SACT_HB3	SACT_HB2	SACT_HB1	SCONF_HB6	SCONF_HB5	SCONF_HB4	SCONF_HB3	SCONF_HB2	SCONF_HB1	TW

Diagnosis Register 1 for HB 7 : HB 10

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OC	PSF	OL	X	X	SACT_HB10	SACT_HB9	SACT_HB8	SACT_HB7	X	X	SCONF_HB10	SCONF_HB9	SCONF_HB8	SCONF_HB7	TW

Table 4 Output (Status) Data Register

Bit	Status Register - 0 HB 1:6	Status Register - 1 HB 7:10	Status Register- 0 HB 1:6 DESCRIPTION	Status Register - 1 HB 7:10 DESCRIPTION
Diagnosis & Register Control				
15	OC (HB1:6)	OC (HB7:10)	Overcurrent Error is set if any one of HB1 to HB6 has an overload, short circuit or cross current; The error is latched and the corresponding output is switched off; Bit 15 error can only be reset via SRR or power-on reset.	Overcurrent Error is set if any one of HB7 to HB10 has an overload, short circuit or cross current; The error is latched and the corresponding output is switched off; Bit 15 error can only be reset via SRR or power-on reset.
14	PSF		Power Supply Failure; Global Error Flag; Bit 14 is set if VS has an overvoltage or undervoltage condition; All outputs are switched OFF. Bit 14 is automatically reset if VS returns to its normal operating range.	
13	OL (HB1:6)	OL (HB7:10)	Open Load Error is set if any one of HB1 to HB6 has a true open load or underload error condition; The error is latched. The corresponding output is switched off if Bit 13, OL SD EN of the Control Register is activated or high. Bit 13 error can only be reset via SRR or power-on reset.	Open Load Error is set if any one of HB7 to HB10 has a true open load or underload error condition; The error is latched. The corresponding output is switched off if Bit 13, OL SD EN of the Control Register is activated or high. Bit 13 error can only be reset via SRR or power-on reset.
Activate Half-Bridge X				
12	SACT_HB 6	X	H => Half Bridge 6 is active L => Half Bridge 6 is in Hi-Z	X => Don't Care
11	SACT_HB 5	X	H => Half Bridge 5 is active L => Half Bridge 5 is in Hi-Z	X => Don't Care

Table 4 Output (Status) Data Register

Bit	Status Register - 0 HB 1:6	Status Register - 1 HB 7:10	Status Register- 0 HB 1:6 DESCRIPTION	Status Register - 1 HB 7:10 DESCRIPTION
10	SACT_HB 4	SACT_HB 10	H => Half Bridge 4 is active L => Half Bridge 4 is in Hi-Z	H => Half Bridge 10 is active L => Half Bridge 10 is in Hi-Z
9	SACT_HB 3	SACT_HB 9	H => Half Bridge 3 is active L => Half Bridge 3 is in Hi-Z	H => Half Bridge 9 is active L => Half Bridge 9 is in Hi-Z
8	SACT_HB 2	SACT_HB 8	H => Half Bridge 2 is active L => Half Bridge 2 is in Hi-Z	H => Half Bridge 8 is active L => Half Bridge 8 is in Hi-Z
7	SACT_HB 1	SACT_HB 7	H => Half Bridge 1 is active L => Half Bridge 1 is in Hi-Z	H => Half Bridge 7 is active L => Half Bridge 7 is in Hi-Z
Configure Half-Bridge X				
6	SCONF_HB 6	X	H => HSD6 = ON & LSD6 = OFF L => HSD6 = OFF & LSD6 = ON	X => Don't Care
5	SCONF_HB 5	X	H => HSD5 = ON & LSD5 = OFF L => HSD5 = OFF & LSD5 = ON	X => Don't Care
4	SCONF_HB 4	SCONF_HB 10	H => HSD4 = ON & LSD4 = OFF L => HSD4 = OFF & LSD4 = ON	H => HSD10 = ON & LSD10 = OFF L => HSD10 = OFF & LSD10 = ON
3	SCONF_HB 3	SCONF_HB 9	H => HSD3 = ON & LSD3 = OFF L => HSD3 = OFF & LSD3 = ON	H => HSD9 = ON & LSD9 = OFF L => HSD9 = OFF & LSD9 = ON
2	SCONF_HB 2	SCONF_HB 8	H => HSD2 = ON & LSD2 = OFF L => HSD2 = OFF & LSD2 = ON	H => HSD8 = ON & LSD8 = OFF L => HSD8 = OFF & LSD8 = ON
1	SCONF_HB 1	SCONF_HB 7	H => HSD1 = ON & LSD1 = OFF L => HSD1 = OFF & LSD1 = ON	H => HSD7 = ON & LSD7 = OFF L => HSD7 = OFF & LSD7 = ON
0	TW		Thermal Warning Bit; Global Error Flag; This bit is treated as an early warning and will be set to High if the junction temperature reaches $T_{JW.}$ The output remains on until one or more sensors reaches T_{SD} causing all outputs to be switched off simultaneously. Bit 0 is automatically reset if the junction temperature cools down to T_{JSO}	

Note: Status HBx represents status of Half-Bridge Driver and NOT status of Control Register.

Note: The PSF and TW bits in the first Diagnosis word will reflect the current clock cycle status, all other remaining bits are 0.

7 Application Information

Note: The following simplified application examples are given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. The function of the described circuits must be verified in the real application.

7.1 Application Diagram

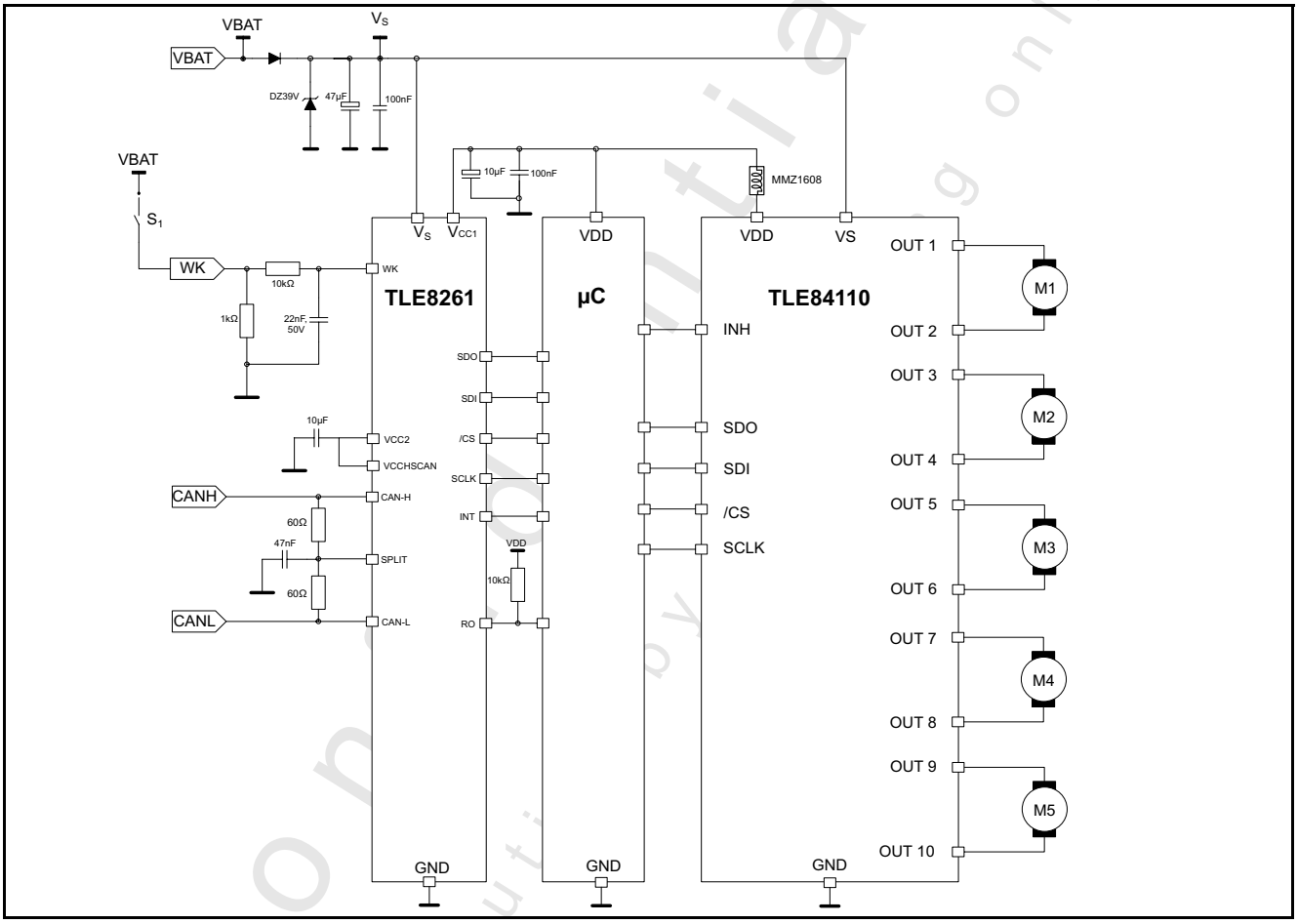


Figure 17 Application Example for DC-motor Loads

For optimum EMC performance, a ferrite is recommended to be placed in series and as close as possible to the Vdd line of the TLE841xy device. This is shown in the above application diagram example. The ferrite should have an impedance of 1000ohm at an effective frequency of 100MHz frequency. A recommended ferrite is the MMZ1608 type series available in a geometry size of 0603 with a DC resistance of 0.6ohm and allowable DC current of 190mA.

7.2 Thermal application information

Ta = -40°C, Ch 1 to Ch 10 are dissipating a total of 2.5W (0.25W each).

Ta = 85°C, Ch 1 to Ch 10 are dissipating a total of 1.8W (0.18W each).

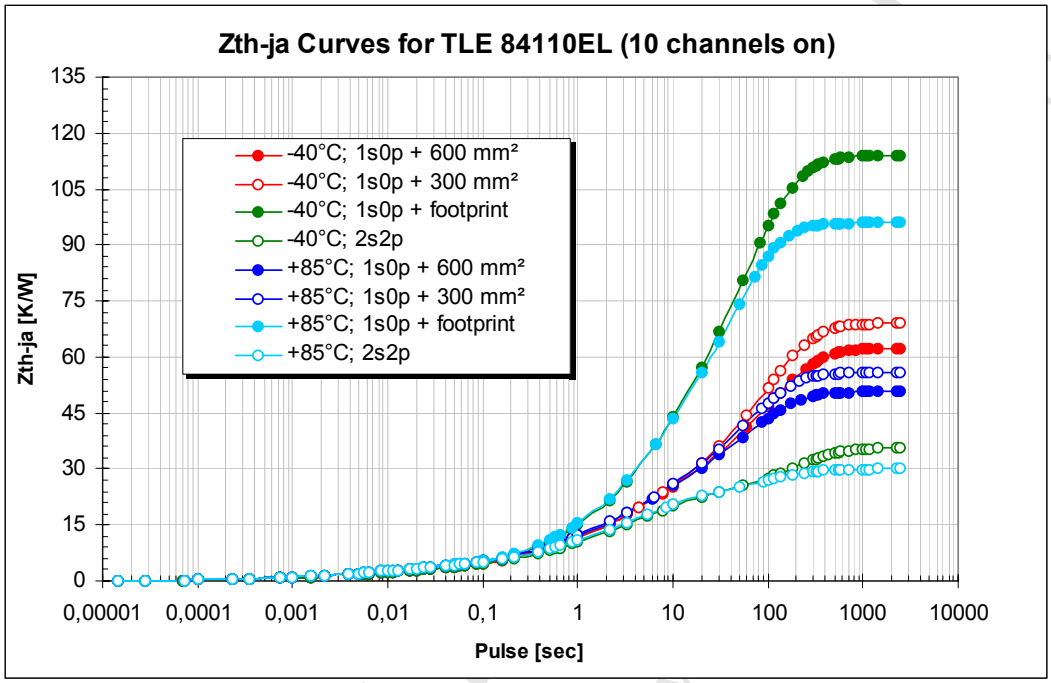


Figure 18 ZthJA Curve for different PCB setups

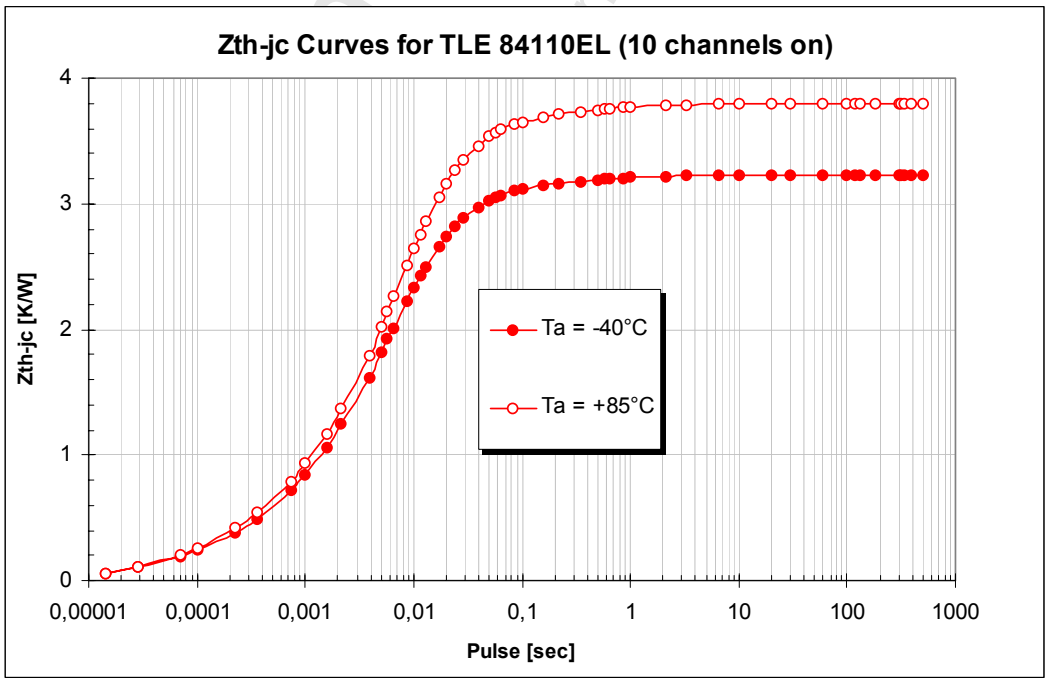


Figure 19 ZthJC Curve

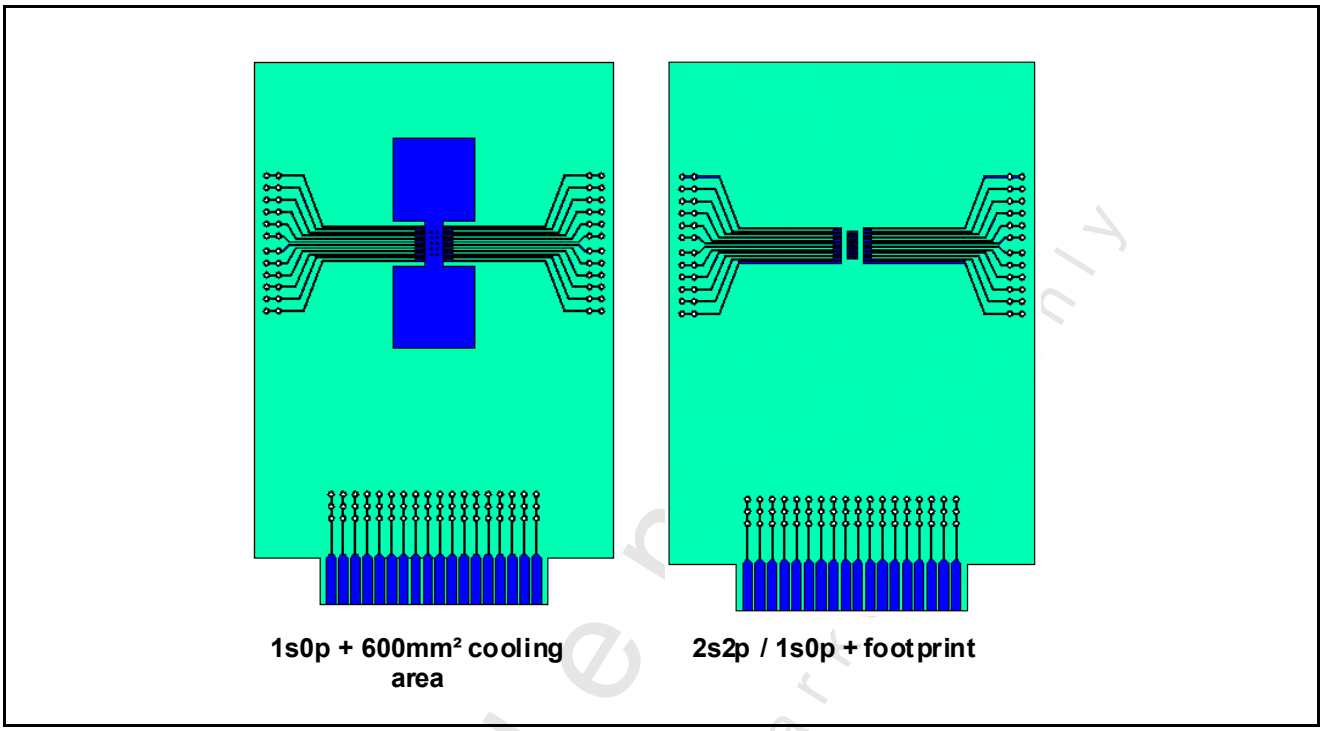


Figure 20 Board Setup

Board Setup based on JESD 51-3, -7 FR4 PCB with 35µm Cu.

8 Package Outlines

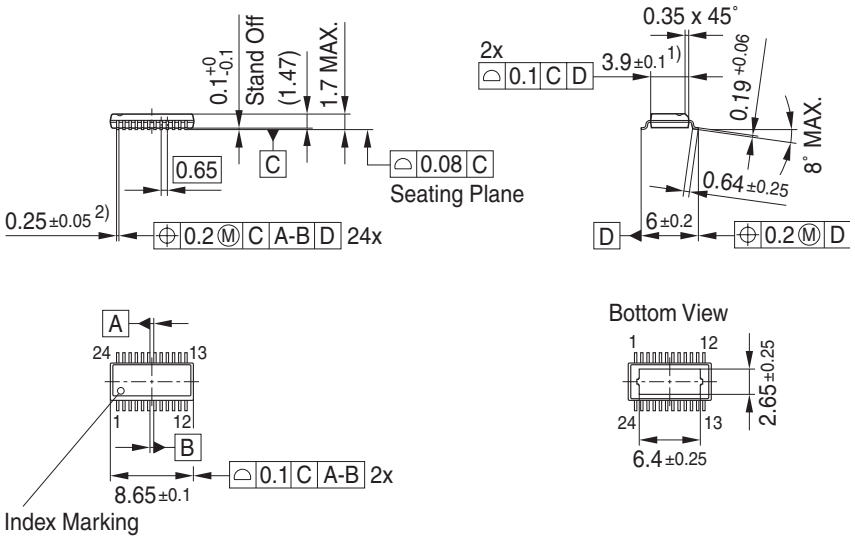


Figure 21 PG-SSOP-24-4 (Plastic/Plastic Green - Dual Small Outline Package)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: **http://www.infineon.com/products**.

Dimensions in mm

9 Revision History

0.30.40.3

TLE84110EL

Revision History: Rev. 1.0, 2010-04-27

Version	Subjects (major changes since last revision)
1.0	Final Data Sheet Release

Edition 2010-04-27

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