7-CHANNEL VIDEO SWITCH

Check for Samples: TS3V712E

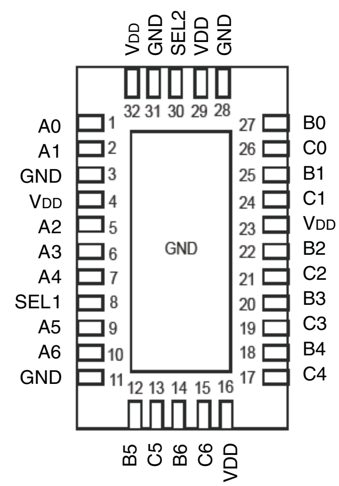
FEATURES

- **High Bandwidth (BW = 1.36 GHz)**
- **Designed for 7-Channel VGA Signals (R,G,B, H_{sync}, V_{sync}, DDC Dat, and DDC CLK)**
- **Separate Control Logic for Data and Control Signals**
- **Operating Voltage: 3.3 V ±10%**
- **Low and Flat ON-State Resistance**
  - **r_{ON} = 3 Ω**
  - **$r_{ON(flat)}$ = 500 mΩ**
- **Low Crosstalk (X_{TALK} = –49.76 dB Typ at 250 MHz)**
- **Low Input/Output Capacitance**
  - **C_{ON} = 7 pF, Typ**
- **ESD Performance Tested**
  - **4-kV IEC61000-4-2, Contact Discharge on Switch IOs**
  - **3-kV Human Body Model Per JESD22-A114E**
  - **6-kV Human Body Model (Switch Pins to GND)**
- **Suitable for Both RGB and Composite-Video Switching**
- **32-Pin Quad Flat Pack No-Lead QFN(RTG) Package**

APPLICATIONS

- **Notebook Computers**
- **Analog VGA Peripheral Ports**

RTG PACKAGE (TOP VIEW)



The exposed center pad must be connected to GND.

DESCRIPTION/ORDERING INFORMATION

The TS3V712E is a high-bandwidth, 7-channel video multiplexer/demultiplexer for switching between multiple VGA sources or end points. The device is designed for ensuring video signal integrity and minimizing the video signal attenuation by providing high bandwidth of 1.36 GHz.

The video signals are protected against high ESD with integrated diodes to V_{DD} and GND that will support up to 6-kV of ESD HBM and 4-kV contact protection.

The TS3V712E is available in a 32-pin QFN package and is characterized for operation over the free-air temperature range of –40°C to 85°C.

ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RTG	Tape and reel	TS3V712ERTGR	TF712E

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

LOGIC DIAGRAM

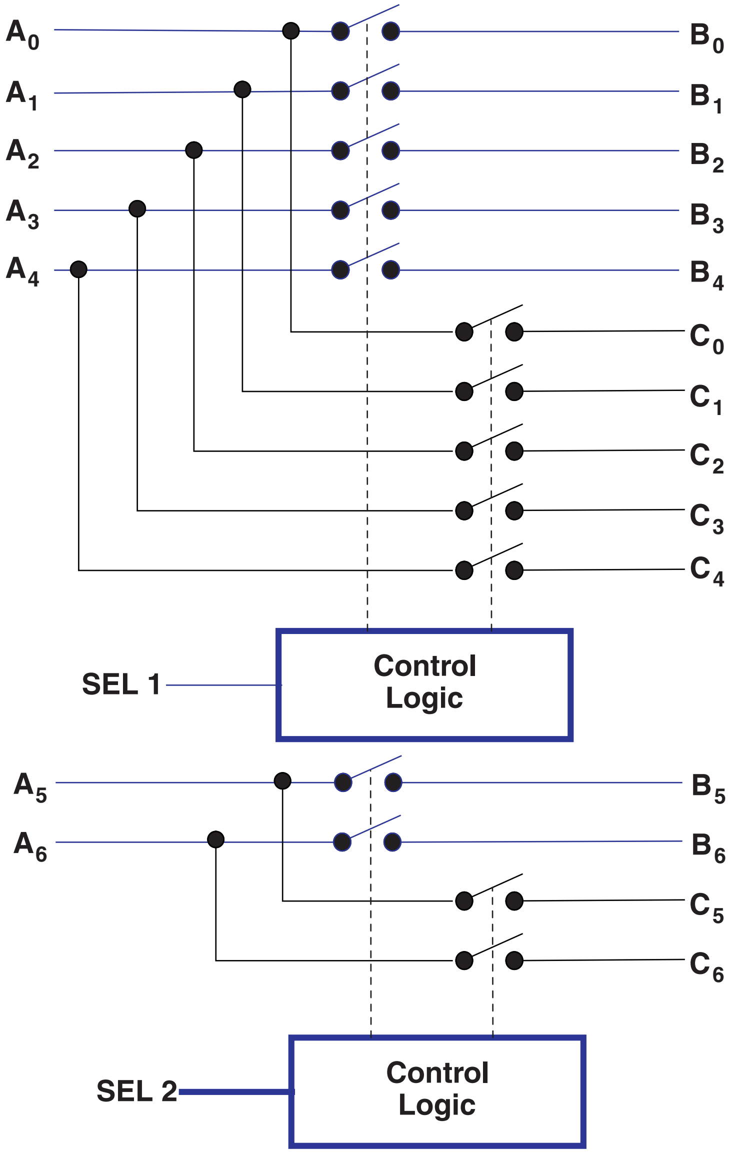


Table 1. FUNCTION TABLE

SEL1	SEL2	FUNCTION		
		A0–A4	A5, A6	Hi-Z
L	L	B0–B4	B5, B6	Cn
L	H	B0–B4	C5, C6	C0–C4, B5, B6
H	L	C0–C4	B5, B6	B0–B4, C5, C6
H	H	C0–C4	C5, C6	Bn

ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage range		–0.5	4.6	V
V_{IN}	Control input voltage range[2] [3]	SEL	–0.5	7	V
$V_{I/O}$	Switch I/O voltage range[2] [3] [4]	All I/O ports	–0.5	7	V
I_{IK}	Control input clamp current	$V_{IN} < 0$ V		–50	mA
$I_{I/OK}$	I/O port clamp current	$V_{I/O} < 0$ V		–50	mA
$I_{I/O}$	ON-state switch current[5]	ON-state switch		±128	mA
	Continuous current through V_{DD} or GND			±100	mA
θ_{JA}	Package thermal impedance	RTG package[6]		39.2	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for $V_{I/O}$.
(5) I_I and I_O are used to denote specific conditions for $I_{I/O}$.
(6) The package thermal impedance is calculated in accordance with JESD 51-5 (High K with via).

RECOMMENDED OPERATING CONDITIONS[1]

		MIN	MAX	UNIT
V_{DD}	Supply voltage	3	3.6	V
V_{IN}	Control input voltage (SEL)	0	5.5	V
V_{IH}	High-level control input voltage (SEL)	2		V
V_{IL}	Low-level control input voltage (EN, IN)	–0.5	0.8	V
$V_{I/O}$	I/O voltage (all ports)	0	V_{DD}	V
T_A	Operating free-air temperature	–40	85	°C

(1) All unused control inputs of the device must be held at V_{DD} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS[1]

for high-frequency switching over recommended operating free-air temperature range, V_{DD} = 3.3 V ±0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS				MIN	TYP[2]	MAX	UNIT
V_{IK}	SEL n	V_{DD} = 3.6 V,	I_{IN} = –18 mA				–0.7	–1.2	V
I_{IH}	SEL n	V_{DD} = 3.6 V,	V_{IN} = V_{DD}					±1	µA
I_{IL}	SEL n	V_{DD} = 3.6 V,	V_{IN} = GND					±1	µA
I_{OFF}		V_{DD} = 0 V,	V_O = 0 to 3.6 V,	V_I = 0,	V_{IN} = 0			1	µA
I_{CC}		V_{DD} = 3.6 V,	$I_{I/O}$ = 0,	V_{IN} = V_{DD} or GND,	Switch ON or OFF		200	500	µA
C_{IN}	SEL n	f = 10 MHz	V_{IN} = 0,				2.7	3	pF
C_{OFF}	3 ports	f = 10 MHz	V_{IN} = 0,	Output open,	Switch OFF		3	4	pF
C_{ON}	3 ports	f = 10 MHz	V_{IN} = 0,	Output open,	Switch ON		7		pF
r_{ON}		V_{DD} = 3 V,	0 V ≤ V_I ≤ 1.2 V,	$I_{I/O}$ = –40 mA			3	4	Ω
$r_{ON(flat)}$ [3]		V_{DD} = 3 V,	V_I = 0 V and 1.2 V	$I_{I/O}$ = –40 mA			0.5	1	Ω
Δr_{ON} [4]		V_{DD} = 3 V,	0 V ≤ V_I ≤ 1.2 V,	$I_{I/O}$ = –40 mA			0.1	1	Ω

(1) V_I, V_O, I_I, and I_O refer to I/O pins. V_{IN} refers to the control inputs.
(2) All typical values are at V_{DD} = 3.3 V (unless otherwise noted), T_A = 25°C.
(3) $r_{ON(flat)}$ is the difference of r_{ON} in a given channel at specified voltages.
(4) Δr_{ON} is the difference of r_{ON} from center port to any other ports.

DYNAMIC CHARACTERISTICS

over recommended operating free-air temperature range, V_{DD} = 3.3 V ±0.3 V, R_L = 50 Ω (unless otherwise noted)

PARAMETER	TEST CONDITIONS			TYP[1]	UNIT
X_{TALK}	R_L = 50 Ω,	f = 250 MHz,	See Figure 8	–49.76	dB
O_{IRR}	R_L = 50 Ω,	f = 250 MHz,	See Figure 8	–37.51	dB
BW	See Figure 6			1.36	GHz

(1) All typical values are at V_{CC} = 5 V (unless otherwise noted), T_A = 25°C.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{DD} = 3.3 V ±0.3 V, R_L = 50 Ω, T_A = 25°C (unless otherwise noted) (see Figure 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP	MAX	UNIT
t_{pd} [1]	An or Bn/Cn	Bn/Cn or An		0.25		ns
t_{PZH}, t_{PZL} [2]	SEL	Bn or Cn	0.5		12	ns
t_{PHZ}, t_{PLZ} [3]	SEL	Bn or Cn	0.5		11	ns
$t_{sk(o)}$ [4]	An, Bn, Cn			0.05	0.1	ns
$t_{sk(p)}$ [5]	An, Bn, Cn			0.05	0.1	ns

(1) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(2) Line enable time: SEL to input, output; also called as SEL to switch turn on time.
(3) Line disable time: SEL to input, output; also called as SEL to switch turn off time.
(4) Output skew between center port to any other ports.
(5) Skew between opposite transitions of the same output. $|t_{PHL} - t_{PLH}|$

TYPICAL CHARACTERISTICS

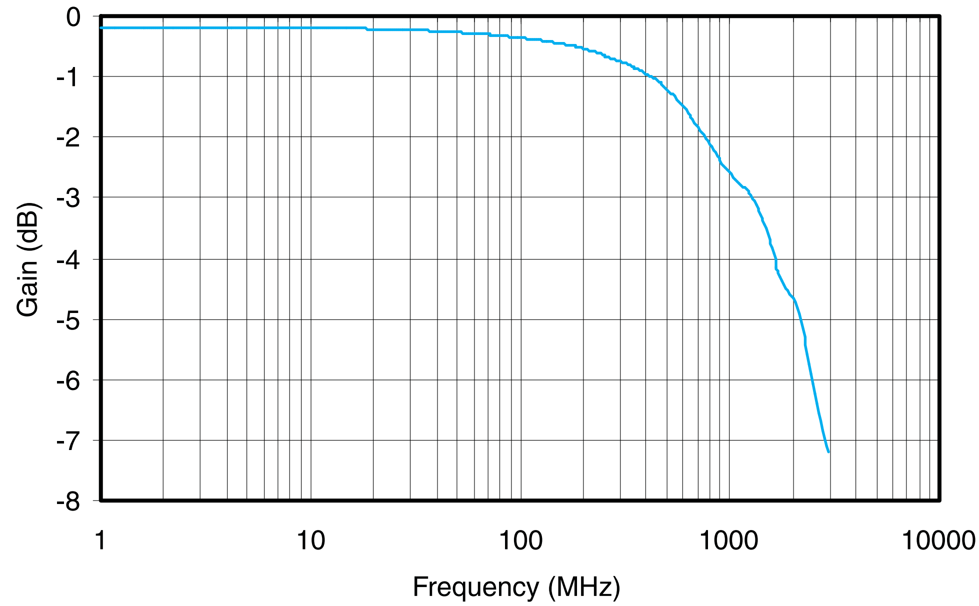


Figure 1. Gain vs Frequency

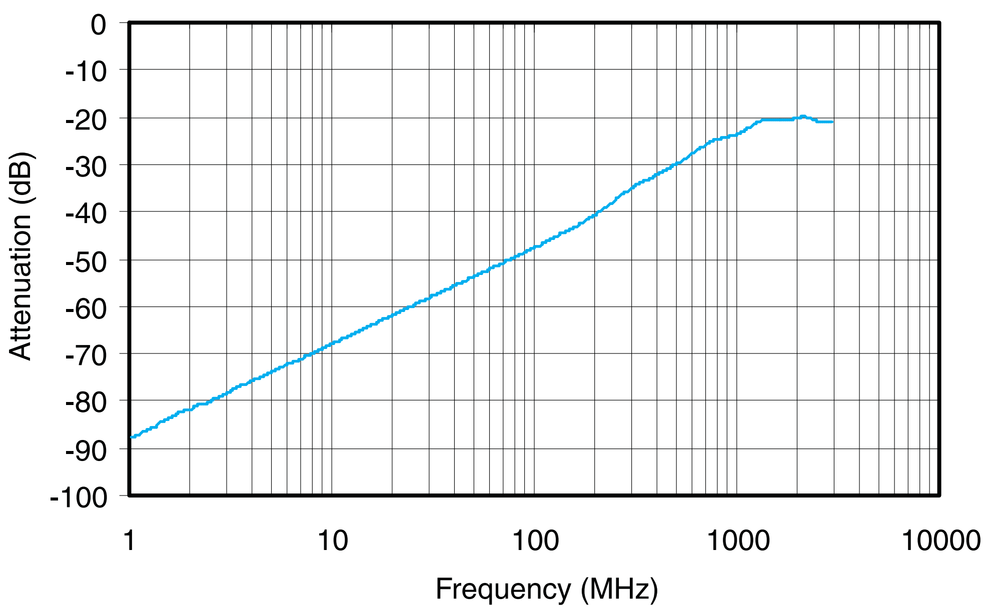


Figure 2. Off Isolation vs Frequency

TYPICAL CHARACTERISTICS (continued)

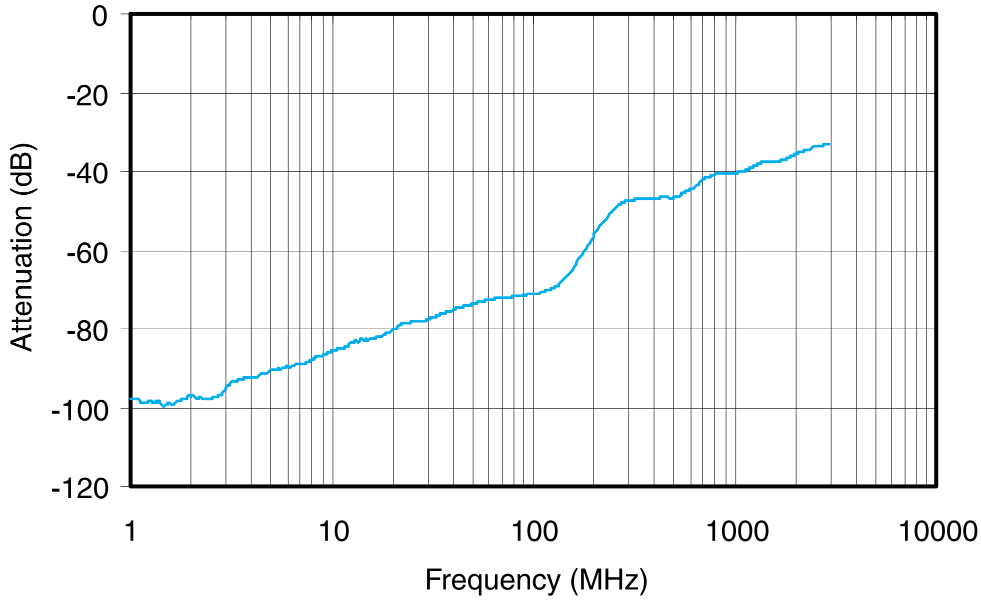


Figure 3. Crosstalk vs Frequency

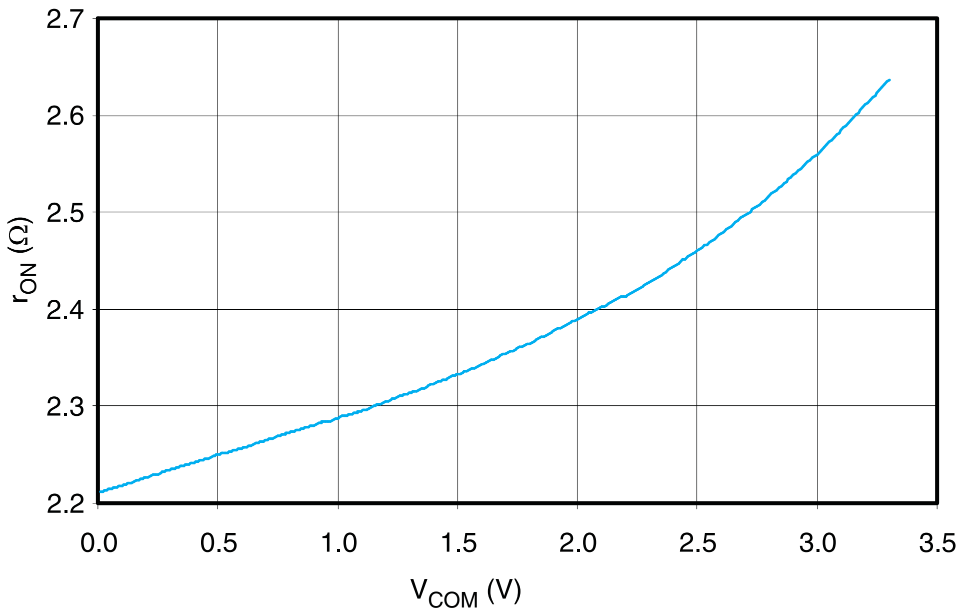
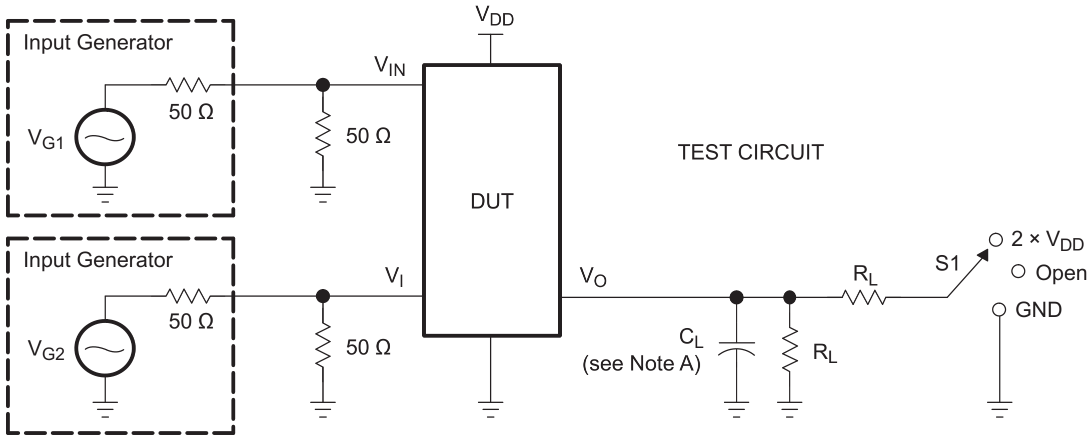
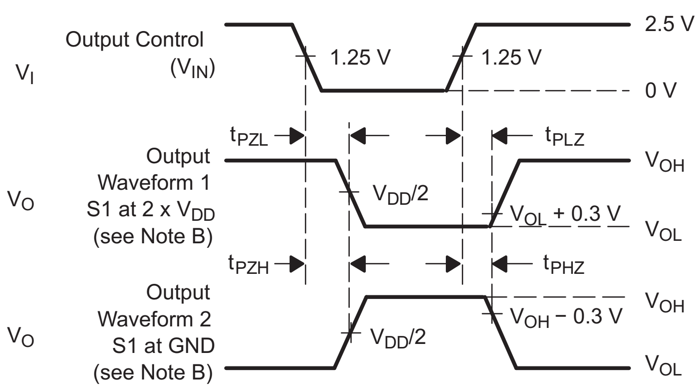


Figure 4. . r_{ON}(Ω) vs V_{COM}(V)

PARAMETER MEASUREMENT INFORMATION



TEST	V_{DD}	S1	R_L	V_{in}	C_L	V_Δ
t_{PLZ}/t_{PZL}	3.3 V	2 × V_{DD}	200 Ω	GND	10 pF	0.3 V
t_{PHZ}/t_{PZH}	3.3 V	GND	200 Ω	V_{DD}	10 pF	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 5. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

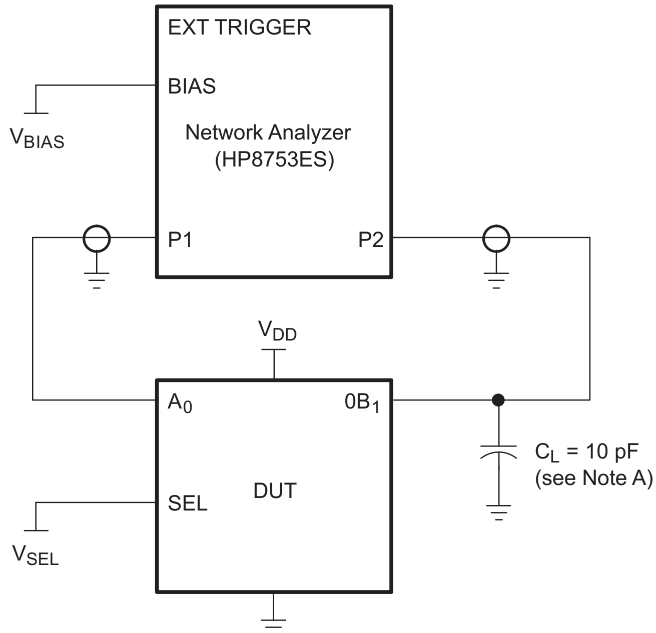


Figure 6. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when V_{SEL} = 0 and A_0 is the input, the output is measured at $0B1_1$. All unused analog I/O ports are left open.

HP8753ES Setup

Average = 4

RBW = 3 kHz

V_{BIAS} = 0.35 V

ST = 2 s

P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION (continued)

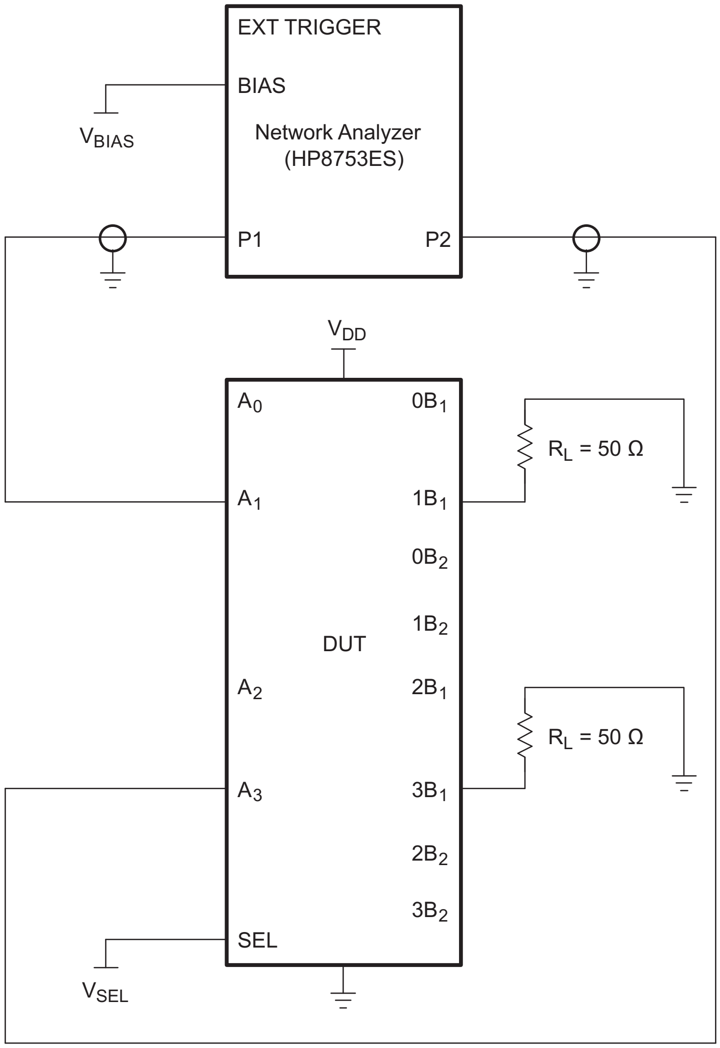


Figure 7. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when V_{IN} = 0, V_{EN} = 0, and D_A is the input, the output is measured at $S1_B$. All unused analog input (D) ports and output (S) ports are connected to GND through 10-Ω and 50-Ω pulldown resistors, respectively.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION (continued)

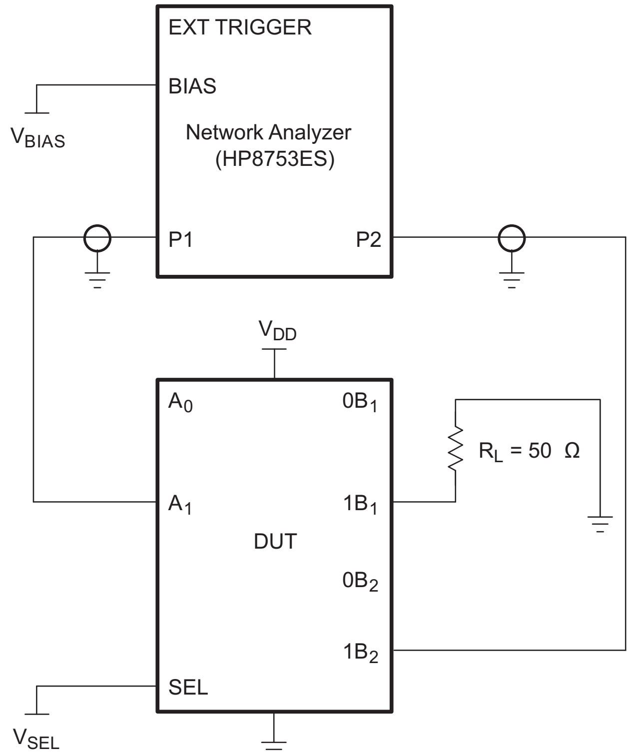


Figure 8. Test Circuit for Off Isolation (O_{IRR})

Off isolation is measured at the output of the OFF channel. For example, when $V_{IN} = V_{CC}$, $V_{EN} = 0$, and D_A is the input, the output is measured at $S1_A$. All unused analog input (D) ports are left open, and output (S) ports are connected to GND through 50-Ω pulldown resistors.

HP8753ES Setup

Average = 4

RBW = 3 kHz

V_{BIAS} = 0.35 V

ST = 2 s

P1 = 0 dBM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TS3V712ERTGR	ACTIVE	WQFN	RTG	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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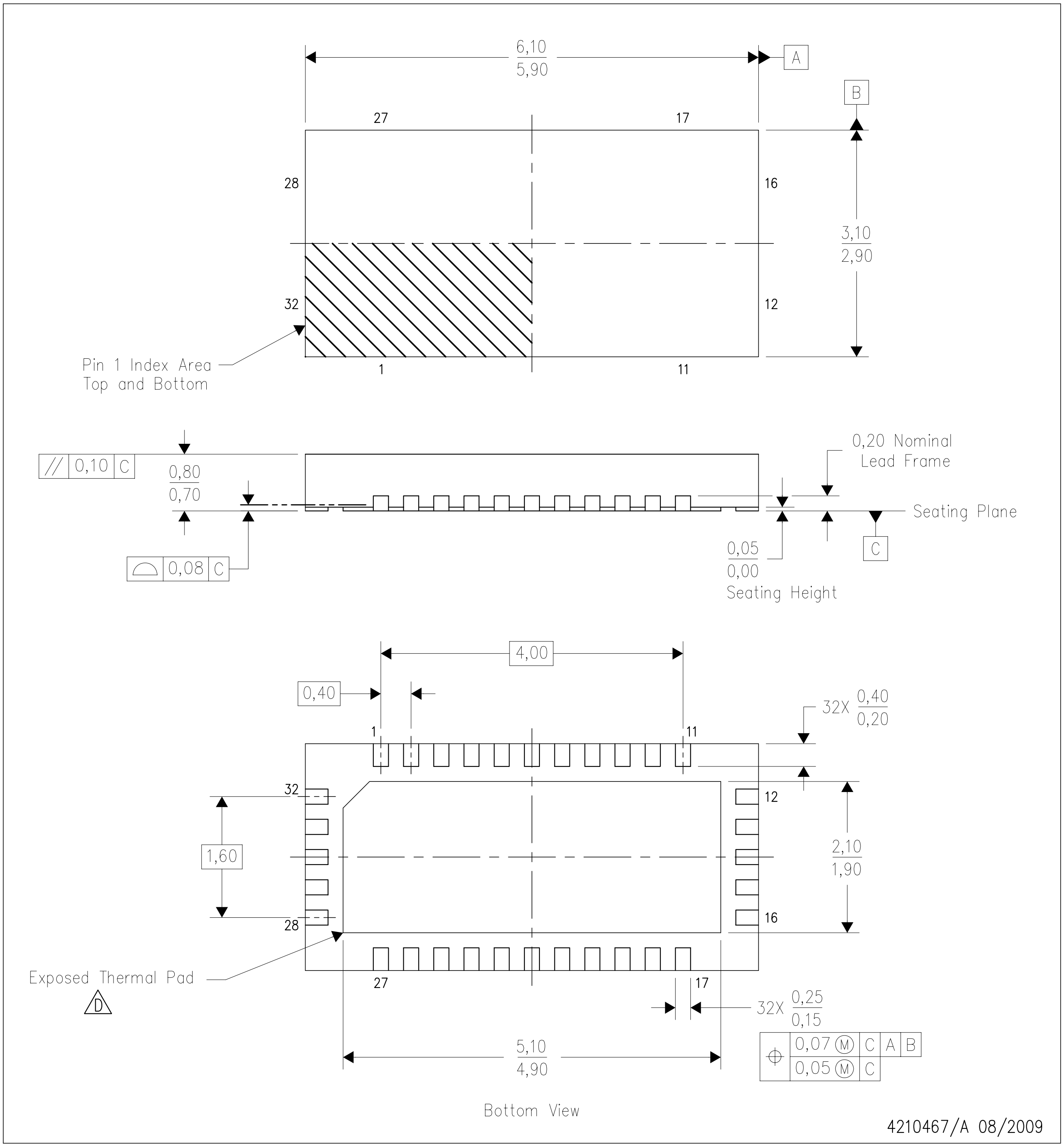
RTG (R–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



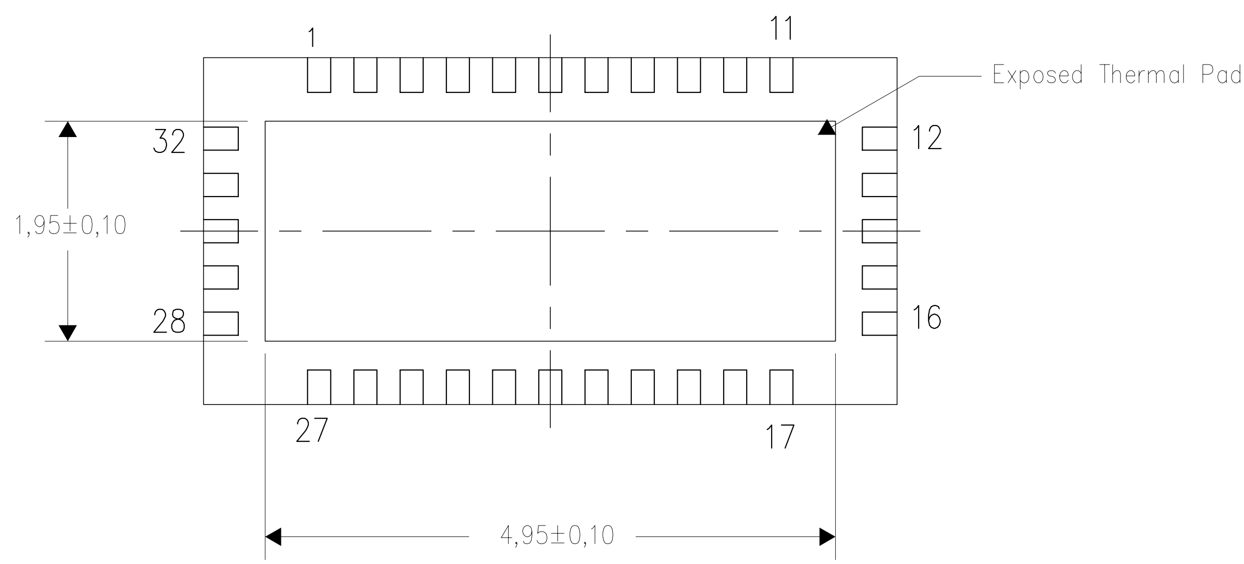
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. Reference JEDEC MO–220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

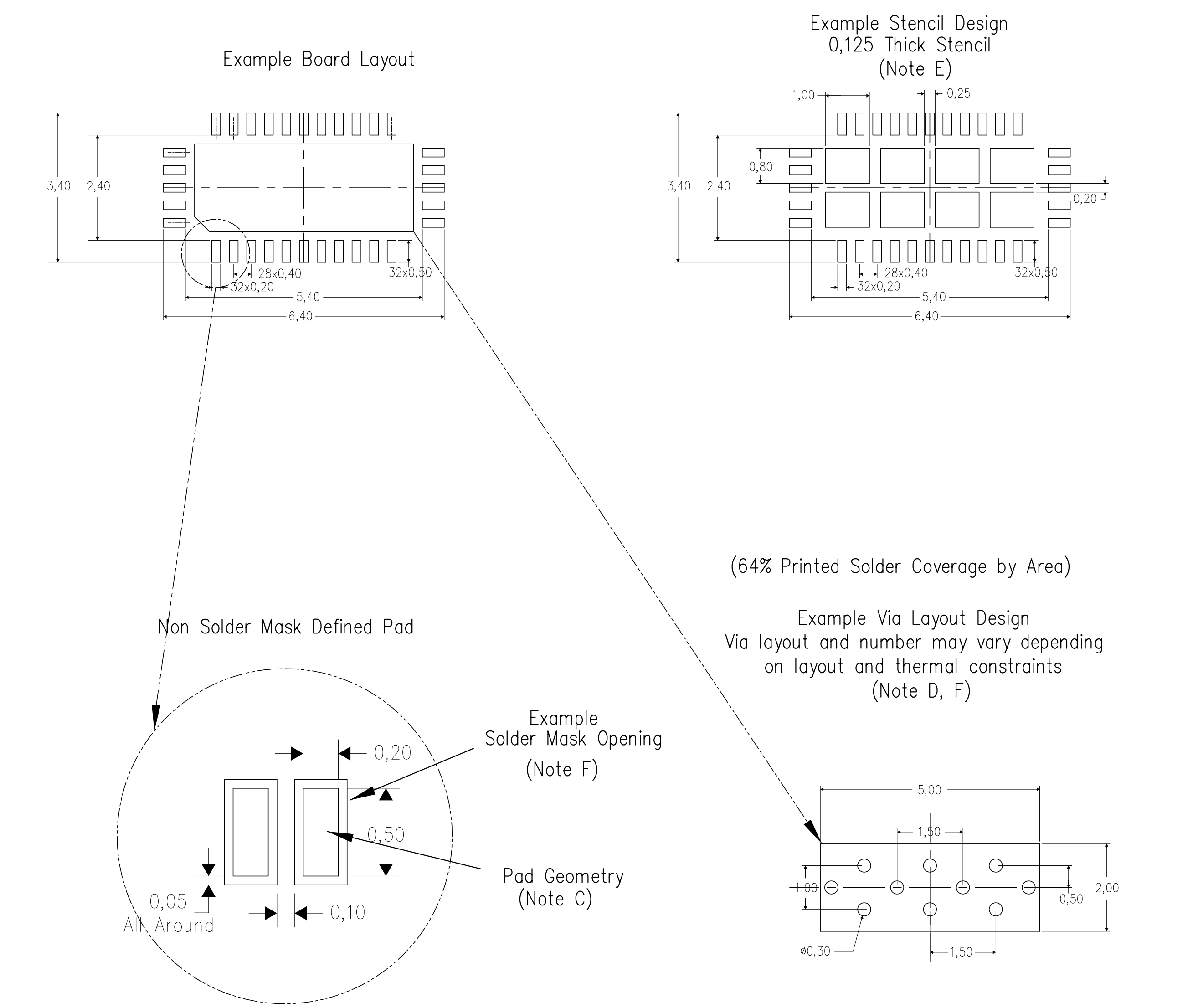


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RTG (R–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

IMPORTANT NOTICE