



## Ultra-small 28.5 mΩ, 1.0 A Integrated Power Switch with Discharge

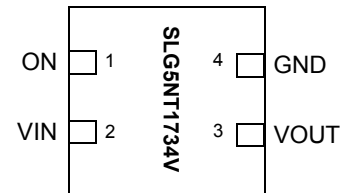
### General Description

The SLG5NT1734V is designed for load switching applications with ultra low quiescent current. The part comes with one 28.5 mΩ 1.0 A rated P-channel MOSFET controlled by a single ON control pin. The product is packaged in an ultra-small 1.0 x 1.0 mm package.

### Features

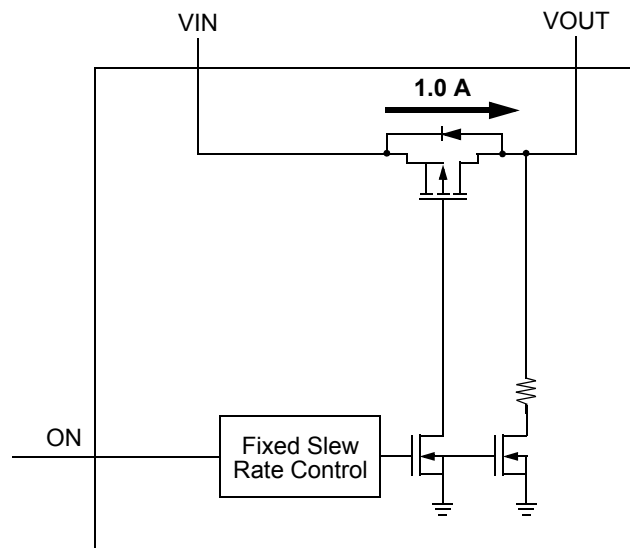
- One 1.0 A MOSFET
- Ultra Low Quiescent Current
- Low  $R_{DS(ON)}$ 
  - 28.5 mΩ @ 5.0 V
  - 36.4 mΩ @ 3.3 V
  - 44.3 mΩ @ 2.5 V
  - 60.8 mΩ @ 1.8 V
  - 77.6 mΩ @ 1.5 V
- $V_{IN} = 1.5 V$  to 5.0 V
- Integrated Discharge Resistor
- Pb-Free / Halogen-Free / RoHS compliant
- STDFN 4L, 1.0 x 1.0 x 0.55 mm

### Pin Configuration



**4-pin STDFN**  
(Top View)

### Block Diagram





### Pin Description

Pin #	Pin Name	Type	Pin Description
1	ON	Input	Turns on MOSFET, active high
2	VIN	MOSFET	Power MOSFET input
3	VOUT	MOSFET	Power MOSFET output
4	GND	GND	Ground

### Ordering Information

Part Number	Type	Production Flow
SLG5NT1734V	STDFN 4L	Industrial, -40 °C to 85 °C
SLG5NT1734VTR	STDFN 4L (Tape and Reel)	Industrial, -40 °C to 85 °C



## Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{IN}$	Power Switch Input Voltage		--	--	6	V
$T_S$	Storage Temperature		-65	--	140	°C
ESD <sub>HBM</sub>	ESD Protection	Human Body Model	2000	--	--	V
ESD <sub>CDM</sub>	ESD Protection	Charged Device Model	1000	--	--	V
MSL	Moisture Sensitivity Level		1			
$\theta_{JA}$	Package Thermal Resistance, Junction-to-Ambient	1 mm x 1 mm STDFN; Determined using 1 in <sup>2</sup> , 1.2 oz. copper pads under VIN and VOUT on FR4 pcb material	--	122	--	°C/W
$W_{DIS}$	Package Power Dissipation		--	--	0.5	W
MOSFET $I_{DS_{PK}}$	Peak Current from Drain to Source	For no more than 1 ms with 1% duty cycle	--	--	1.5	A

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Electrical Characteristics

$T_A = -40\text{ °C to }85\text{ °C}$  (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{IN}$	Power Switch Input Voltage	-40 °C to 85 °C	1.5	--	5.0	V
$I_{IN}$	Power Switch Current (PIN 2)	when OFF, $V_{IN} = 5.0\text{ V}$	--	0.03	1	μA
		when ON = $V_{IN}$ , No load	--	0.05	0.5	μA
$I_{ON\_LKG}$	ON Pin Input Leakage		--	--	0.1	μA
$R_{DS_{ON}}$	ON Resistance @ $T_A\ 25\text{ °C}$	@ 5.0 V, 100 mA	--	28.5	37	mΩ
		@ 3.3 V, 100 mA	--	36.4	45	mΩ
		@ 2.5 V, 100 mA	--	44.3	54	mΩ
		@ 1.8 V, 100 mA	--	60.8	73.5	mΩ
		@ 1.5 V, 100 mA	--	77.6	93.2	mΩ
$R_{DS_{ON}}$	ON Resistance @ $T_A\ 85\text{ °C}$	@ 5.0 V, 100 mA	--	34	43.6	mΩ
		@ 3.3 V, 100 mA	--	43.8	53.6	mΩ
		@ 2.5 V, 100 mA	--	53.3	64.3	mΩ
		@ 1.8 V, 100 mA	--	72.2	86	mΩ
		@ 1.5 V, 100 mA	--	90.7	107.2	mΩ
MOSFET $I_{DS}$	Current from VIN to VOUT	Continuous	--	--	1.0	A
$T_{ON\_Delay}$	ON pin Delay Time	50% ON to Ramp Begin $V_{IN} = 5.0\text{ V}$ , $C_{LOAD} = 0.1\ \mu\text{F}$ , $R_{LOAD} = 10\ \Omega$	0.4	1.1	2.2	ms
		50% ON to Ramp Begin $V_{IN} = 3.3\text{ V}$ , $C_{LOAD} = 0.1\ \mu\text{F}$ , $R_{LOAD} = 10\ \Omega$	0.56	1.3	2.6	ms
		50% ON to Ramp Begin $V_{IN} = 1.5\text{ V}$ , $C_{LOAD} = 0.1\ \mu\text{F}$ , $R_{LOAD} = 10\ \Omega$	0.73	1.8	3.35	ms



### Electrical Characteristics (continued)

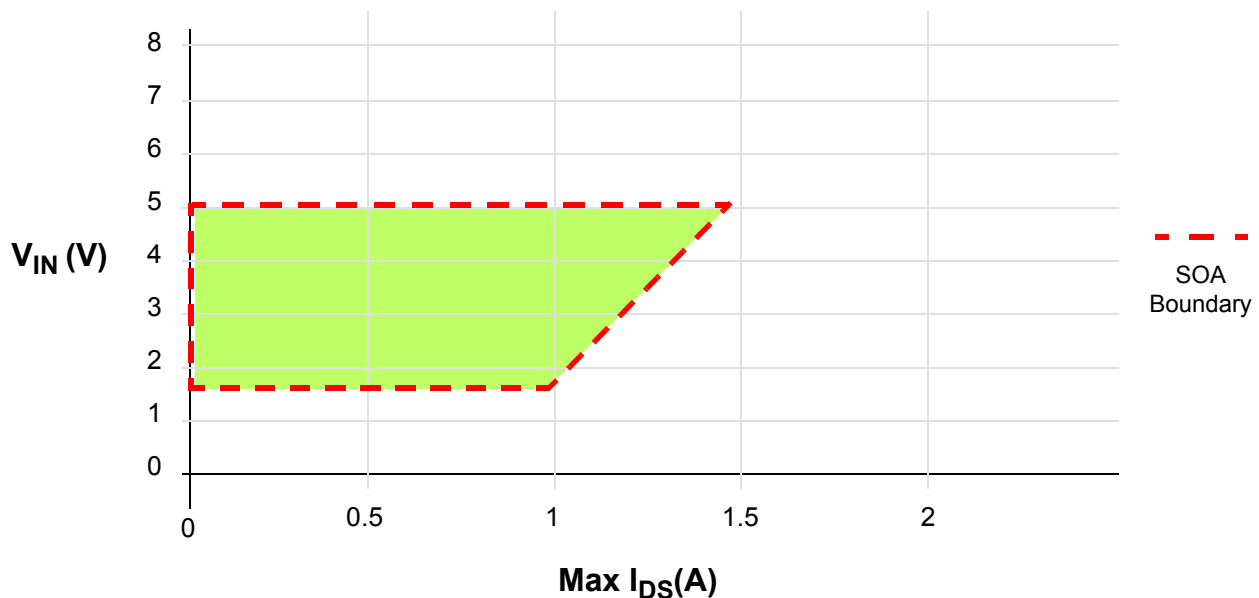
T<sub>A</sub> = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
T <sub>Total_ON</sub>	Total Turn On Time	50% ON to 90% V <sub>OUT</sub> V <sub>IN</sub> = 5.0 V, C <sub>LOAD</sub> = 0.1 μF, R <sub>LOAD</sub> = 10 Ω	2.12	3.7	6.18	ms
		50% ON to 90% V <sub>OUT</sub> V <sub>IN</sub> = 3.3 V, C <sub>LOAD</sub> = 0.1 μF, R <sub>LOAD</sub> = 10 Ω	2.04	3.6	6.18	ms
		50% ON to 90% V <sub>OUT</sub> V <sub>IN</sub> = 1.5 V, C <sub>LOAD</sub> = 0.1 μF, R <sub>LOAD</sub> = 10 Ω	1.97	3.2	5.61	ms
T <sub>RISE</sub>	Rise Time	10% V <sub>OUT</sub> to 90% V <sub>OUT</sub> V <sub>IN</sub> = 5.0 V, C <sub>LOAD</sub> = 0.1 μF, R <sub>LOAD</sub> = 10 Ω	1.40	2.30	3.63	ms
		10% V <sub>OUT</sub> to 90% V <sub>OUT</sub> V <sub>IN</sub> = 3.3 V, C <sub>LOAD</sub> = 0.1 μF, R <sub>LOAD</sub> = 10 Ω	1.1	1.91	3.1	ms
		10% V <sub>OUT</sub> to 90% V <sub>OUT</sub> V <sub>IN</sub> = 1.5 V, C <sub>LOAD</sub> = 0.1 μF, R <sub>LOAD</sub> = 10 Ω	0.79	1.30	2.2	ms
R <sub>DIS</sub>	Discharge Resistance	V <sub>IN</sub> = 1.5 V to 5.0 V, V <sub>OUT</sub> = 0.4 V Input Bias	46	96	250	Ω
ON_V <sub>IH</sub>	Initial Turn On Voltage		0.85	--	V <sub>IN</sub>	V
ON_V <sub>IL</sub>	Low Input Voltage on ON pin		-0.3	0	0.3	V
T <sub>OFF_Delay</sub>	OFF Delay Time	50% ON to V <sub>OUT</sub> Fall Start, V <sub>IN</sub> = 5.0 V, R <sub>LOAD</sub> = 10 Ω, no C <sub>LOAD</sub>	4.56	5.9	7.44	μs

Notes:

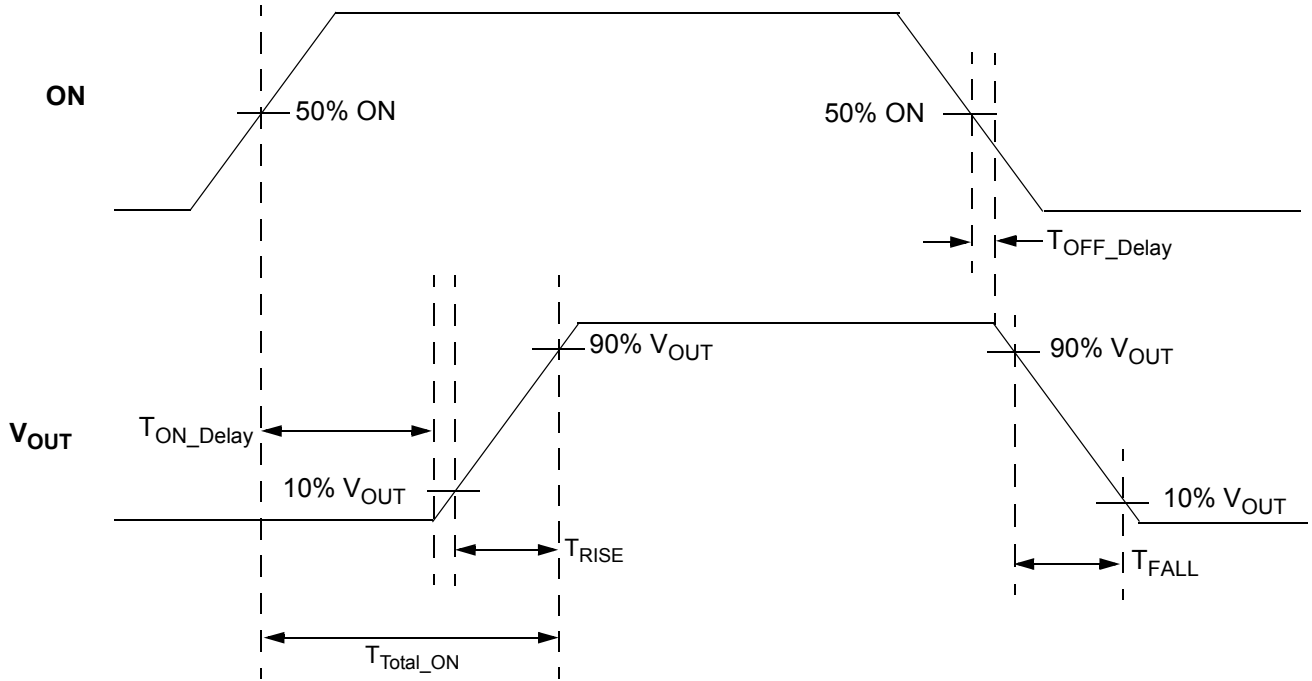
- V<sub>IN</sub> ≥ 2 V, linear and monotonic power on ramp. (Figure 11)
- V<sub>IN</sub> < 2 V with 2 Ω load, non-linear and monotonic power on ramp. (Figure 10, V<sub>IN</sub> = 1.5 V, C<sub>LOAD</sub> = 0.1 μF, R<sub>LOAD</sub> = 1.5 Ω)

### V<sub>IN</sub> vs. Max I<sub>DS</sub>, Safe Operation Area





$T_{Total\_ON}$ ,  $T_{ON\_Delay}$  and Slew Rate Measurement



Note: Rise and Fall times of the ON signal are 100 ns



### Typical Turn-on Waveforms

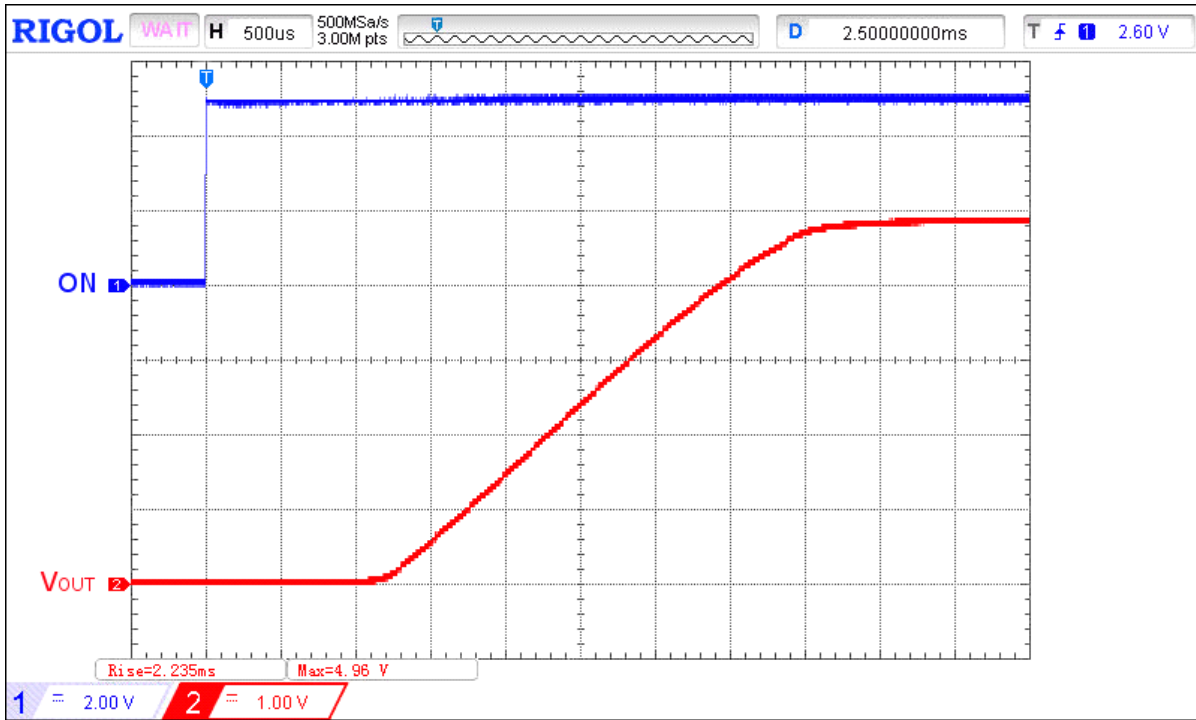


Figure 1. Typical Turn ON operation waveform for  $V_{IN} = 5\text{ V}$ ,  $C_{LOAD} = 0.1\ \mu\text{F}$ ,  $R_{LOAD} = 10\ \Omega$

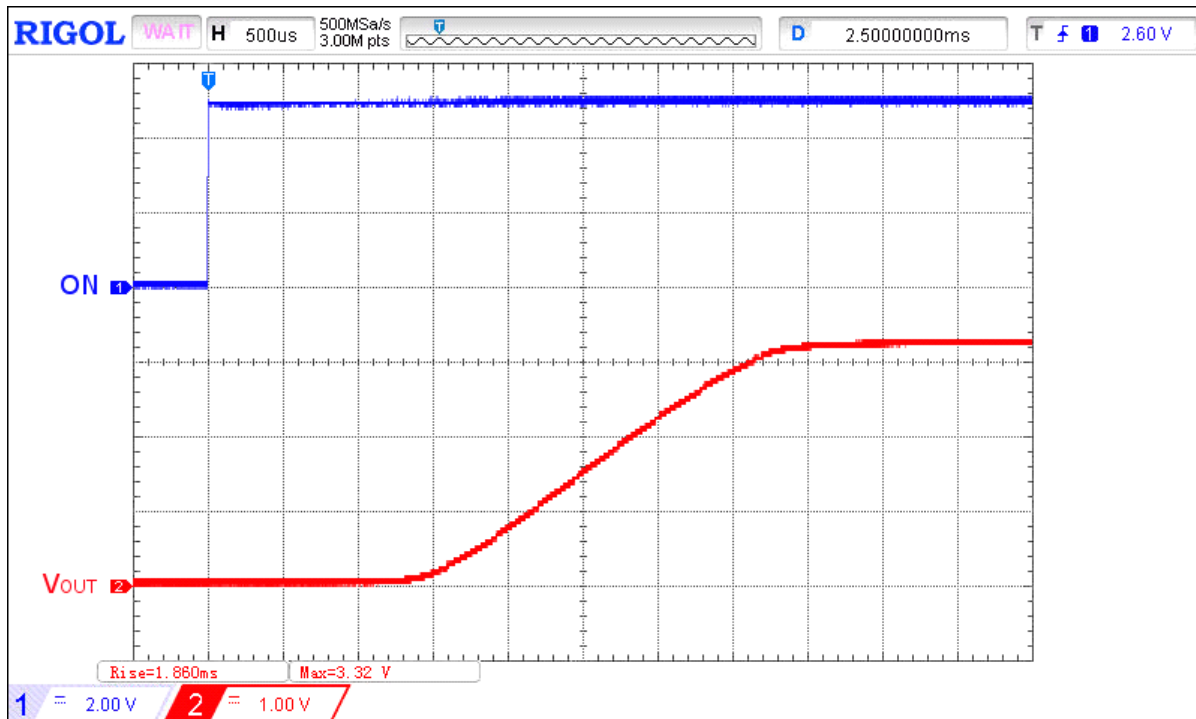


Figure 2. Typical Turn ON operation waveform for  $V_{IN} = 3.3\text{ V}$ ,  $C_{LOAD} = 0.1\ \mu\text{F}$ ,  $R_{LOAD} = 10\ \Omega$

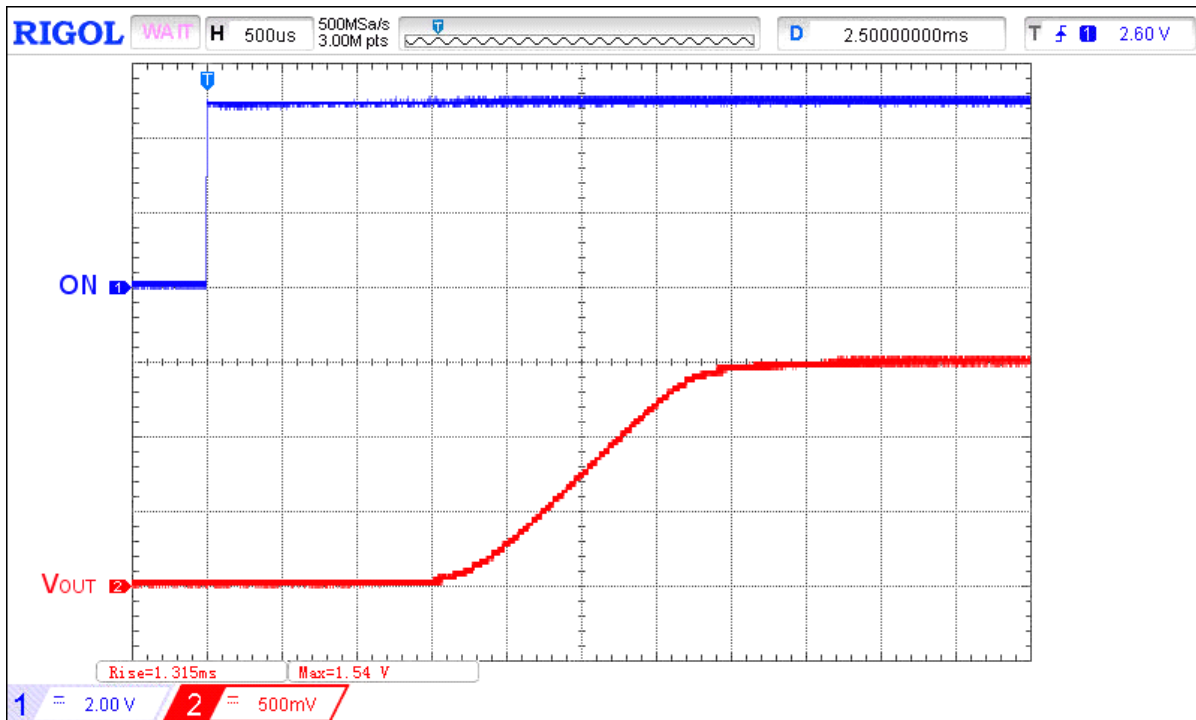


Figure 3. Typical Turn ON operation waveform for  $V_{IN} = 1.5\text{ V}$ ,  $C_{LOAD} = 0.1\ \mu\text{F}$ ,  $R_{LOAD} = 10\ \Omega$



### Typical Turn-off Waveforms

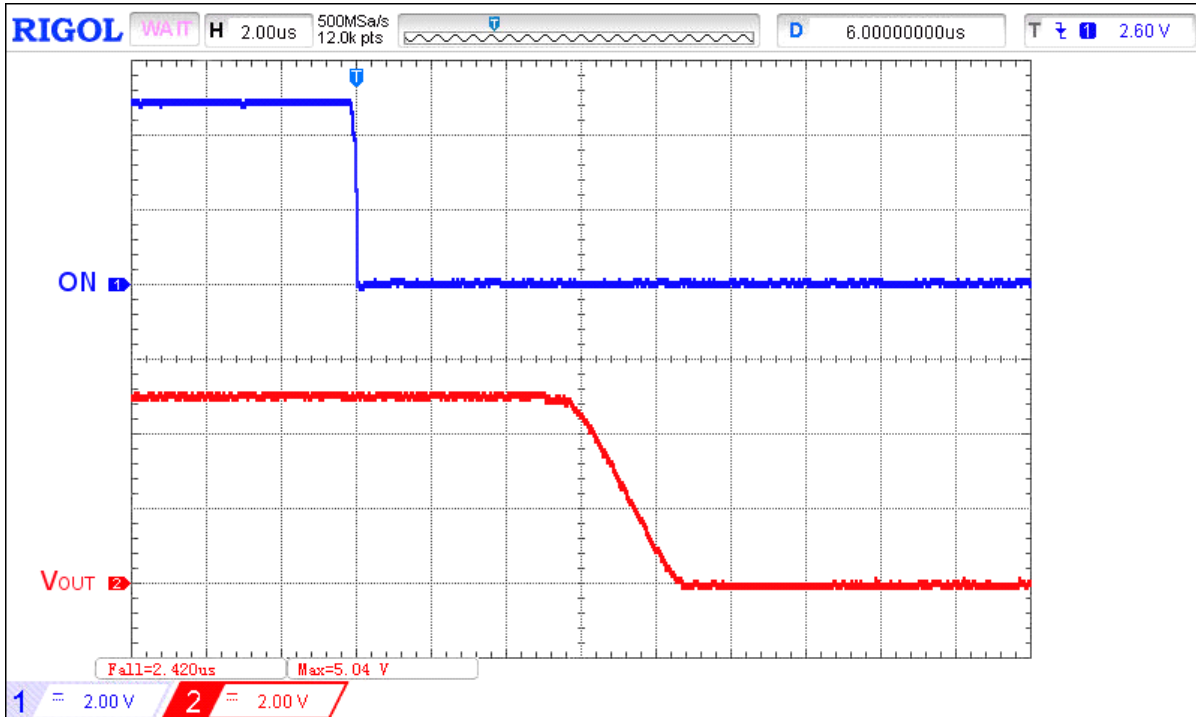


Figure 4. Typical Turn OFF operation waveform for  $V_{IN} = 5\text{ V}$ , no  $C_{LOAD}$ ,  $R_{LOAD} = 10\ \Omega$

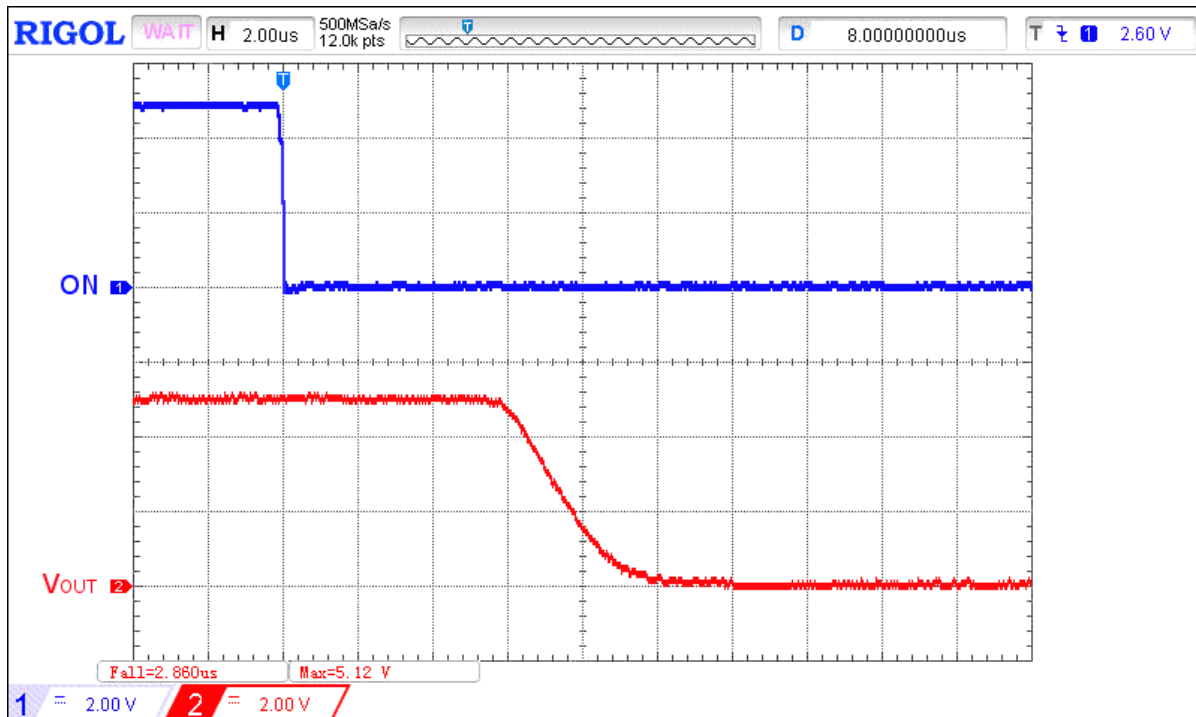


Figure 5. Typical Turn OFF operation waveform for  $V_{IN} = 5\text{ V}$ ,  $C_{LOAD} = 0.1\ \mu\text{F}$ ,  $R_{LOAD} = 10\ \Omega$



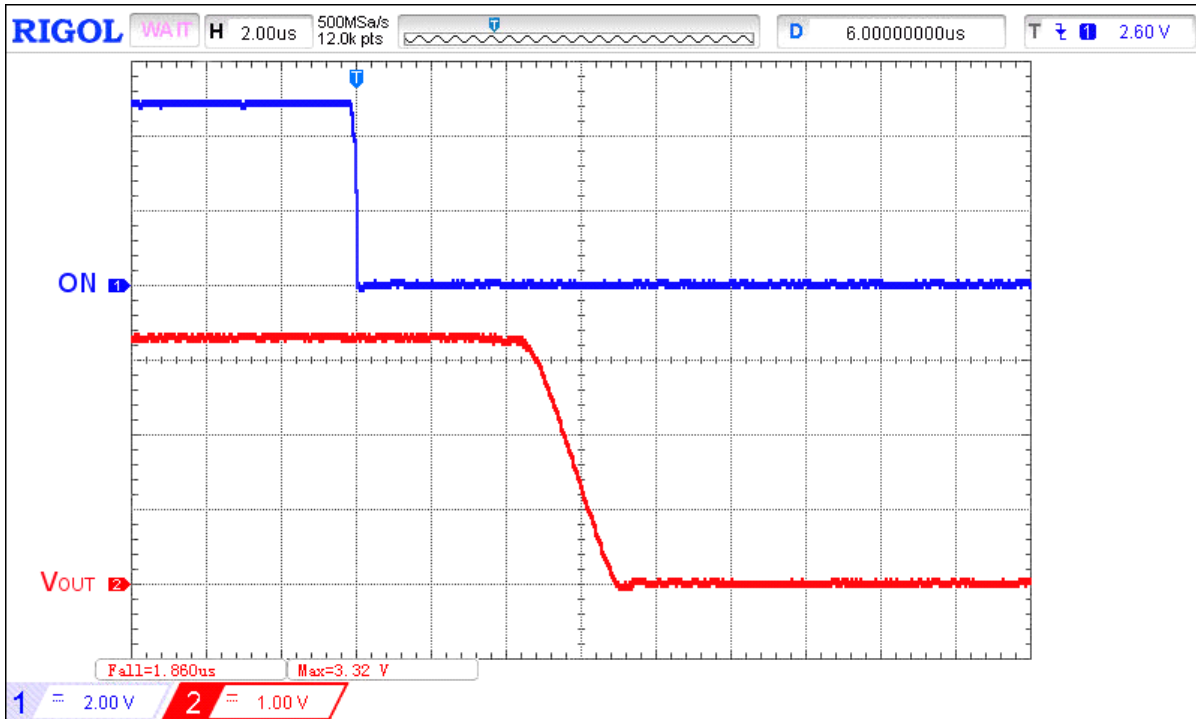


Figure 6. Typical Turn OFF operation waveform for  $V_{IN} = 3.3\text{ V}$ , no  $C_{LOAD}$ ,  $R_{LOAD} = 10\ \Omega$

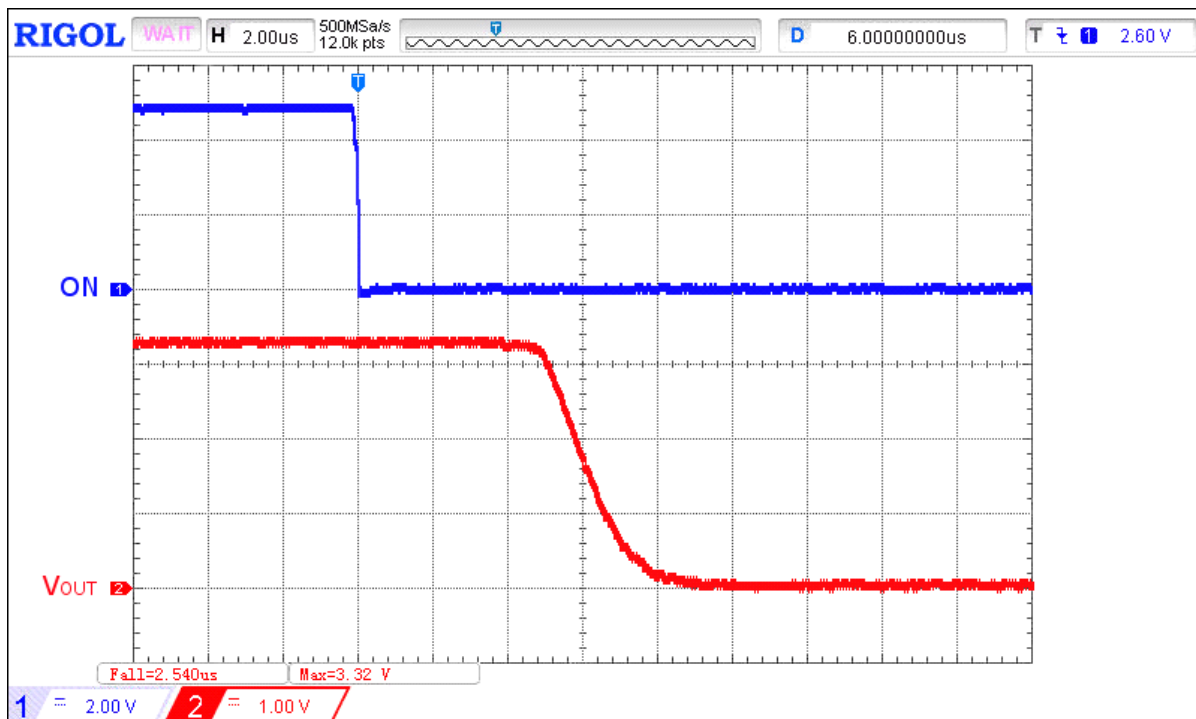


Figure 7. Typical Turn OFF operation waveform for  $V_{IN} = 3.3\text{ V}$ ,  $C_{LOAD} = 0.1\ \mu\text{F}$ ,  $R_{LOAD} = 10\ \Omega$

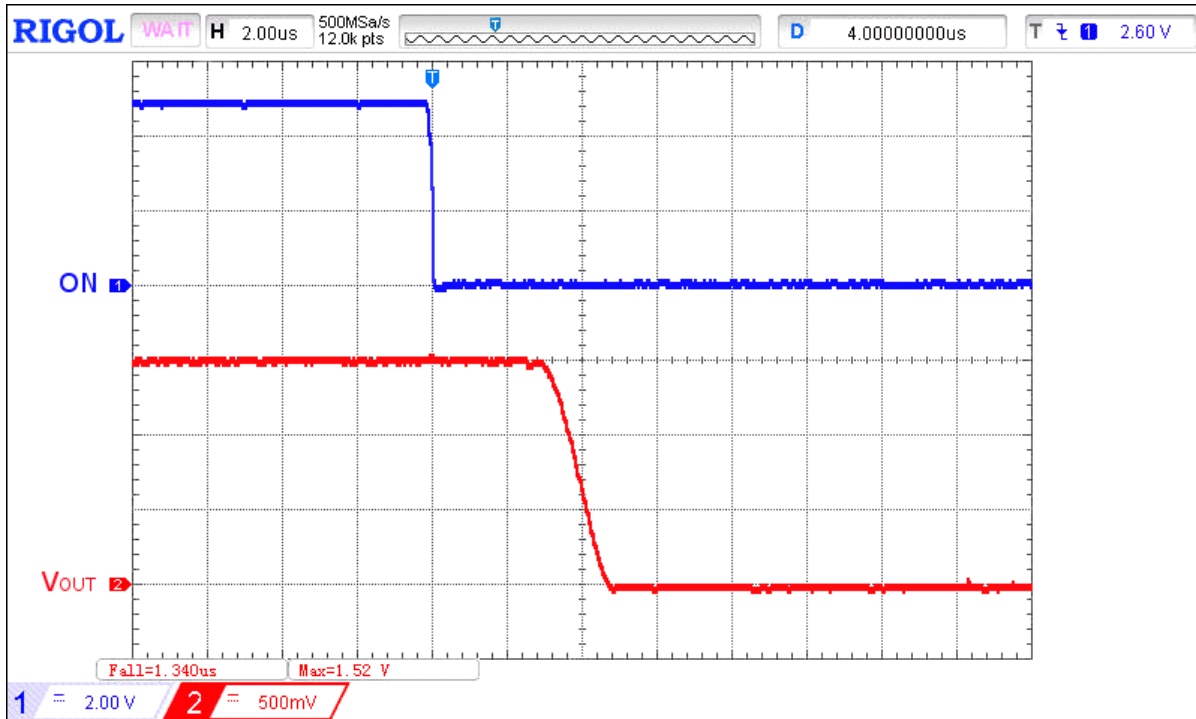


Figure 8. Typical Turn OFF operation waveform for  $V_{IN} = 1.5\text{ V}$ , no  $C_{LOAD}$ ,  $R_{LOAD} = 10\ \Omega$

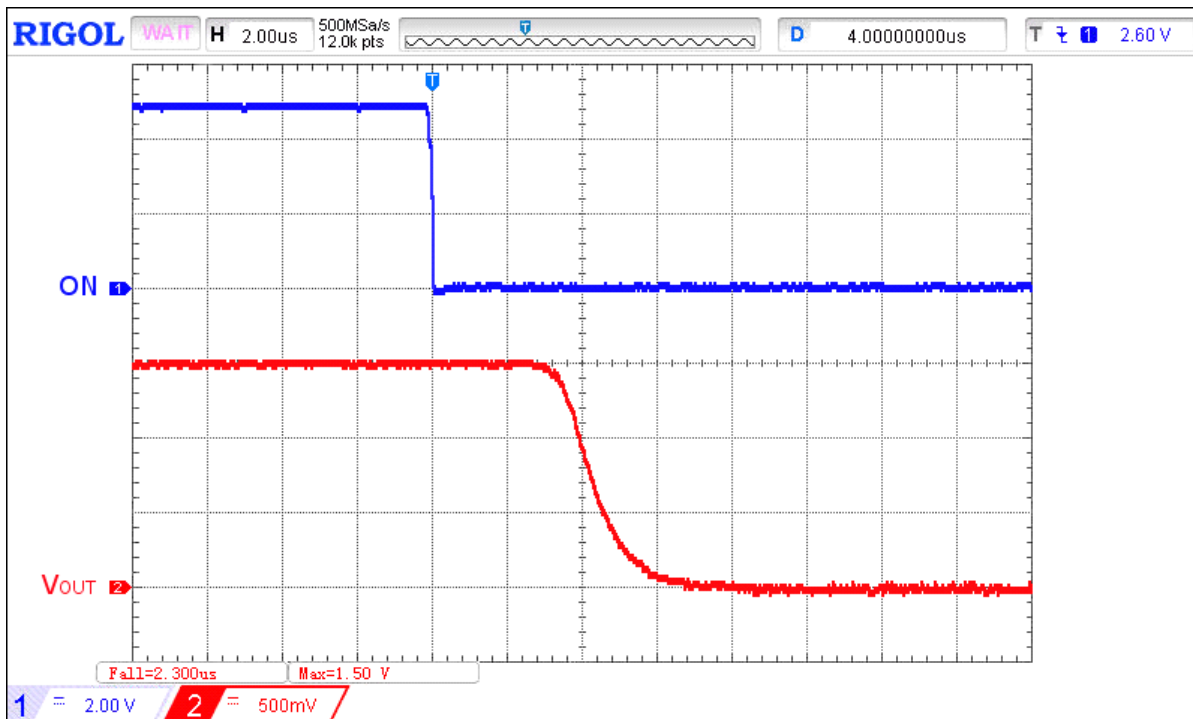


Figure 9. Typical Turn OFF operation waveform for  $V_{IN} = 1.5\text{ V}$ ,  $C_{LOAD} = 0.1\ \mu\text{F}$ ,  $R_{LOAD} = 10\ \Omega$



### Monotonic Turn-on Waveforms

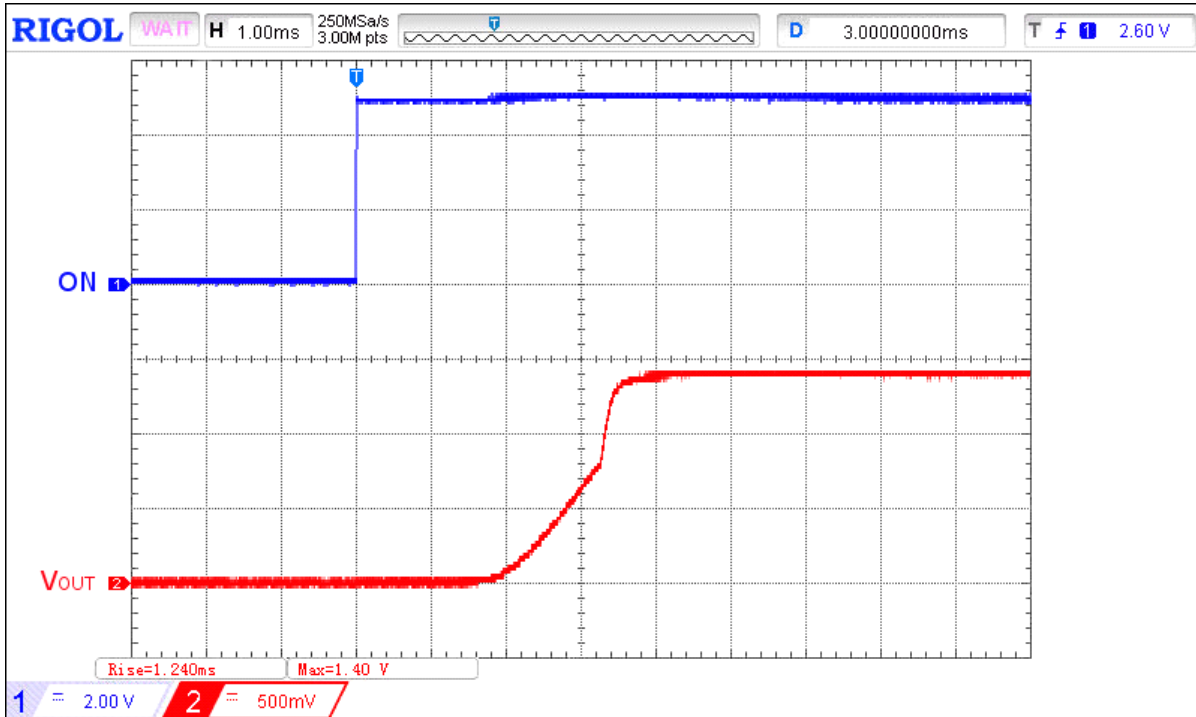


Figure 10. Non-linear and monotonic turn ON operation waveform for  $V_{IN} = 1.5\text{ V}$ ,  $C_{LOAD} = 0.1\ \mu\text{F}$ ,  $R_{LOAD} = 1.5\ \Omega$

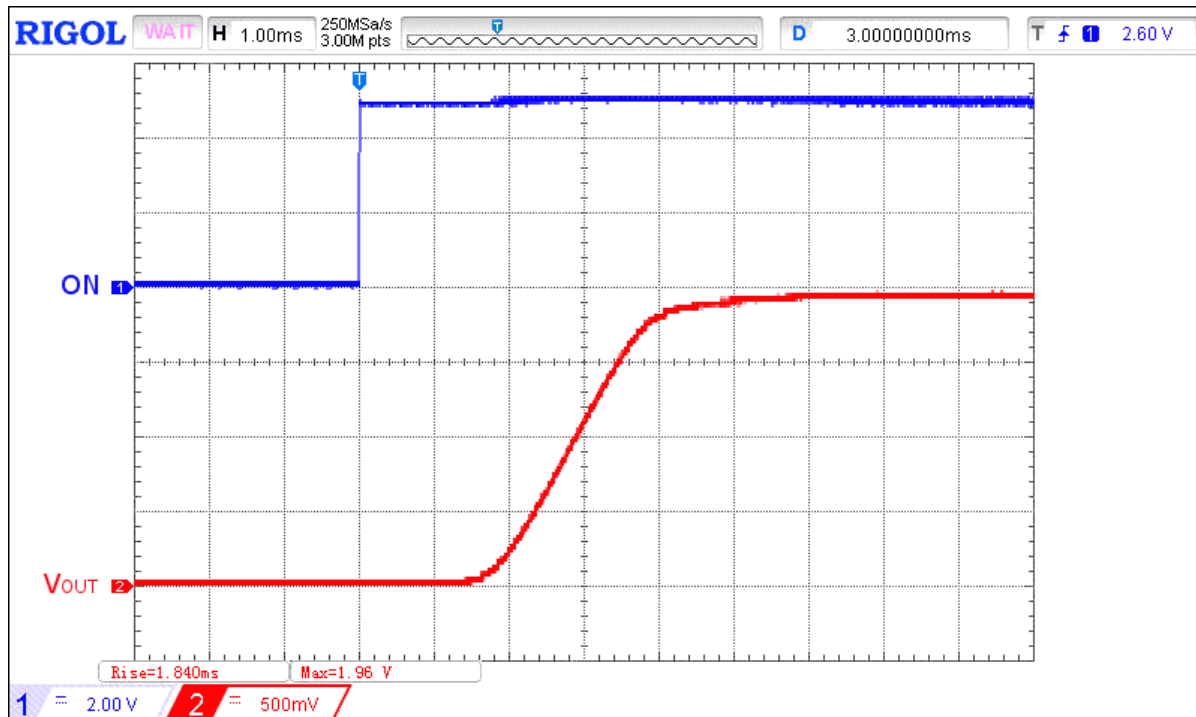


Figure 11. Linear and monotonic turn ON operation waveform for  $V_{IN} = 2\text{ V}$ ,  $C_{LOAD} = 0.1\ \mu\text{F}$ ,  $R_{LOAD} = 2\ \Omega$

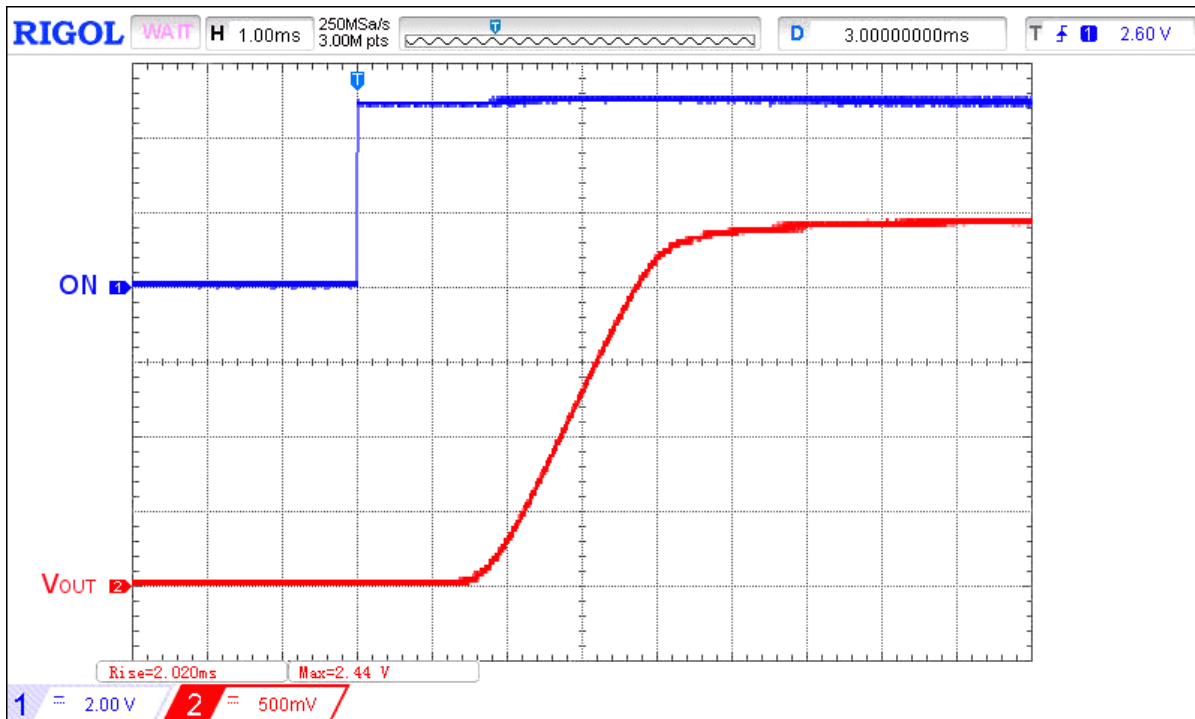


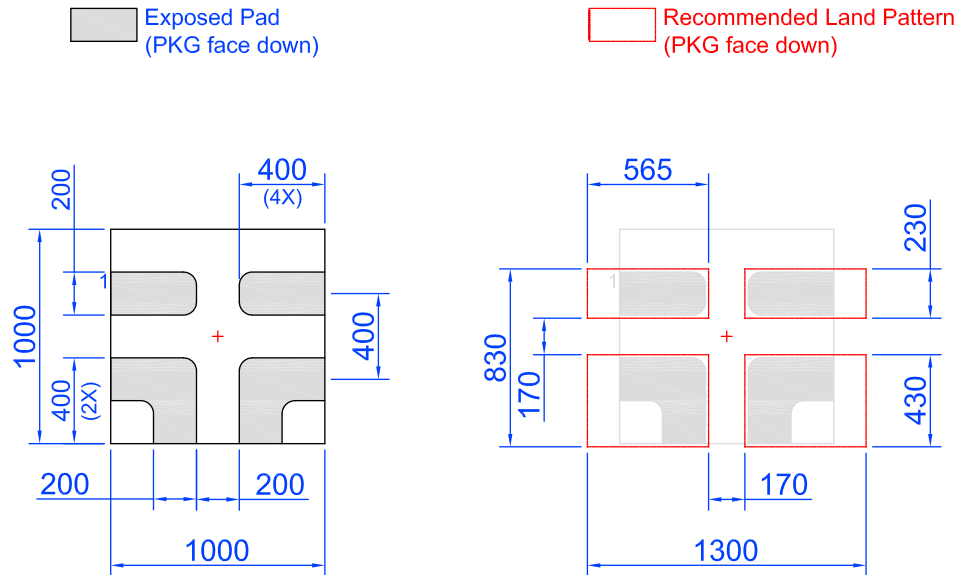
Figure 12. Typical Turn ON operation waveform for  $V_{IN} = 2.5\text{ V}$ ,  $C_{LOAD} = 0.1\ \mu\text{F}$ ,  $R_{LOAD} = 2.2\ \Omega$



### SLG5NT1734V Power-Up/Power-Down Sequence Considerations

A nominal power-up sequence is to apply  $V_{IN}$  and toggle the ON pin LOW-to-HIGH after  $V_{IN}$  is at least 90% of its final value. A nominal power-down sequence is the power-up sequence in reverse order. If  $V_{IN}$  ramp is too fast, a voltage glitch may appear on the output pin at VOUT. To prevent glitches at the output, it is recommended to connect at least 0.1 $\mu$ F capacitor from the VOUT pin to GND or to keep the  $V_{IN}$  ramp time more than 2 ms.

### SLG5NT1734V Layout Suggestion

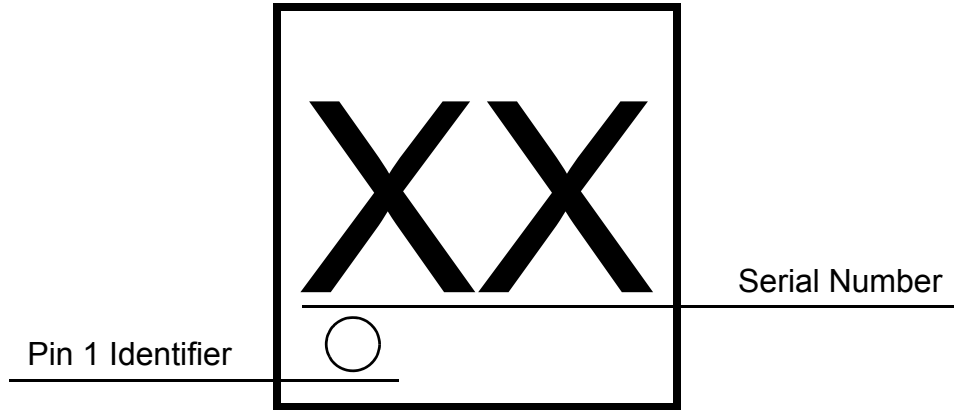


Note: All dimensions shown in micrometers ( $\mu$ m)



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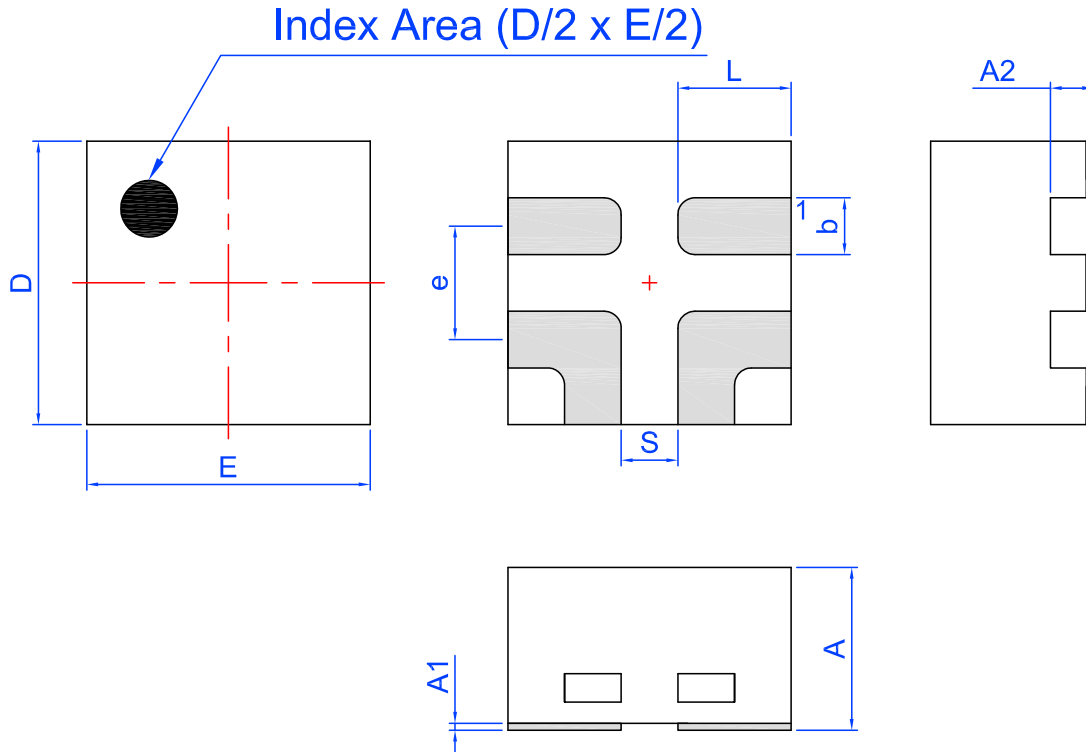
Package Top Marking System Definition





### Package Drawing and Dimensions

4 Lead STDFN Package 1.0 x 1.0 mm



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	0.95	1.00	1.05
A1	0.005	-	0.060	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.15	0.20	0.25	S	0.2 REF		
e	0.40 BSC						

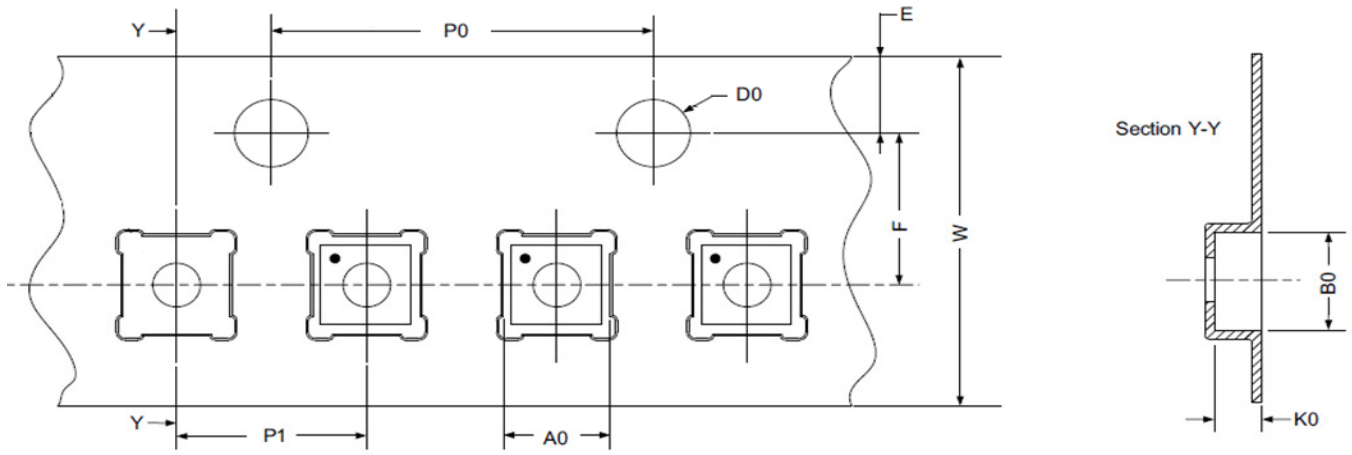


**Tape and Reel Specifications**

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STDFN 4L 1x1mm 0.4P FC Green	4	1.0 x 1.0 x 0.55	8000	8000	178 / 60	200	400	200	400	8	2

**Carrier Tape Drawing and Dimensions**

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STDFN 4L 1x1mm 0.4P FC Green	1.16	1.16	0.63	4	2	1.5	1.75	3.5	8



Refer to EIA-481 specification

**Recommended Reflow Soldering Profile**

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.55 mm<sup>3</sup> (nominal). More information can be found at [www.jedec.org](http://www.jedec.org).





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**Revision History**

Date	Version	Change
8/7/2017	1.00	Production Release