

ISL97687

4-Channel LED Driver with Phase Shift Control and 10-Bit Dimming Resolution

FN7714  
Rev.3.00  
Sep 13, 2017

The [ISL97687](#) is a PWM controlled LED driver that supports 4 channels of LED current, for Monitor and TV LCD backlight applications. It is capable of driving 160mA per channel from a 9V to 32V input supply, with current sources rated up to 75V absolute maximum.

The ISL97687's current sources achieve typical current matching to  $\pm 1\%$ , while dynamically maintaining the minimum required  $V_{OUT}$  necessary for regulation. This adaptive scheme compensates for the non-uniformity of forward voltage variance in the LED strings.

The ISL97687 can decode both an incoming PWM signal and an analog input voltage, for DC-to-PWM dimming applications. Modes include direct PWM and several modes where the PWM frequency is synthesized on chip at 10-bit resolution. This can be either free running, or synchronized with the frame rate to give both a frequency and a phase lock, minimizing panel to panel variation and display flicker. Phase shift is supported, reducing flicker and audio noise, as is multiplication of the incoming decoded analog and PWM values.

The ISL97687 has an advanced dynamic headroom control function, which monitors the highest LED forward voltage string, and regulates the output to the correct level to minimize power loss. This proprietary regulation scheme also allows for extremely linear PWM dimming from 0.02% to 100%. The LED current can also be switched between two current levels, giving support for 3D applications. The ISL97687 incorporates extensive protections of string open and short circuit detections, OVP, and OTP.

Features

- 4x160mA, 75V rated channels with integrated channel regulation FETs
- Channels can be ganged for high current
  - 2x350mA
  - 1x700mA
- 9V~32V input voltage
- Dimming modes:
  - Direct PWM dimming from 100Hz~30kHz
  - PWM dimming with adjustable output frequency
    - 10-bit dimming resolution
    - $V_{SYNC}$  function to synchronize PWM signal to frame rate
    - Phase shift
  - Analog to PWM dimming with 8-bit resolution
- 2 selectable current levels for 3D applications
- Current matching of  $\pm 1\%$
- Integrated fault protection features such as string open circuit protection, string short circuit protection, overvoltage protection, and over-temperature protection
- 28 Ld 5mmx5mm TQFN and 28 Ld 300mil SOIC Packages Available

Applications

- Monitor/TV LED Backlighting
- General/Industrial/Automotive Lighting

Related Literature

- For a full list of related documents, visit our website
- [ISL97687](#) product page

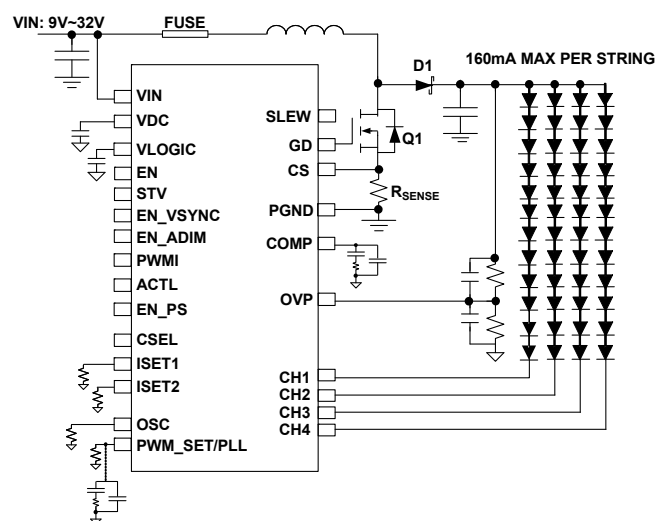


FIGURE 1. ISL97687 APPLICATION DIAGRAM

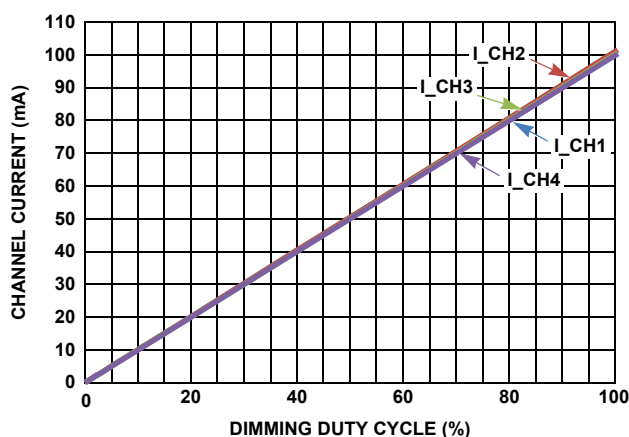


FIGURE 2. PWM DIMMING LINEARITY

Block Diagram

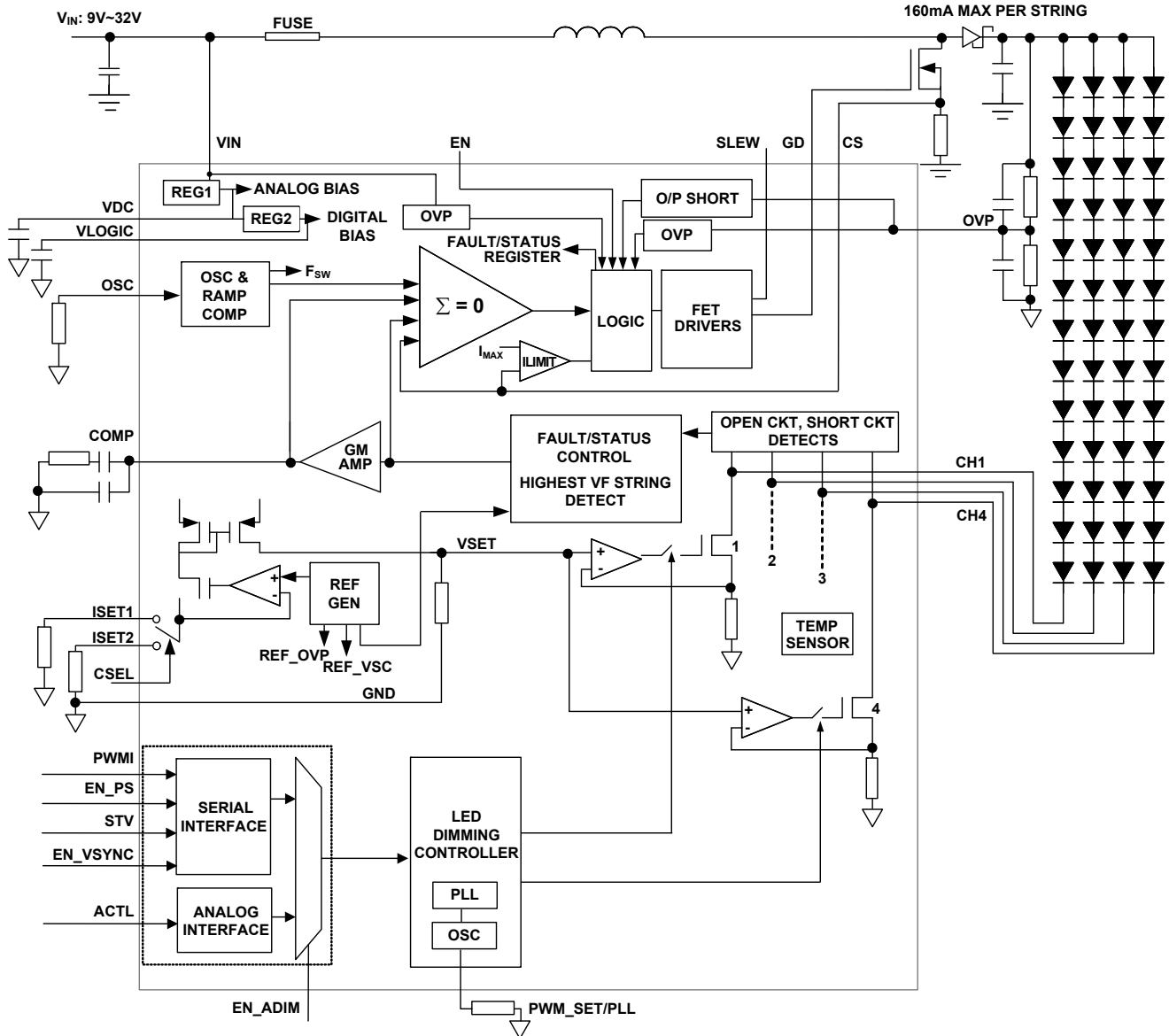
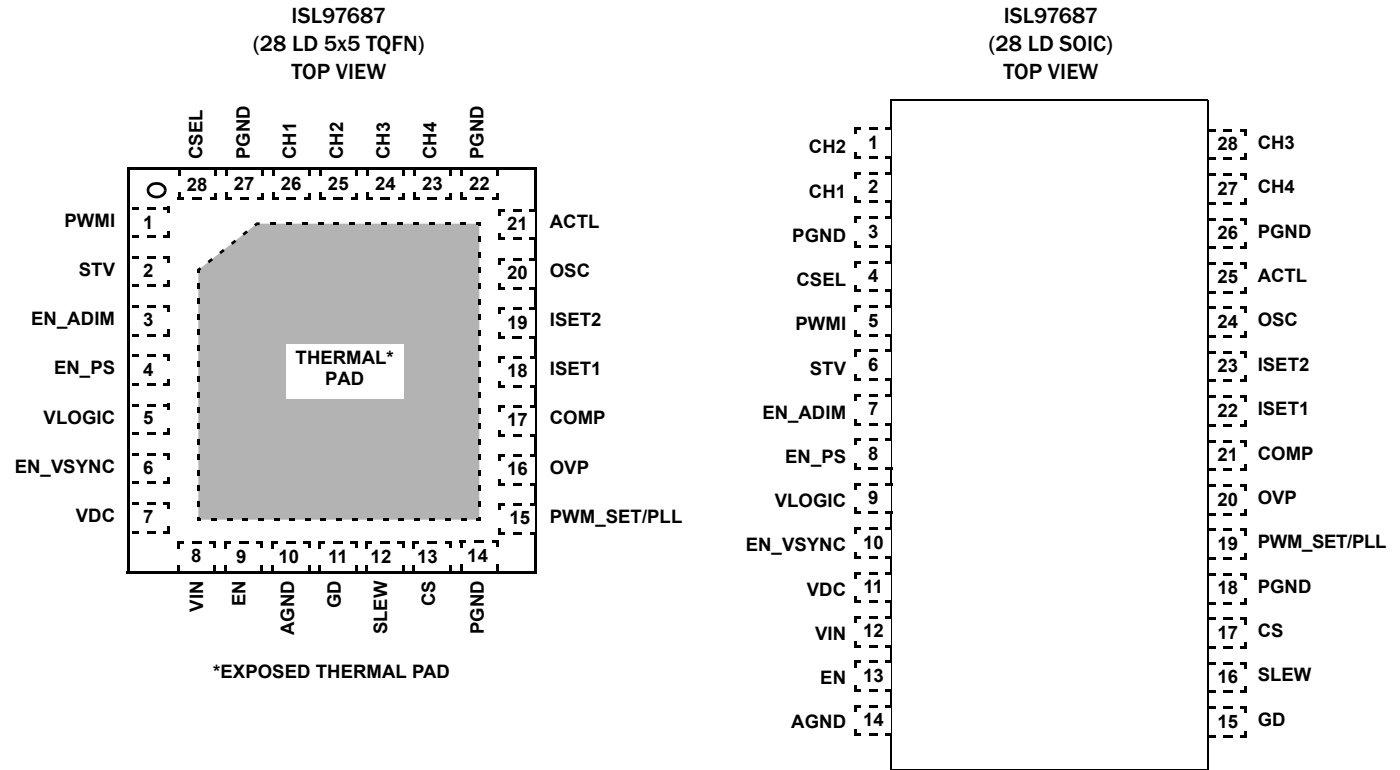


FIGURE 3. ISL97687 BLOCK DIAGRAM

## Pin Configurations



## Pin Descriptions

TQFN	SOIC	PIN NAME	PIN TYPE	PIN DESCRIPTION
1	5	PWMI	I	PWM Brightness Control Input pin.
2	6	STV	I	Start Vertical Frame signal; used in VSYNC mode.
3	7	EN_ADIM	I	Enable Analog Dimming
4	8	EN_PS	I	Enable Phase Shift
5	9	VLOGIC	S	Internal 2.5V Digital Bias Regulator. Needs Decoupling Capacitor added to ground.
6	10	EN_VSYNC	I	Frame synchronization enable. Ties high to VDC for enable $V_{\text{SYNC}}$ function. PWM_SET/PLL also needs to be configured with an RC network. Pin can be tied to VDC or VLOGIC to enable function.
7	11	VDC	S	Internal 5V Analog Bias Regulator. Needs Decoupling Capacitor added to ground.
8	12	VIN	S	Main Power Input. Range: 9V to 32V.
9	13	EN	I	LED Driver Enable. Whole chip will shut down when low.
10	14	AGND	S	Analog Ground
11	15	GD	O	External Boost FET gate control
12	16	SLEW	I	Boost Regulation Switching Slew Rate control.
13	17	CS	I	External Boost FET current sense input.
14	18	PGND	S	Boost FET gate driver power ground and ground reference for CS pin.
15	19	PWM_SET/ PLL	I	For direct PWM mode, tie this pin high to VDC. For other non-VSYNC modes, connect to a resistor to set the dimming frequency. If the VSYNC function is enabled, connect this pin to the PLL loop filter network.
16	20	OVP	I	Overvoltage Protection Input as well as Output Voltage feedback pin.
17	21	COMP	I	Boost compensation

## Pin Descriptions (Continued)

TQFN	SOIC	PIN NAME	PIN TYPE	PIN DESCRIPTION
18	22	ISET1	I	Resistor connection for setting LED current. $28.7k\Omega = 100mA$ .
19	23	ISET2	I	Resistor connection for setting LED current. $28.7k\Omega = 100mA$ .
20	24	OSC	I	Boost switching frequency adjustment.
21	25	ACTL	I	Analog dimming input (input range is 0.3V to 3V).
22	26	PGND	S	Power Ground return for LED current.
23	27	CH4	I	LED PWM Driver
24	28	CH3	I	LED PWM Driver
25	1	CH2	I	LED PWM Driver
26	2	CH1	I	LED PWM Driver
27	3	PGND	S	Power Ground return for LED current.
28	4	CSEL	I	ISET Resistor Selection Pin. CSEL = 0 : ISET 1 resistor sets LED current CSEL = 1 : ISET 2 resistor sets LED current

## Ordering Information

PART NUMBER (Notes 3, 4)	PART MARKING	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL97687IRTZ (Note 1)	ISL9768 7IRTZ	28 Ld 5x5 TQFN	L28.5x5B
ISL976787IBZ (Note 2)	ISL97687IBZ	28 Ld SOIC (300mil)	M28.3
ISL97687IRTZ-LEVALZ	Evaluation Board (12 LEDs populated in each channel)		
ISL97687IRTZ-HEVALZ	Evaluation Board (22 LEDs populated in each channel)		
ISL97687IBZEV1Z	Evaluation Board (None of LEDs on the evaluation board)		

### NOTES:

1. Add "-T" suffix for 6k unit tape and reel option. Refer to [TB347](#) for details on reel specifications.
2. Add "-T" suffix for 1k unit tape and reel option. Refer to [TB347](#) for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), see product information page for [ISL97687](#). For more information on MSL, refer to [TB363](#).

# Table of Contents

<b>Absolute Maximum Ratings</b> .....	<b>6</b>
<b>Thermal Information</b> .....	<b>6</b>
<b>Operating Conditions</b> .....	<b>6</b>
<b>Electrical Specifications</b> .....	<b>6</b>
<b>Typical Performance Curves</b> .....	<b>8</b>
<b>Theory of Operation</b> .....	<b>11</b>
PWM Boost Converter .....	11
OVP and $V_{OUT}$ .....	11
Current Matching and Current Accuracy .....	11
Dynamic Headroom Control .....	11
Dimming Controls .....	11
LED DC Current Setting .....	11
PWM Dimming Frequency Adjustment .....	13
Phase Shift Control .....	13
$V_{OUT}$ Control when LEDs are Off .....	13
Switching Frequency .....	14
5V and 2.4V Low Dropout Regulators .....	14
Soft-Start and Boost Current Limit .....	14
Fault Protection and Monitoring .....	14
Short Circuit Protection (SCP) .....	14
Open Circuit Protection (OCP) .....	15
Undervoltage Lock-out .....	15
Over-Temperature Protection (OTP) .....	15
Shutdown .....	15
<b>Component Selections</b> .....	<b>16</b>
Input Capacitor .....	16
Inductor .....	17
Output Capacitors .....	17
Channel Capacitor .....	17
Schottky Diode .....	17
High Current Applications .....	17
<b>PCB Layout Considerations</b> .....	<b>18</b>
Two Layers PCB Layout with TQFN Package .....	18
General Power PAD Design Considerations .....	18
One Layer PCB Layout with SOIC Package .....	18
<b>Equivalent Circuit Diagrams</b> .....	<b>21</b>
<b>Revision History</b> .....	<b>22</b>
<b>About Intersil</b> .....	<b>22</b>
<b>Package Outline Drawings</b> .....	<b>23</b>

**Absolute Maximum Ratings** ( $T_A = +25^\circ\text{C}$ )

VIN, EN, PWM1, ACTL	-0.3V to 45V
VDC	-0.3V to 5.75V
VLOGIC	-0.3V to 2.75V
COMP, ISET1, ISET2, PWM_SET, OSC, CS, OVP	-0.3V to min (VDC+0.3V, 5.75V)
EN_VSYNC, CSEL	-0.3V to 5.75V
STV, EN_ADIM, EN_PS	-0.3V to 5.75V
CH1 - CH4	-0.3V to 75V
GD, SLEW	-0.3V to 18V
PGND	-0.3V to +0.3V

Above voltage ratings are all with respect to AGND pin

**ESD Rating**

Human Body Model (Tested per JESD22-A114F)	2kV
Machine Model (Tested per JESD22-A115C)	200V
Charged Device Model (JESD22-C101E)	1kV
Latch Up (Tested per JESD-78B; Class 2, Level A)	100mA

**Thermal Information**

Thermal Resistance	$\theta_{JA}$ ( $^\circ\text{C}/\text{W}$ )	$\theta_{JC}$ ( $^\circ\text{C}/\text{W}$ )
28 Ld TQFN (4 layer + vias, Notes 5, 6)	32	4
28 Ld SOIC (4 layer, Notes 7, 8)	54	25
Thermal Characterization (Typical, Note 9)		$\text{PSI}_{JT}$ ( $^\circ\text{C}/\text{W}$ )
28 Ld TQFN		1
28 Ld SOIC		4
Maximum Continuous Junction Temperature		+125 $^\circ\text{C}$
Storage Temperature		-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$
Power Dissipation	TQFN (W)	SOIC (W)
$T_A < +25^\circ\text{C}$	3.13	1.85
$T_A < +70^\circ\text{C}$	1.72	1.02
$T_A < +85^\circ\text{C}$	1.25	0.74
$T_A < +105^\circ\text{C}$	0.63	0.37

**Operating Conditions**

Temperature Range	-40 $^\circ\text{C}$ to +105 $^\circ\text{C}$
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**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

**NOTES:**

- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief [TB379](#).
- For  $\theta_{JC}$ , the "case temp" location is the center of the exposed metal pad on the package underside.
- For  $\theta_{JC}$ , the "case temp" location is taken at the package top center.
- $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief [TB379](#) for details.
- $\text{PSI}_{JT}$  is the PSI junction-to-top thermal characterization parameter. If the package top temperature can be measured with this rating then the die junction temperature can be estimated more accurately than the  $\theta_{JC}$  and  $\theta_{JC}$  thermal resistance ratings.

**Electrical Specifications** All specifications below are characterized at  $T_A = -40^\circ\text{C}$  to +105 $^\circ\text{C}$ ;  $V_{IN} = 12\text{V}$ ,  $\text{EN} = 5\text{V}$ . **Boldface limits apply over the operating temperature range, -40 $^\circ\text{C}$  to +105 $^\circ\text{C}$ .**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 10)	TYP	MAX (Note 10)	UNIT
<b>GENERAL</b>						
$V_{IN}$	Backlight Supply Voltage	(Note 11)	<b>9</b>		<b>32</b>	V
$I_{VIN\_STBY}$	VIN Shutdown Current	$\text{EN} = 0$			<b>5</b>	$\mu\text{A}$
$I_{VIN\_ACTIVE}$	Switching	$R_{FPWM} = 3.3\text{k}\Omega$ , $I_{LED} = 100\text{mA}$ , $f_{SW} = 600\text{kHz}$ , $C_{OUT\_SW} = 1\text{nF}$		10	<b>13</b>	mA
	Non-switching			4	<b>5.5</b>	mA
$V_{UVLO}$	Undervoltage Lock-out Threshold		<b>2.9</b>		<b>3.3</b>	V
$V_{UVLO\_HYS}$	Undervoltage Lock-out Hysteresis			300		mV
<b>LINEAR REGULATOR</b>						
$V_{DC}$	5V Analog Bias Regulator	$V_{IN} > 6\text{V}$	<b>4.8</b>	5	<b>5.1</b>	V
$V_{DC\_DROP}$	$V_{DC}$ LDO Load Regulation Tolerance	$I_{VDC} = 30\text{mA}$		71	<b>100</b>	mV
$V_{LOGIC}$	2.5V Logic Bias Regulator	$V_{IN} > 6\text{V}$	<b>2.3</b>	2.4	<b>2.5</b>	V
$V_{LOGIC\_DROP}$	$V_{LOGIC}$ LDO Load Regulation Tolerance	$I_{VLOGIC} = 30\text{mA}$		31	<b>100</b>	mV
<b>BOOST SWITCH CONTROLLER</b>						
$t_{SS}$	Soft-Start			16		ms
$I_{SW\_LIMIT}$	Boost FET Current Limit (See Equation 5)	$R_{SENSE} = 50\text{m}\Omega$	<b>3.1</b>	3.4	<b>3.8</b>	A
$t_R$	Gate Rise Time	$C_{OUT\_SW} = 1000\text{pF}$		20		ns
$t_F$	Gate Falling Time	$C_{OUT\_SW} = 1000\text{pF}$		17.6		ns
$V_{GD}$	Gate Driver Output Voltage	$C_{OUT\_SW} = 1000\text{pF}$		10		V

**Electrical Specifications** All specifications below are characterized at  $T_A = -40^\circ\text{C}$  to  $+105^\circ\text{C}$ ;  $V_{IN} = 12\text{V}$ ,  $EN = 5\text{V}$ . **Boldface limits apply over the operating temperature range,  $-40^\circ\text{C}$  to  $+105^\circ\text{C}$ .** (Continued)

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 10)	TYP	MAX (Note 10)	UNIT
$D_{MAX}$	Boost Maximum Duty Cycle	$f_{SW} = 600\text{kHz}$	<b>92</b>			%
$D_{MIN}$	Boost Minimum Duty Cycle	$f_{SW} = 1.2\text{MHz}$			<b>26</b>	%
$f_{SW}$	Boost Switching Frequency (See Equation 4)	$R_{OSC} = 250\text{k}\Omega$	<b>180</b>	200	<b>220</b>	kHz
		$R_{OSC} = 83\text{k}\Omega$	<b>540</b>	600	<b>660</b>	kHz
		$R_{OSC} = 42\text{k}\Omega$	<b>1.08</b>	1.2	<b>1.32</b>	MHz
$EFF_{PEAK}$	Boost Peak Efficiency			90		%
<b>REFERENCE</b>						
$I_{MATCH}$	Channel-to-Channel Current Matching	Channels are in a single IC, $I_{LED} = 100\text{mA}$	<b>-2</b>	$\pm 1$	<b>2</b>	%
$I_{ACC}$	Absolute Current	$R_{ISET1/2} = 28.7\text{k}\Omega$	<b>-3</b>		<b>3</b>	%
<b>FAULT DETECTION</b>						
$V_{SC}$	Channel Short Circuit Threshold		<b>7.2</b>	8	<b>8.8</b>	V
$V_{TEMP}$	Over-Temperature Threshold			150		$^\circ\text{C}$
$V_{TEMP\_ACC}$	Over-Temperature Threshold Accuracy			5		$^\circ\text{C}$
$V_{OVP\_OUT}$	Overvoltage Limit on OVP Pin		<b>1.18</b>	1.22	<b>1.24</b>	V
$V_{OVP\_IN}$	Overvoltage Limit on VIN Pin			35		V
<b>DIGITAL I/O LOGIC LEVEL SPECIFICATIONS</b>						
$V_{IL}$	Logic Input Low Voltage - STV, EN_PS, EN_VSYNC, EN_ADIM, PWMI, CSEL, EN				<b>0.8</b>	V
$V_{IH}$	Logic Input High Voltage - STV, EN_PS, EN_VSYNC, EN_ADIM, PWMI, CSEL, EN		<b>1.5</b>		<b>5.5</b>	V
STV	Frame frequency		<b>30</b>		<b>240</b>	Hz
<b>CURRENT SOURCES</b>						
$V_{HEADROOM}$	Dominant Channel Current Source Headroom at CH Pin	$I_{LED} = 160\text{mA}$ $T_A = +25^\circ\text{C}$		0.75 (Note 12)		V
$V_{HEADROOM\_RANGE}$	Dominant Channel Current Sink Headroom Range at CHX Pin	$I_{LED} = 20\text{mA}$ , $T_A = +25^\circ\text{C}$		90		mV
$V_{ISET1,2}$	Voltage at ISET1 and 2 Pins		<b>1.18</b>	1.21	<b>1.24</b>	V
$I_{LED\_MAX}$	Maximum LED Current per Channel		<b>160</b>			mA
<b>PWM GENERATOR</b>						
$f_{PWM}$	Generated PWM Frequency (See Equation 3)	$R_{PWM\_SET} = 333\text{k}\Omega$	<b>45</b>	50	<b>55</b>	Hz
		$R_{PWM\_SET} = 3.3\text{k}\Omega$	<b>4.5</b>	5	<b>5.5</b>	kHz
Dimming Range	PWM Dimming Duty Cycle Limits	$f_{PWM} \leq 20\text{kHz}$	<b>0.1</b>		<b>100</b>	%
$f_{PWMI}$	PWMI Input Frequency Range		<b>60</b>		<b>20k</b>	Hz
$V_{PWM\_SET}$	PWM_SET Voltage	$R_{PWM\_SET} = 3.3\text{k}\Omega$	<b>1.18</b>	1.21	<b>1.25</b>	V
$V_{ACTL}$	Analog Dimming Input	0% Dimming	<b>0.28</b>	0.3	<b>0.31</b>	V
		100% Dimming	<b>2.95</b>	3	<b>3.1</b>	V
$t_{PWM\_MIN}$	Minimum PWM On Time in Direct PWM Mode			350		ns

**NOTES:**

- Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ\text{C}$ , unless otherwise specified. Temperature limits established by characterization and are not production tested.
- At maximum  $V_{IN}$  of 32V, minimum  $V_{OUT}$  is 35V. Minimum  $V_{OUT}$  can be lower at lower  $V_{IN}$ .
- Varies within the range specified by  $V_{HEADROOM\_RANGE}$ .

# Typical Performance Curves

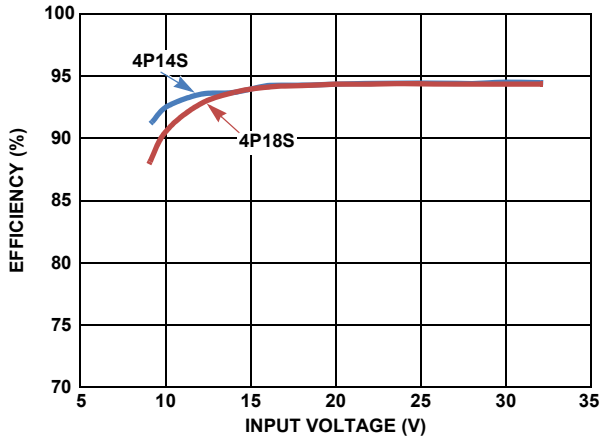


FIGURE 4. EFFICIENCY vs  $V_{IN}$  ( $I_{CH}$ : 100mA,  $f_{DIM}$ : 200Hz,  $V_{OUT}$ : 45V FOR 4P14S AND 55V FOR 4P18S)

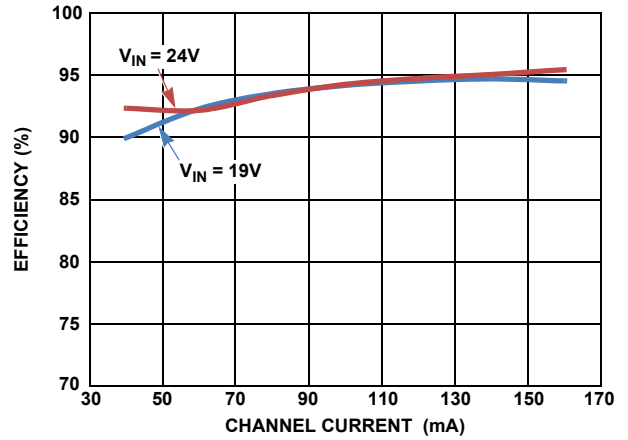


FIGURE 5. EFFICIENCY vs  $I_{CH}$  ( $V_{OUT}$ : 55V FOR 4P18S,  $f_{DIM}$ : 200Hz)

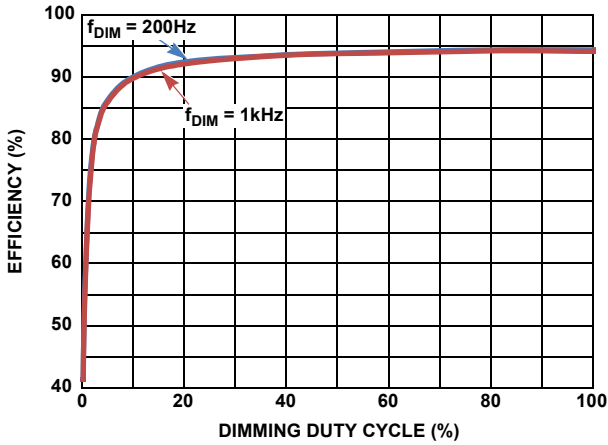


FIGURE 6. EFFICIENCY vs PWM DIMMING ( $V_{IN}$ : 24V,  $V_{OUT}$ : 55V FOR 4P18S,  $I_{CH}$ : 100mA)

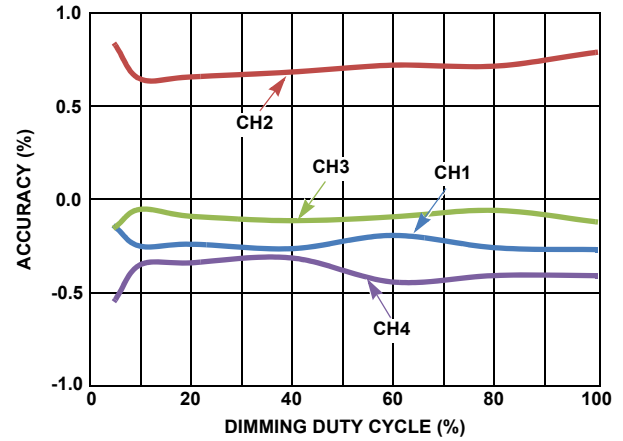


FIGURE 7. ACCURACY vs PWM DIMMING ( $V_{IN}$ : 24V,  $V_{OUT}$ : 55V FOR 4P18S,  $I_{CH}$ : 100mA)

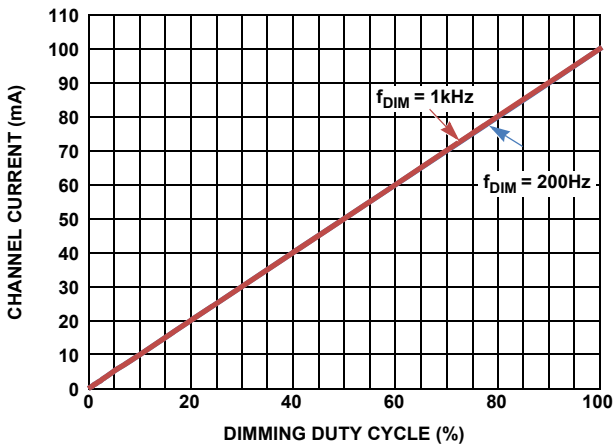


FIGURE 8. PWM DIMMING LINEARITY ( $V_{IN}$ : 24V,  $V_{OUT}$ : 55V FOR 4P18S)

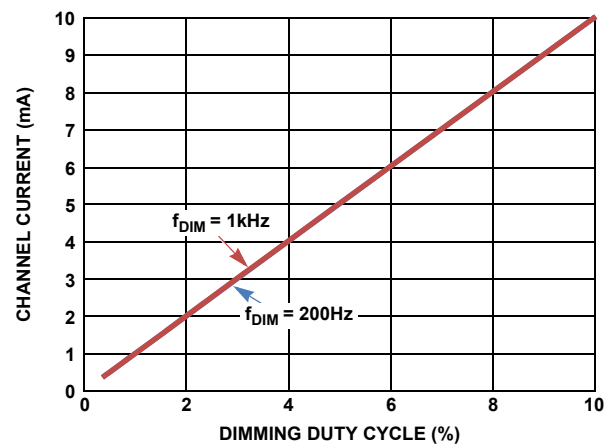


FIGURE 9. PWM DIMMING LINEARITY ( $V_{IN}$ : 24V,  $V_{OUT}$ : 55V FOR 4P18S)



## Typical Performance Curves (Continued)

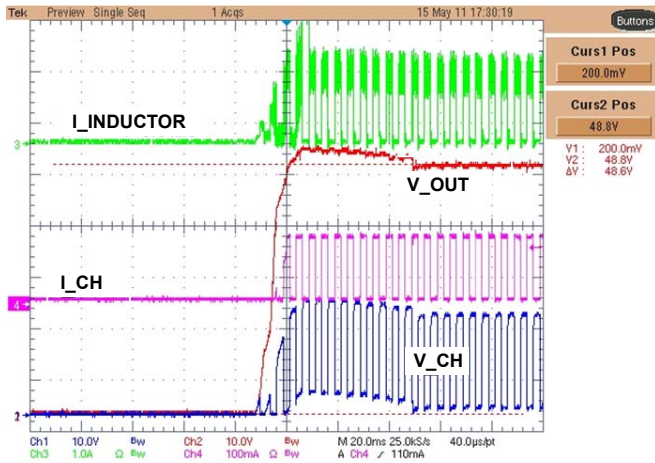


FIGURE 10. START-UP (DIRECT PWM DIMMING,  $V_{IN}$ : 19V,  $I_{CH}$ : 120mA, LEDs: 4P18S,  $f_{DIM}$ : 200Hz)

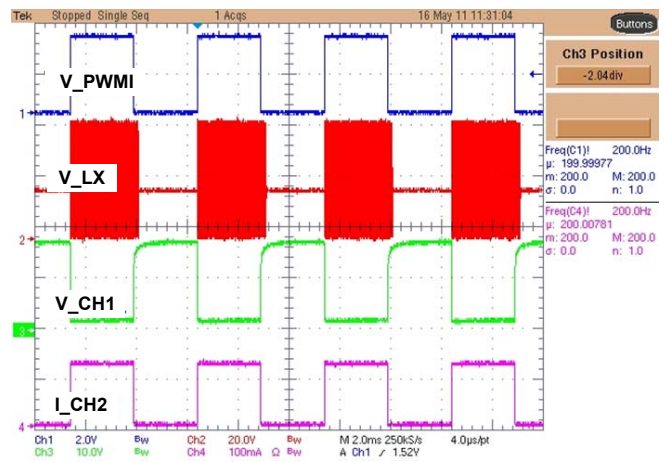


FIGURE 11. DIRECT PWM DIMMING ( $V_{IN}$ : 19V, LEDs: 4P18S,  $f_{DIM}$ : 200Hz)

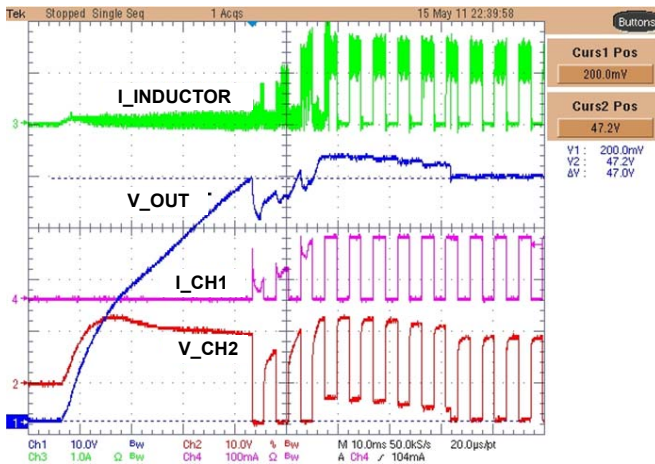


FIGURE 12. START-UP WITHOUT PHASE SHIFT ( $V_{IN}$ : 19V,  $I_{CH}$ : 120mA, LEDs: 4P18S,  $f_{DIM}$ : 200Hz)

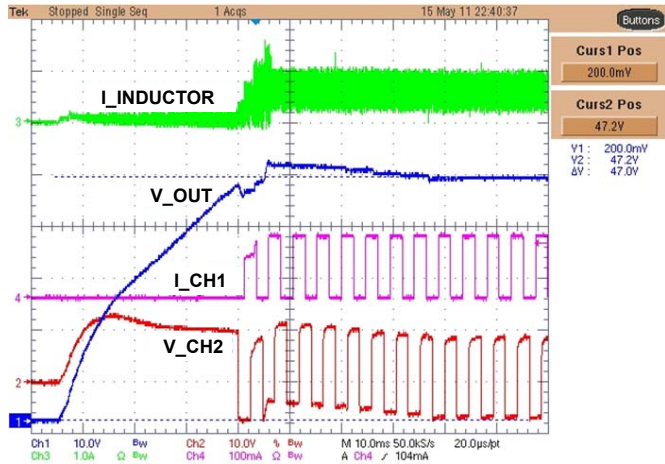


FIGURE 13. START-UP WITH PHASE SHIFT ( $V_{IN}$ : 19V,  $I_{CH}$ : 120mA, LEDs: 4P18S,  $f_{DIM}$ : 200Hz)

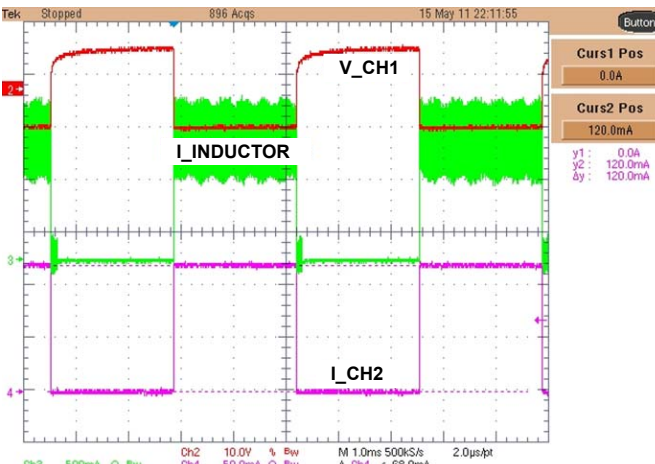


FIGURE 14. PWM DIMMING WITHOUT PHASE SHIFT ( $V_{IN}$ : 19V,  $I_{CH}$ : 120mA, LEDs: 4P18S,  $f_{DIM}$ : 200Hz)

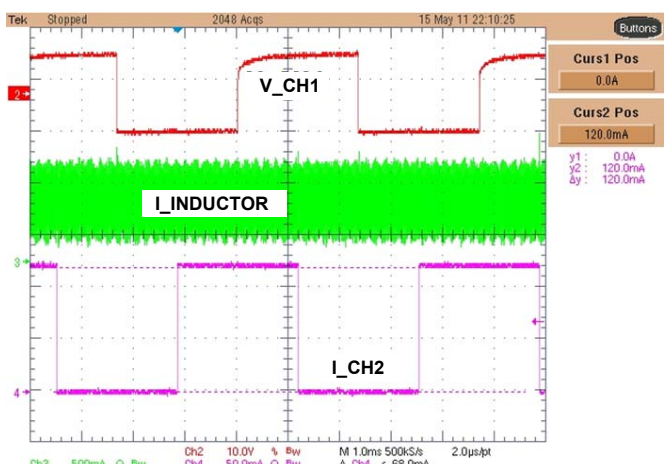
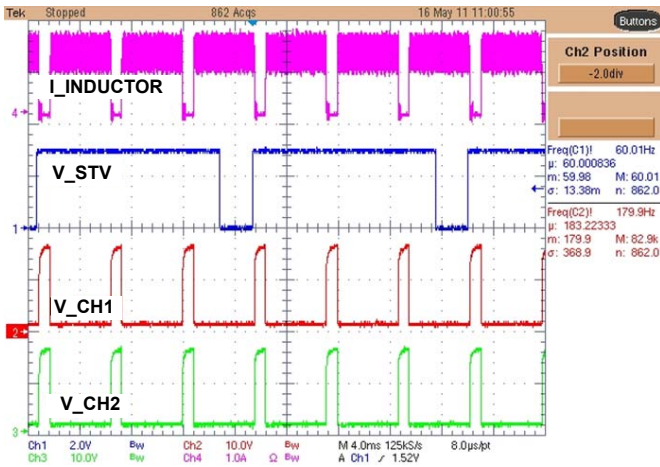
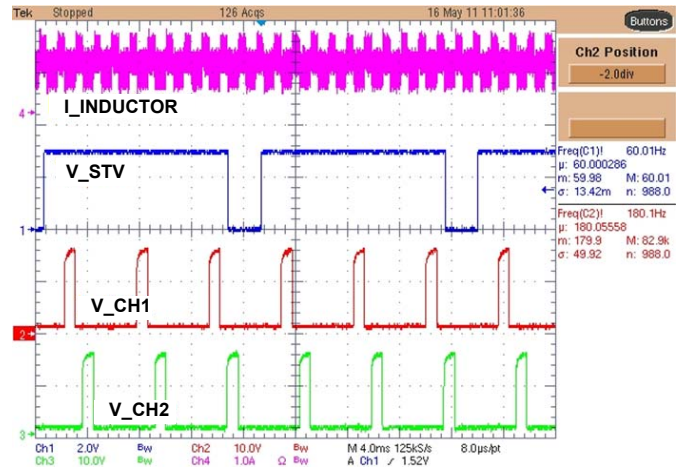


FIGURE 15. PWM DIMMING WITH PHASE SHIFT ( $V_{IN}$ : 19V,  $I_{CH}$ : 120mA, LEDs: 4P18S,  $f_{DIM}$ : 200Hz)

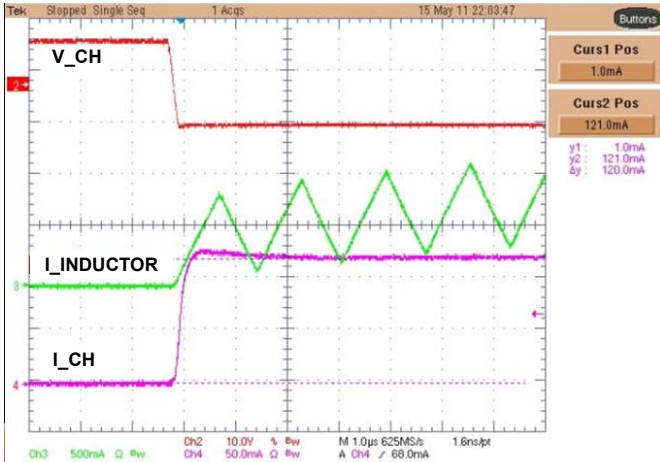
## Typical Performance Curves (Continued)



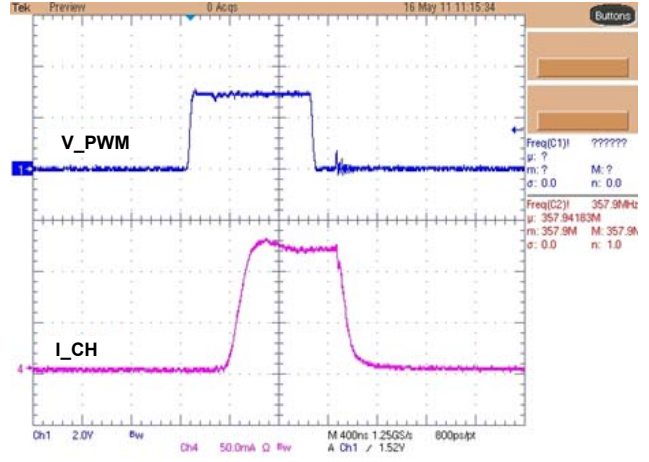
**FIGURE 16.  $V_{SYNC}$  ENABLED DIMMING WITHOUT PHASE SHIFT ( $V_{IN}$ : 19V,  $I_{CH}$ : 120mA, LEDs: 4P18S, 180Hz OUTPUT PHASE AND FREQUENCY LOCKED TO 60Hz STV)**



**FIGURE 17.  $V_{SYNC}$  ENABLED WITH PHASE SHIFT ( $V_{IN}$ : 19V,  $I_{CH}$ : 120mA, LEDs: 4P18S, 180Hz OUTPUT PHASE AND FREQUENCY LOCKED TO 60Hz STV)**



**FIGURE 18. PWM SWITCHING AND TRANSIENT RESPONSE OF INDUCTOR CURRENT**



**FIGURE 19. MINIMUM DIMMING DUTY CYCLE (0.05%,  $f_{DIM}$ : 500Hz,  $I_{CH}$  = 120mA, DIRECT PWM MODE)**

## Theory of Operation

### PWM Boost Converter

The current mode PWM boost converter produces the minimal voltage needed to enable the LED string with the highest forward voltage drop to run at the programmed current. The ISL97687 employs current mode control boost architecture that has a fast current sense loop and a slow voltage feedback loop. The number of LEDs that can be driven by ISL97687 depends on the type of LED chosen in the application. The ISL97687 is capable of boosting up to greater than 70V and driving 4 Channels of LEDs at a maximum of 160mA per channel.

### OVP and $V_{OUT}$

The Overvoltage Protection (OVP) pin has a function of setting the overvoltage trip level as well as limiting the  $V_{OUT}$  regulation range.

The ISL97687 OVP threshold is set by  $R_{UPPER}$  and  $R_{LOWER}$  as shown in Equation 1:

$$V_{OUT\_OVP} = \frac{1.21(R_{UPPER} + R_{LOWER})}{R_{LOWER}} \quad (EQ. 1)$$

and  $V_{OUT}$  can only regulate between 30% and 100% of the  $V_{OUT\_OVP}$  such that:

Allowable  $V_{OUT} = 30\%$  to  $100\%$  of  $V_{OUT\_OVP}$

For example, a  $1M\Omega$   $R_{UPPER}$  and  $19k\Omega$   $R_{LOWER}$  sets OVP to 65.9V. The boost can regulate down to 30% of OVP, so it can go as low as 19.5V. If  $V_{OUT}$  needs to be lower than this, the OVP level must be reduced. Otherwise,  $V_{OUT}$  will regulate to 19.5V, and the ISL97687 may overheat. However, it's recommended that the OVP be set to no more than 20% above the nominal operating voltage. This prevents the need for output capacitor voltage ratings and the inductor current rating to be set significantly higher than needed under normal conditions, allowing a smaller and cheaper solution, as well as keeping the maximum voltages and currents that can be seen in the system during fault conditions at less extreme levels.

Parallel capacitors should be placed across the OVP resistors such that  $R_{UPPER}/R_{LOWER} = C_{LOWER}/C_{UPPER}$ . Using a  $C_{UPPER}$  value of at least 30pF is recommended. These capacitors reduce the AC impedance of the OVP node, which is important when using high value resistors. The ratio of the OVP capacitors should be the inverse of the OVP resistors. For example, if  $R_{UPPER}/R_{LOWER} = 33/1$ , then  $C_{UPPER}/C_{LOWER} = 1/33$  with  $C_{UPPER} = 100pF$  and  $C_{LOWER} = 3.3nF$ . These components are not always needed, but it is highly recommended to include placeholders.

### Current Matching and Current Accuracy

The LED current in each channel is regulated using an active current source circuit, as shown in Figure 20. The peak LED current is set by translating the  $R_{ISET}$  current to the output with a scaling factor of  $2919/R_{ISET}$ . The drain terminals of the current source MOSFETs are designed to operate within a range of about 750mV to optimize power loss versus accuracy requirements. The sources of channel-to-channel current matching error come from the op amp offsets, reference voltage, and current source

sense resistors. These parameters are optimized for current matching and absolute current accuracy. However, the absolute accuracy is additionally determined by the external  $R_{ISET}$ . A 0.1% tolerance resistor is therefore recommended.

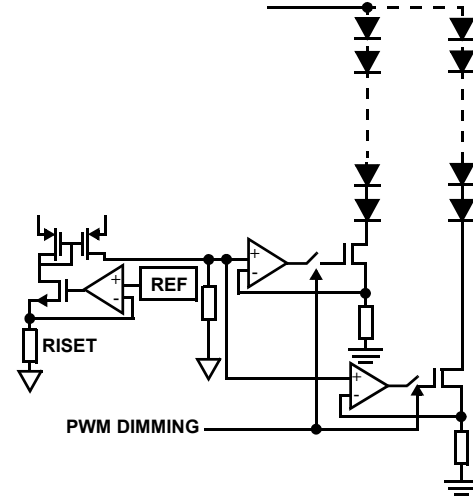


FIGURE 20. SIMPLIFIED CURRENT SOURCE CIRCUIT

### Dynamic Headroom Control

The ISL97687 features a proprietary dynamic headroom control circuit that detects the highest forward voltage string, or effectively the lowest voltage from any of the CH pins. The system will regulate the output voltage to the correct level to allow the channel with the lowest voltage to have just sufficient headroom to correctly regulate the LED current. Since all LED strings are connected to the same output voltage, the other CH pins will have a higher voltage, but the regulated current source circuit on each channel will ensure that each channel has the correct current level. The output voltage regulation is dynamic, and is updated as needed, to allow for temperature and aging effects in the LEDs.

### Dimming Controls

The ISL97687 provides two basic ways to control the LED current, and therefore, the brightness. These are described in detail in subsequent sub-sections, but can be broadly divided into the following two types of dimming:

Step 1. LED DC current adjustment

Step 2. PWM chopping of the LED current defined in Step 1

### LED DC Current Setting

The initial brightness should be set by choosing an appropriate value for the resistor on the ISET1/2 pins. This resistor must connect to AGND, and should be chosen to fix the maximum possible LED current:

$$I_{LEDmax} = \frac{2919}{R_{ISET}} \quad (EQ. 2)$$

The ISL97687 includes two built-in levels of current, individually set by the resistors on ISET1 and ISET2, according to Equation 2, which can be switched between by using the CSEL pin.

CSEL = 0: The current setting is based on ISET1

CSEL = 1: The current setting is based on ISET2

This is typically used in 3D systems to provide a higher current level in 3D modes, but is not restricted to this application. CSEL can be switched in operation and updates immediately in direct PWM mode, and at the start of the next PWM dimming cycle in other modes.

**LED DC DIMMING**

It is possible to control the LED current by applying a DC voltage  $V_{DIM}$  to the ISET1/2 pin via a resistor as in Figure 21.

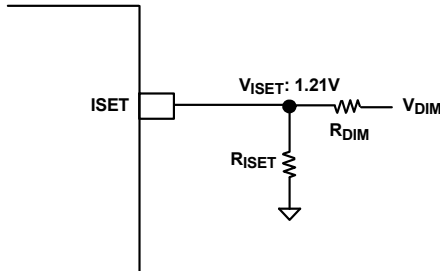


FIGURE 21. LED CURRENT CONTROL WITH  $V_{DIM}$

If the  $V_{DIM}$  is above  $V_{ISET}$  1.21V, the brightness will reduce, and vice versa. In this configuration, it is important that the control voltage be set to the maximum brightness (minimum voltage) level when the ISL97687 is enabled, even if the LEDs are not lit at this point. This is necessary to allow the chip to calibrate to the maximum current level that will need to be supported. Otherwise, on-chip power dissipation will be higher at current levels above the start-up level. Dimming with this technique should be limited to a minimum of 10~20% brightness, as LED current accuracy is increasingly degraded at lower levels.

**LED PWM CONTROL**

The ISL97687 provides many different PWM dimming methods. Each of these results in PWM chopping of the current in the LEDs of all 4 channels, to provide an average LED current and control the brightness. During the on-periods, the LED peak current will be defined by the value of the resistor on ISET1 or ISET2, as described in Equation 2.

Dimming can either be “direct PWM” mode, where both the frequency and duty cycle of the LEDs match that of the incoming PWMI signal, or the duty cycle and frequency sources must be selected from the following.

**SUPPORTED LED DUTY CYCLE SOURCES**

- Decoded PWMI pin duty cycle (PWM input mode)
- Decoded ACTL pin voltage (Analog input mode)
- Analog\*PWM input mode (Both PWM and Analog inputs are used)

**SUPPORTED LED FREQUENCY SOURCES**

- Free running internal oscillator (Internal PWM frequency mode)
- Frequency can be phase and frequency locked to frame rate ( $V_{SYNC}$  mode)

Additionally, phase shift mode can be enabled in all configurations except direct PWM, allowing the LED strings to turn on in sequence.

**LED PWM DIMMING IN DIRECT PWM MODE**

When the PWM\_SET/PLL pin is tied to VDC, the PWMI input signal is used to directly control the LEDs. The dimming frequency and phase of the LEDs will be the same as that of PWMI. This mode can be used to get very high effective PWM resolution, as the resolution is effectively determined by the PWMI signal source.

**LED PWM DIMMING – DUTY CYCLE CONTROL**

In non-direct PWM mode, the ISL97687 can decode the incoming PWMI duty cycle information at 10-bit resolution and the ACTL voltage level at 8-bit resolution and apply these values to the LEDs as a PWM output at a new frequency.

For applications where DC-PWM dimming is required, the analog dimming mode must be enabled (EN\_ADIM = high). The analog control input pin (ACTL) must then be fed with a voltage of 0.3V to 3.0V. This is decoded as an 8-bit duty cycle of 0% to 100% respectively. This interface supports backward compatibility with CCFL backlight driving systems, but can also be used in other applications, such as analog ALS interfaces. External circuitry can be used to shift most analog input ranges to the required level. Figure 22 is an example that maps a 0V to 3.5V input to give a 10-100% output range, but this can be tailored to other requirements. The PWM dimming frequency, set by the PWM\_SET pin, should be at least 1kHz when EN\_ADIM is high.

In Analog mode, the decoded 10-bit PWM duty cycle information from the PWMI pin is also used, multiplied by the 8-bit level decoded from the ACTL pin. For example, if ACTL = 2.3V (74%) and PWMI = 50%, then LED dimming will be 74% x 50% = 37%. For analog dimming applications where this multiplication is not needed, PWMI should be tied high, giving the ACTL pin full control over the duty cycle range. For applications where analog dimming is not needed, EN\_ADIM should be low and PWMI should be driven with the required duty cycle.

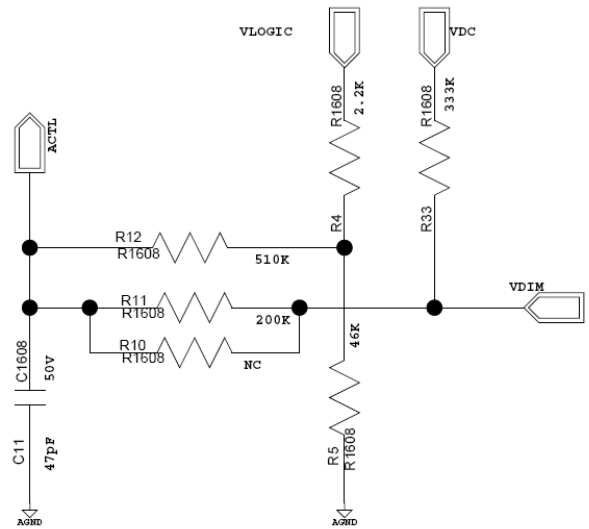


FIGURE 22. EXAMPLE OF ACTL INPUT ADJUSTMENT

## PWM Dimming Frequency Adjustment

The dimming frequencies of serial interface and ACTL modes are set by an external resistor at the PWM\_SET pin, as shown in Equation 3:

$$f_{\text{PWM}} = \frac{(1.665) \times 10^7}{R_{\text{PWMSET}}} \quad (\text{EQ. 3})$$

where  $f_{\text{PWM}}$  is the desirable PWM dimming frequency and  $R_{\text{PWMSET}}$  is the setting resistor.

### V<sub>SYNC</sub> FUNCTION

The V<sub>SYNC</sub> function is used to provide accurate LED dimming frequencies and make sure that the video data is properly aligned with the frame rate. A phase locked loop (PLL) is used to lock the frequency to a multiple of the frame rate. Additionally, the phase of the PWM output is aligned with the frame rate to provide very predictable video performance. In V<sub>SYNC</sub> mode, the PWM\_SET/PLL pin is used as the PLL loop compensation pin and needs a loop filter connected between it and ground.

Frame rates between 30Hz and 300Hz are supported, and an automatic frequency detection circuit will provide the same output frequency at 30, 60, 120, 180, 240, and 300Hz.

Additionally, the PWM dimming frequency can be pre-selected to any of the following values shown in Table 1 (Note that for the 60Hz range, the frequencies will be scaled by a factor of framerate/60Hz and for the 120Hz range they will be scaled by a factor of framerate/120Hz).

TABLE 1. PRE-SELECTED PWM DIMMING FREQUENCY AT V<sub>SYNC</sub> MODE

DIMMING FREQUENCY			
(Hz)	(kHz)	(kHz)	(kHz)
180	1.26	5.70	13.38
240	1.38	6.18	13.86
300	1.50	6.66	14.34
360	1.62	7.14	14.82
420	1.74	7.62	15.30
480	1.86	8.10	15.78
540	1.98	8.58	16.26
600	2.10	9.06	16.74
660	2.34	9.54	17.22
720	2.58	10.02	17.70
780	2.88	10.50	18.18
840	3.36	10.98	18.66
900	3.78	11.46	19.14
960	4.20	11.94	19.62
1.02k	4.74	12.42	20.10
1.14k	5.22	12.90	20.58

## Phase Shift Control

The ISL97687 is capable of delaying the phase of each current source within the PWM cycle. Conventional LED drivers present the worst load transients to the boost converter, by turning on all channels simultaneously, as shown in Figure 23. The ISL97687 can be configured to phase shift each channel by 90°, individually turning them on and off at different points during the PWM dimming period, as shown in Figure 24. At duty cycles below 100%, the load presented to the boost will peak at a lower level and/or spend less time at the peak, when compared to that of a conventional LED driver, as shown in Figure 23. Additionally, load steps are limited to the LED current of one CH pin, one quarter of that of a standard driver. This can help reduce transients on V<sub>OUT</sub> and also reduces audio noise by limiting the magnitude of changes in magnetic field required in the inductor needed to track the load. Audio noise is also generally improved for PWM frequencies in the audio band, as the effective frequency of the boost load is multiplied by a factor of 4, meaning that, for example, a 5kHz LED frequency offers an effective boost load frequency of 20kHz.

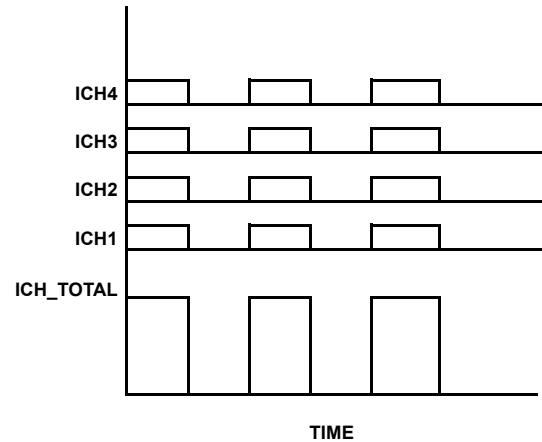


FIGURE 23. NON PHASE SHIFT PWM DIMMING AT 50% DUTY CYCLE

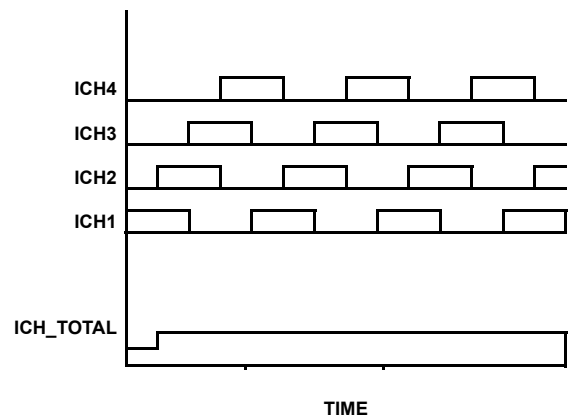


FIGURE 24. PHASE SHIFT PWM DIMMING AT 50% DUTY CYCLE

## V<sub>OUT</sub> Control when LEDs are Off

When the backlight is enabled but all LEDs are off (i.e., during the PWM off times), the switching regulator of a typical LED drivers will stop switching, which can allow the output to begin to discharge.

This is not a problem when the LED off times are short and the duty cycle is running at a high duty cycle, or the output capacitance is large. However, it presents two problems. First, for low duty cycles at low frequencies,  $V_{OUT}$  can droop between on-times, resulting in under-regulation of the current when the LEDs are next switched on. Second, at high PWM frequencies or very low duty cycles, LED on-times can be shorter than the minimum number of boost cycles needed to ramp up the inductor current to the required level to support the load. For example, a 1% on-time while running at 20kHz PWM dimming frequency is only 500ns. If the boost switching frequency is set at 500kHz, this only represents a quarter of a switching cycle per LED on-time, which may not be sufficient to ramp the inductor current to the required level.

The ISL97687 incorporates an additional PFM switching mechanism that allows the boost stage to continue to switch at low current levels in order to replace the energy lost from the output capacitor due to the OVP stack resistance and capacitor self discharge. For very short pulses, this also means that the charge delivered to the LEDs in the on-times is provided entirely by the output capacitor, kept at the correct voltage by the PFM mode in the off-times. This allows the output to always remain very close to the required level, so that when the LEDs are re-enabled, the boost output is already at the correct level. This dramatically improves LED PWM performance, providing industry leading linearity down to sub 1% levels, and reduces the overshoot in the boost inductor current, caused by transient switching when the LEDs are switched on, to a minimum level.

The system will continue to maintain  $V_{OUT}$  at the target level for 120ms after the last time the LEDs were on. If all LEDs are off for a longer period than this, the converter will stop switching and go into a sleep mode, allowing  $V_{OUT}$  to decay, in order to save power during long backlight-off periods.

## Switching Frequency

The boost switching frequency can be adjusted by the resistor on the OSC pin, which must be connected to AGND, and follows Equation 4:

$$f_{sw} = \frac{(5 \times 10^{10})}{R_{osc}} \quad (\text{EQ. 4})$$

where  $f_{sw}$  is the desirable boost switching frequency and  $R_{osc}$  is the setting resistor.

## 5V and 2.4V Low Dropout Regulators

A 5V LDO regulator is used to provide the low voltage supply needed to drive internal circuits. The output of this LDO is the VDC pin. A decoupling capacitor of 1 $\mu$ F or more is required between this pin and AGND for correct operation. Similarly, a 2.4V LDO regulator is present at the VLOGIC pin, and also requires a 1 $\mu$ F decoupling capacitor. Both pins can be used as a coarse voltage reference, or as a supply for other circuits, but can only support a load of up to ~10mA and should not be used to power noisy circuits that can feed significant noise onto their supply.

## Soft-Start and Boost Current Limit

The boost current limit should be set by using a resistor from CS to PGND. The typical current limit can be calculated as:

$$I_{LIMIT} = \frac{0.17}{R_{CS}} \quad (\text{EQ. 5})$$

The CS resistor should be chosen based on the maximum load that needs to be driven. Typically, a limit of 30~40% more than is required under DC conditions is sufficient to allow for necessary overshoots during load transients. Values of 20~100m $\Omega$  are supported.

It is important that PGND pin 14 (QFN)/18 (SOIC) is connected directly to the base of the sense resistor, with no other connection to the ground system, except via this path. This is because this pin is used as a ground reference for the CS pin. Connecting it here gives the maximum noise immunity and the best stability characteristics.

The ISL97687 uses a digital current limit based soft start. The initial limit level is set to one ninth of the full current limit, with eight subsequent steps increasing this by a ninth of the final value every 2ms until it reaches the full limit. In the event that no LEDs have been conducting during the interval since the last step (for example if the LEDs are running at low duty cycle at low PWM frequency), the step will be delayed until the LEDs are conducting again.

If the LEDs are off for more than 120ms, making the converter go into sleep mode, soft-start will be restarted when the LEDs are re-enabled.

## Fault Protection and Monitoring

The ISL97687 features extensive protection functions to cover all perceivable failure conditions. The failure mode of an LED can be either open or short circuit. The behavior of an open circuit LED can additionally take the form of either infinite or very high resistance or, for some LEDs, a zener diode, which is integrated into the device, in parallel with the now opened LED.

For basic LEDs (which do not have built-in zener diodes), an open circuit LED failure will only result in the loss of one channel of LEDs, without affecting other channels. Similarly, a short circuit condition on a channel that results in that channel being turned off does not affect other channels, unless a similar fault is occurring.

Due to the lag in boost response to any load change at its output, certain transient events (such as significant step changes in LED duty cycle, or a change in LED current caused by CSEL switching) can transiently look like LED fault modes. The ISL97687 uses feedback from the LEDs to determine when it is in a stable operating region and prevents apparent faults during these transient events from allowing any of the LED strings to fault out. See Figure 26 and Table 2 for more details.

## Short Circuit Protection (SCP)

The short circuit detection circuit monitors the voltage on each channel and disables faulty channels which are detected to be more than the short circuit threshold, 8V above the lowest CH pin, following a timeout period.

### Open Circuit Protection (OCP)

When any of the LEDs become open circuit during the operation, that channel will be disabled after a timeout period, and the part will continue to drive the other channels. The ISL97687 monitors the current in each channel such that any string which reaches the intended output current is considered “good”. Should the current subsequently fall below the target, the channel will be considered an “open circuit”. Furthermore, should the boost output of the ISL97687 reach the OVP limit, all channels which are not “good” will be timed out.

Unused CH pins should be grounded, which will disable them from start-up. This will prevent  $V_{OUT}$  having to ramp to OVP at start-up, in order to determine that they are open.

### Undervoltage Lock-out

If the input voltage falls below the UVLO level of 2.8V, the device will stop switching and reset. Operation will restart, with all digital settings returning to their default states, once the input voltage is back in the normal operating range.

### Over-Temperature Protection (OTP)

The OTP threshold is set to +150°C. When this is reached, the boost will stop switching and the output current sources will be switched off and stay off until power or EN is cycled. For the extensive fault protection conditions, please refer to Figure 26 and Table 2.

### VIN OVP

If VIN exceeds 35V, the part will be shut down until power or EN is cycled. At this point, all digital settings will be reset to their default states.

### Shutdown

When the EN pin is low the entire chip is shut down to give close to zero shutdown current. The digital interfaces will not be active during this time. The EN can be high before VIN.

### COMPENSATION

The ISL97687 boost regulator uses a current mode control architecture, with an external compensation network connected to the COMP pin. The component values shown in Figure 25 should be used. The network comprises a 47pF capacitor from COMP to AGND, in parallel with a series RC of 25kΩ and 2.2nF, also from COMP to AGND.

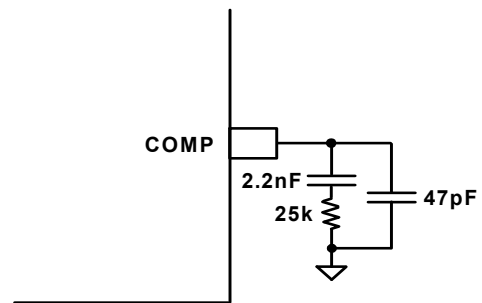


FIGURE 25. COMPENSATION NETWORK

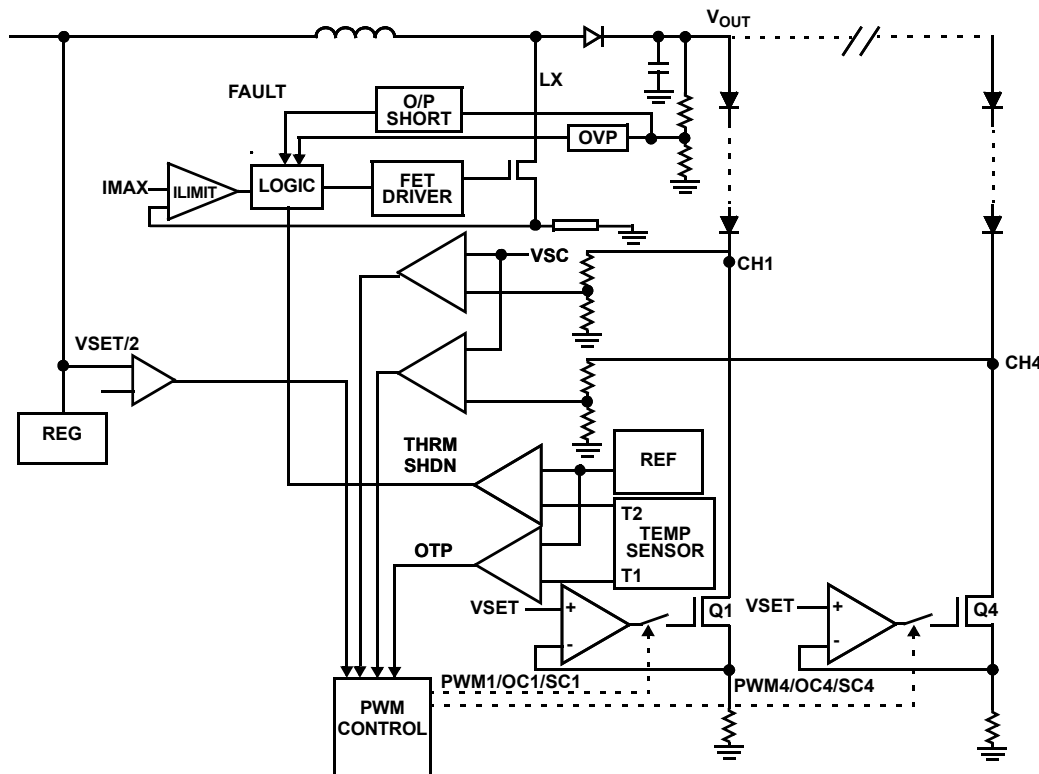


FIGURE 26. SIMPLIFIED FAULT PROTECTIONS

TABLE 2. PROTECTIONS TABLE

CASE	FAILURE MODE	DETECTION MODE	FAILED CHANNEL ACTION	GOOD CHANNELS ACTION	V <sub>OUT</sub> REGULATED BY
1	CH1 Short Circuit	Over-Temperature Protection limit (OTP) not triggered and VCH1 < VSC	CH1 ON and burns power	CH2 through CH4 Normal	Highest VF of CH2 through CH4
2	CH1 Short Circuit	OTP not triggered but VCH1 > VSC	CH1 disabled after 6 PWM cycles time-out. (Note: Time-out can be longer than 6 PWM cycles in direct PWM mode)	If 3 channels are already shut down, all channels will be shut down. Otherwise CH2-4 will remain as normal	Highest VF of CH2 through CH4
3	CH1 Open Circuit with infinite resistance	OTP not triggered and VCH1 < VSC	V <sub>OUT</sub> will ramp to OVP. CH1 will time-out after 6 PWM cycles and switch off. V <sub>OUT</sub> will drop to normal level.	CH2 through CH4 Normal	Highest VF of CH2 through CH4
4	CH1 Open Circuit with infinite resistance during operation	OTP triggered and VCH1 < VSC	All IC shut down		V <sub>OUT</sub> disabled
5	CH1 LED Open Circuit but has paralleled Zener	OTP not triggered and VCH1 < VSC	CH1 remains ON and has highest VF, thus V <sub>OUT</sub> increases	CH2 through CH4 ON, Q2 through Q4 burn power. CH2-4 will fault out if they reach VSC as a result of V <sub>OUT</sub> increase due to increase VF in CH1	VF of CH1
6	CH1 LED Open Circuit but has paralleled Zener	OTP not triggered but VCHx > VSC	CH1 remains ON and has highest VF, thus V <sub>OUT</sub> increases.	V <sub>OUT</sub> increases then CH-X switches OFF. This is an unwanted shut off and can be prevented by setting OVP at an appropriate level.	VF of CH1
7	Channel-to-Channel ΔVF too high	OTP triggered but VCHx < VSC	All channels switched off		V <sub>OUT</sub> disabled
8	Output LED string voltage too high	V <sub>OUT</sub> reaches OVP and not sufficient to regulate LED current	Driven with normal current. Any channel that is below the target current will time-out after 6 PWM cycles. (Note: Time-out can be longer than 6 PWM cycles in case direct PWM mode)		V <sub>OUT</sub> disabled
9	V <sub>OUT</sub> /SW shorted to GND		SW will not switch if started up in this condition. V <sub>OUT</sub> shorted to ground during operation will also cause the converter to shut down		

## Component Selections

According to the inductor Voltage-Second Balance principle, the change of inductor current during the power MOSFET switching on-time is equal to the change of inductor current during the power MOSFET switching off-time under steady state operation. The voltage across an inductor is shown in Equation 6:

$$V_L = L \times \Delta I_L / \Delta t \quad (\text{EQ. 6})$$

and  $\Delta I_L @ t_{ON} = \Delta I_L @ t_{OFF}$ , therefore:

$$(V_I - 0) / L \times D \times t_{sw} = (V_O - V_D - V_I) / L \times (1 - D) \times t_{sw} \quad (\text{EQ. 7})$$

where D is the switching duty cycle defined by the turn-on time over the switching period. V<sub>D</sub> is a Schottky diode forward voltage, which can be neglected for approximation. t<sub>sw</sub> is the switching period where t<sub>sw</sub> = 1/f<sub>sw</sub>, and the f<sub>sw</sub> is the switching frequency of the boost converter.

Rearranging the terms without accounting for V<sub>D</sub> gives the boost ratio and duty cycle respectively as Equations 8 and 9:

$$V_O / V_I = 1 / (1 - D) \quad (\text{EQ. 8})$$

$$D = (V_O - V_I) / V_O \quad (\text{EQ. 9})$$

## Input Capacitor

Switching regulators require input capacitors to deliver peak charging current and to reduce the impedance of the input supply. This reduces interaction between the regulator and input supply, thereby improving system stability. The high switching frequency of the loop causes almost all ripple current to flow in the input capacitor, which must be rated accordingly.

A capacitor with low internal series resistance should be chosen to minimize heating effects and improve system efficiency, such as X5R or X7R ceramic capacitors, which offer small size and a lower value of temperature and voltage coefficient compared to other ceramic capacitors.

During the normal continuous conduction mode of the boost converter, its input current flows continuously into the inductor; AC ripple component is only proportional to the rate of the inductor charging, thus, smaller value input capacitors may be used. It is recommended that an input capacitor of at least 10μF be used. Ensure the voltage rating of the input capacitor is suitable to handle the full supply range.



## Inductor

The selection of the inductor should be based on its maximum current ( $I_{SAT}$ ) characteristics, power dissipation, EMI susceptibility (shielded vs unshielded), and size. Inductor type and value influence many key parameters, including the inductor ripple current, current limit, efficiency, transient performance and stability.

The inductor's maximum current capability must be large enough to handle the peak current at the worst case condition. If an inductor core is chosen with a lower current rating, saturation in the core will cause the effective inductor value to fall, leading to an increase in peak to average current level, poor efficiency and overheating in the core. The series resistance, DCR, within the inductor causes conduction loss and heat dissipation. A shielded inductor is usually more suitable for EMI susceptible applications, such as LED backlighting.

The peak current can be derived from the voltage across the inductor during the off period, as expressed in Equation 10:

$$I_{L_{peak}} = (V_O \times I_O) / (85\% \times V_I) + 1/2 [V_I \times (V_O - V_I) / (L \times V_O \times f_{SW})] \quad (\text{EQ. 10})$$

The choice of 85% is just an average term for the efficiency approximation. The first term is the average current, which is inversely proportional to the input voltage. The second term is the inductor current change, which is inversely proportional to L and  $f_{SW}$ . As a result, for a given switching frequency, minimum input voltage must be used to calculate the input/inductor current as shown in Equation 10. For a given inductor size, the larger the inductance value, the higher the series resistance because of the extra number of turns required, thus, higher conductive losses. The ISL97687 current limit should be less than the inductor saturation current.

## Output Capacitors

The output capacitor acts to smooth the output voltage and supplies load current directly during the conduction phase of the power switch. Output ripple voltage consists of the discharge of the output capacitor during the FET turn-on period and the voltage drop due to load current flowing through the ESR of the output capacitor. The ripple voltage is shown in Equation 11:

$$\Delta V_{CO} = (I_O / C_O \times D / f_{SW}) + (I_O \times \text{ESR}) \quad (\text{EQ. 11})$$

where  $I_O$  represents the output current,  $C_O$  is the output capacitance, D is the duty ratio as described in Equation 9. ESR is the equivalent series resistance of the output capacitance and  $f_{SW}$  is the switching frequency of the converter. Equation 11 shows the importance of using a low ESR output capacitor for minimizing output ripple.

As shown in Equation 11, the output ripple voltage,  $\Delta V_{CO}$ , can be reduced by increasing the output capacitance,  $C_O$  or the switching frequency,  $f_{SW}$ , or using output capacitors with small ESR. In general, ceramic capacitors are the best choice for output capacitors in small to medium sized LCD backlight applications due to their cost, form factor, and low ESR.

The choice of X7R over Y5V ceramic capacitors is highly recommended because the X7R type capacitor is less sensitive to capacitance change overvoltage. Y5V's absolute capacitance

can be reduced to 10%~20% of its rated capacitance at the maximum voltage. Because of this, Y5V type ceramic capacitors should be avoided.

A larger output capacitor will also ease the driver response during PWM dimming off period due to the longer sample and hold effect of the output drooping. The driver does not need to boost as much on the next on period, which minimizes transient current. The output capacitor also plays an important role for system compensation.

## Channel Capacitor

It is recommended to use at least 1nF capacitors from CH pins to  $V_{OUT}$ . Larger capacitors will reduce LED current ripple at boost frequency, but will degrade transient performance at high PWM frequencies. The best value is dependant on PCB layout. Up to 4.7nF is sufficient for most configurations.

## Schottky Diode

A high speed rectifier diode is necessary to prevent excessive voltage overshoot, especially in the boost configuration. Low forward voltage and reverse leakage current will minimize losses, making Schottky diodes the preferred choice. Although the Schottky diode turns on only during the boost switch off period, it carries the same peak current as the inductor, therefore, a suitable current rated Schottky diode must be used.

## High Current Applications

Each channel of the ISL97687 can support up to 160mA. For applications that need higher current, multiple channels can be grouped to achieve the desirable current. For example, in Figure 27, the cathodes of the last LEDs can be connected to CH1/CH2 and CH3/CH4, this configuration can be treated as a single string with up to 350mA current driving capability.

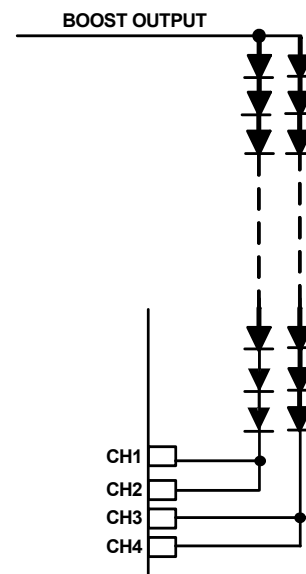


FIGURE 27. GROUPING MULTIPLE CHANNELS FOR HIGH CURRENT APPLICATIONS

## PCB Layout Considerations

### Two Layers PCB Layout with TQFN Package

Great care is needed in designing a PC board for stable ISL97687 operation. As shown in the typical application diagram (Figure 1, page 1), the separation of PGND and AGND of each ISL97687 is essential, keeping the AGND referenced only local to the chip. This minimizes switching noise injection to the feedback sensing and analog areas, as well as eliminating DC errors from high current flow in resistive PC board traces. PGND and AGND should be on the top and bottom layers respectively in the two layer PCB. A star ground connection should be formed by connecting the LED ground return and AGND pins to the thermal pad with 9-12 vias. The ground connection should be into this ground net, on the top plane. The bottom plane then forms a quiet analog ground area, that both shields components on the top plane, as well as providing easy access to all sensitive components. For example, the ground side of the ISET1/2 resistors can be dropped to the bottom plane, providing a very low impedance path back to the AGND pin, which does not have any circulating high currents to interfere with it. The bottom plane can also be used as a thermal ground, so the AGND area should be sized sufficiently large to dissipate the required power. For multi-layer boards, the AGND plane can be the second layer. This provides easy access to the AGND net, but allows a larger thermal ground and main ground supply to come up through the thermal vias from a lower plane.

This type of layout is particularly important for this type of product, as the ISL97687 has a high power boost, resulting in high current flow in the main loop's traces. Careful attention should be focussed on the below layout details:

1. Boost input capacitors, output capacitors, inductor and Schottky diode should be placed together in a nice tight layout. Keeping the grounds of the input, output, ISL97687 and the current sense resistor connected with a low impedance and wide metal is very important to keep these nodes closely coupled.
2. Figure 29 shows important traces of current sensor (RS) and OVP resistors (RU, RL). The current sensor track line should be short, so that it remains as close as possible to the Current Sense (CS) pin. Additionally, the CS pin is referenced from the adjacent PGND pin. It is extremely important that this PGND pin is placed with a good reference to the bottom of the sense resistor. In Figure 29 you can see that this ground pin is not connected to the thermal pad, but instead used to effectively sense the voltage at the bottom of the current sense resistor. However, this pin also takes the gate driver current, so it must still have a wide connection and a good connection back from the sense resistor to the star ground. Also, the RC filter on CS should be placed referenced to this PGND pin and be close to the chip.
3. If possible, try to maintain central ground node on the board and use the input capacitors to avoid excessive input ripple for high output current supplies. The filtering capacitors should be placed close by the VIN pin.
4. For optimum load regulation and true  $V_{OUT}$  sensing, the OVP resistors should be connected independently to the top of the output capacitors and away from the higher  $dv/dt$  traces. The

OVP connection then needs to be as short as possible to the pin. The AGND connection of the lower OVP components is critical for good regulation. At 70V output, a 100mV change at  $V_{OUT}$  translates to a 1.7mV change at OVP, so a small ground error due to high current flow, if referenced to PGND, can be disastrous.

5. The bypass capacitors connected to VDC and VLOGIC need to be as close to the pin as possible, and again should be referenced to AGND. This is also true for the COMP network and the rest of the analog components (on ISED1/2, FPWM, etc.).
6. The heat of the chip is mainly dissipated through the exposed thermal pad so maximizing the copper area around it is a good idea. A solid ground is always helpful for the thermal and EMI performance.
7. The inductor and input and output capacitors should be mounted as tight as possible, to reduce the audible noise and inductive ringing.

### General Power PAD Design Considerations

Figure 28 shows an example of how to use vias to remove heat from the IC. We recommend you fill the thermal pad area with vias. A typical via array would be to fill the thermal pad foot print with vias spaced such that the centre to centre spacing is three times the radius of the via. Keep the vias small, but not so small that their inside diameter prevents solder wicking through the holes during reflow.

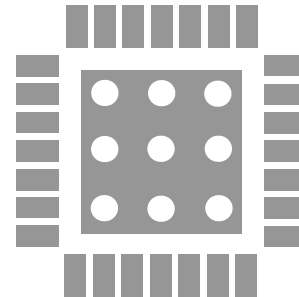


FIGURE 28. ISL97687 TQFN PCB VIA PATTERN

### One Layer PCB Layout with SOIC Package

The general rules of two layer PCB layout can be applied to the one layer PCB layout of the SOIC package, although this layout is much more challenging and very easy to get wrong. The noisy PGND of the switching FET area and quiet AGND must be placed on the same plane as shown in Figure 30, therefore, great care must be taken to maintain stable and clean operation, due to increased risk of noise injection to the quiet area.

1. The GND plane should be extended as far as possible as space allows to spread out heat dissipation.
2. All ground pads for input caps, current sensor, output caps should be close to the PGND pin adjacent to the CS pin of ISL97687 with wide metal connection shown in the Figure 30. This guarantees a low differential voltage between these critical points.
3. The connection point between AGND pin 14 and PGND pin 18 should be "Narrow" neck, effectively making a star ground at the AGND pin.

4. The relatively quiet AGND area, to the right of the neck needs to be traced out carefully in unbroken metal, via the shortest possible path to the ground side of the components connected to OVP, COMP, ISET, PWM\_SET/PLL, and ACTL. This is also true for the filtering caps on PWMI and STV. These are needed to reject noise and cause decoding errors in some conditions.
5. The current sensing line is shielded by a metal trace, coming from its source, to prevent pickup from the GD pin beside it.
6. The filtering cap of the current sensing line should be placed close to the CS pin rather than in the area of current sense resistor, as it needs to couple this pin to the adjacent PGND pin.
7. The noisy switching FET should be kept far away from the quiet pin area.
8. The area on the switching node should be determined by the dissipation requirements of the boost power FET.

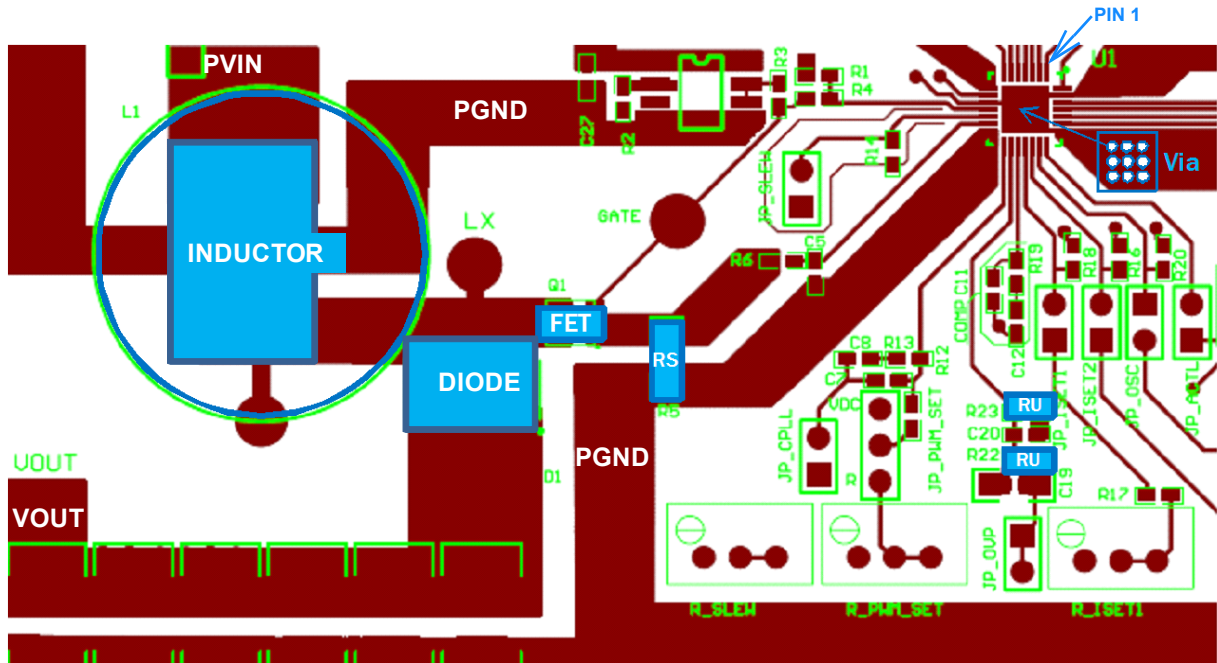


FIGURE 29. EXAMPLE OF TWO LAYER PCB LAYOUT

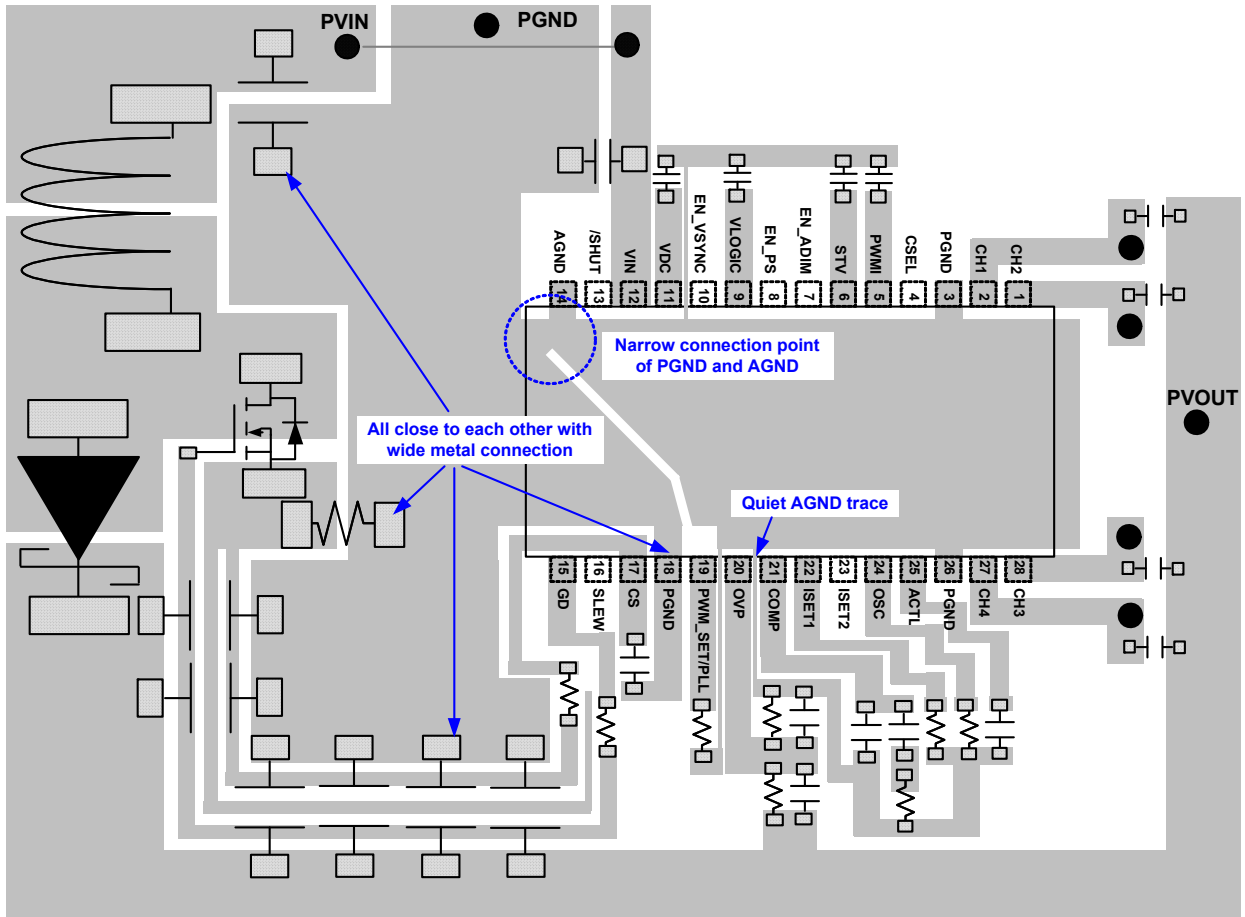
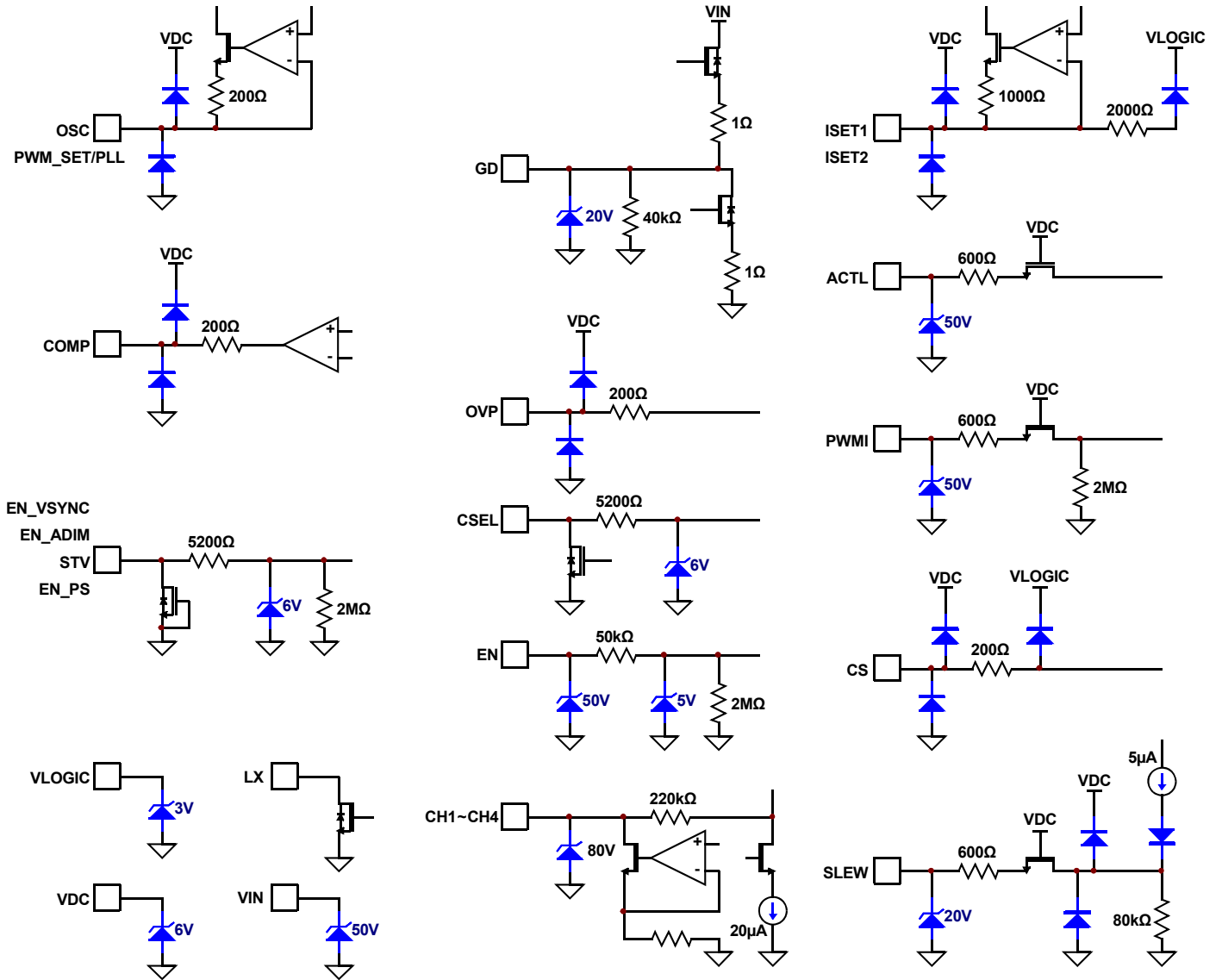


FIGURE 30. EXAMPLE OF ONE LAYER PCB LAYOUT

# Equivalent Circuit Diagrams



## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
September 13, 2017	FN7714.3	Applied new header/footer. Updated Ordering Information notes. Added V <sub>HEADROOM_RANGE</sub> spec to Electrical Specifications table. Added corresponding Note 11. In the Current Matching and Current Accuracy section - updated third sentence in paragraph 2 for clarification. Updated About Intersil section. Updated POD M28.3 to the latest revision. Change: Added land pattern
November 13, 2013	FN7714.2	Changed Eval Board name in ordering information on page 4 from "ISL97687IBZ-EVAL1Z" TO "ISL97687IBZEV1Z"
September 21, 2012	FN7714.1	Corrected PGND symbol in Figures 1 and 3. Corrected conditions for "VIH" in the "Electrical Specifications" table on page 7 from "Logic input low.." to "Logic input high.." Corrected label typo in Figure 20 from "RSET" to "RISET". Corrected "PWMI" and "CSEL" labels in the "Equivalent Circuit Diagrams" on page 21. Added Note 8 and corrected Note reference in "Thermal Information" on page 6 for SOIC from Note 5 to Note 8. Corrected I <sub>CH1</sub> to V <sub>CH1</sub> in Figures 16 and 17 on page 10. Corrected FPWM pin to PWM_SET/PLL pin in first paragraph of "V <sub>sync</sub> Function" on page 13 Added "The PWM dimming frequency, set by the PWM_SET pin, should be at least 1kHz when EN_ADIM is high." to second paragraph of "LED PWM Dimming – Duty Cycle Control" on page 12.
September 15, 2011	FN7714.0	Initial Release

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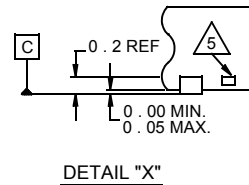
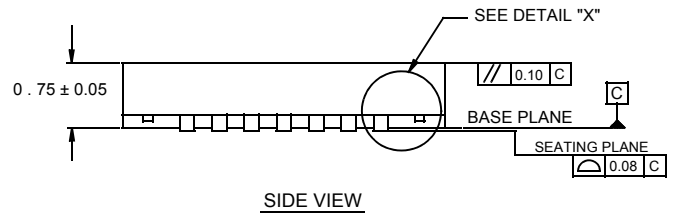
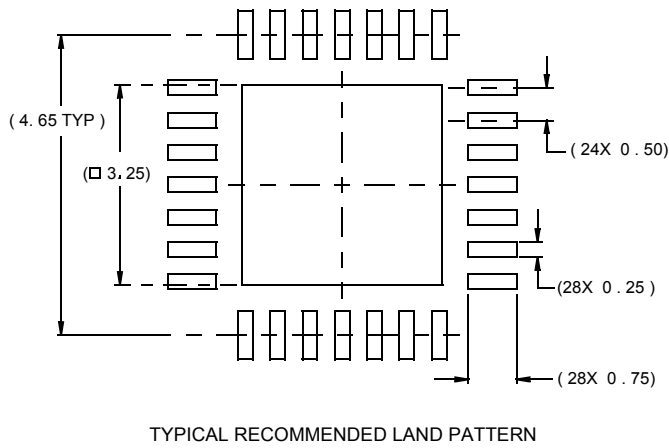
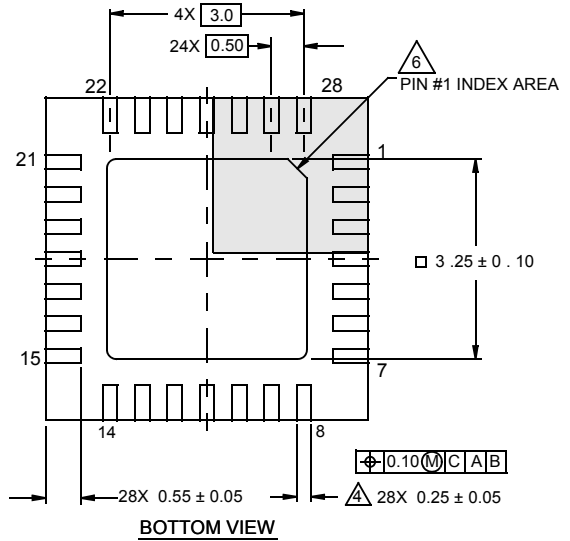
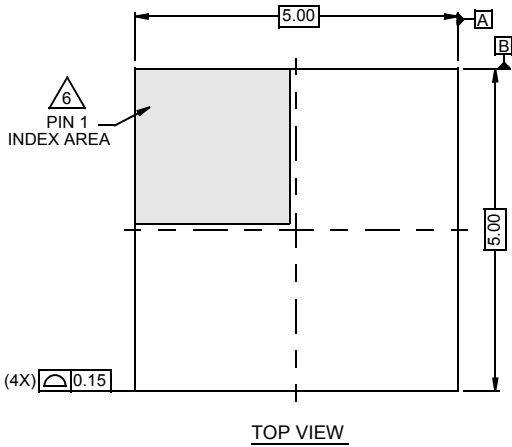
# Package Outline Drawings

For the most recent package outline drawing, see [L28.5x5B](#).

## L28.5x5B

28 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 1, 10/07

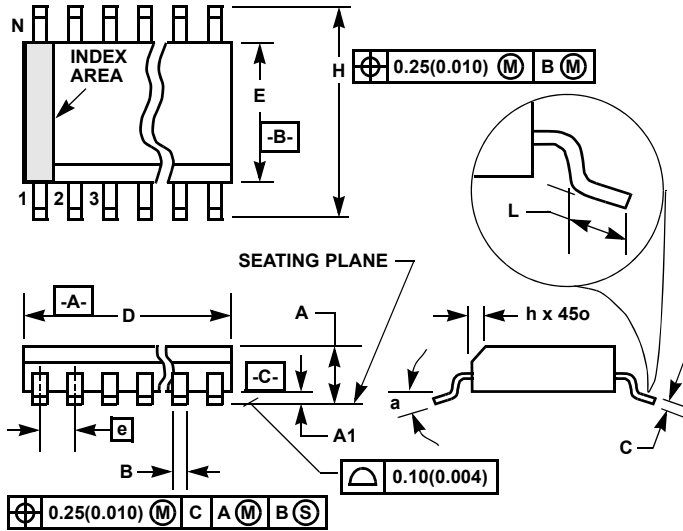


**NOTES:**

1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

**Small Outline Plastic Packages (SOIC)**

For the most recent package outline drawing, see [M28.3](#).



**M28.3 (JEDEC MS-013-AE ISSUE C)  
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
$\alpha$	0°	8°	0°	8°	-

Rev. 1, 1/13

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

**TYPICAL RECOMMENDED LAND PATTERN**

