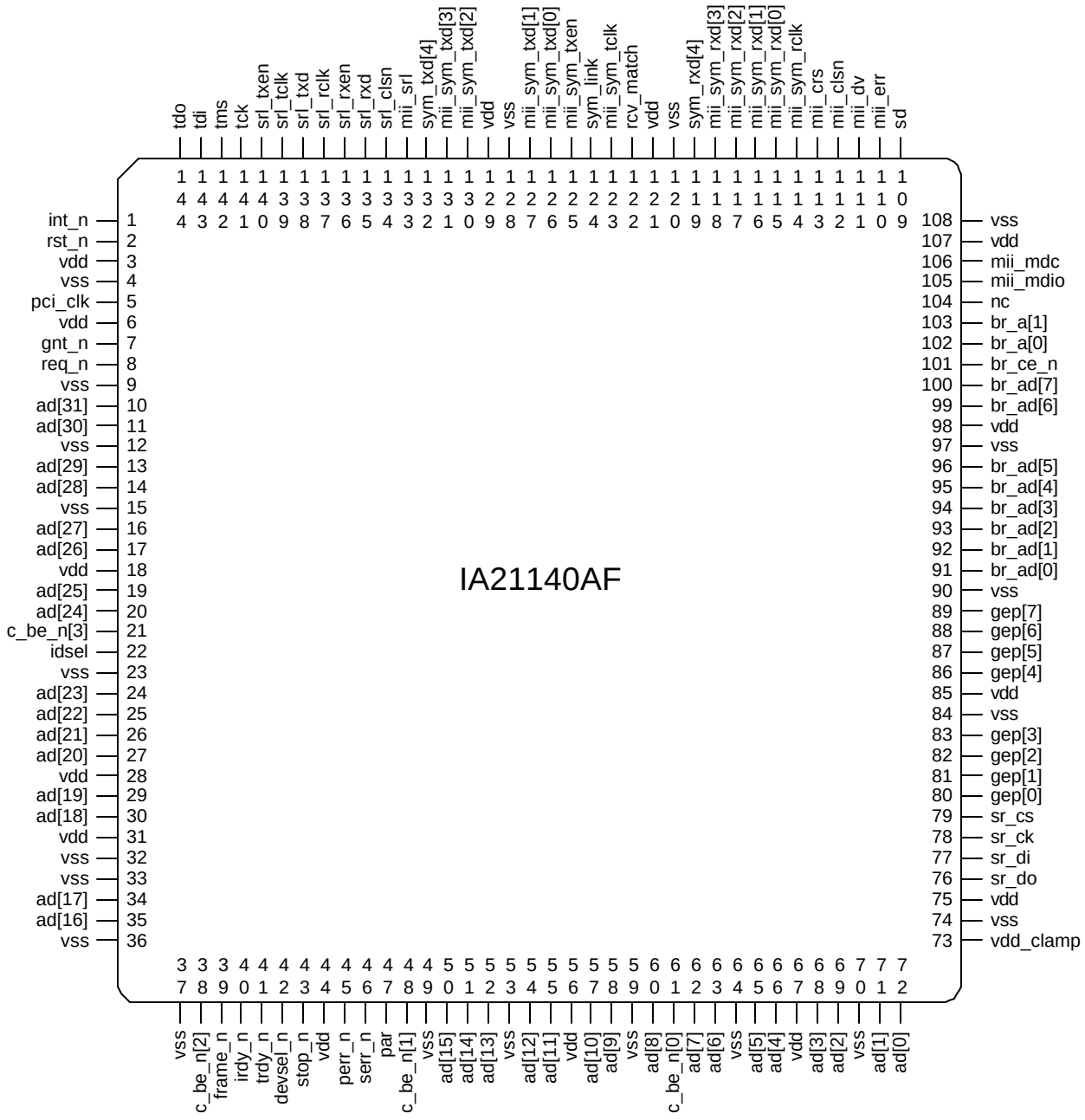
Features

- **Form, Fit and Function Compatible with the DECÔ 21140AF**
- **Available in 144 Pin PQFP Package**
- **Integrated Ethernet controller with PCI bus interface**
- **Supports 10 Mb/s and 10/100 Mb/s network interface**
- **PCS and scrambler/descrambler circuitry on chip**
- **Supports multiple PCI features:**
  - Unlimited PCI burst
  - PCI read multiple
  - PCI write and invalidate
  - PCI read line
  - PCI 5.0V and 3.3V environments
- **Multiple interrupt sources**
- **Contains two independent 3K FIFOs to minimize external memory additions**
- **Provides sleep or snooze low-power modes**
- **Interfaces with MicroWireä Serial ROM**
- **Provides a JTAG test port with boundary scan function**
- **Complies with IEEE 802.3, ANSI 8802-3, and Ethernet standards**

The IA21140AF is a "plug-and-play" drop-in replacement for the original IC. innovASIC produces replacement ICs using its MILES™, or Managed IC Lifetime Extension System, cloning technology. This technology produces replacement ICs far more complex than "emulation" while ensuring they are compatible with the original IC. MILES™ captures the design of a clone so it can be produced even as silicon technology advances. MILES™ also verifies the clone against the original IC so that even the "undocumented features" are duplicated. This data sheet documents all necessary engineering information about the IA21140AF including functional and I/O descriptions, electrical characteristics, and applicable timing.

Package Pinout

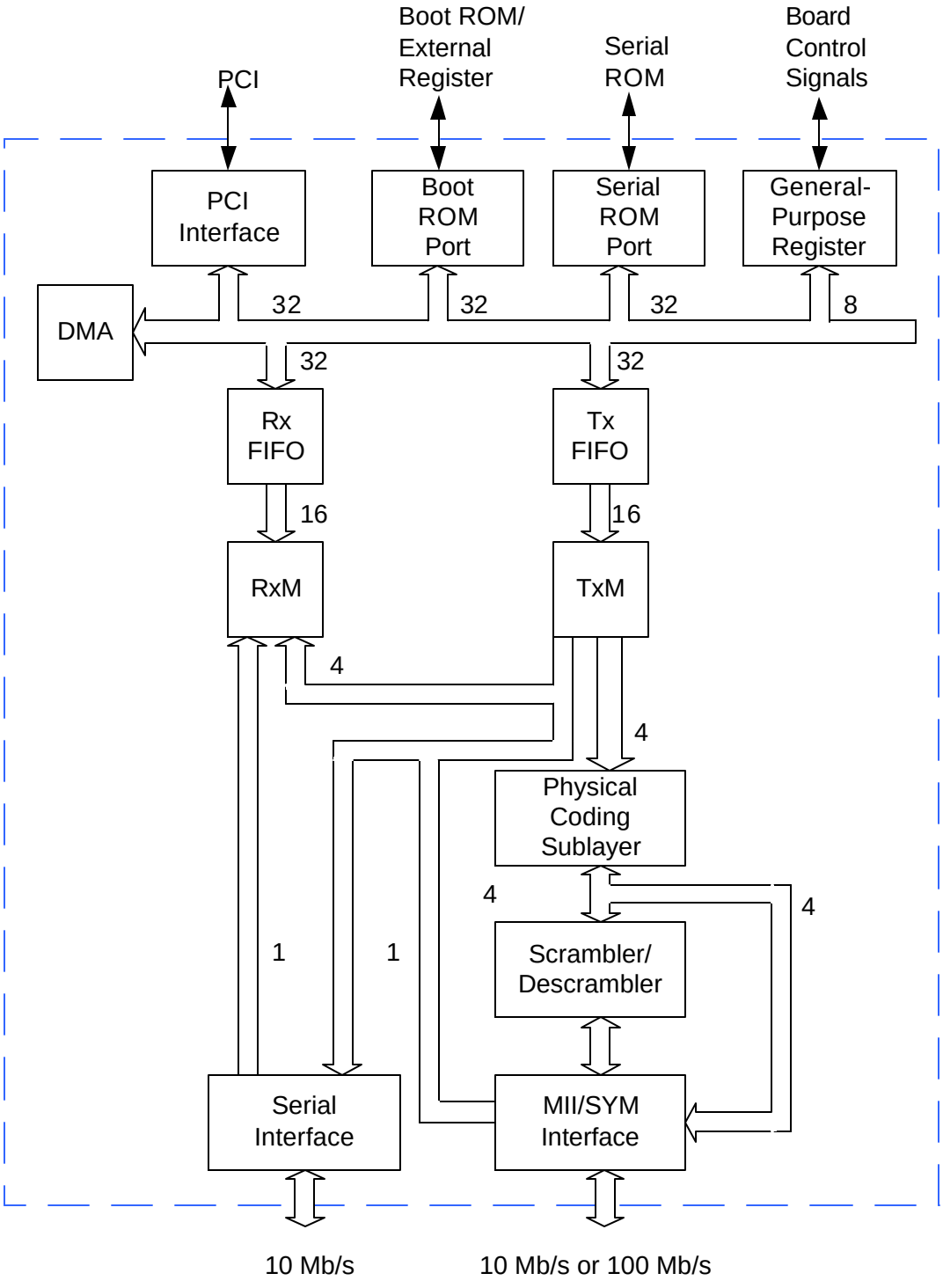


Description

The innovASIC IA21140AF Fast Ethernet LAN controller provides a direct interface connection to the PCI (Peripheral Component Interface) bus. It interfaces with the PCI bus by using on-chip control and status registers (CSR's), and a shared CPU memory area. The memory is initialized once during setup to minimize CPU overhead during normal operation. Large receive and transmit FIFO's are contained on-chip so no additional on board memory is required. The IA21140AF includes two on chip direct memory access (DMA) controllers with programmable burst size providing for low CPU utilization. A PCI clock frequency from dc to 33 MHz (20-33 MHz for operational network interface) is supported. Two network ports are supported. A serial standard 7-wire 10-Mbps port (SRL) and a media independent interface/symbol 10/100-Mbps port (MII/SYM). The 10 Mbps implements a direct interface to the external 10 Mbps front-end decoder (ENDEC). The 10/100 Mbps port supports two modes. The first is a 100BASE-X physical coding sublayer (PCS). The second is a full implementation of the MII standard. The IA21140AF functions in a full-duplex environment for either network port.

System Block Diagram

This block below illustrates the major functions of the IA21140AF.



I/O Description

The following section provides a functional description of the I/O pins on the IA21140AF.

NAME	Type	Description
Vdd	P	3.3 volt input supply voltage.
Vdd_clamp	P	5.0 volt reference for 5.0 volt signaling environments and 3.3 volt reference for 3.3 volt signaling environments.
Vss	P	Ground Pin
ad[31:0]	I/O	The PCI address and data lines are multiplexed on the same PCI pins. During the first clock cycle of a transaction, the 32 bits contain an address and during subsequent clock cycles, they contain data. Both read and write bursts are supported in master operation only. Big or Little Indian byte ordering can be used.
br_a[1:0]	O	Address line bit 0 also carries in two consecutive address cycles (bits 16 and 17) in a 256KB configuration. Bit 1 also latches the boot ROM address and control lines via two external latches.
br_ad[7:0]	I/O	In the first of two consecutive address cycles, these multiplexed lines contain the boot ROM address bits [7:2], oe_n, and we_n. The second cycle contains boot ROM address bits [15:8]. Bits 7 through 0 contain data during the data cycle. These lines are used to carry data to and from the external register.
br_ce_n	O	Enable pin for the Boot ROM or an external register. Pin has an internal 5 k O pull-up resistor.
c_be_n[3:0]	I/O	Bus command and byte enable are multiplexed on the same PCI pins. These bits provide the bus command during the address phase of the transaction. They provide the byte enable during the data phase. Byte enable determines which byte lines carry valid data. Bit 0 coincides with byte 0. Bit 1 coincides with byte 1, etc.
devsel_n	I/O	Indicates that the driving device has decoded its address as the target of the current access. As an input, determines whether a device on the bus has been selected.
frame_n	I/O	The IA21140AF bus master asserts this signal to indicate the beginning and duration of a bus transaction access. Data transfer continues while this signal is asserted. Deasserting this signal indicates the transaction is in the final phase.
gep[7:0]	I/O	These pins can be configured by software to perform either input or output functions for system specific applications.
gnt_n	I	Indicates to the IA21140AF that access to the bus has been granted.
Idsel	I	Used as a chip select by the host to indicate configuration read and write cycles.
int_n	O/D	When one of the appropriate bits in CSR5 gets set, interrupt request gets asserted if the corresponding mask bit in CSR7 is not set. If more than one interrupt bit in CSR5 is set and all input bits are not cleared, interrupt request gets deasserted for one clock cycle. Interrupt request gets deasserted by writing a “1” into the appropriate CSR5 bit. This pin must be pulled up by an external resistor.

NAME	Type	Description
irdy_n	I/O	When the IA21140AF is the bus master, this signal is asserted during write operations indicating valid data is present on the 32-bit ad bus. It is asserted during read operations to indicate the master is ready to accept data. It is asserted during a write to indicate that valid data is on the AD lines. A data phase is completed on any rising edge of the clock when both irdy_n and trdy_n are asserted. Wait cycles are inserted until both these signals are asserted together.
mii_clsn	I	When an external physical layer protocol (PHY) device detects a collision, it asserts this signal.
Carrier sense mii_crs	I	The PHY sets this bit when the media is active.
mii_dv	I	An external PHY sets this bit when receive data is on the mii_sym_rxd lines and is cleared at the end of the packet. This signal is synchronized with mii_sym_rclk.
mii_err	I	When a data decoding error is detected by an external PHY device, this pin gets set. It is synchronized to mii_sym_rclk and can be set for a minimum of one receive clock. It sets the cyclic redundancy check (CRC) error bit in the receive descriptor (RDES0) when it is set during a packet reception.
mii_mdc	O	Goes to the PHY devices as timing reference for the transfer of information on the mii_mdio signal.
mii_mdio	I/O	Transfers control information and status between the IA21140AF and PHY.
mii_srl	O	Set when the MII/SYM port is selected. Cleared when the SRL port is selected.
mii_sym_rclk	I	This clock, recovered by the PHY, supports either the 25 MHz or 2.5 MHz receive clock.
mii_sym_rxd[3:0]	I	When MII mode is selected, these four parallel data lines receive data that is driven by external PHY that attached the media. Synchronized to the mii_sym_rclk signal.
mii_sym_tclk	I	This 25 MHz or 2.5 MHz transmit clock is supplied by the external physical layer medium dependent device (PMD) and must always be active.
mii_sym_txd[3:0]	O	These four parallel transmit data lines are synchronized and latched by the external PHY on the rising edge of the mii_sym_tclk signal.
mii_txen	O	This signal indicates a transmit to an external PHY device. It reflects the transmit activity of the MAC sublayer when in the PCS mode (CSR6[23]).
Nc	O	No connection pins
Par	I/O	Even parity bit for the 32-bit ad bus and the 4-bit c_be_n lines. It is driven by the master for address and write data phases and driven by the target for read data phases.
pci_clk	I	Timing of the PCI related functions is based on this DC to 33 MHz clock. All bus signals except int_n and rst_n are sampled on the rising edge of this clock.
perr_n	I/O	Used for reporting data parity errors during all PCI transactions except a special cycle.
rcv_match	O	Set when a received packet passes address recognition.
req_n	O	Request to the bus arbiter for the IA21140AF to use the bus.
rst_n	I	When asserted for at least 10 PCI clock cycles, the IA21140AF is reset to its initial state. PCI output pins are tristated and all PCI O/D signals are left floating.
sd	I	Supplied by an external PMD device.

NAME	Type	Description
serr_n	O/D	Reports errors other than parity. Signal must be valid for at least one clock cycle. This pin pulled up by an external resistor.
sr_ck	O	Serial ROM clock.
sr_cs	O	Serial ROM chip-select pin pulled down by an internal 2 k O resistor.
sr_di	O	Serial ROM data-in.
sr_do	I	Serial ROM data-out pin pulled up by an internal 5 k O resistor.
srl_clsn	I	Indicates a collision occurrence on the Ethernet cable to the IA21140AF. Asserted and deasserted asynchronously by the external ENDEC with respect to the receive clock.
srl_rclk	I	Carries the recovered receive clock supplied by an external ENDEC. May be inactive during idle periods.
srl_rxd	I	Carries the input receive data from the external ENDEC. Incoming data should be synchronous with receive clock (srl_rclk) signal.
srl_rxen	I	Set when receive data is present on the Ethernet cable and cleared at the end of a frame. Set and cleared asynchronously to the receive clock by the external ENDEC.
srl_tclk	I	Carries the transmit clock supplied by an external ENDEC. Must be always active, even during reset.
srl_txd	O	Carries the serial output data from the IA21140AF and is synchronized to transmit clock signal.
srl_txen	O	Signals an external ENDEC that the IA21140AF transmit is in progress.
stop_n	I/O	The current target is requesting the bus master to stop the current transaction.
sym_link	O	Descrambler is locked to the input data signal.
sym_rxd[4]	I	This signal and the four receive lines mii_sym_rxd[3:0], provide five parallel data lines in symbol form for use in PCS mode. Data is driven by an external PMD device and is synchronized with respect to the mii_sym_rclk signal.
sym_txd[4]	O	This signal and the four transmit lines mii_sym_txd[3:0], provide five parallel data lines in symbol form for use in PCS mode. Data is synchronized on the rising edge of mii_sym_tclk.
tck	I	During JTAG test operations this clock shifts state information and test data into and out of the IA21140AF. The pin should not be left unconnected.
Tdi	I	During JTAG test operations this pin serially shifts test data and instruction into the IA21140AF. The pin is pulled up by an internal 5 k O resistor and should not be left unconnected.
tdo	O	During JTAG test operations this pin serially shifts test data and instructions out of the IA21140AF.
tms	I	Controls the state operation of JTAG testing in the IA21140AF. The pin is pulled up by an internal 5 k O resistor and should not be left unconnected.
trdy_n	I/O	Indicates the readiness of the target's agent to complete the current data phase of the transaction. During reads, this signal indicates that valid data is present on AD lines. During writes, this signal indicates the target is ready to accept data. A data phase is completed on any clock when both irdy_n and trdy_n are set.

AC/DC Parameters

DC Characteristics

Absolute Max Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage (3.3V)	3	3.6	V
V_{DD}	Supply Voltage (5V)	4.75	5.25	V
T_A	Ambient Temperature (Commercial)	0	70	°C
T_J	Junction Temperature (Commercial)	0	85	°C
	Storage Temperature	-55	125	°C

CMOS Input Specifications (3.0V < VDD < 3.6V; 0°C < T < 70°C)

Symbol	Parameter	Min	Max	Unit
Vil	Low level input voltage	-	$0.3*V_{DD}$	V
Vih	High level input voltage	$0.7*V_{DD}$	-	V
Lil	Low level input current	-	-1	µA
Iih	High level input current	-	1	µA
Iil	Input pull-up current	-27	-75	µA
Iih	Input pull-down current	35	112	µA
Vt-	Schmitt negative threshold	$0.2*V_{DD}$	-	V
Vt+	Schmitt positive threshold	-	$0.8*V_{DD}$	V
Vh	Schmitt hysteresis	0.8	-	V

TTL Input Specifications (3.0V < VDD < 3.6V; 0°C < T < 70°C)

Symbol	Parameter	Min	Max	Unit
Vil	Low level input voltage	-	0.8	V
Vih	High level input voltage	2	-	V
Lil	Low level input current	-	-1	µA
Iih	High level input current	-	1	µA
Iil	Input pull-up current	-27	-75	µA
Iih	Input pull-down current	35	112	µA
Vt-	Schmitt negative threshold	0.7	-	V
Vt+	Schmitt positive threshold	-	2.1	V
Vh	Schmitt hysteresis	0.4	-	V

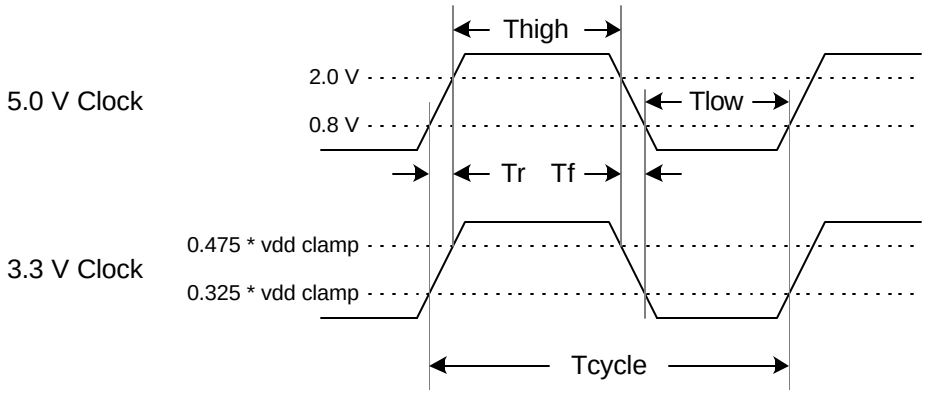
Output Operating Specifications (3.0V <VDD <3.6V; 0°C < T < 70°C)

Driver	Vol Max (V)	Voh Min (V)	Iol Max (mA)	Ioh Max (mA)
1 mA Driver	0.4	2.4	1	-1
2 mA Driver	0.4	2.4	2	-2
4 mA Driver	0.4	2.4	4	-4
8 mA Driver	0.4	2.4	8	-8
16 mA Driver	0.4	2.4	16	-16

AC Characteristics

PCI Clock:

Timing Diagram

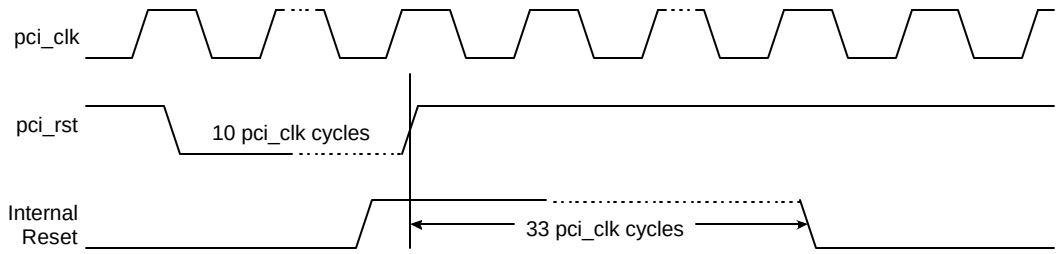


PCI Clock Specification Timing Characteristics

Symbol	Parameter	Min	Max	Unit
Tcycle	Cycle time	30	50	ns
Thigh	pci_clk high time	11	-	ns
Tlow	pci_clk low time	11	-	ns
Tr	pci_clk slew rate	1	4	V/ns
Tf	pci_clk slew rate	1	4	V/ns

PCI Reset:

Timing Diagram

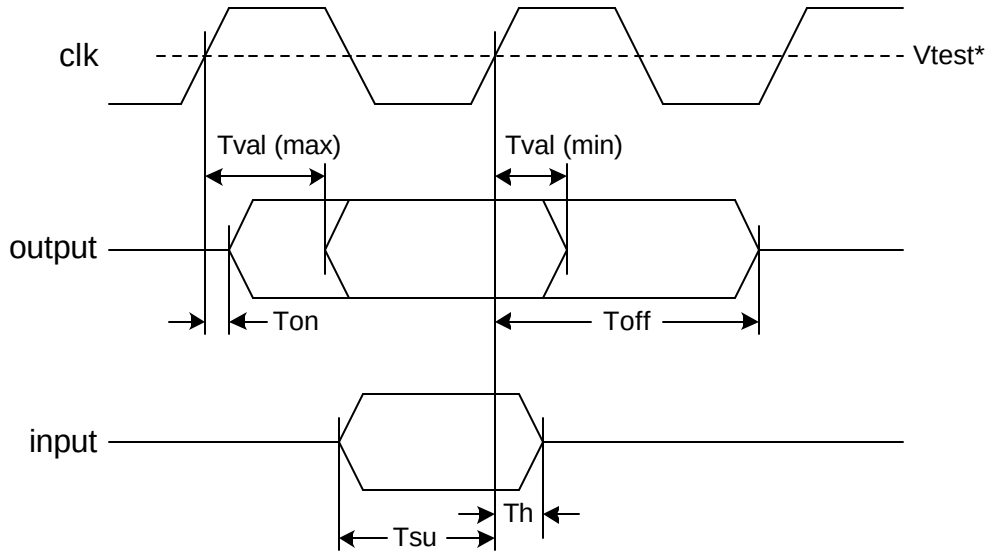


Timing Characteristics

Symbol	Parameter	Min	Max	Conditions
Trst	pci_rst pulse width	10 * Tcycle	Not applicable	pci_clk active

PCI Other Signals:

Timing Diagram



Note: Vtest is 1.5 V in a 5.0 V signaling environment and is 0.4 * vdd_clamp in a 3.3 V signaling environment.

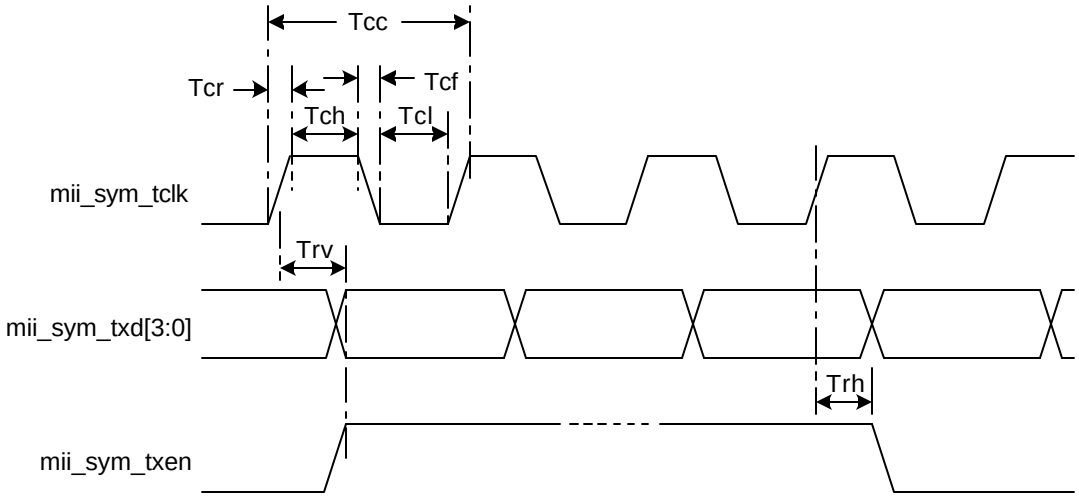
Timing Characteristics

Symbol	Parameter	Min	Max	Unit
Tval	clk-to-signal valid delay	2	11	ns
Ton	Float-to-active delay from clk	2	-	ns
Toff	Active-to-float delay from clk	-	28	ns
Tsu	Input signal valid setup time before clk	7	-	ns
Th	Input signal hold time from clk	0	-	ns

MII/SYM Port Timing Waveforms:

Transmit:

Timing Diagram



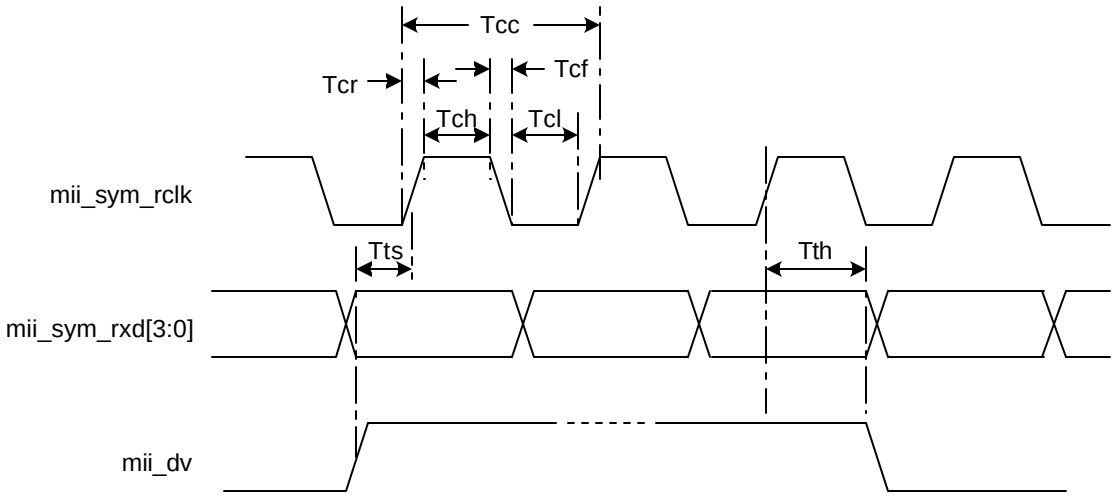
Timing Characteristics

Symbol	Definition	Min*	Typ*	Max*	Units
Tcc	mii_sym_tclk cycle time (±50 ppm)	-	40t	-	ns
Tch	mii_sym_tclk high time	14t	-	26t	ns
Tcl	mii_sym_tclk low time	14t	-	26t	ns
Tcr	mii_sym_tclk rise time	-	8	-	ns
Tcf	mii_sym_tclk fall time	-	8	-	ns
Trv	mii_ tclk rise to mii_txen valid time or mii_sym_tclk rise to mii_sym_txd valid time	-	-	20	ns
Trh	mii_txen hold after mii_tclk rise time	5	-	-	ns

- t = 1 for 100 Mbps operation and t = 10 for 10 Mbps operation.

Receive:

Timing Diagram



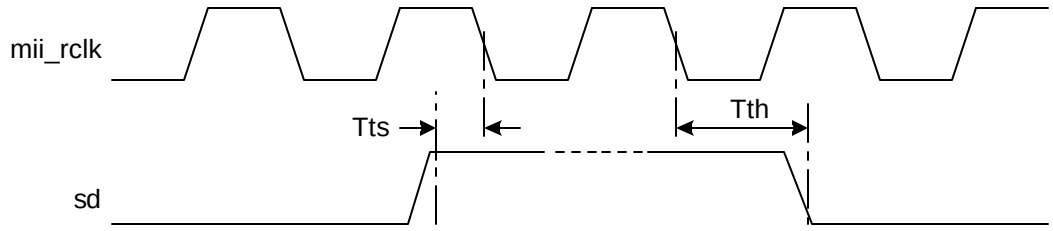
Timing Characteristics

Symbol	Definition	Min*	Typ*	Max*	Unit
Tcc	mii_sym_rclk cycle time (±50 ppm)	-	40t	-	ns
Tch	mii_sym_rclk high time	14t	-	26t	ns
Tcl	mii_sym_rclk low time	14t	-	26t	ns
Tcr	mii_sym_rclk rise time	-	8	-	ns
Tcf	mii_sym_rclk fall time	-	8	-	ns
Tts	mii_sym_rxd setup (both rise and fall) to mii_sym_rclk rise time or mii_dv setup (both rise and fall) to mii_rclk rise time	8	-	-	ns
Tth	mii_sym_rxd hold (both rise and fall) after mii_sym_rclk rise time or mii_dv hold (both rise and fall) after mii_rclk rise time.	10	-	-	ns

* t = 1 for 100 Mbps operation and t = 10 for 10 Mbps operation.

Receive Error:

Timing Diagram

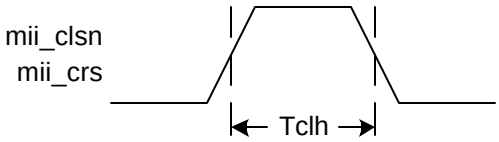


Timing Characteristics

Symbol	Definition	Min	Max	Units
Tts	mii_err setup (both rise and fall) to mii_rclk rise time	10	-	ns
Tth	mii_err hold (both rise and fall) after mii_rclk rise time.	10	26t	ns

Collision and Carrier Sense:

Timing Diagram



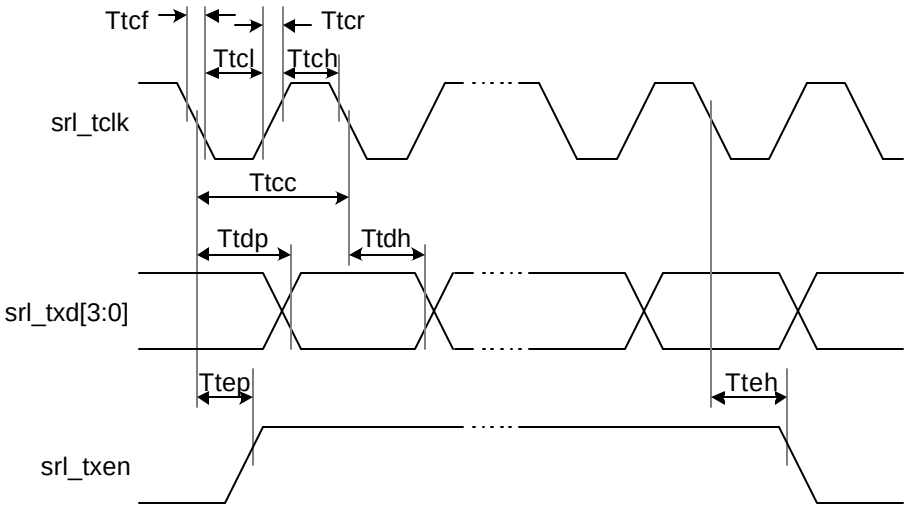
Timing Characteristics

Symbol	Definition	Min	Max	Units
Tclh	Mii_crs, mii_clsn high time	20	-	ns

Serial Port Timing Waveforms:

Transmit:

Timing Diagram

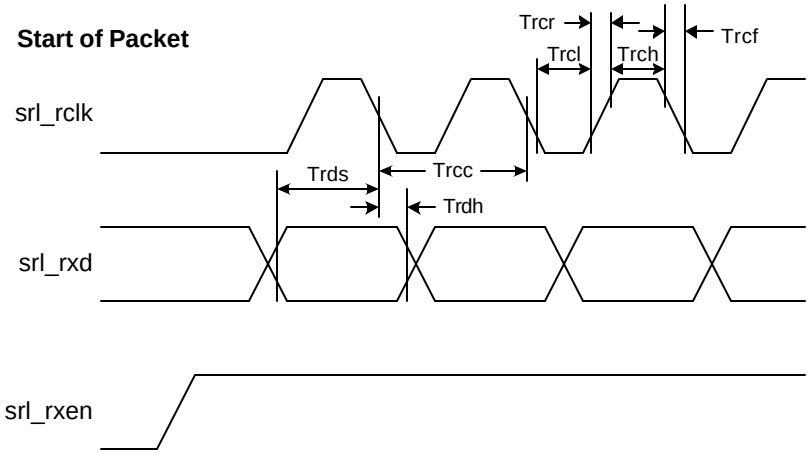


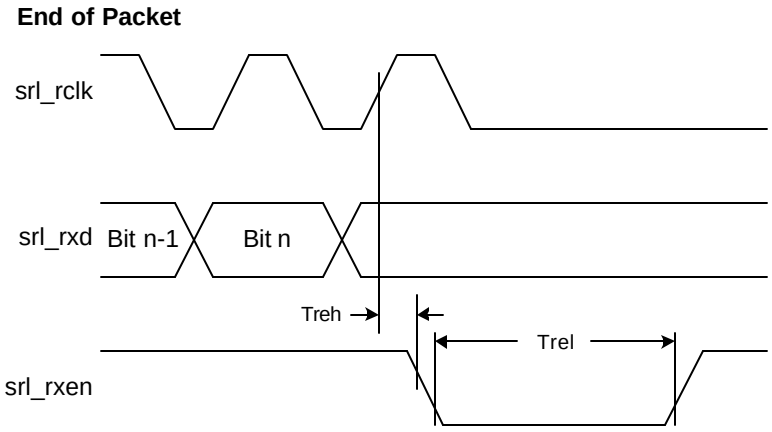
Timing Characteristics

Symbol	Definition	Min	Max	units
Ttcl	srl_tclk low time	45	55	ns
Ttch	srl_tclk high time	45	55	ns
Ttcr	srl_tclk rise time	-	8	ns
Ttcf	srl_tclk fall time	-	8	ns
Ttdp	srl_tclk fall time to srl_txd valid	-	26	ns
Ttdh	srl_txd hold after srl_tclk fall time	5	-	ns
Ttep	srl_tclk fall time to srl_txen valid	-	26	ns
Tteh	srl_txen hold after srl_tclk fall time	5	-	ns

Receive:

Timing Diagram



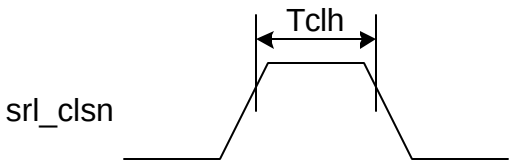


Timing Characteristics

Symbol	Definition	Min	Max	Units
Trcc	srl_rclk cycle time	85	118	ns
Trcl	srl_rclk low time	38	80	ns
Trch	srl_rclk high time	38	80	ns
Trcr	srl_rclk rise time	-	8	ns
Trcf	srl_rclk fall time	-	8	ns
Trds	srl_rxd setup to srl_rclk fall time	10	-	ns
Trdh	srl_rxd hold after srl_rclk fall time	5	-	ns
Trel	srl_rxen low time	120	-	ns
treh	srl_rxen hold after srl_rclk rise time	10	100	ns

Collision:

Timing Diagram



Timing Characteristics

Symbol	Definition	Min	Max	Units
Tclh	srl_clsn high time	20	-	ns

Ordering Information

Order Number	Environment	Package Type
IA21140AF-PQF144I	Industrial	144 Pin Plastic Quad Flat Package

Cross Reference to Original Manufacturer Part Numbers:

innovASIC Part Number	DEC Part Number
IA21140AF-PQF144I	❑ 21140-AA
	❑ 21140-AE
	❑ 21140-AF