AN4164
Application note

STEVAL-ISA113V1: 12 V/4 W, 115 kHz non-isolated flyback

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Introduction

This document describes a 12 V-350 mA power supply set in non-isolated flyback topology with the new VIPer06 offline high voltage converter by STMicroelectronics.

The features of the device are:

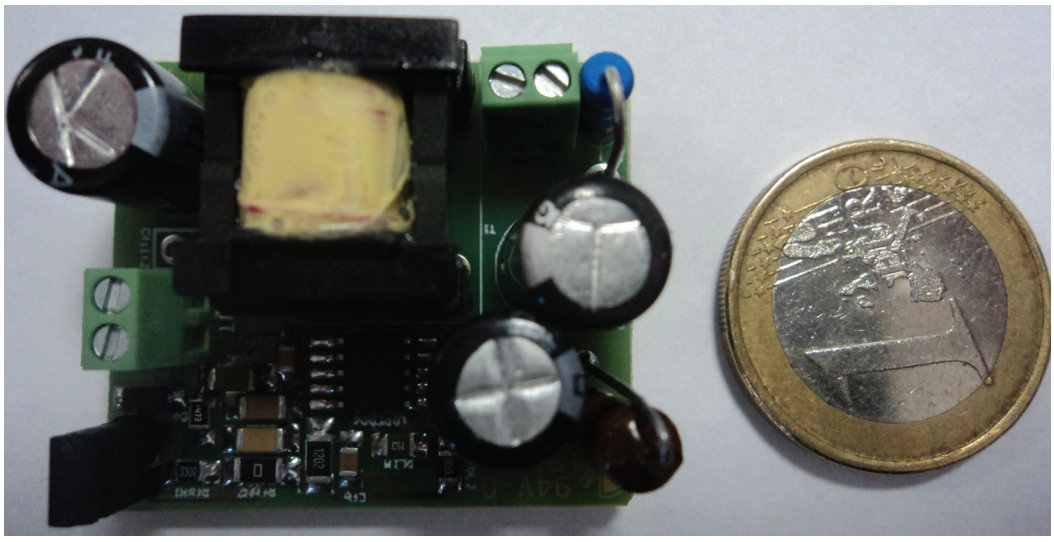
- 800 V avalanche rugged power section
- PWM operation at 115 kHz with frequency jittering for lower EMI
- Limiting current with adjustable set point
- Onboard soft-start
- Safe auto-restart after a fault condition (overload, short-circuit)
- SSO-10 package

Moreover, the VIPER06 does not require a biasing circuit to operate because the IC can be supplied by an internal current generator, therefore saving the cost of the transformers auxiliary winding (self-biasing). If the device is biased through an auxiliary winding or through a diode connected to the output (external biasing), it can reach very low standby consumption (< 50 mW at 265 V_{AC}).

Both cases are treated in the present document.

The available protection features are: thermal shutdown with hysteresis, delayed overload protection, and open loop failure protection (the last is available only if the IC is externally biased).

Figure 1. Demonstration board image



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1 Adapter features

The electrical specifications of the demonstration board are listed in *Table 1*.

Table 1. Electrical specifications

Parameter	Symbol	Value
Input voltage range	V_{IN}	[90 V_{AC}; 265 V_{AC}]
Output voltage	V_{OUT}	12 V
Max. output current	I_{OUT}	0.35 A
Precision of output regulation	ΔV_{OUT_LF}	± 5%
High frequency output voltage ripple	ΔV_{OUT_HF}	50 mV
Max. ambient operating temperature	T_{AMB}(1)	30 °C (self biasing)
		60 °C (external biasing)

1. see *Section 2: Circuit description*

2 Circuit description

The power supply is set in flyback topology. The schematic is given in *Figure 2*, and the bill of material in *Table 2*. The input section includes a resistor R0 for inrush current limiting, a diode bridge (D0) and a Pi filter for EMC suppression (Cin1, Lin, Cin2). The transformer core is a standard E13. The output voltage value is set in a simple way through the RfbH-RfbL voltage divider between the output terminal and the FB pin, according to the following formula:

Equation 1

$$V_{OUT} = 3.3V \cdot \left(1 + \frac{RfbH}{RfbL}\right)$$

In fact, the FB pin is the input of an error amplifier and is an accurate 3.3 V voltage reference. In the schematic the upper resistor RfbH has been split into RfbH1 and RfbH2; and the lower resistor RfbL into RfbL1 and RfbL2 in order to allow a better tuning of the output voltage value. The compensation network is connected between the COMP pin (which is the output of the error amplifier) and the GND pin, and is made up of Cp, Cc and Rc.

The resistor RLIM, placed between the LIM and GND pins, has the purpose of reducing the drain current limitation, from IDLIM to about 250 mA in order to limit the deliverable output power of the converter and keep safe the power components. At power-up, as the rectified input voltage rises over the $V_{DRAINSTART}$ threshold, the high voltage current generator starts charging the V_{DD} capacitor, CVDD, from 0 V up to V_{DDon}. At this point the Power MOSFET starts switching, the HV current generator is turned off and the IC is biased by the energy stored in CVDD.

In this demonstration board, if the jumper J1 is not selected, the IC is biased through the internal high-voltage startup current generator, which is automatically turned on as the V_{DD} voltage drops down to V_{DDCSon} and switched off as V_{DD} is charged up to V_{DDon} (self-biasing).

Self-biasing is excluded by keeping the V_{DD} pin voltage always above the V_{DDCSon} threshold. In this board, since the output voltage is higher than V_{DDCSon}, this is obtained by just selecting the jumper J1, which connects the output terminal to the V_{DD} pin through a small signal diode. If the output voltage is lower than V_{DDCSon}, the self-biasing can be excluded only using an auxiliary winding. The IC biasing through auxiliary winding or through the output is referred to as external biasing. In *Figure 3* the V_{DD} waveforms for both cases (IC external biased and self-biased) are shown.

The use of self-biasing means higher power dissipation across the IC (which must be avoided if low standby consumption and/or high efficiency is required) and higher IC temperature respect to external biasing (at given ambient temperature, the maximum deliverable output power is lower; or, a lower maximum ambient temperature is required to deliver the same power throughput).

For this reason, two different maximum T_{AMB} values, in full load condition, are indicated in *Table 1*, depending on the selection of weather self biasing or external biasing. These values are confirmed by the thermal measurements reported in *Section 8*.

3 Schematic and bill of material

Figure 2. Application schematic

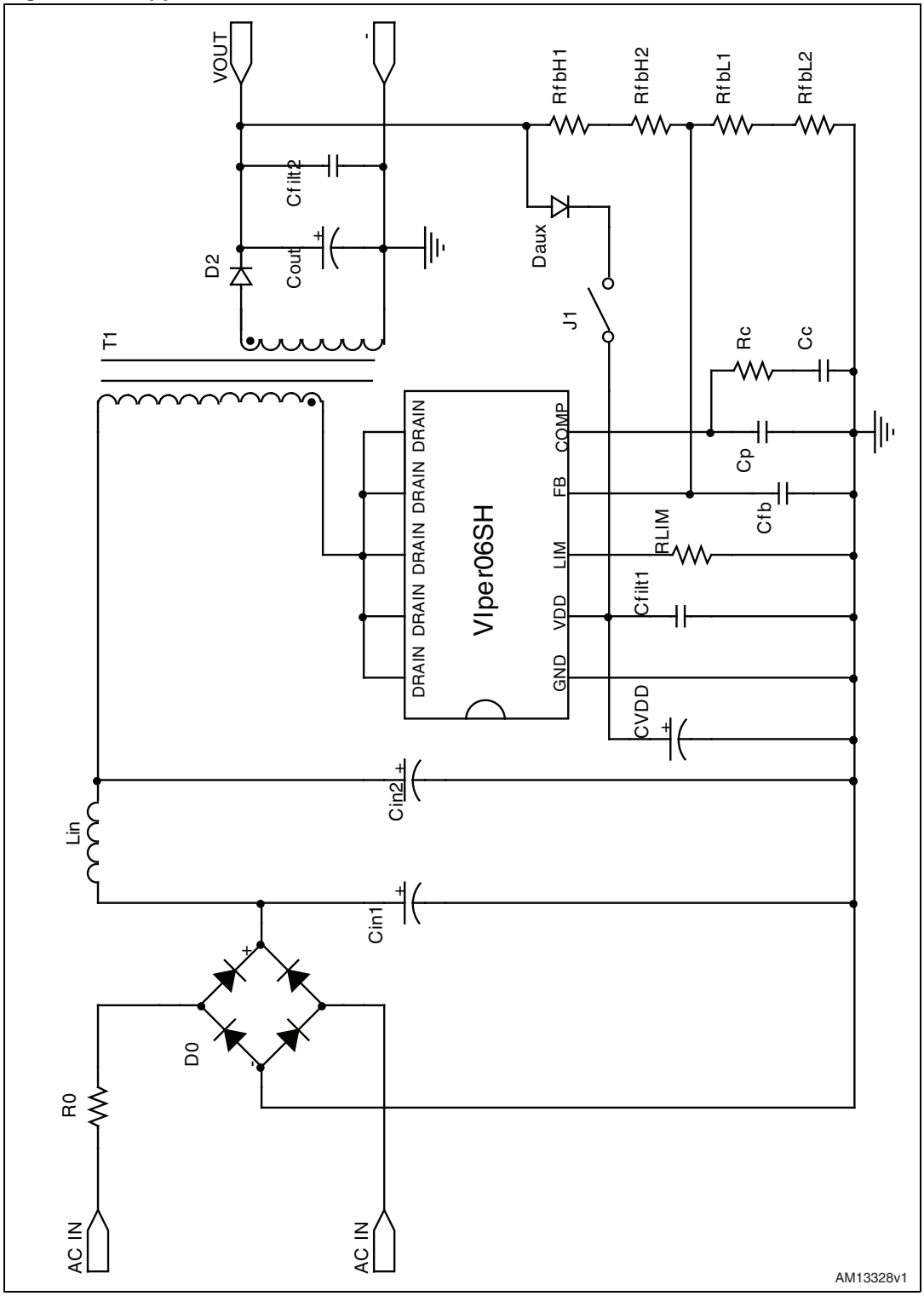


Table 2. Bill of material

Ref.	Part	Description	Package	Manufacturer
Cin1		2.2 µF, 400 V NHG series electrolytic capacitor		
Cin2		4. 7 µF, 400 V AX series electrolytic capacitor		Saxon
CVDD		1 µF, 50 V electrolytic capacitor	1206	Murata
Cfilt1		100 nF, 50 V ceramic capacitor	0805	
Cfilt2	Not mounted			
Cc		10 nF, 50 V ceramic capacitor	1206	
Cp		1 nF, 50 V ceramic capacitor	1206	
Cfb		1 nF, 50 V ceramic capacitor	0805	
Cout		330 µF, 16 V ZL series ultra-low ESR electrolytic cap.		Rubycon
D0	MB6S	600 V 1 A diode bridge	TO-269AA	Vishay
D2	STPS2H100	100 V, 2 A, power schottky rectifier	SMA	ST
Daux	1N4148W	Surface mount fast switching diode	SOD-123	Zetex
R0		4.7 Ω 3/4 W resistor		
RLIM		15 kΩ 5% 1/4 W resistor	0805	
Rc		47 kΩ 5% 1/4 W resistor	0805	
RfbH1		33 kΩ 1% 1/4 W resistor	0805	
RfbH2		0 Ω	1206	
RfbL1		12 kΩ 1% 1/4 W resistor	1206	
RfbL2		0.47 kΩ 1% 1/4 W resistor	0805	
IC1	VIPer06HS	Offline high-voltage PWM controller	SSO-10	ST
T1	1921.0040	Transformer		Magnetica
Lin	B82144A2105J	1 mH inductor LBC series		Epcos

Figure 3. V_{DD} waveforms IC externally biased (J1 selected)

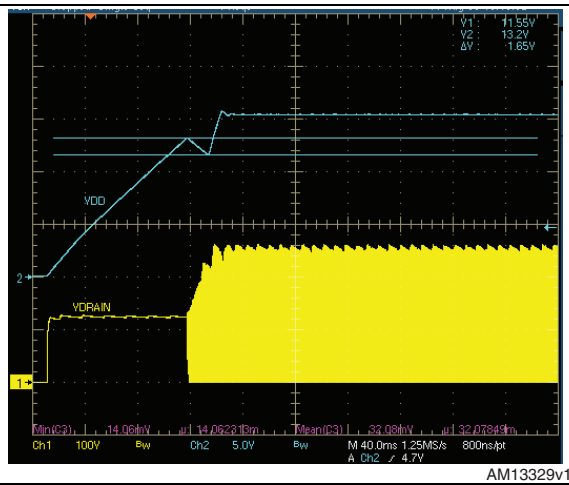
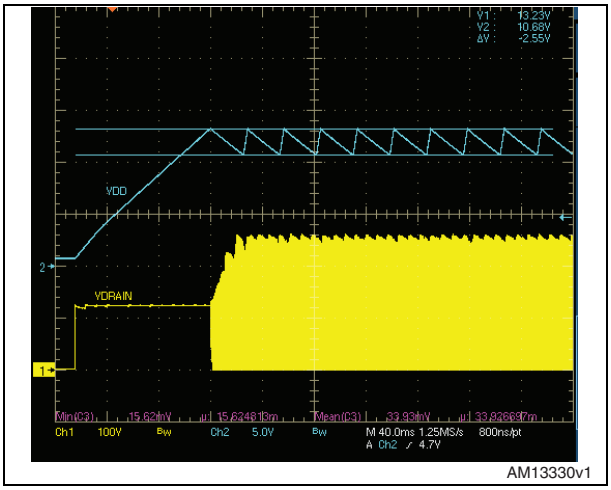


Figure 4. V_{DD} waveforms IC self-biased (J1 not selected)



4 Transformer

The characteristics of the transformer are listed in the table below.

Table 3. Transformer characteristics

Parameter	Value	Test conditions
Manufacturer	Magnetica	
Part number	1921.0040	
Primary inductance (pins 3 - 4)	1.2 mH ± 15%	Measured at 1 kHz 0.1 V
Leakage inductance	2.8%	Measured at 10 kHz 0.1 V
Primary to secondary turn ratio (3 - 4)/(5 - 8)	6.11 ± 5%	Measured at 10 kHz 0.1 V
Primary to auxiliary turn ratio (3 - 4)/(2 - 1)	5 ± 5%	Measured at 10 kHz 0.1 V

The following figures show the electrical diagram, size and pin distances (in mm) of the transformer.

Figure 5. Transformer, pin distances

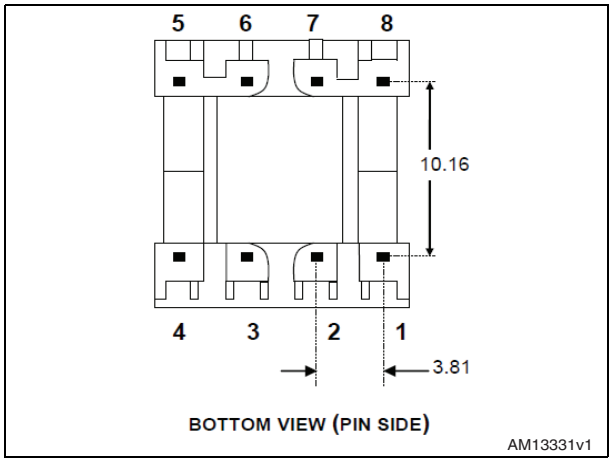


Figure 6. Transformer, electrical diagram

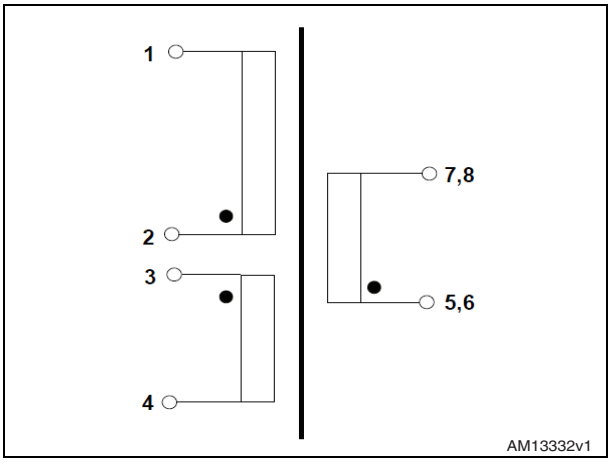


Figure 7. Transformer side view 1

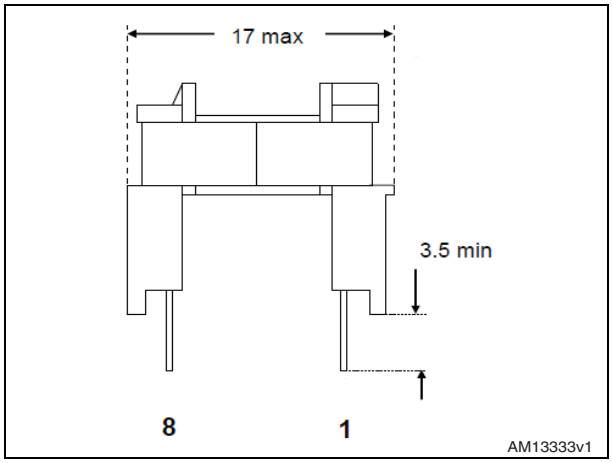
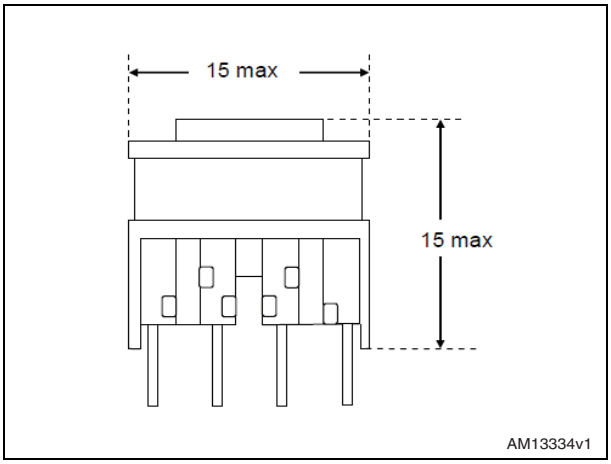


Figure 8. Transformer side view 2



5 Testing the board

5.1 Typical waveforms

Drain voltage and current waveforms in full load condition are shown for the two nominal input voltages in *Figure 9* and *10*, and for minimum and maximum input voltage in *Figure 11* and *12* respectively.

Figure 9. Drain current/voltage at 115 V_{ac}, max. load

Figure 10. Drain current/voltage at 230 V_{ac}, max. load

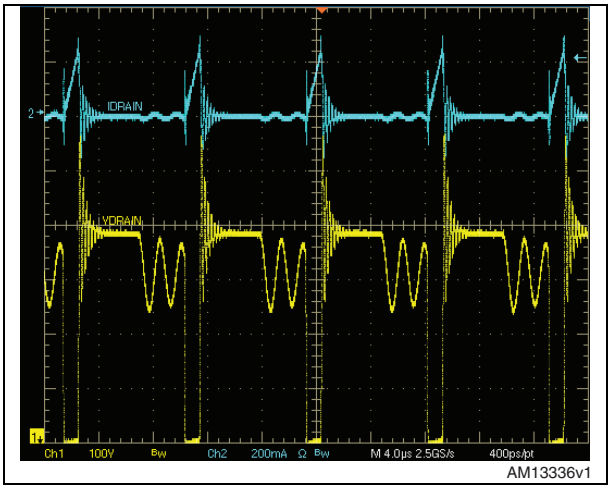


Figure 11. Drain current/voltage at 90 V_{ac}, max. load

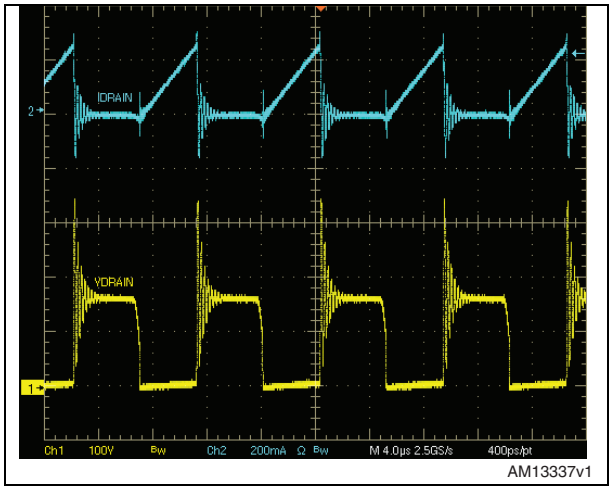
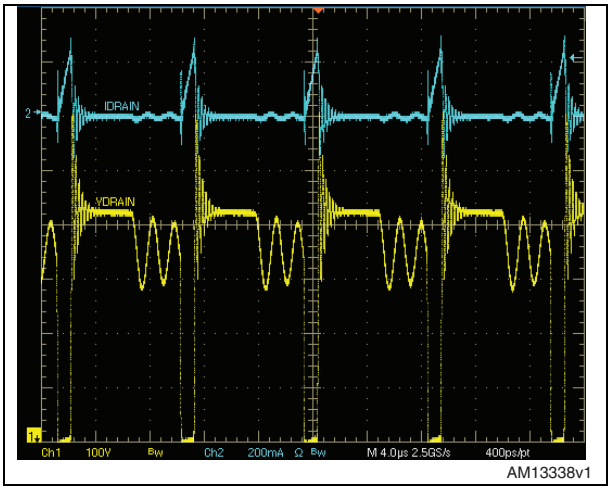


Figure 12. Drain current/voltage at 265 V_{ac}, max. load



5.2 Line/load regulation and output voltage ripple

The output voltage of the board has been measured in different line and load conditions. The results are shown in *Table 4*. The output voltage is practically not affected by the line condition and by the IC biasing (self-biasing or external biasing).

Table 4. Output voltage line-load regulation

V_{IN} [V_{AC}]	V_{OUT}[V]							
	No load		50% load		75% load		100% load	
	IC externally biased	IC self biased	IC externally biased	IC self biased	IC externally biased	IC self biased	IC externally biased	IC self biased
90	12.04	12.05	12.00	11.98	12.00	11.98	11.99	11.97
115	12.05	12.05	12.00	11.99	12.00	11.98	11.99	11.97
150	12.05	12.05	12.00	11.98	12.00	11.98	11.99	11.97
180	12.05	12.04	12.00	11.98	12.00	11.98	11.99	11.97
230	12.05	12.04	12.00	11.98	12.00	11.98	11.99	11.97
265	12.05	12.04	12.00	11.98	12.00	11.98	11.99	11.97

Figure 13. Line regulation, IC externally biased (J1 selected)

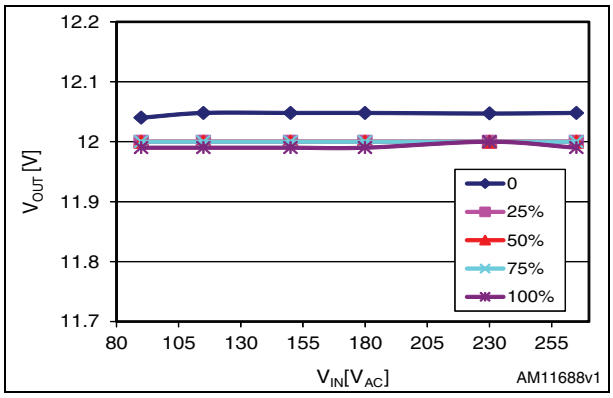


Figure 14. Line regulation, IC self-biased (J1 not selected)

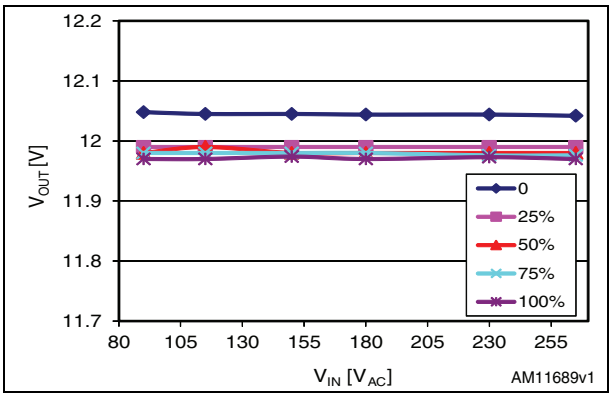


Figure 15. Load regulation, IC externally biased (J1 selected)

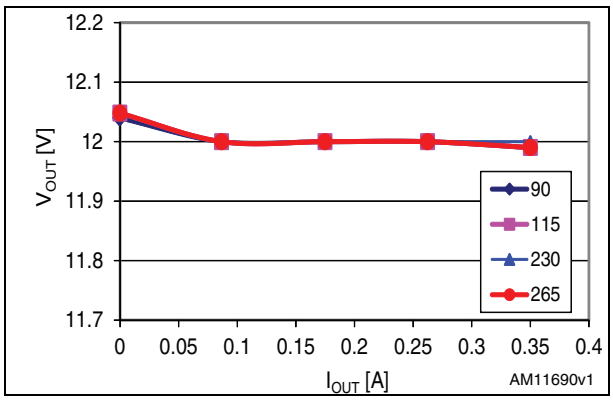
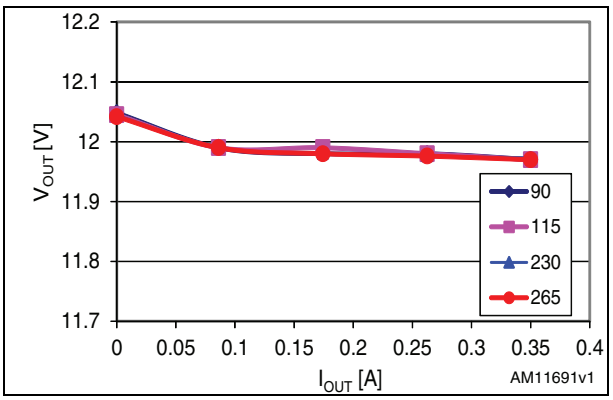


Figure 16. Load regulation, IC self-biased (J1 not selected)



5.3 Burst mode and output voltage ripple

When the converter is lightly loaded, the COMP pin voltage decreases. As it reaches the shutdown threshold, VCOMPL (1.1 V, typical), the switching is disabled and the energy is not transferred to the secondary side anymore. At this point, the feedback reaction to the stop of the energy delivery makes the COMP pin voltage increase again. As it rises 40 mV above the V_{COMPL} threshold, the normal switching operation is resumed. This results in a controlled on/off operation which is referred to as “burst mode”. This mode of operation keeps the frequency-related losses low when the load is very light or disconnected, making it easier to comply with energy saving regulations.

The figures below show the output voltage ripple when the converter is no/lightly loaded and supplied with 115 V_{AC} and with 230 V_{AC} respectively.

Figure 17. Output voltage ripple at 115 V_{AC} no load

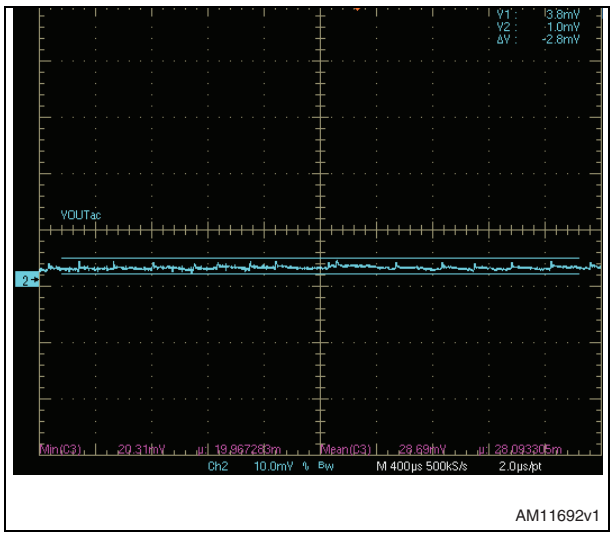


Figure 18. Output voltage ripple at 230 V_{AC} no load

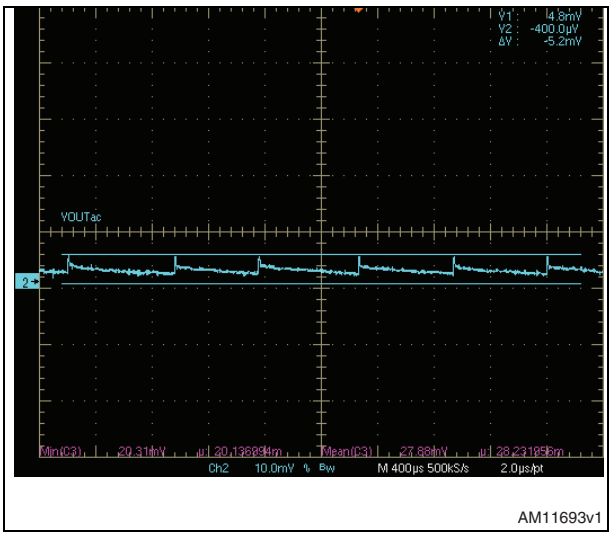


Figure 19. Output voltage ripple at 115 V_{AC} 25 mA

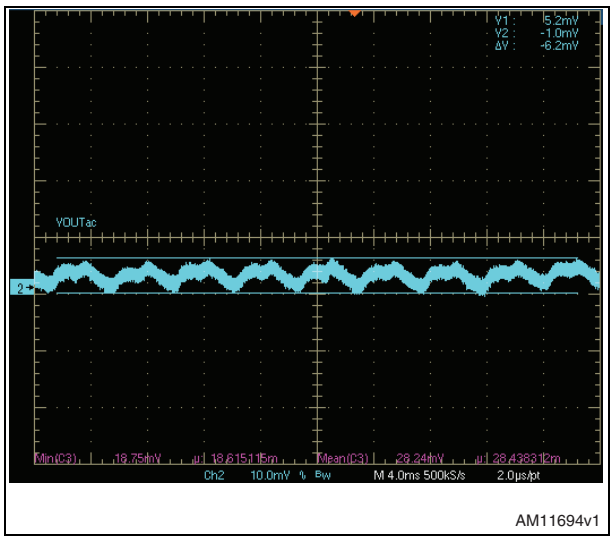


Figure 20. Output voltage ripple at 230 V_{AC} 25 mA

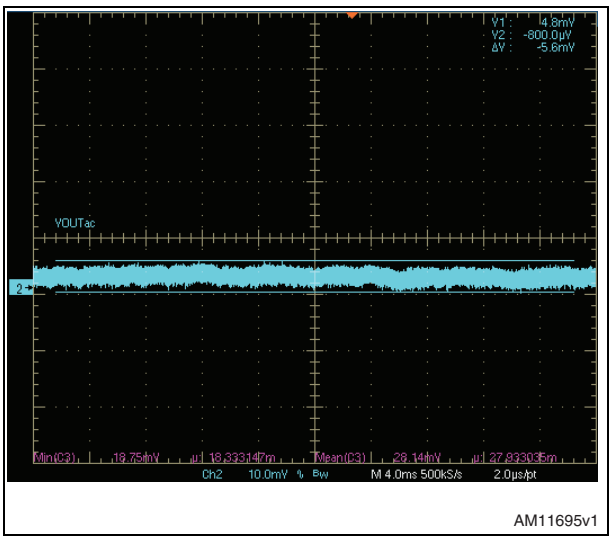


Table 5 shows the measured value of the burst mode frequency ripple measured in different operating conditions. The ripple in burst mode operation is very low.

Table 5. Output voltage ripple at no/light load

V_{IN} [V_{AC}]	V_{OUT} [mV]	
	No load	25 mA load
90	2	7
115	2	7
230	4	8
265	4	9

5.4 Efficiency

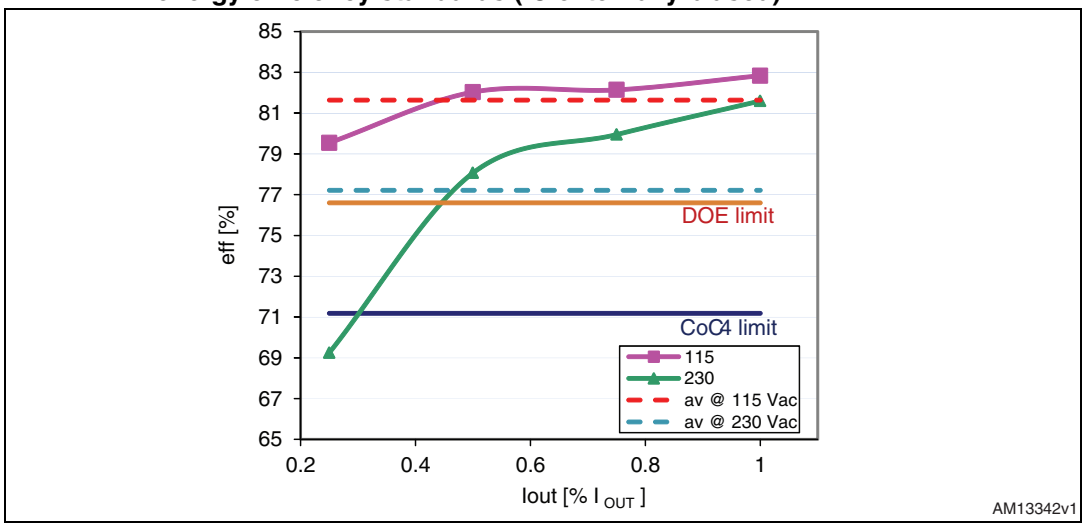
The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, 75% and 100% of maximum load, at nominal input voltage (V_{IN} = 115 V_{AC} and V_{IN} = 230 V_{AC}).

External power supplies (the power supplies are contained in a separate housing from the end-use devices they are powering) need to comply with the Code of Conduct (version 4.0) “active mode efficiency” criterion, which states an active mode efficiency higher than 71.18% for a power throughput of 4.2 W.

Another standard to be applied to external power supplies in the coming years is the DOE (Department of energy) recommendation, whose active mode efficiency requirement for the same power throughput is 76.6%.

If the IC is externally biased, the presented demonstration board is compliant with both standards, as can be seen from *Figure 21*, where the average efficiencies of the board at 115 V_{AC} (81.6%) and at 230 V_{AC} (77.2%) are plotted with dotted lines, together with the above limits. In the same figure the efficiency at 25%, 50%, 75% and 100% of output load for both input voltages is also shown.

Figure 21. Active mode efficiency of the demonstration board and comparison with energy efficiency standards (IC externally biased)



5.5 Light load performance

The input power of the converter has been measured in no load condition for different input voltages and the results are reported in *Table 6*.

Table 6. No load input power

V_{IN} [V_{AC}]	P_{IN} [mW]	
	IC externally biased	IC self-biased
90	17.6	108
115	18.9	138
150	20.9	179
180	23.1	214
230	26.9	275
265	30.2	317

In version 4 of the Code of Conduct, also the power consumption of the power supply when it is no loaded is considered. The criteria to be compliant with are reported in the table below:

Table 7. Energy consumption criteria for no load

Nameplate output power (P_{no})	Maximum power in no load for AC-DC EPS
0 W ≤ P_{no} ≤ 50 W	< 0.3 W
50 W < P_{no} < 250 W	< 0.5 W

The performance of the presented board (when the self-biasing function is not used) is much better than required; the power consumption is more than ten times lower than the limit fixed by version 4 of the Code of Conduct. Even though the performance seems to be disproportionally better than requirements, it is worth noting that often AC-DC adapter or battery charger manufacturers have very strict requirements about no load consumption and if the converter is used as an auxiliary power supply, the line filter is often the big line filter of the entire power supply that increases greatly the standby consumption.

Even though version 4 of the Code of Conduct does not have other requirements regarding light load performance, in order to give a more complete overview we report the input power and efficiency of the demonstration board also in two other light load cases. *Table 8* and *Table 9* show the performance when the output load is 25 mW and 50 mW respectively.

Table 8. Light load performance P_{OUT}=25 mW

V_{IN} [V_{AC}]	P_{OUT} [mW]	P_{IN} [mW]		Efficiency (%)	
		IC externally biased	IC self-biased	IC externally biased	IC self-biased
90	25	49.7	128	50.30	19.6
115	25	51.5	157	48.54	15.9
150	25	54.7	200	45.70	12.5
180	25	57.3	236	43.63	10.6
230	25	61.7	296	40.52	8.4
265	25	64.8	337	38.58	7.4

Table 9. Light load performance P_{OUT}=50 mW

V_{IN} [V_{AC}]	P_{OUT} [mW]	PIN [mW]		Efficiency (%)	
		IC externally biased	IC self-biased	IC externally biased	IC self-biased
90	50	82.4	167	60.71	29.94
115	50	85.0	198	58.82	25.25
150	50	89.3	242	55.99	20.66
180	50	93.0	280	53.76	17.86
230	50	98.0	341	51.02	14.66
265	50	101.1	384	49.46	13.02

The input power vs. input voltage for no load and light load condition (*Table 6*, *8* and *9*) is shown in the figures below.

Figure 22. P_{IN} vs. V_{IN} at no load and light load; IC externally biased (J1 selected)

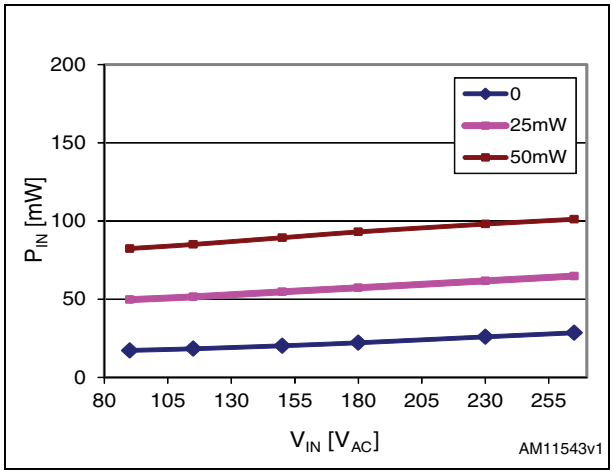
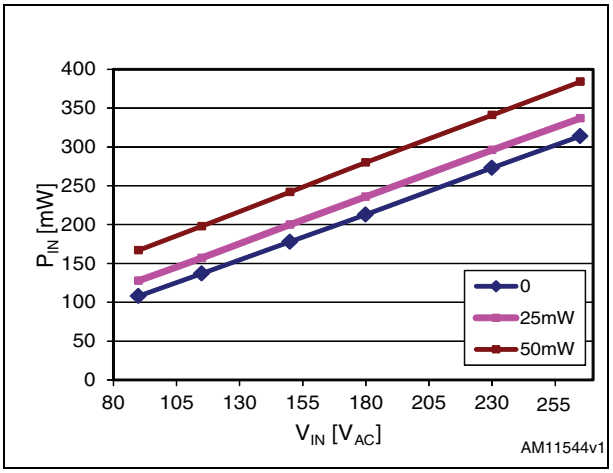


Figure 23. P_{IN} vs. V_{IN} at no load and light load, IC self-biased (J1 not selected)



Depending on the equipment supplied, it's possible to have several criteria to measure the standby or light load performance of a converter. One criterion is the measurement of the output power when the input power is equal to one watt. In *Table 10* the output power needed to have 1 W of input power in a different line conditions is given. *Figure 24* and *25* show the diagram of the output powers corresponding to P_{IN} = 1 W for different values of the input voltage.

Table 10. P_{OUT} @ P_{IN}=1 W

V_{IN} [V_{AC}]	P_{IN} [W]	P_{OUT} [W]		Efficiency (%)	
		IC externally biased	IC self-biased	IC externally biased	IC self-biased
90	1	0.78	0.64	78	64
115	1	0.77	0.60	77	60
150	1	0.73	0.55	73	55
180	1	0.70	0.49	70	49
230	1	0.68	0.43	68	43
265	1	0.65	0.40	65	40

Figure 24. Efficiency at P_{IN} = 1 W; IC externally biased (J1 selected)

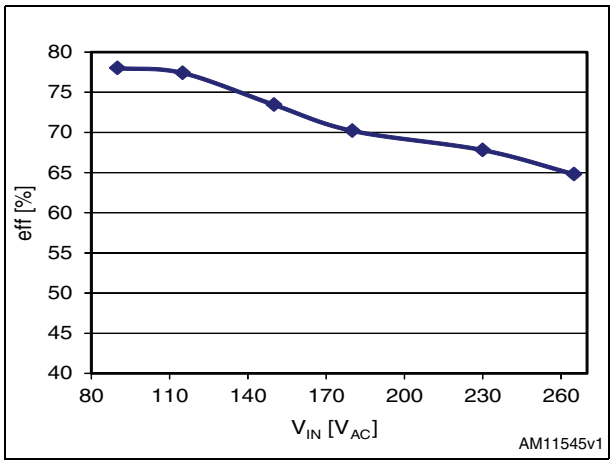
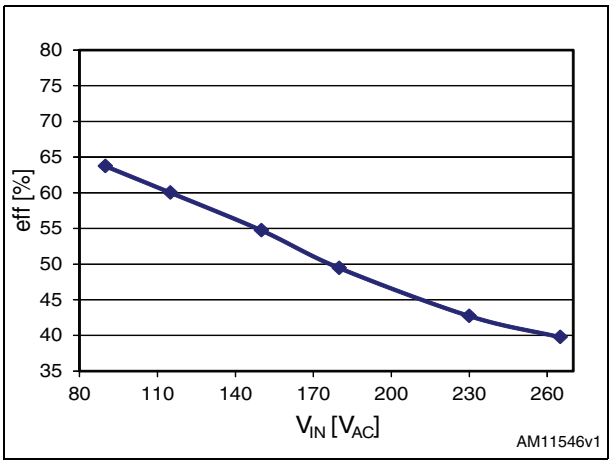


Figure 25. Efficiency at P_{IN} = 1 W; IC self biased (J1 not selected)



Another requirement (EuP lot 6) is that the input power should be less than 500 mW when the converter is loaded with 250 mW. The performances are shown in *Figure 26* for external biasing and in *Figure 27* for self biasing. In the former case the converter can satisfy even this requirement.

Figure 26. P_{IN} at P_{OUT} = 250 mW; IC externally biased (J1 selected)

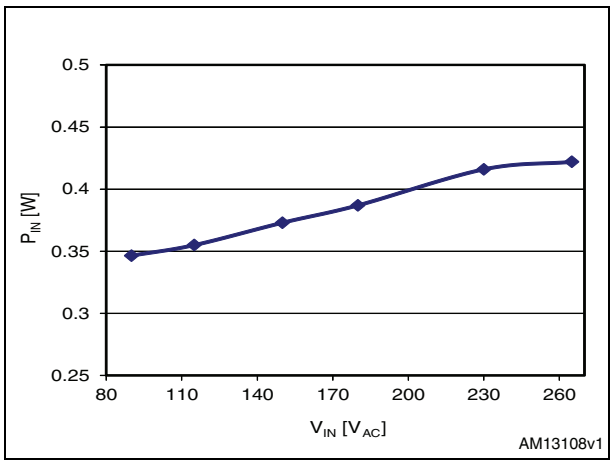
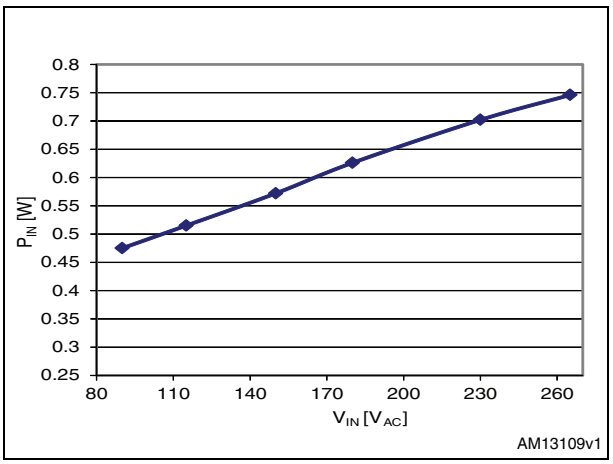


Figure 27. P_{IN} at P_{OUT} = 250 mW; IC self biased (J1 not selected)



6 Functional check

6.1 Soft-start

At startup, the current limitation value reaches IDLIM after an internally fixed time, t_{SS}, whose typical value is 8.5 msec. This time is divided into 16 time intervals, each corresponding to a current limitation step progressively increasing. In this way the drain current is limited during the output voltage increase, therefore reducing the stress on the secondary diode.

The soft-start phase is shown in *Figure 28* and *29*.

Figure 28. Soft-start @ startup

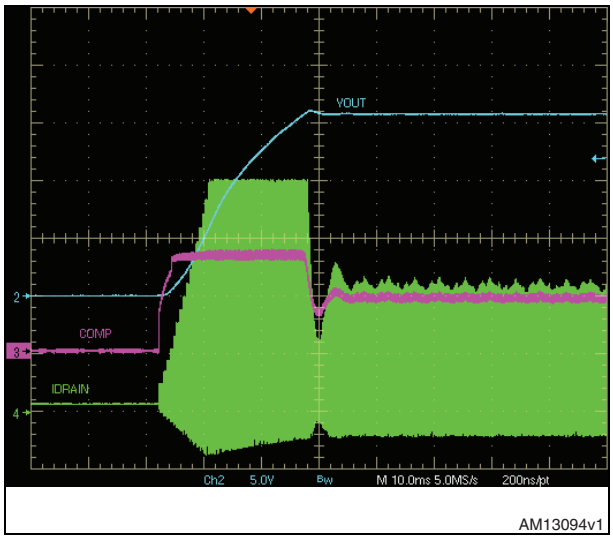
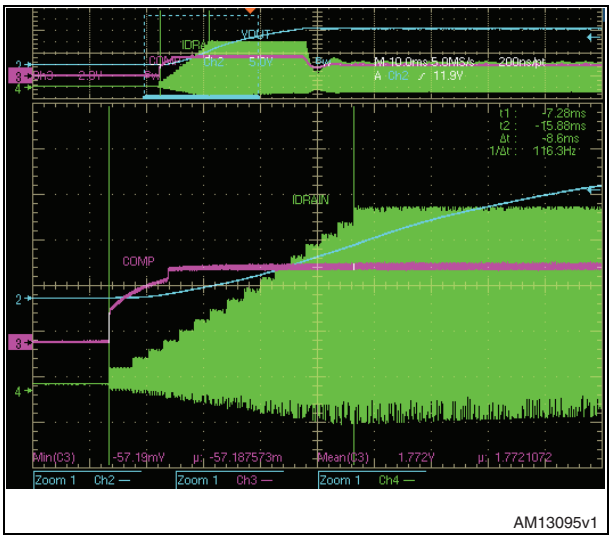


Figure 29. Soft-start @ startup (zoom)



6.2 Overload protection

In the case of overload or short-circuit (see *Figure 30*), the drain current reaches the IDLIM value (or the one set by the user through the RLIM resistor). In every cycle where this condition is met, a counter is incremented; if it is maintained continuously for the time t_{OVL} (50 msec typical, internally fixed), the overload protection is tripped, the power section is turned off and the converter is disabled for a $t_{RESTART}$ time (1 second typ.). After this time has elapsed, the IC resumes switching and, if the short is still present, the protection occurs indefinitely in the same way (*Figure 31*). This ensures restart attempts of the converter with low repetition rate, so that it works safely with extremely low power throughput and avoids the IC overheating in the case of repeated overload events.

Furthermore, every time the protection is tripped, the internal soft-startup function is invoked (*Figure 32*), in order to reduce the stress on the secondary diode.

After the short removal, the IC resumes normal working. If the short is removed during t_{SS} or t_{OVL}, i.e. before the protection tripping, the counter is decremented on a cycle-by-cycle basis down to zero and the protection is not tripped.

If the short-circuit is removed during $t_{RESTART}$, the IC must wait for the $t_{RESTART}$ period to elapse before switching is resumed (*Figure 33*).

Figure 30. OLP short-circuit applied: OLP tripping

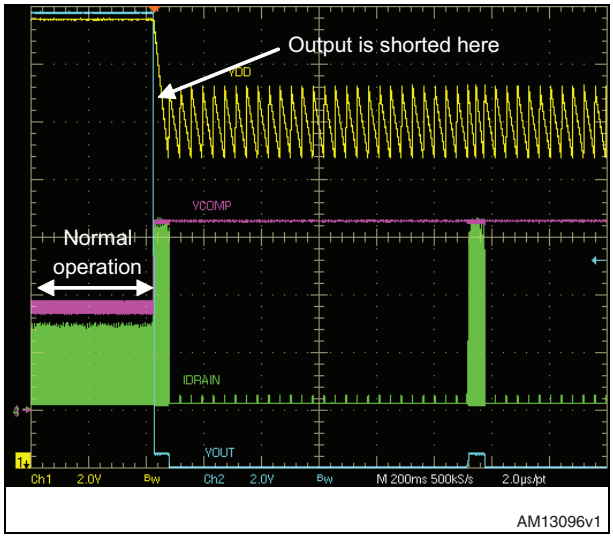


Figure 31. Output short-circuit maintained: OLP steady-state

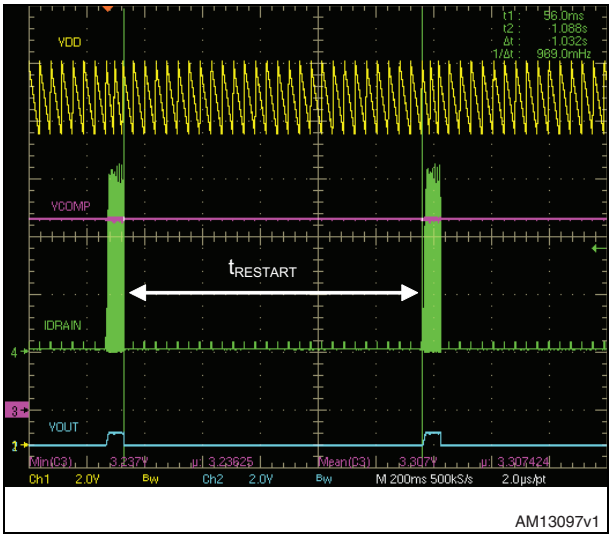


Figure 32. Output short-circuit maintained: OLP steady-state (zoom)

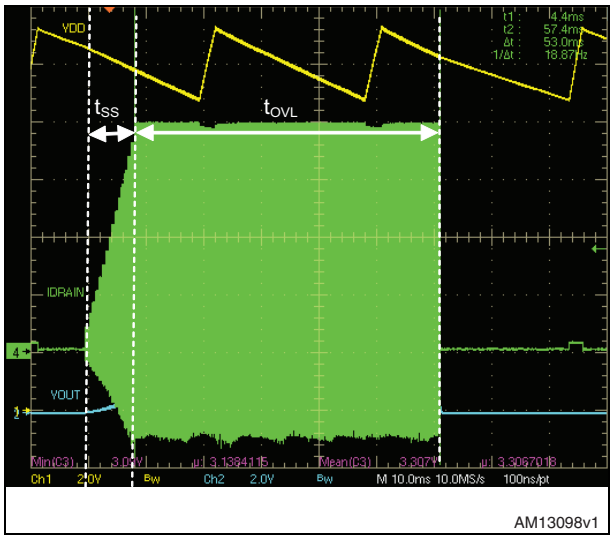
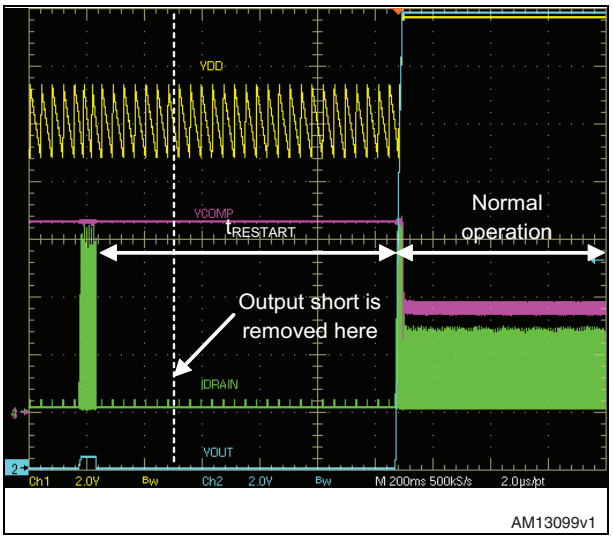


Figure 33. Output short-circuit removal and converter restart



6.3 Feedback loop failure protection

This protection is available any time the IC is not self-biased. As the loop is broken (RfbL shorted or RfbH open), the output voltage V_{OUT} increases and the VIPER06 runs at its maximum current limitation. The V_{DD} pin voltage increases as well, because it is linked to the V_{OUT} voltage either directly or through the auxiliary winding, depending on the cases.

If the V_{DD} voltage reaches the $V_{DDclamp}$ threshold (23.5 V min.) in less than 50 msec, the IC is shut down by open loop failure protection (see *Figure 34* and *35*), otherwise by OLP, as described in the previous section. The breaking of the loop has been simulated by shorting the low-side resistor of the output voltage divider, RfbL = RfbL1+RfbL2. The same behavior can be induced opening the high-side resistor, RfbH = RfbH1+RfbH2.

The protection acts in auto-restart mode with $t_{RESTART}$ = 1sec (*Figure 35*). As the fault is removed, normal operation is restored after the last $t_{RESTART}$ interval has been completed (*Figure 37*).

Figure 34. Feedback loop failure protection: tripping

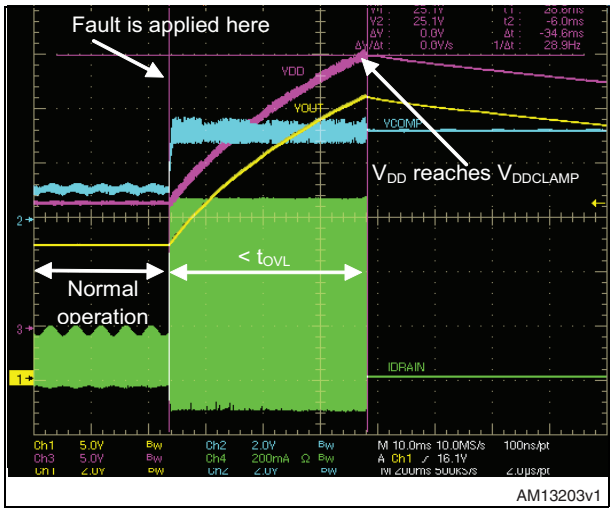


Figure 35. Feedback loop failure protection: steady-state

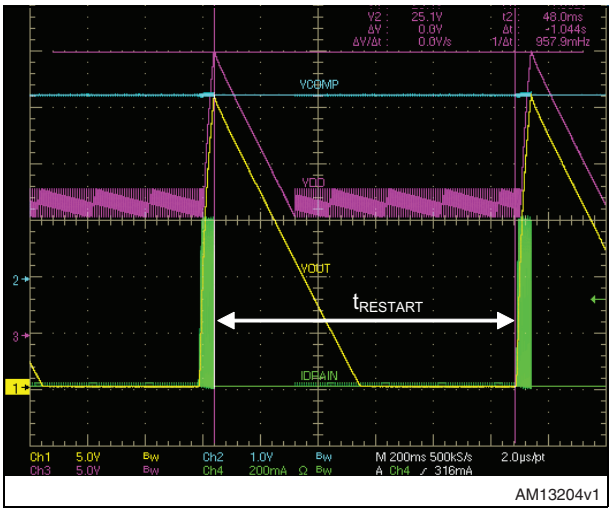


Figure 36. Feedback loop failure protection: steady-state, zoom

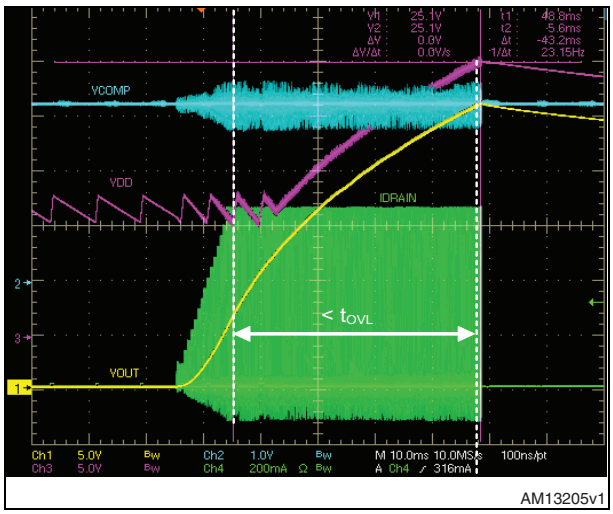
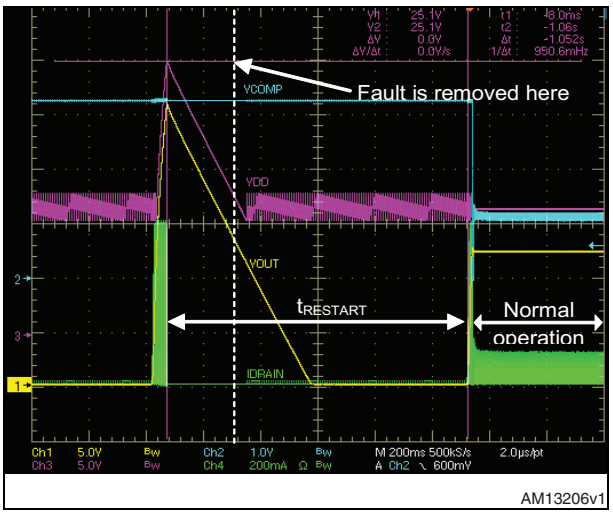


Figure 37. Feedback loop failure protection: converter restart

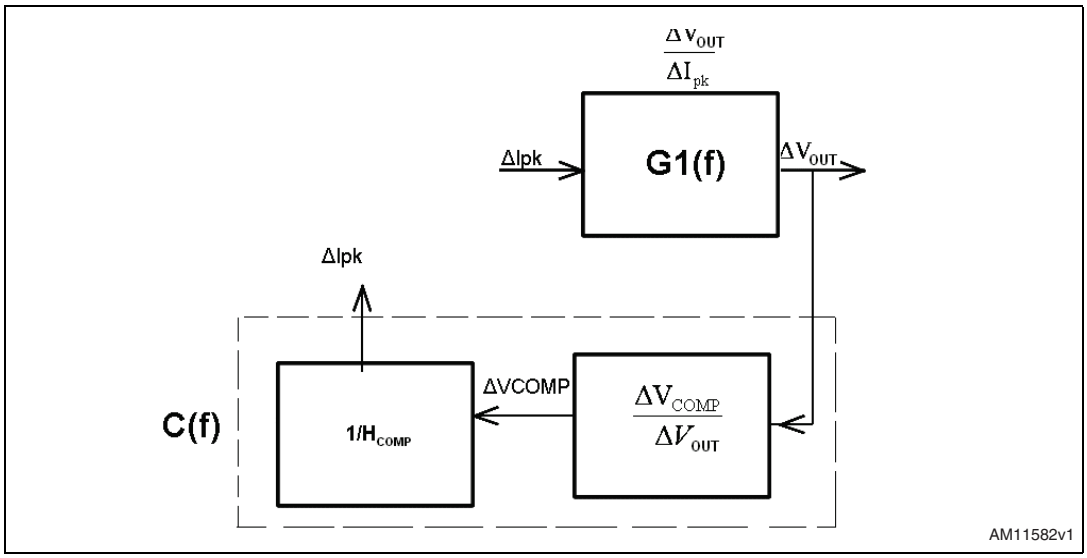


7 Feedback loop calculation guidelines

7.1 Transfer function

The set PWM modulator + power stage is indicated with G1(f), while C(f) is the “controller”, i.e. the network which is in charge to ensure the stability of the system.

Figure 38. Control loop block diagram



The mathematical expression of the power plant G1(f) is the following:

Equation 2

$$G_1(f) = \frac{\Delta V_{OUT}}{\Delta I_{pk}} = \frac{V_{OUT} \cdot (1 + \frac{j \cdot 2 \cdot \pi \cdot f}{z})}{Ipkp(fsw, Vdc) \cdot (1 + \frac{j \cdot 2 \cdot \pi \cdot f}{p})} = \frac{V_{OUT} \cdot (1 + \frac{j \cdot f}{fz})}{Ipkp(fsw, Vdc) \cdot (1 + \frac{j \cdot f}{fp})}$$

where V_{OUT} is the output voltage, Ipkp is the primary peak current, fp is the frequency of the pole due to the output load and fz the frequency of the zero due to the ESR of the output capacitor:

Equation 3

$$fp = \frac{1}{\pi \cdot C_{OUT} \cdot (R_{OUT} + 2ESR)}$$

Equation 4

$$fz = \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot ESR}$$

The mathematical expression of the compensator C(f) is:

Equation 5

$$C(f) = \frac{\Delta I_{pk}}{\Delta V_{OUT}} = \frac{C_0}{H_{COMP}} \cdot \frac{1 + \frac{f \cdot j}{fZc}}{2 \cdot \pi \cdot f \cdot j \cdot \left(1 + \frac{f \cdot j}{fPc}\right)}$$

where:

Equation 6

$$Co = -\frac{Gm}{Cc + Cp} \cdot \frac{RfbL}{RfbL + RfbH}$$

Equation 7

$$fZc = \frac{1}{2 \cdot \pi \cdot Rc \cdot Cc}$$

Equation 8

$$fPc = \frac{Cc + Cp}{2 \cdot \pi \cdot Rc \cdot Cc \cdot Cp}$$

are chosen in order to censure the stability of the overall system. Gm = 2 mA/V (typical) is the VIPER06 transconductance.

7.2 Compensation procedure

The first step is to choose the pole and zero of the compensator and the crossing frequency, for instance:

- fZc = fp/2
- fPc = fz
- fcross = fcross_sel ≤fsw/10

G1(fcross_sel) can be calculated from equation (*2*) and, since by definition it is | C(fcross_sel)*G1(fcross_sel)| = 1, C_0, can be calculated as follows:

Equation 9

$$C_0 = \frac{\left|2 \cdot \pi \cdot fcross\_sel \cdot j\right| \cdot \left|1 + \frac{fcross\_sel \cdot j}{fPc}\right|}{\left|1 + \frac{fcross\_sel \cdot j}{fZc}\right|} \cdot \frac{H_{COMP}}{\left|G1(fcross\_sel)\right|}$$

At this point the bode diagram of G1(f)*C(f) can be plotted, in order to check the phase margin for the stability. If the margin is not high enough, another choice for fZc, fPc and fcross_sel should be made, and the procedure repeated. When the stability is ensured, the next step is to find the values of the schematic components, which can be calculated, using the above formulas, as follows:

Equation 10

$$RfbL = \frac{RfbH}{\frac{Vout}{3.3V} - 1}$$

Equation 11

$$Cp = \frac{fZc}{fPc} \cdot \frac{Gm}{|C_0|} \cdot \frac{RfbL}{RfbL + RfbH}$$

Equation 12

$$Cc = Cp \cdot \left(\frac{fPc}{fZc} - 1 \right)$$

Equation 13

$$Rc = \frac{Cc + Cp}{2 \cdot \pi \cdot fPc \cdot Cc \cdot Cp}$$

8 Thermal measurements

A thermal analysis of the demonstration board in full load condition at T_{AMB} = 25 °C, both with and without the self-biasing function, has been performed using an IR camera.

The results are shown in the following figures. When the self-biasing function is used the VIPER06 temperature is higher, due to the power dissipated by the HVstartup generator.

Figure 39. Thermal measurement at V_{IN} = 90 V_{AC}, full load, IC externally biased

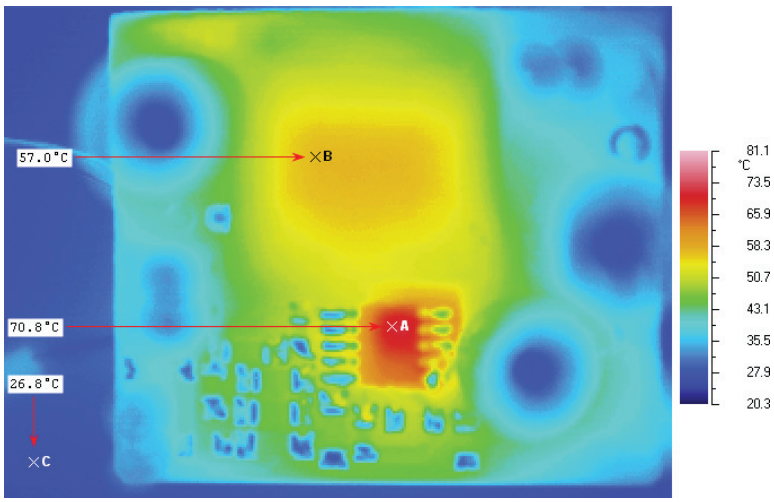


Figure 40. Thermal measurement at V_{IN} = 115 V_{AC}, full load, IC externally biased

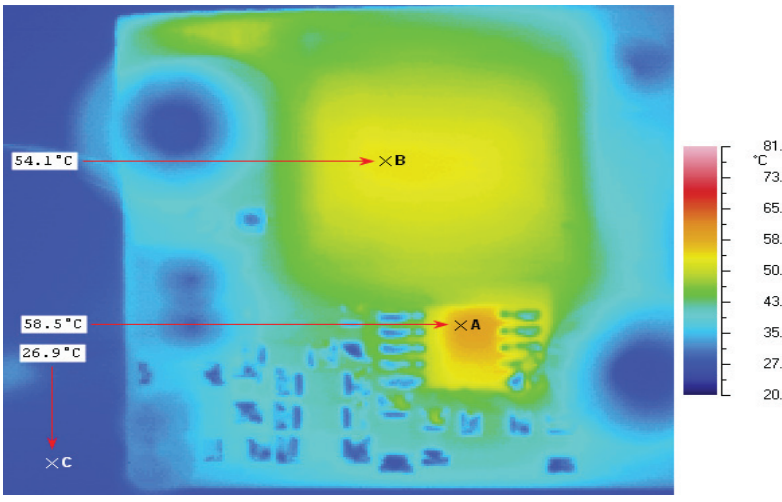


Figure 41. Thermal measurement at V_{IN} = 230 V_{AC}, full load, IC externally biased

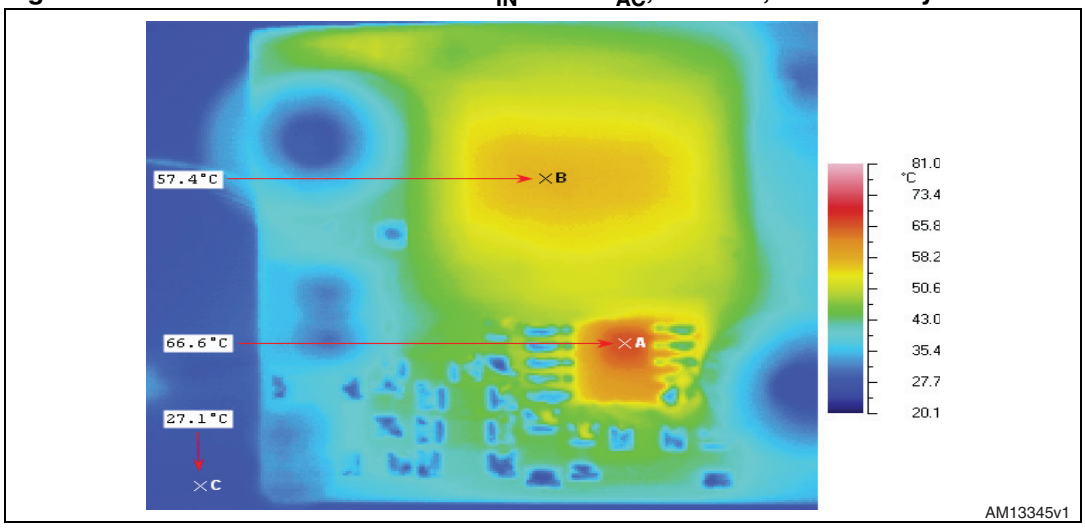


Figure 42. Thermal measurement at V_{IN} = 265 V_{AC}, full load, IC externally biased

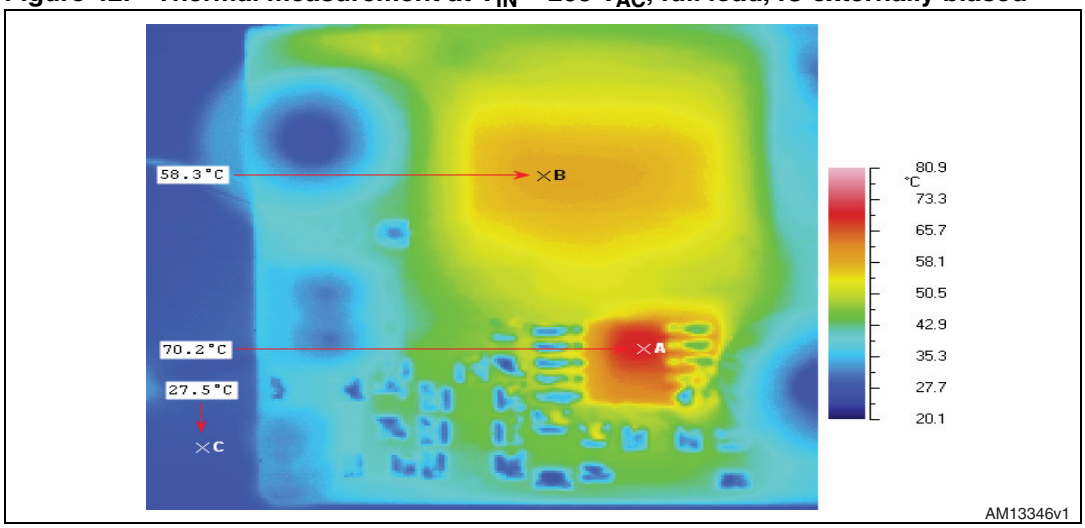


Figure 43. Thermal measurement at V_{IN} = 90 V_{AC}, Iout = 310 mA, IC self biased

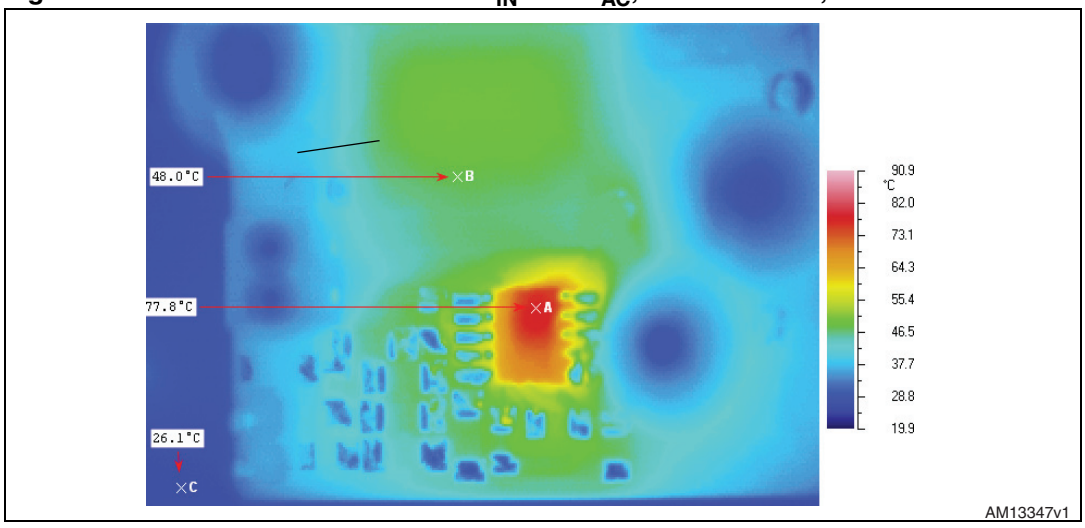


Figure 44. Thermal measurement at V_{IN} = 115 V_{AC}, Iout = 310 mA, IC self biased

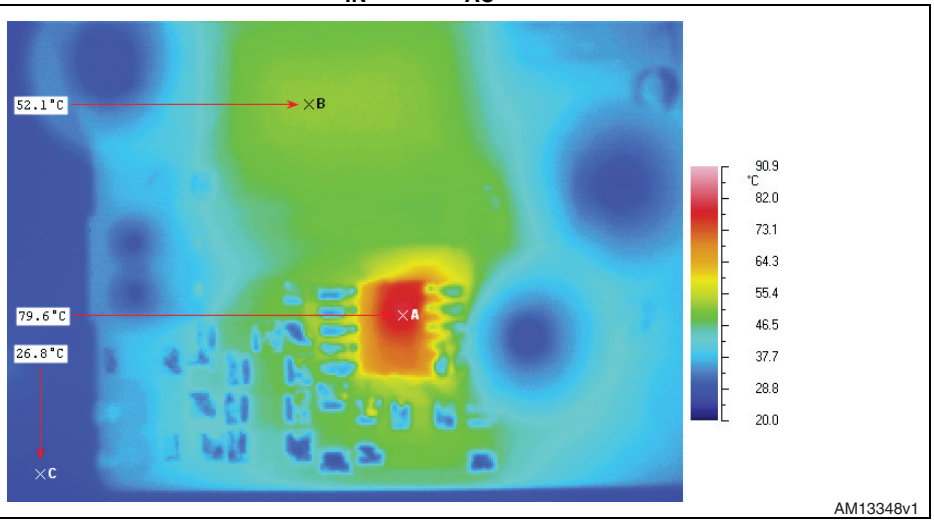


Figure 45. Thermal measurement at V_{IN} = 230 V_{AC}, full load, IC self biased

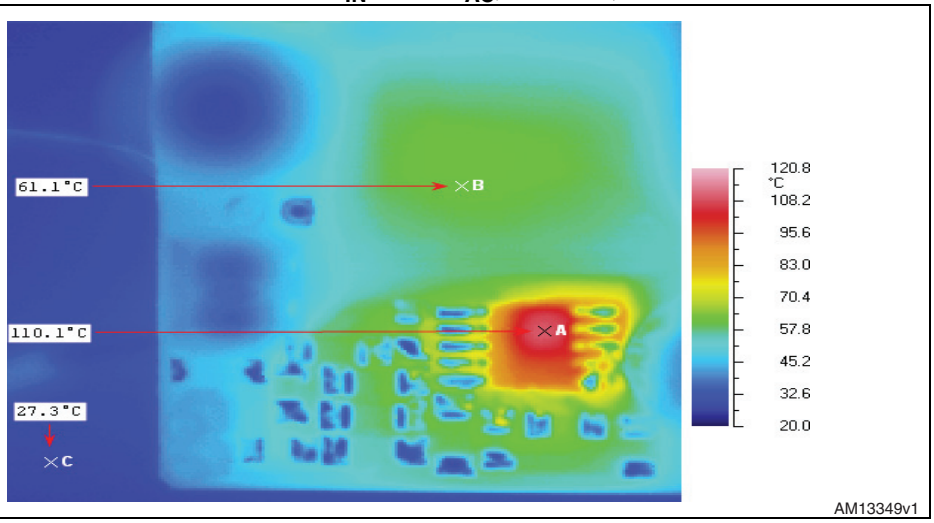
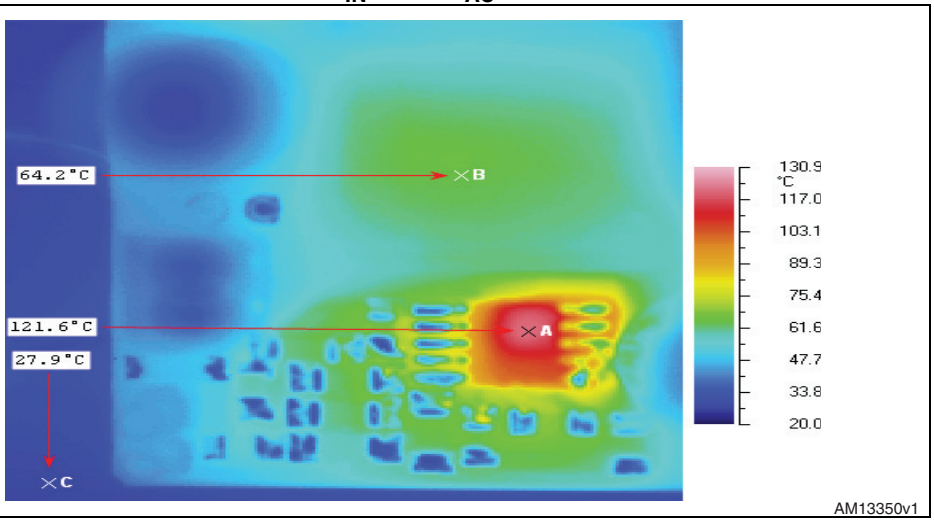


Figure 46. Thermal measurement at V_{IN} = 265 V_{AC}, full load, IC self biased



9 EMI measurements

A pre-compliance test to the EN55022 (class B) european normative has been performed using an EMC analyzer and an LISN. Average measurements are reported in the following figures.

Figure 47. Average measurements at full load, T_{AMB}=25 °C, 115 V_{AC}, IC externally biased

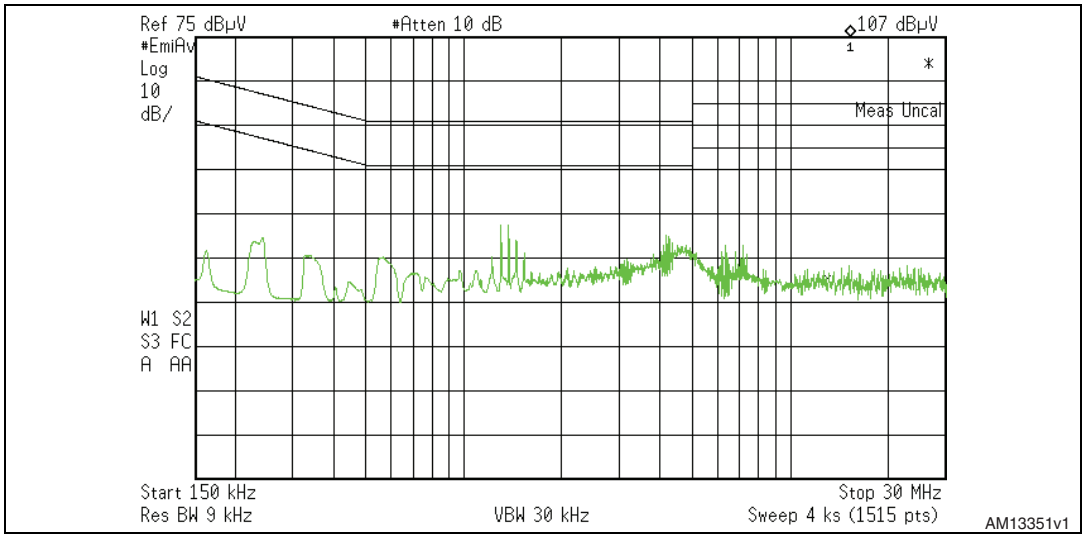
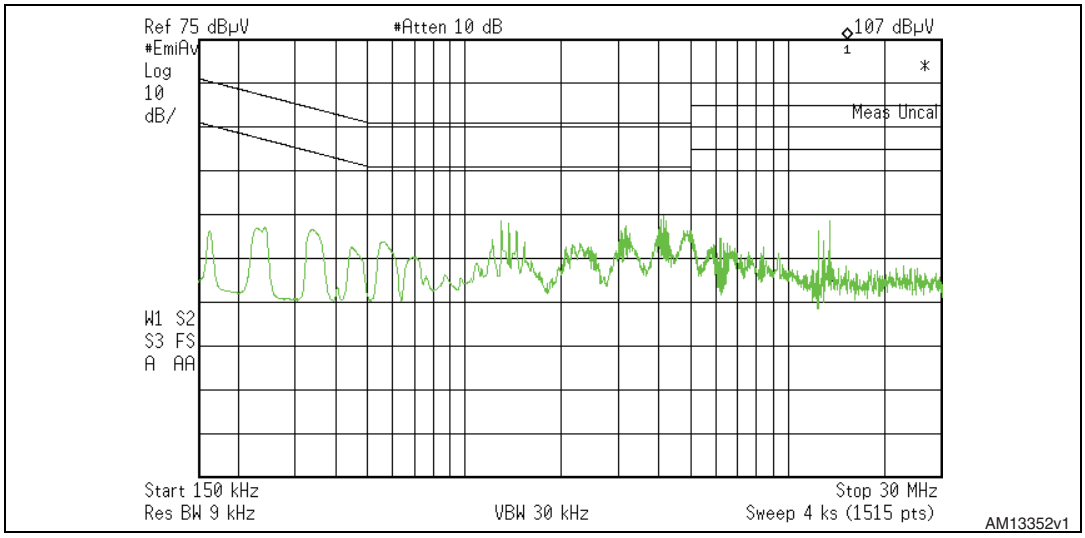


Figure 48. Average measurements at full load, T_{AMB}=25 °C, 230 V_{AC}, IC externally biased



10 Board layout

Figure 49. Board layout - complete

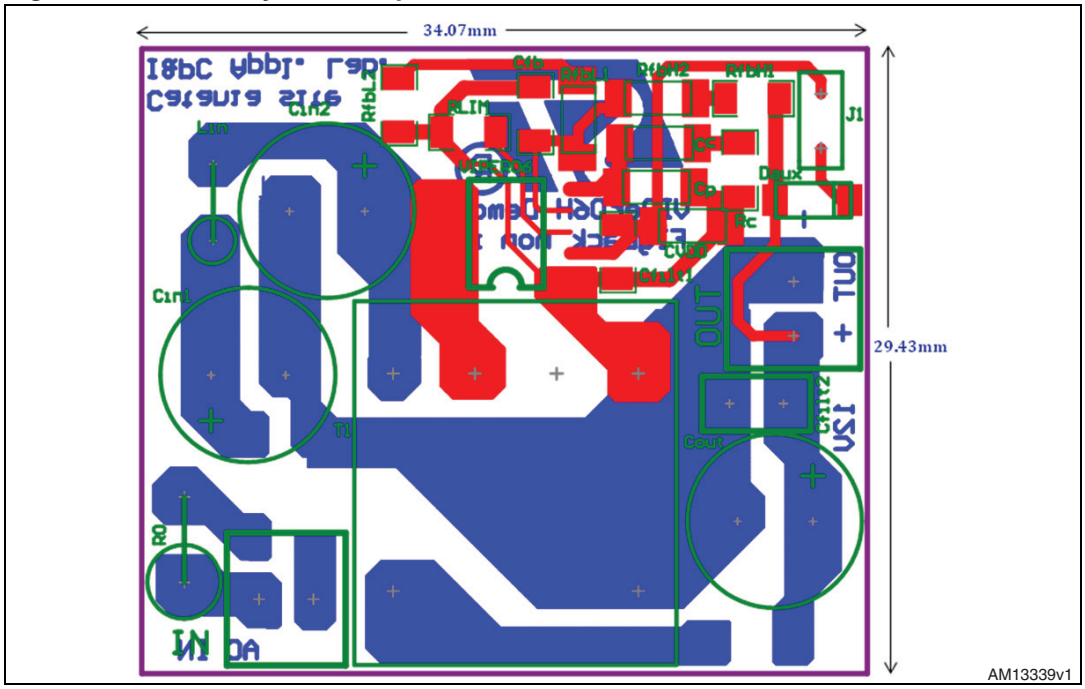


Figure 50. Board layout - top layer + top overlay

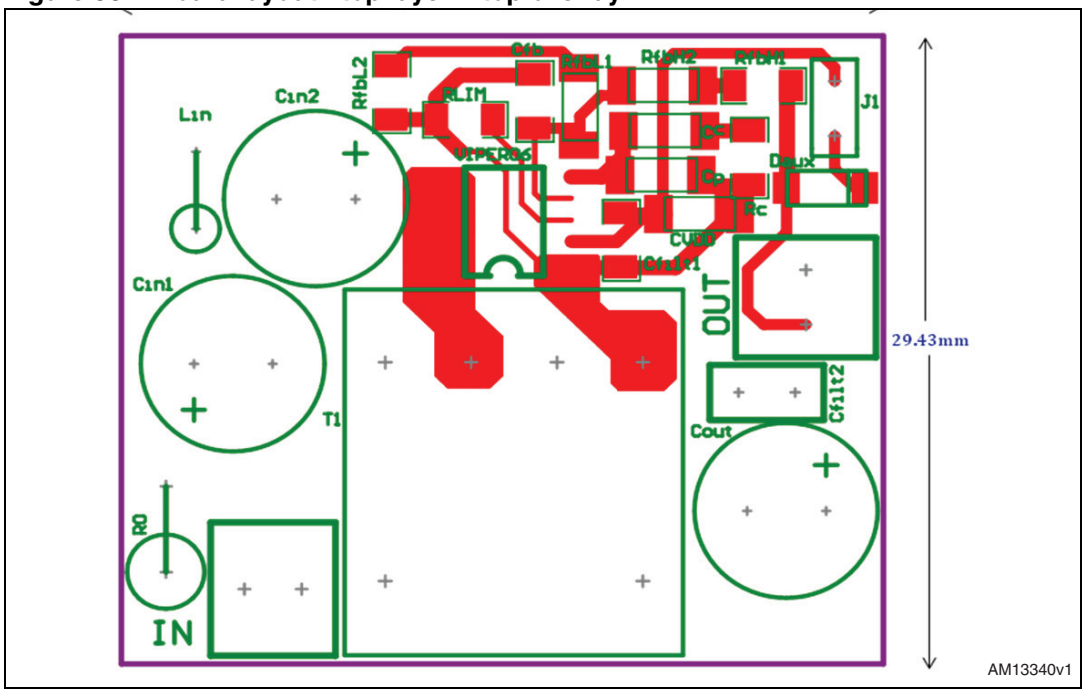
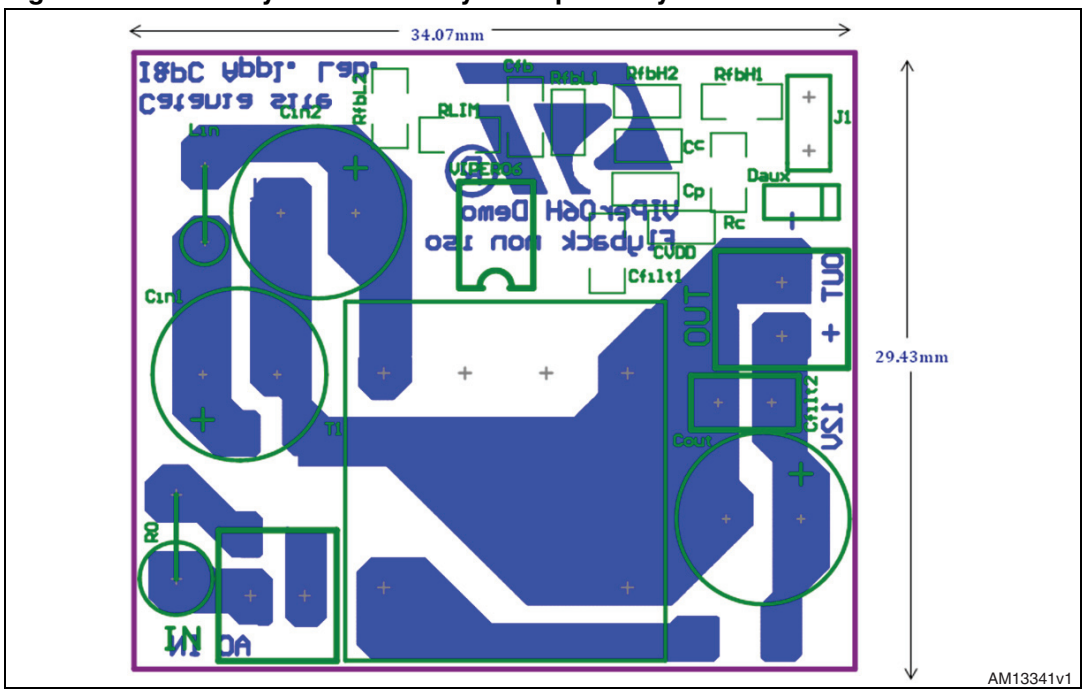


Figure 51. Board layout - bottom layer + top overlay



11 Conclusions

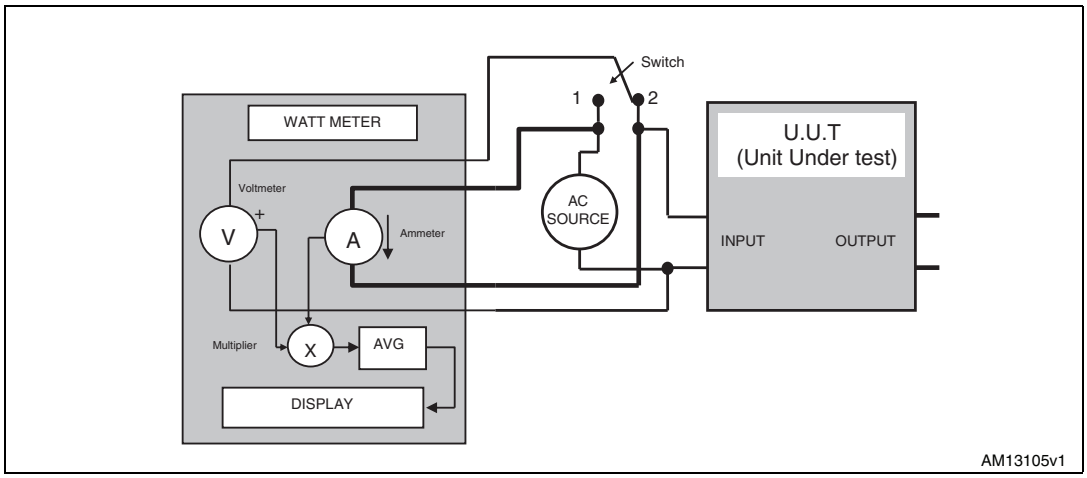
The VIPER06 allows a non-isolated converter to be designed in a simple way and with few external components. In this document a flyback has been described and characterized. Special attention has been given to light load performance. The efficiency performance has been compared to the requirements of the Code of Conduct (version 4) for an external AC-DC adapter with very good results, the measured active mode efficiency is always higher with respect to the minimum required.

Appendix A Test equipment and measurement of efficiency and light load performance

The converter input power has been measured using a wattmeter. The wattmeter measures simultaneously the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). The wattmeter is a digital instrument so it samples the current and voltage and converts them to digital form. The digital samples are then multiplied giving the instantaneous measured power. The sampling frequency is in the range of 20 kHz (or higher depending on the instrument used). The display provides the average measured power, averaging the instantaneous measured power in a short period of time (1 second typ.).

Figure 52 shows how the wattmeter is connected to the UUT (unit under test) and to the AC source and the wattmeter internal block diagram.

Figure 52. Connection of the UUT to the wattmeter for power measurements



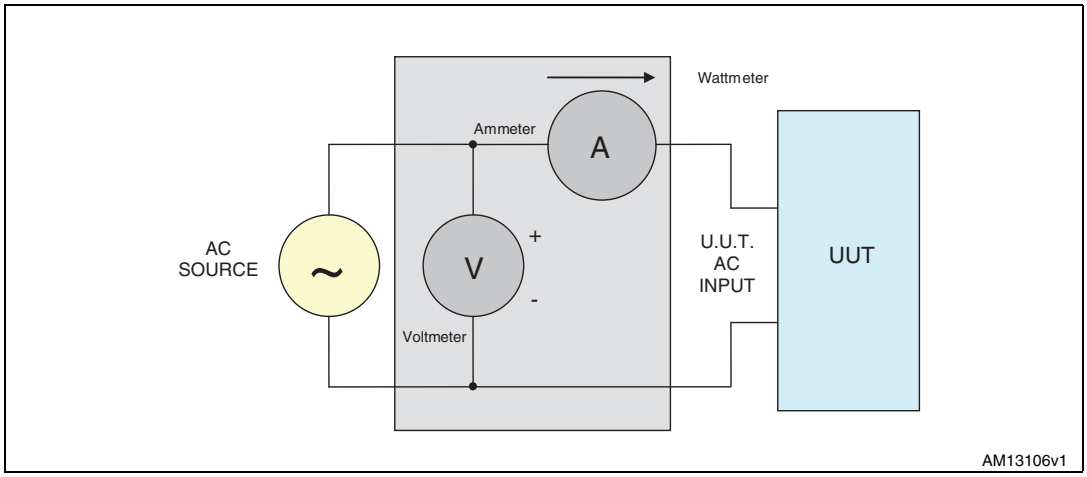
An electronic load has been connected to the output of the power converter (UUT), allowing to set and measure the converter's load current, while the output voltage has been measured by a voltmeter. The output power is the product between load current and output voltage. The ratio between the output power, calculated as previously stated, and the input power, measured by the wattmeter, is the converter's efficiency, which has been measured in different input/output conditions.

A.1 Measuring input power

With reference to *Figure 52*, the UUT input current causes a voltage drop across the ammeter's internal shunt resistance (the ammeter is not ideal as it has an internal resistance higher than zero) and across the cables connecting the wattmeter to the UUT.

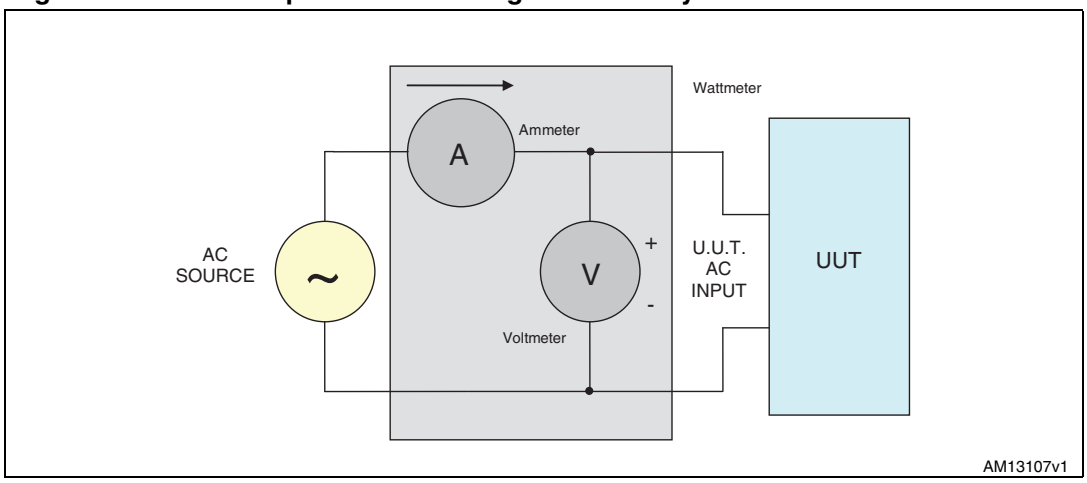
If the switch of *Figure 52* is in position 1 (see also the simplified scheme of *Figure 53*), this voltage drop causes an input measured voltage higher than the input voltage at the UUT input that, of course, affects the measured power. The voltage drop is generally negligible if the UUT input current is low (for example when measuring the input power of UUT in light load condition).

Figure 53. Switch in position 1 - setting for standby measurements



In the case of high UUT input current (i.e. for measurements in heavy-load conditions), the voltage drop can be relevant compared to the UUT real input voltage. If this is the case, the switch in *Figure 52* can be changed to position 2 (see simplified scheme of *Figure 54*) where the UUT input voltage is measured directly at the UUT input terminal and the input current does not affect the measured input voltage.

Figure 54. Switch in position 2 - setting for efficiency measurements



On the other hand, the position of *Figure 54* may introduce a relevant error during light load measurements, when the UUT input current is low and the leakage current inside the voltmeter itself (which is not an ideal instrument and doesn't have infinite input resistance) is not negligible. This is the reason why it is recommended to use the setting of *Figure 53* for light load measurements and *Figure 54* for heavy load measurements.

If it is not clear which measurement scheme has the lesser effect on the result, try with both and register the lower input power value.

As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT is operated at 100% of nameplate output current for at least 30 minutes (warm-up period) immediately prior to conducting efficiency measurements. After this warm-up period, the AC input power is monitored for a period of 5 minutes to assess the stability of the UUT. If the power level does not drift by more than 5% from the maximum value

observed, the UUT can be considered stable and the measurements can be recorded at the end of the 5-minute period. If AC input power is not stable over a 5-minute period, the average power or accumulated energy is measured over time for both AC input and DC output.

Some wattmeter models allow the measured input power to be integrated in a time range and then the energy absorbed by the UUT to be measured during the integration time. The average input power is calculated by dividing it by the integration time itself.

12 References

1. Code of conduct on energy efficiency of external power supplies, version 4
2. VIPER06 datasheet

13 Revision history

Table 11. Document revision history

Date	Revision	Changes
08-Feb-2013	1	Initial release.