Elektronische Bauelemente

SPRD4503-C

N-Ch: 28A, 30V, $R_{DS(ON)}$ 18mΩ
P-Ch: -22A, -30V, $R_{DS(ON)}$ 30mΩ
N & P-Ch Enhancement Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

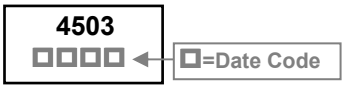
The SPRD4503-C is the highest performance trench N-Ch and P-Ch MOSFETs with extreme high cell density, which provide excellent $R_{DS(ON)}$ and gate charge for most of the synchronous buck converter applications.

The SPRD4503-C meet the RoHS and Green Product requirement with full function reliability approved.

FEATURES

- Advanced High Cell Density Trench Technology
- Super Low Gate Charge
- Green Device Available

MARKING



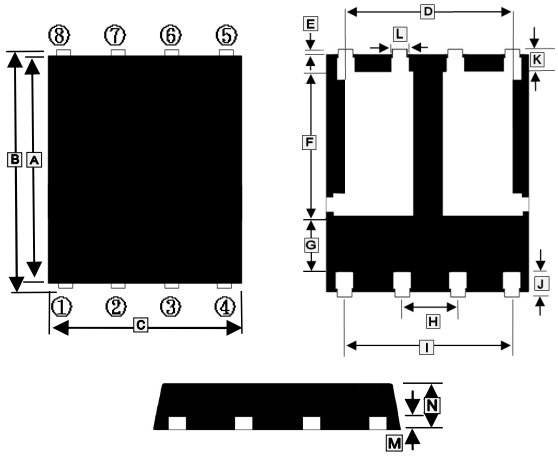
PACKAGE INFORMATION

Package	MPQ	Leader Size
DFN5x6-8D	3K	13 inch

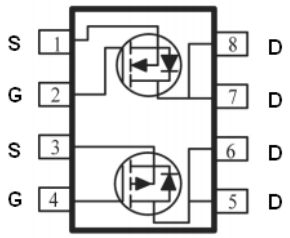
ORDER INFORMATION

Part Number	Type
SPRD4503-C	Lead (Pb)-free and Halogen-free

DFN5x6-8D



REF.	Millimeter Min.	Millimeter Max.	REF.	Millimeter Min.	Millimeter Max.
A	5.7	5.8	H	1.27 BSC.	
B	5.9	6.1	I	3.61	3.96
C	4.8	5	J	0.51	0.71
D	3.61	3.96	K	0.41	0.61
E	0.06	0.20	L	0.33	0.51
F	3.38	3.78	M	0.2	0.3
G	1.1	-	N	0.9	1.1



ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Ratings N-Ch	Ratings P-Ch	Unit
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	±20		V
Continuous Drain Current, @V_{GS}=10V [1]	T_C=25°C	I_D	28	-22	A
	T_C=100°C		18	-14	
	T_A=25°C		7	-5.4	
	T_A=70°C		5.6	-4.3	
Pulsed Drain Current [3]		I_{DM}	62	-48	A
Total Power Dissipation	T_C=25°C	P_D	22		W
Total Power Dissipation	T_A=25°C	P_D	1.7		
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55~150		°C
Thermal Data					
Thermal Resistance Junction-Ambient [1]		$R_{\theta JA}$	73.5		°C/W
Thermal Resistance Junction-Ambient [2]			125		
Thermal Resistance Junction-Case [1]		$R_{\theta JC}$	5.7		

N-CHANNEL ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	30	-	-	V	V_{GS}=0, I_D=250μA
Gate Threshold Voltage		$V_{GS(th)}$	1	-	3	V	V_{DS}=V_{GS}, I_D=250μA
Forward Transfer Conductance		g_{fs}	-	6	-	S	V_{DS}=5V, I_D=7A
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	T_J=25°C	I_{DSS}	-	-	1	μA	V_{DS}=24V, V_{GS}=0
	T_J=55°C		-	-	5		
Static Drain-Source On-Resistance [4]		$R_{DS(ON)}$	-	-	18	mΩ	V_{GS}=10V, I_D=6A
			-	-	28		V_{GS}=4.5V, I_D=4A
Total Gate Charge		Q_g	-	6	-	nC	I_D=6A V_{DS}=15V V_{GS}=4.5V
Gate-Source Charge		Q_{gs}	-	2.5	-		
Gate-Drain Change		Q_{gd}	-	2.1	-		
Turn-on Delay Time		$T_{d(on)}$	-	2.4	-	nS	V_{DS}=15V V_{GS}=10V I_D=6A R_G=3.3Ω
Rise Time		T_r	-	7.8	-		
Turn-off Delay Time		$T_{d(off)}$	-	22	-		
Fall Time		T_f	-	4	-		
Input Capacitance		C_{iss}	-	572	-	pF	V_{GS}=0 V_{DS}=15V f=1MHz
Output Capacitance		C_{oss}	-	80	-		
Reverse Transfer Capacitance		C_{rss}	-	65	-		
Source-Drain Diode							
Forward on Voltage [4]		V_{SD}	-	-	1.2	V	I_S=1A, V_{GS}=0, T_J=25°C
Continuous Source Current [1]		I_S	-	-	7	A	
Pulsed Source Current [3]		I_{SM}	-	-	28		

P-CHANNEL ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage		BV_{DSS}	-30	-	-	V	V_{GS}=0, I_D= -250μA
Gate Threshold Voltage		$V_{GS(th)}$	-1	-	-3	V	V_{DS}=V_{GS}, I_D= -250μA
Forward Transfer Conductance		g_{fs}	-	13	-	S	V_{DS}= -5V, I_D= -7A
Gate-Source Leakage Current		I_{GSS}	-	-	±100	nA	V_{GS}= ±20V
Drain-Source Leakage Current	T_J=25°C	I_{DSS}	-	-	-1	μA	V_{DS}= -24V, V_{GS}=0
	T_J=55°C		-	-	-5		
Static Drain-Source On-Resistance [4]		$R_{DS(ON)}$	-	-	30	mΩ	V_{GS}= -10V, I_D= -6A
			-	-	45		V_{GS}= -4.5V, I_D= -4A
Total Gate Charge		Q_g	-	9.8	-	nC	I_D= -6A V_{DS}= -20V V_{GS}= -4.5V
Gate-Source Charge		Q_{gs}	-	2.2	-		
Gate-Drain Change		Q_{gd}	-	3.4	-		
Turn-on Delay Time		$T_{d(on)}$	-	16.4	-	nS	V_{DS}= -24V V_{GS}= -10V I_D= -1A R_G=3.3Ω
Rise Time		T_r	-	20.2	-		
Turn-off Delay Time		$T_{d(off)}$	-	55	-		
Fall Time		T_f	-	10	-		
Input Capacitance		C_{iss}	-	930	-	pF	V_{GS}=0 V_{DS}= -15V f=1MHz
Output Capacitance		C_{oss}	-	148	-		
Reverse Transfer Capacitance		C_{rss}	-	115	-		
Source-Drain Diode							
Forward on Voltage [4]		V_{SD}	-	-	-1.2	V	I_S= -1A, V_{GS}=0, T_J=25°C
Continuous Source Current [1]		I_S	-	-	-5.4	A	
Pulsed Source Current [3]		I_{SM}	-	-	-21.6		

Notes:
1. Surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2. When mounted on Min. copper pad.
3. Pluse width limited by maximum junction temperature, pulse width≦300μs, duty cycle≦2%.
4. The data tested by pulsed, pulse width≦300μs, duty cycle≦2%.

N-CHANNEL CHARACTERISTIC CURVE

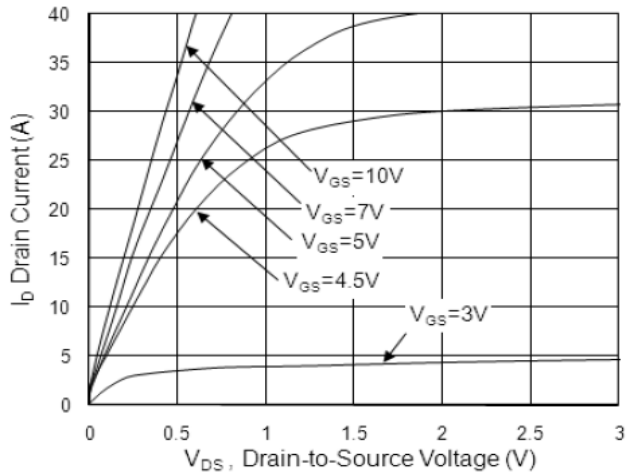


Fig.1 Typical Output Characteristics

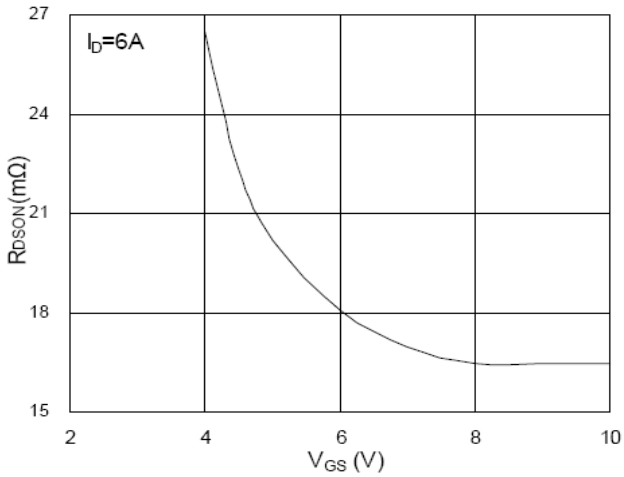


Fig.2 On-Resistance vs. Gate-Source

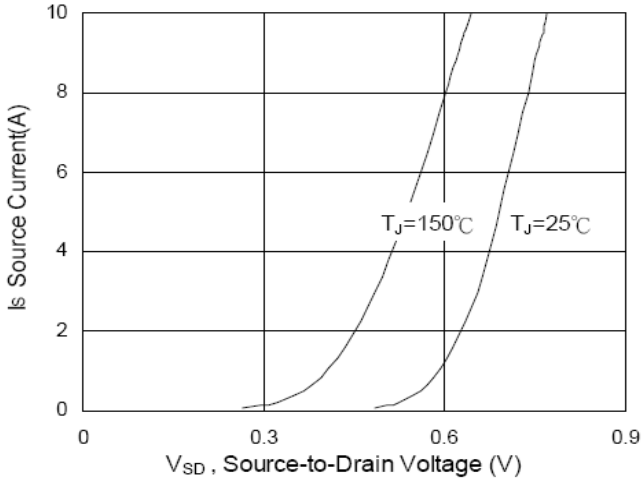


Fig.3 Forward Characteristics Of Reverse

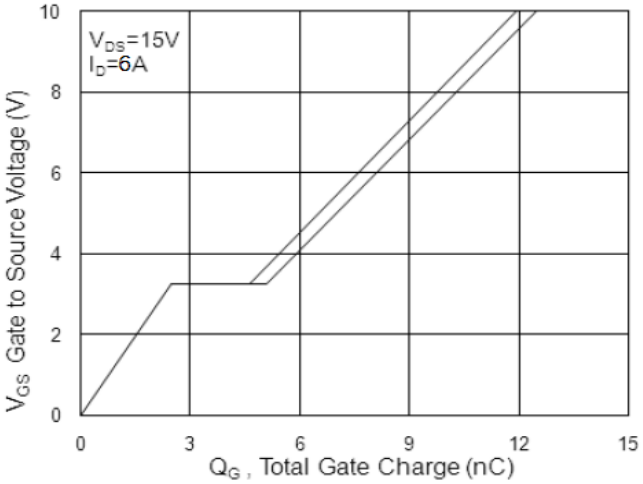


Fig.4 Gate-Charge Characteristics

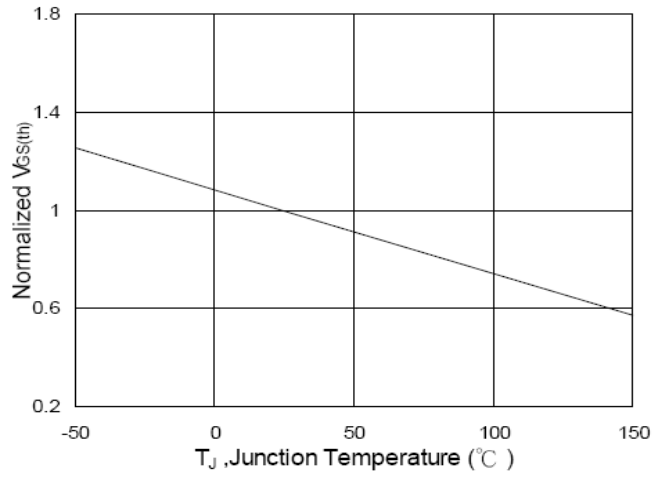


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

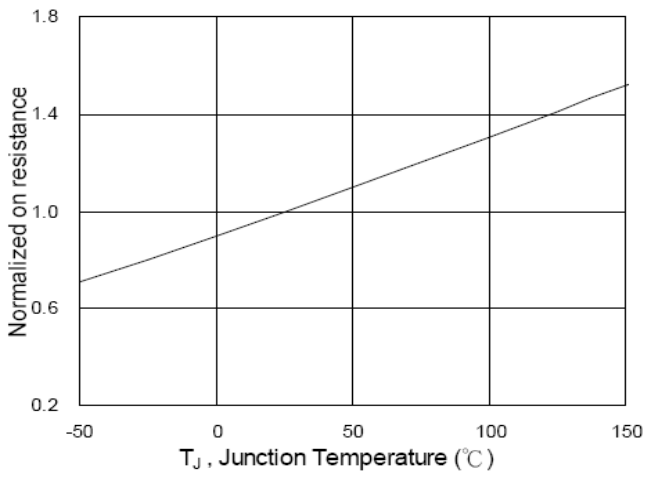


Fig.6 Normalized R_{DSON} vs. T_J

N-CHANNEL CHARACTERISTIC CURVE

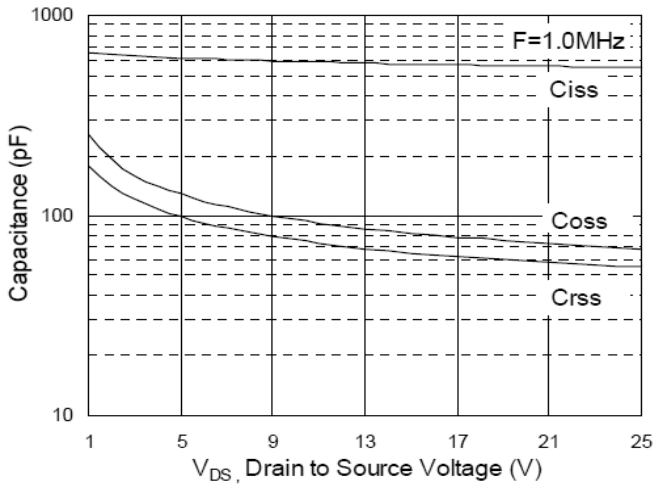


Fig.7 Capacitance

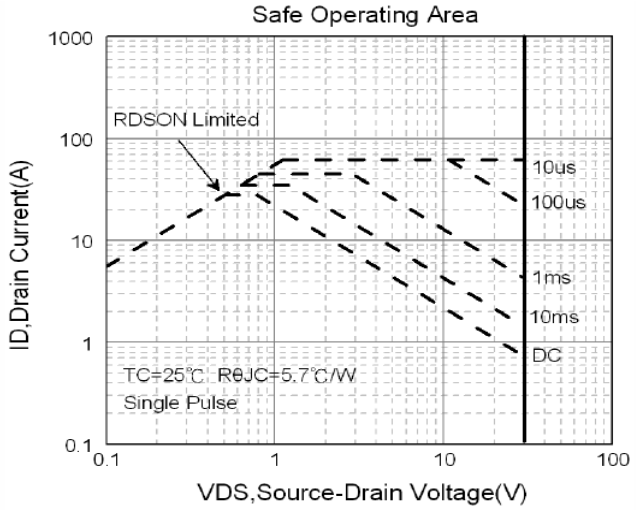


Fig.8 Safe Operating Area

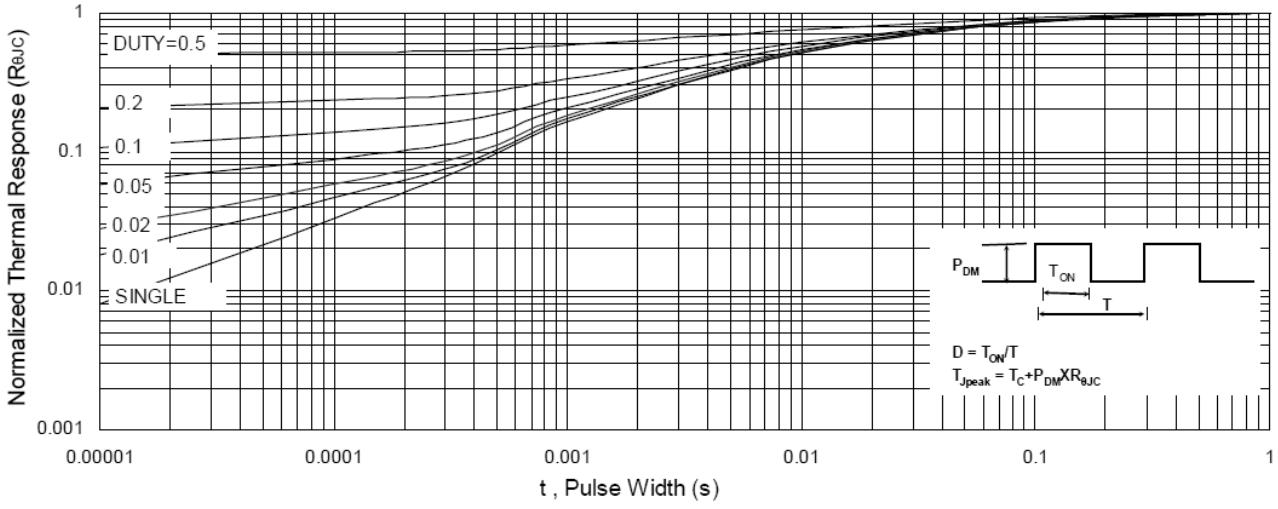


Fig.9 Normalized Maximum Transient Thermal Impedance

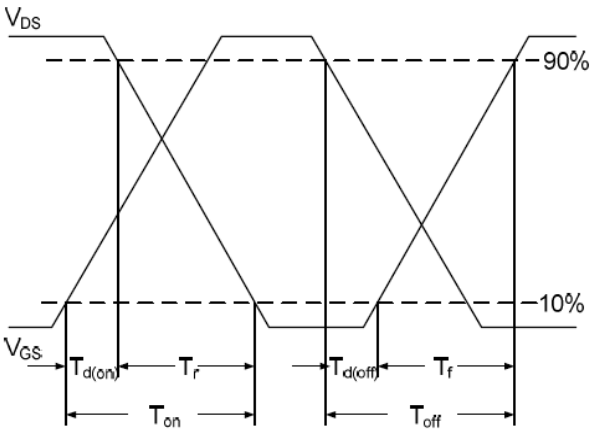


Fig.10 Switching Time Waveform

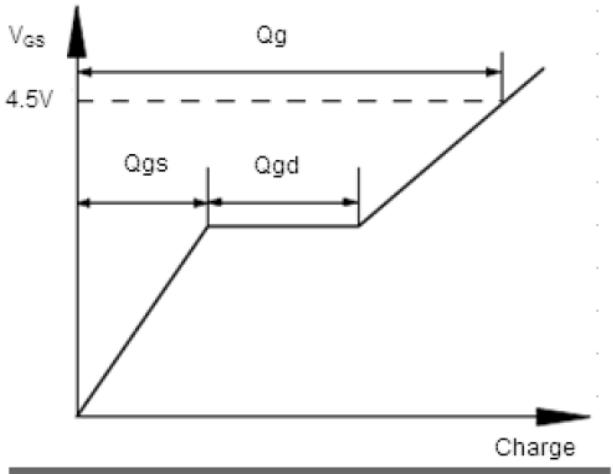


Fig.11 Gate Charge Waveform

P-CHANNEL CHARACTERISTIC CURVE

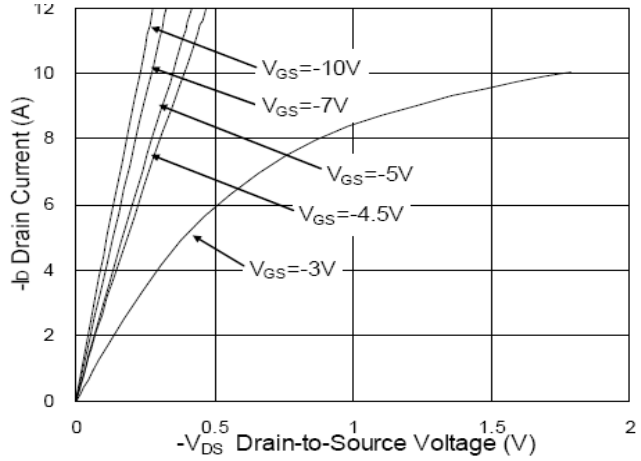


Fig.1 Typical Output Characteristics

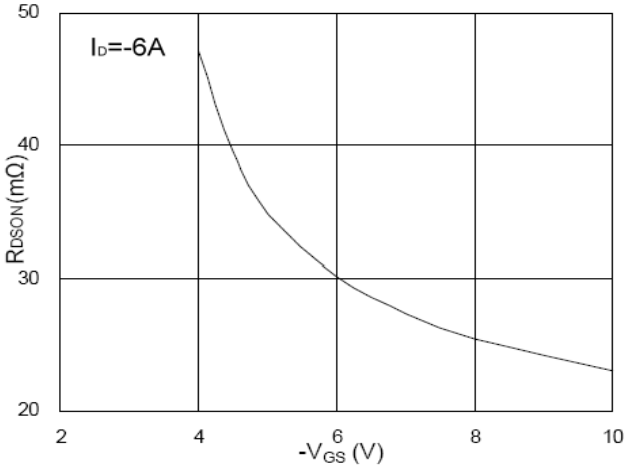


Fig.2 On-Resistance v.s Gate-Source

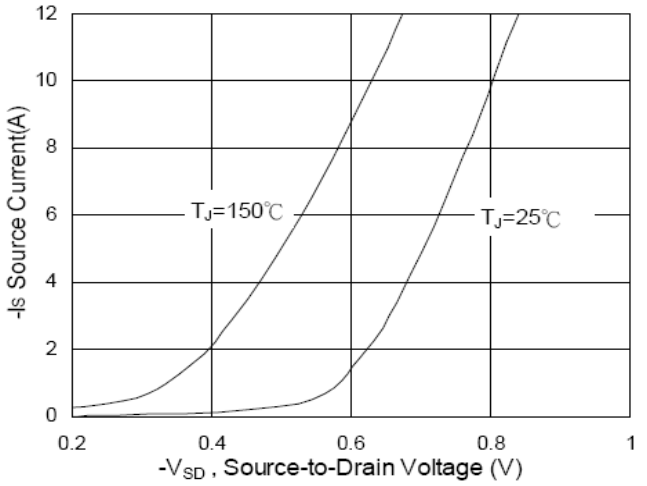


Fig.3 Forward Characteristics of Reverse

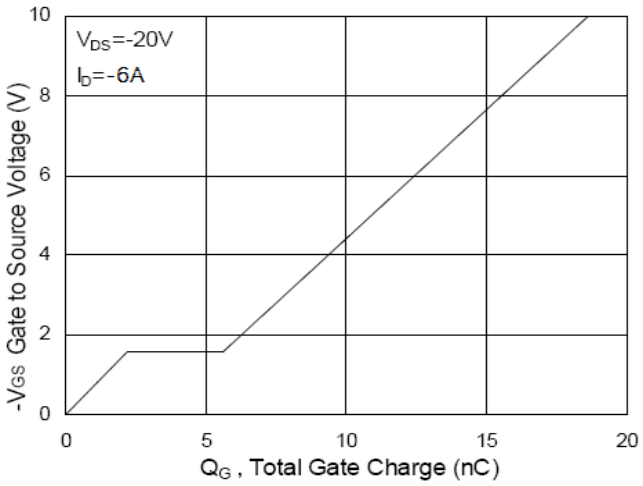


Fig.4 Gate-Charge Characteristics

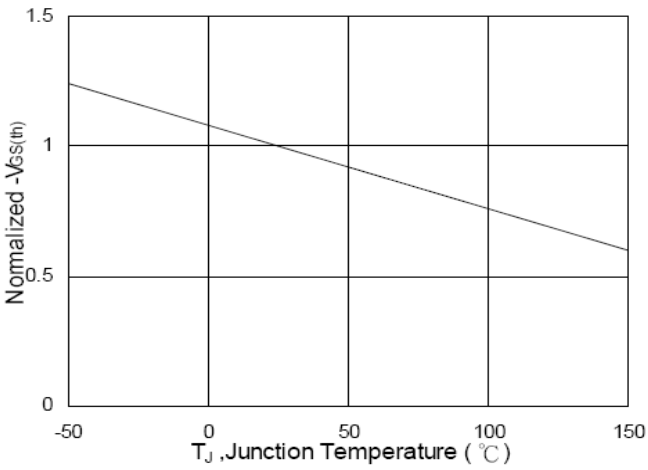


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

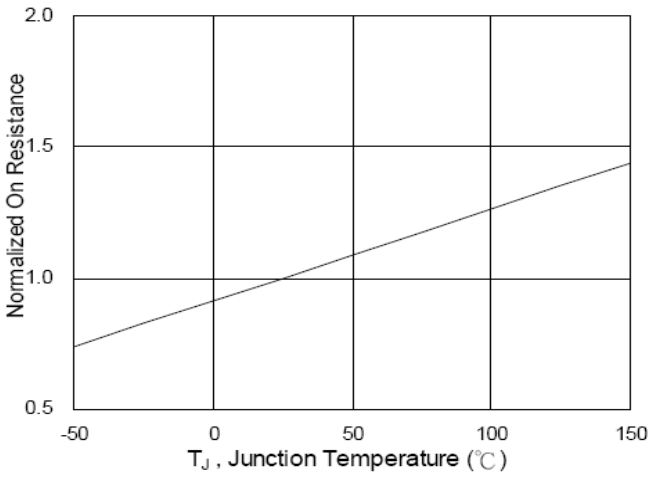


Fig.6 Normalized R_{DSON} v.s T_J

P-CHANNEL CHARACTERISTIC CURVE

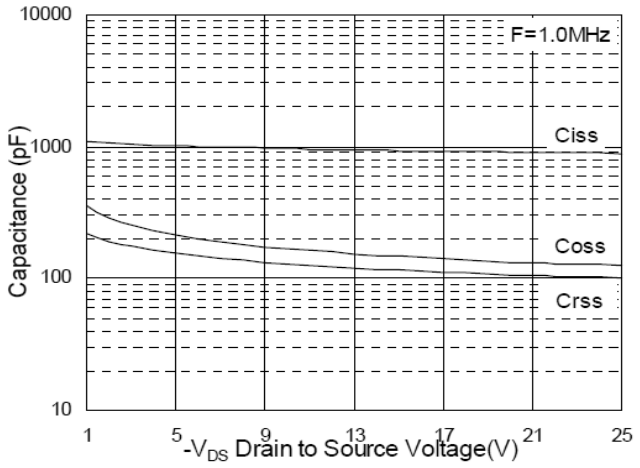


Fig.7 Capacitance

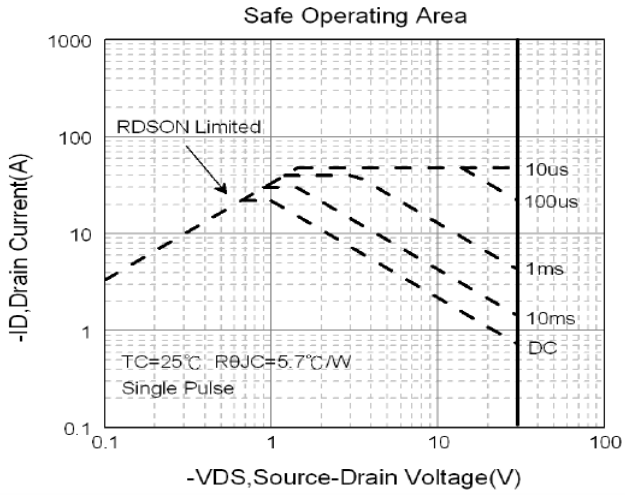


Fig.8 Safe Operating Area

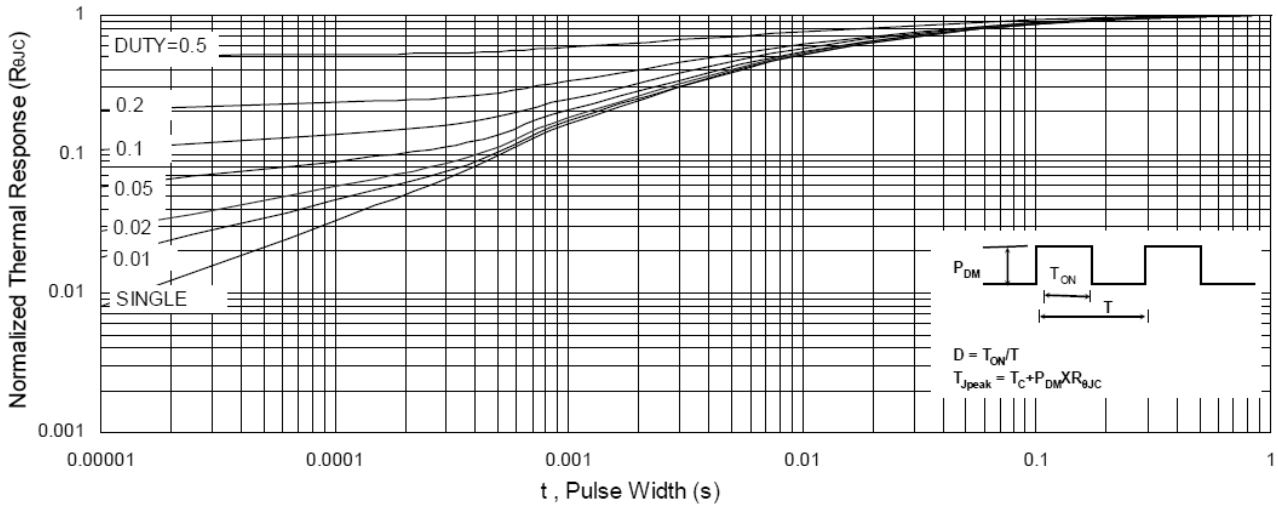


Fig.9 Normalized Maximum Transient Thermal Impedance

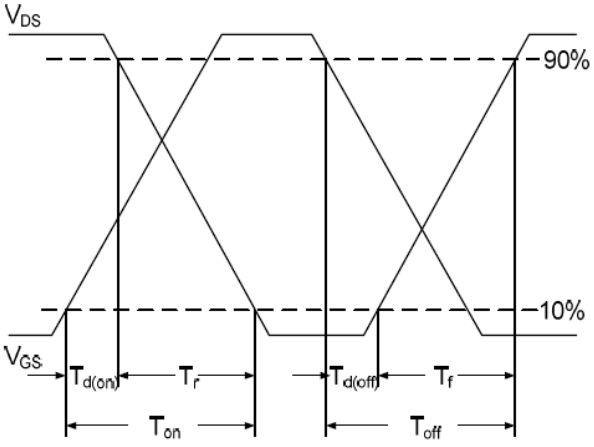


Fig.10 Switching Time Waveform

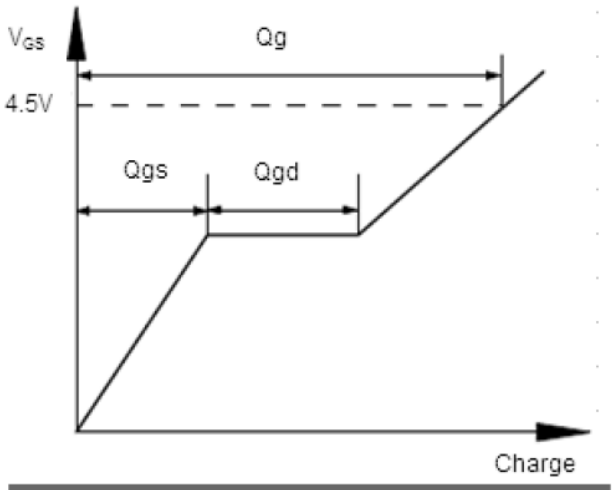


Fig.11 Gate Charge Waveform