

Radiation Hardened 5V 32-Channel Analog Multiplexer

ISL71831SEH

The [ISL71831SEH](#) is a radiation tolerant, 32-channel multiplexer that is fabricated using Intersil's proprietary P6-SOI process technology to provide excellent latch-up performance. It operates with a single supply range from 3V to 5.5V and has a 5-bit address line plus an enable that can be driven with adjustable logic thresholds to conveniently select one of 32 available channels. An inactive channel is separated from the active channel by a high impedance, which inhibits any interaction between them.

The ISL71831SEH's low $r_{DS(ON)}$ allows for improved signal integrity and reduced power losses. The ISL71831SEH is also designed for cold sparing, making it excellent for redundancy in high reliability applications. It is designed to provide a high impedance to the analog source in a powered off condition, making it easy to add additional backup devices without incurring extra power dissipation. The ISL71831SEH also has analog overvoltage protection on the input that disables the switch during an overvoltage event to protect upstream and downstream devices.

The ISL71831SEH is available in a 48 Ld CQFP and operates across the extended temperature range of -55°C to +125°C.

There is also a 16-channel version available offered in a 28 Ld CDIP. Refer to the [ISL71830SEH](#) datasheet for more information. For a list of differences, refer to [Table 1 on page 2](#).

Related Literature

- For a full list of related documents, visit our website
 - [ISL71831SEH](#) product page

Features

- DLA SMD# [5962-15248](#)
- Fabricated using P6 SOI process technology
- Rail-to-rail operation
- No latch-up
- Low $r_{DS(ON)}$ <120Ω (maximum)
- Single supply operation 3V to 5.5V
 - Adjustable logic threshold control
- Cold sparing capable -0.4V to 7V
- Analog overvoltage range -0.4V to 7V
- Switch input off leakage 120nA
- Transition times (t_{AHL}) 70ns
- Internally grounded metal lid
- Break-before-make switching
- ESD protection ≥5kV (HBM)
- Operating temperature range -55°C to +125°C
- Radiation tolerance
 - Low dose rate (0.01rad(Si)/s) 75krad(Si)
 - SEL/SEB LET_{TH} (V⁺ = 6.3V) 60MeV • cm²/mg

NOTE: All lots are assurance tested to 75krad (0.01rad(Si)/s) wafer-by-wafer.

Applications

- Telemetry signal processing
- Harsh environments
- Down-hole drilling

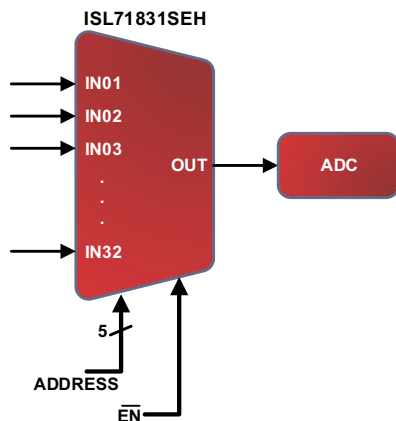


FIGURE 1. TYPICAL APPLICATION

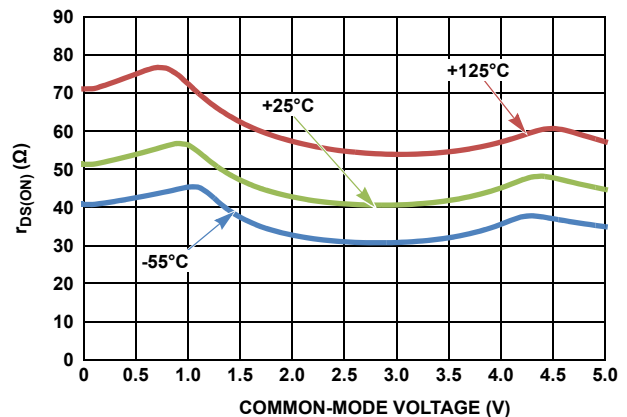


FIGURE 2. $r_{DS(ON)}$ vs COMMON-MODE VOLTAGE (V⁺ = 5V)

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Ordering Information

ORDERING NUMBER (Note 2)	PART NUMBER (Note 1)	TEMP RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
5962L1524801VXC	ISL71831SEHVF	-55 to +125	48 Ld CQFP	R48.A
N/A	ISL71831SEHF/PROTO	-55 to +125	48 Ld CQFP	R48.A
5962L1524801V9A	ISL71831SEHVX	-55 to +125	DIE	
N/A	ISL71831SEHX/SAMPLE	-55 to +125	DIE	
N/A	ISL71831SEHEV1Z	Evaluation Board		

NOTES:

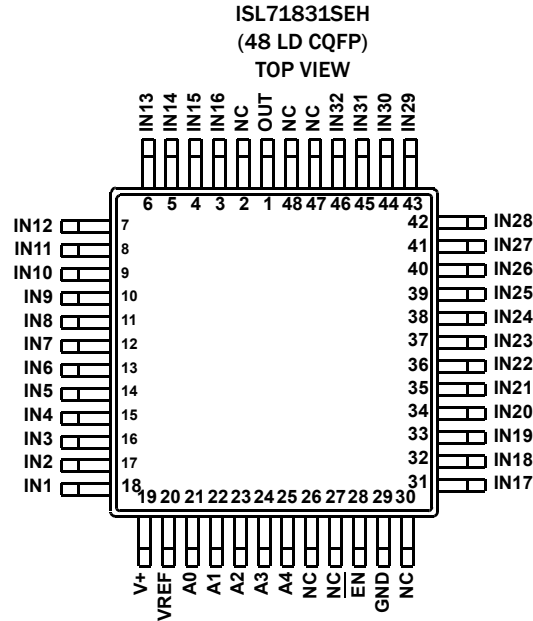
1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	NUMBER OF CHANNELS	OUTPUT LEAKAGE	PACKAGE
ISL71830SEH	16	60nA	28 Ld CDFP
ISL71831SEH	32	120nA	48 Ld CQFP

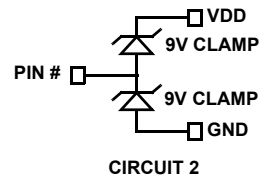
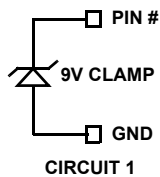
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Pin Configuration



Pin Descriptions

PIN NAME	ESD CIRCUIT	PIN NUMBER	DESCRIPTION
OUT	2	1	Output for multiplexer.
V ⁺	1	19	Positive power supply.
IN _x	1	3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46	Inputs for multiplexer.
A _x	1	21, 22, 23, 24, 25	Address lines for multiplexer.
$\overline{\text{EN}}$	1	28	Enable control for multiplexer (active low).
VREF	1	20	Reference voltage used to set logic thresholds.
GND	-	29	Ground
LID	-	-	Package lid is internally connected to GND (pin 29).
NC	-	2, 26, 27, 30, 47, 48	Not electrically connected.



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Absolute Maximum Ratings

Maximum Supply Voltage (V ⁺ to GND)	7V
Maximum Supply Voltage (V ⁺ to GND) (Note 5)	6.3V
Analog Input Voltage Range (INX)	-0.4V to 7V
Digital Input Voltage Range (EN, Ax)	(GND - 0.4V) to V _{REF}
V _{REF} to GND	7V
ESD Tolerance	
Human Body Model (Tested per MIL-STD-883 TM 3015)	5kV
Charged Device Model (Tested per JESD22-C101D)	250V
Machine Model (Tested per JESD22-A115-A)	250V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
48 Ld CQFP (Notes 3, 4)	59	5
Storage Temperature Range	-65°C to +150°C	

Recommended Operating Conditions

Ambient Operating Temperature Range	-55°C to +125°C
Maximum Operating Junction Temperature	+150°C
Supply Voltage	3V to 5.5V
V _{REF} to GND	3V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See Tech Brief [TB379](#) for details.
- For θ_{JC} , the "case temp" location is the center of the package underside.
- Tested in a heavy ion environment at LET = 60MeV • cm²/mg at +125°C.

Electrical Specifications (V⁺ = 5V)

GND = 0V, V_{REF} = 3.3V, V_{IH} = 3.3V, V_{IL} = 0V, T_A = +25°C, unless otherwise noted. Boldface limits apply across the operating temperature range, -55°C to +125°C.; over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
Analog Input Signal Range	V _{IN}		0		V ⁺	V
Channel On-Resistance	r _{DS(ON)}	V ⁺ = 4.5V, V _{IN} = 0V to V ⁺ I _{OUT} = 1mA	-	40	120	Ω
r _{DS(ON)} Match between Channels	Δr _{DS(ON)}	V ⁺ = 4.5V, V _{IN} = 0V, 2.25V, 4.5V I _{OUT} = 1mA	-	-	5	Ω
On-Resistance Flatness	r _{FLAT(ON)}	V ⁺ = 4.5V, V _{IN} = 0V to V ⁺	-	-	40	Ω
Switch Input Off Leakage	I _{IN(OFF)}	V ⁺ = 5.5V, V _{IN} = 5V, Unused inputs and V _{OUT} = 0.5V	-30	-	30	nA
		V ⁺ = 5.5V, V _{IN} = 0.5V, Unused inputs and V _{OUT} = 5V	-30	-	30	nA
Switch Input Off Overvoltage Leakage	I _{IN(OFF-OV)}	V ⁺ = 5.5V, V _{IN} = 7V, Unused inputs and V _{OUT} = 0V T _A = +25°C, -55°C	-30	-	30	nA
		T _A = +125°C	-30	-	120	nA
		Post radiation, +25°C	-30	-	30	nA
Switch Input Off Leakage with Supply Voltage Grounded	I _{IN(POWER-OFF)}	V _{IN} = 7V, V _{OUT} = 0V V ⁺ = V _{EN} = V _{REF} = 0V T _A = +25°C, -55°C	-20	-	20	nA
		T _A = +125°C	-20	-	100	nA
		Post radiation, +25°C	-20	-	20	nA
Switch Input Off Leakage with Supply Voltage Open	I _{IN(POWER-OFF)}	V _{IN} = 7V, V _{OUT} = 0V V ⁺ = V _{EN} = V _{REF} = Open, T _A = +25°C, -55°C	-20	-	20	nA
		T _A = +125°C	-20	-	100	nA
		Post radiation, +25°C	-20	-	20	nA
Switch On Input Leakage with Overvoltage Applied to the Input	I _{IN(ON-OV)}	V ⁺ = 5.5V, V _{IN} = 7V V _{OUT} = Open	2.75	-	5.50	μA

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Electrical Specifications ($V^+ = 5V$) $GND = 0V$, $V_{REF} = 3.3V$, $V_{IH} = 3.3V$, $V_{IL} = 0V$, $T_A = +25^\circ C$, unless otherwise noted.

Boldface limits apply across the operating temperature range, $-55^\circ C$ to $+125^\circ C$.; over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of $<10\text{mrad(Si)/s}$. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
Switch Output Off Leakage	$I_{OUT(OFF)}$	$V^+ = 5.5V$, $V_{OUT} = 5V$ All inputs = 0.5V, $T_A = +25^\circ C$, $-55^\circ C$	-30	-	30	nA
		$T_A = +125^\circ C$	0	-	200	nA
		Post radiation, $+25^\circ C$	-30	-	30	nA
		$V^+ = 5.5V$, $V_{OUT} = 0.5V$ All inputs = 5V, $T_A = +25^\circ C$, $-55^\circ C$	-30	-	30	nA
		$T_A = +125^\circ C$	-60	-	0	nA
		Post radiation, $+25^\circ C$	-30	-	30	nA
Switch Output Leakage with Switch Enabled	$I_{OUT(ON)}$	$V^+ = 5.5V$, $V_{IN} = V_{OUT} = 5V$ All unused inputs at 0.5V $T_A = +25^\circ C$, $-55^\circ C$	-30	-	30	nA
		$T_A = +125^\circ C$	0	-	200	nA
		Post radiation, $+25^\circ C$	-30	-	30	nA
		$V^+ = 5.5V$, $V_{IN} = V_{OUT} = 0.5V$ All unused inputs at 5V $T_A = +25^\circ C$, $-55^\circ C$	-30	-	30	nA
		$T_A = +125^\circ C$	-60	-	0	nA
		Post radiation, $+25^\circ C$	-30	-	30	nA
Logic Input Voltage High/Low	$V_{IH/L}$	$V^+ = 5.5V$ $V_{REF} = 3.3V$	1.3	-	1.6	V
Input Current with V_{AH} , V_{ENH}	I_{AH} , I_{ENH}	$V^+ = 5.5V$ $V_{EN} = V_A = V_{REF}$	-0.1	-	0.1	μA
Input Current with V_{AL} , V_{ENL}	I_{AL} , I_{ENL}	$V^+ = 5.5V$ $V_{EN} = V_A = 0V$	-0.1	-	0.1	μA
Quiescent Supply Current	I_{SUPPLY}	$V^+ = V_{REF} = V_{EN} = 5.5V$ $V_A = 0V$, $T_A = +25^\circ C$, $-55^\circ C$	-	-	100	nA
		$T_A = +125^\circ C$	-	-	500	nA
		Post radiation, $+25^\circ C$	-	-	300	nA
Reference Quiescent Supply Current	I_{REF}	$V^+ = V_{REF} = V_{EN} = 5.5V$ $V_A = 0V$	-	-	200	nA
DYNAMIC						
Addressing Transition Time	t_{AHL}	$V^+ = 4.5V$; Figure 3	10	-	70	ns
Break-Before-Make Delay	t_{BBM}	$V^+ = 4.5V$; Figure 5	5	18	40	ns
Enable Turn-On Time	$t_{EN(ON)}$	$V^+ = 4.5V$; Figure 4	-	-	40	ns
Enable Turn-Off Time	$t_{EN(OFF)}$	$V^+ = 4.5V$; Figure 4	-	-	50	ns
Charge Injection	V_{CTE}	$C_L = 100\text{pF}$, $V_{IN} = 0V$, Figure 6	-	1.4	5.0	pC
Off Isolation	V_{ISO}	$V_{EN} = V_{REF}$, $R_L = \text{open}$, $f = 1\text{kHz}$	60	-	-	dB
Crosstalk	V_{CT}	$V_{EN} = 0V$, $f = 1\text{kHz}$, $V_{P,P} = 1V$ $R_L = \text{open}$	73	-	-	dB
Input Capacitance	$C_{IN(OFF)}$	$f = 1\text{MHz}$	-	-	5	pF
Output Capacitance	$C_{OUT(OFF)}$	$f = 1\text{MHz}$	-	-	25	pF

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Electrical Specifications ($V^+ = 3.3V$) $V_{REF} = 3.3V, V_{IH} = 3.3V, V_{IL} = 0V, T_A = +25^\circ C$, unless otherwise noted.

Boldface limits apply across the operating temperature range, $-55^\circ C$ to $+125^\circ C$.; over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of $<10\text{mrad(Si)/s}$.

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{IN}	Analog Input Signal Range		0		V^+	V
$r_{DS(ON)}$	Channel On-Resistance	$V^+ = 3V, V_{IN} = 0V$ to V^+ $I_{OUT} = 1\text{mA}$	25	70	200	Ω
$\Delta r_{DS(ON)}$	$r_{DS(ON)}$ Match Between Channels	$V^+ = 3V, V_{IN} = 0.5V, 2.5V$ $I_{OUT} = 1\text{mA}$	-	-	5	Ω
$r_{FLAT(ON)}$	On-Resistance Flatness	$V^+ = 3V, V_{IN} = 0V$ to V^+	-	-	50	Ω
$I_{IN(OFF)}$	Switch Input Off Leakage	$V^+ = 3.6V, V_{IN} = 3.1V,$ Unused inputs and $V_{OUT} = 0.5V$	-30	-	30	nA
		$V^+ = 3.6V, V_{IN} = 0.5V,$ Unused inputs and $V_{OUT} = 3.1V$	-30	-	30	nA
$I_{IN(OFF-OV)}$	Switch Input Off Overvoltage Leakage	$V^+ = 3.6V, V_{IN} = 7V,$ Unused inputs and $V_{OUT} = 0V,$ $T_A = +25^\circ C, -55^\circ C$	-30	-	30	nA
		$T_A = +125^\circ C$	-30	-	100	nA
		Post radiation, $+25^\circ C$	-30	-	30	nA
$I_{IN(ON-OV)}$	Switch On Input Leakage with Overvoltage Applied to the Input	$V^+ = 3.6V, V_{IN} = 7V$ $V_{OUT} = \text{OPEN}$	1.8	-	3.6	μA
$I_{OUT(OFF)}$	Switch Output Off Leakage	$V^+ = 3.6V, V_{OUT} = 3.1V,$ All inputs = $0.5V,$ $T_A = +25^\circ C, -55^\circ C$	-30	-	30	nA
		$T_A = +125^\circ C$	0	-	120	nA
		Post radiation, $+25^\circ C$	-30	-	30	nA
		$V^+ = 3.6V, V_{OUT} = 0.5V,$ All inputs = $3.1V,$ $T_A = +25^\circ C, -55^\circ C$	-30	-	30	nA
		$T_A = +125^\circ C$	0	-	30	nA
$I_{OUT(ON)}$	Switch Output Leakage with Switch Enabled	$V^+ = 3.6V, V_{IN} = V_{OUT} = 3.1V$ All unused inputs at $0.5V,$ $T_A = +25^\circ C, -55^\circ C$	-30	-	30	nA
		$T_A = +125^\circ C$	0	-	120	nA
		Post radiation, $+25^\circ C$	-30	-	30	nA
		$V^+ = 3.6V, V_{IN} = V_{OUT} = 0.5V$ All unused inputs at $3.1V,$ $T_A = +25^\circ C, -55^\circ C$	-30	-	30	nA
		$T_A = +125^\circ C$	0	-	30	nA
I_{SUPPLY}	Quiescent Supply Current	$V^+ = V_{REF} = V_{EN} = 3.6V$ $V_A = 0V, T_A = +25^\circ C, -55^\circ C$	-	-	100	nA
		$T_A = +125^\circ C$	-	-	300	nA
		Post radiation, $+25^\circ C$	-	-	300	nA
I_{REF}	Reference Quiescent Supply Current	$V^+ = V_{REF} = V_{EN} = 3.6V, V_A = 0V$	-	-	200	nA

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Electrical Specifications ($V^+ = 3.3V$) $V_{REF} = 3.3V, V_{IH} = 3.3V, V_{IL} = 0V, T_A = +25^\circ C$, unless otherwise noted.

Boldface limits apply across the operating temperature range, $-55^\circ C$ to $+125^\circ C$.; over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of $<10\text{mrad(Si)/s}$. (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
DYNAMIC						
t_{AHL}	Addressing Transition Time	$V^+ = 3V$; Figure 3	10	-	100	ns
t_{BBM}	Break-Before-Make Delay	$V^+ = 3V$; Figure 5	5	15	50	ns
$t_{EN(ON)}$	Enable Turn-On Time	$V^+ = 3V$; Figure 4	-	-	60	ns
$t_{EN(OFF)}$	Enable Turn Off Time	$V^+ = 3V$; Figure 4	-	-	80	ns

NOTE:

- Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

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TABLE 2. TRUTH TABLE

A4	A3	A2	A1	A0	$\overline{\text{EN}}$	"ON"-CHANNEL
X	X	X	X	X	1	None
0	0	0	0	0	0	1
0	0	0	0	1	0	2
0	0	0	1	0	0	3
0	0	0	1	1	0	4
0	0	1	0	0	0	5
0	0	1	0	1	0	6
0	0	1	1	0	0	7
0	0	1	1	1	0	8
0	1	0	0	0	0	9
0	1	0	0	1	0	10
0	1	0	1	0	0	11
0	1	0	1	1	0	12
0	1	1	0	0	0	13
0	1	1	0	1	0	14
0	1	1	1	0	0	15
0	1	1	1	1	0	16
1	0	0	0	0	0	17
1	0	0	0	1	0	18
1	0	0	1	0	0	19
1	0	0	1	1	0	20
1	0	1	0	0	0	21
1	0	1	0	1	0	22
1	0	1	1	0	0	23
1	0	1	1	1	0	24
1	1	0	0	0	0	25
1	1	0	0	1	0	26
1	1	0	1	0	0	27
1	1	0	1	1	0	28
1	1	1	0	0	0	29
1	1	1	0	1	0	30
1	1	1	1	0	0	31
1	1	1	1	1	0	32

Note: X = Don't care, "1" = Logic High, "0" = Logic Low

Timing Diagrams

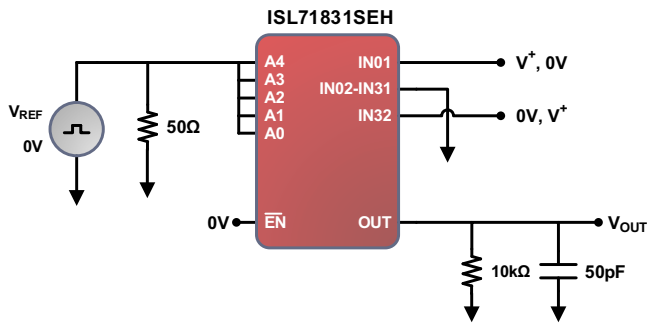


FIGURE 3. ADDRESS TIME TO OUTPUT TEST CIRCUIT

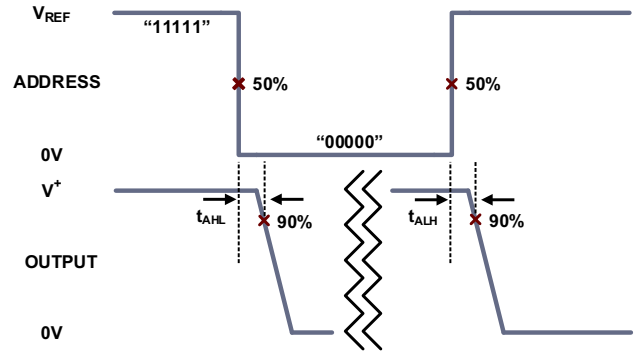


FIGURE 4. ADDRESS TIME TO OUTPUT DIAGRAM

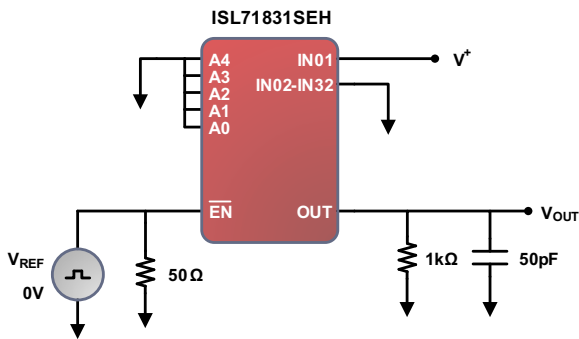


FIGURE 5. TIME TO ENABLE/DISABLE OUTPUT TEST CIRCUIT

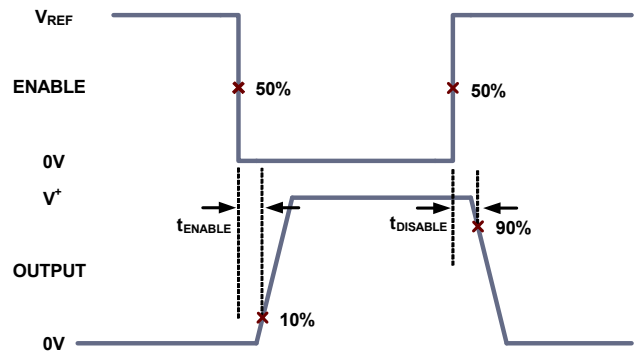


FIGURE 6. TIME TO ENABLE/DISABLE OUTPUT DIAGRAM

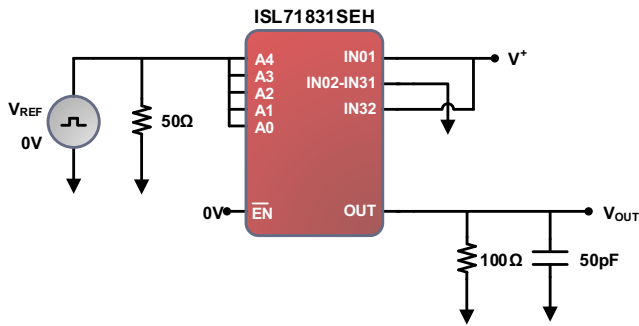


FIGURE 7. BREAK-BEFORE-MAKE TEST CIRCUIT

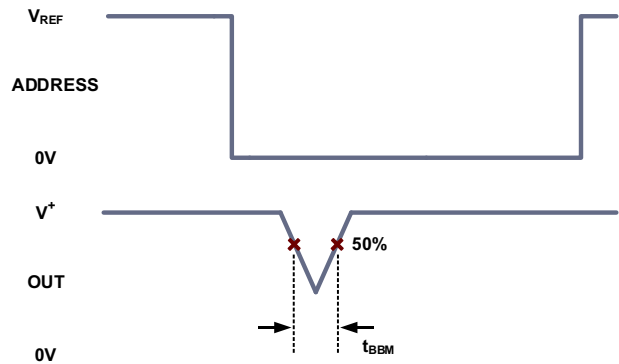


FIGURE 8. BREAK-BEFORE-MAKE DIAGRAM

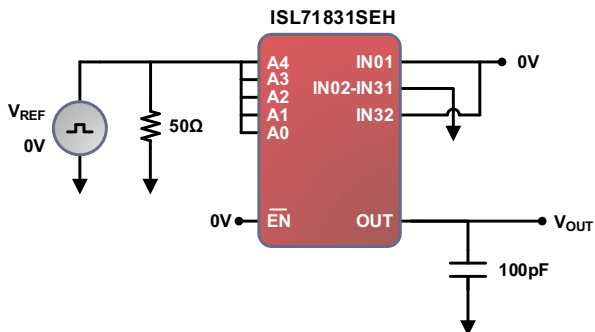


FIGURE 9. CHARGE INJECTION TEST CIRCUIT

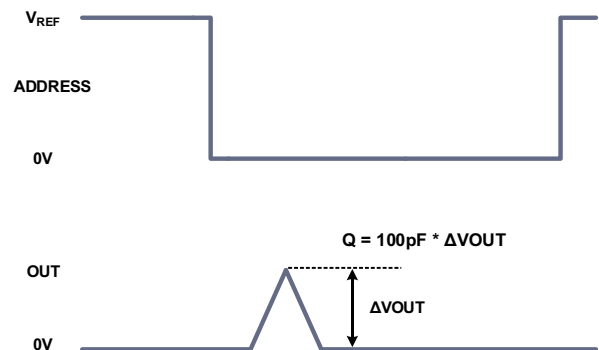


FIGURE 10. CHARGE INJECTION DIAGRAM

Typical Performance Curves

$V^+ = 5V$, $V_{REF} = 3.3V$, $V_{IN} = 0V$, $R_L = \text{Open}$, $T_A = +25^\circ\text{C}$,
unless otherwise specified.

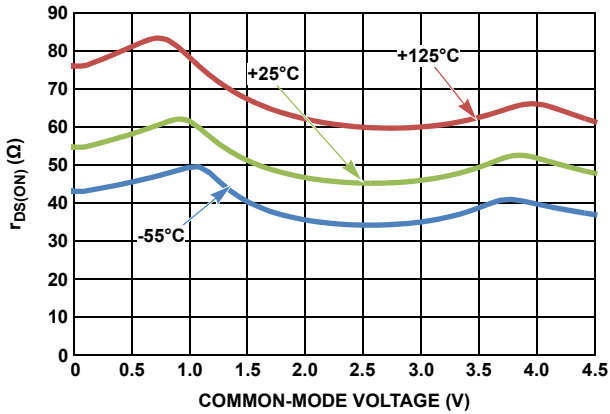


FIGURE 11. $r_{DS(ON)}$ vs COMMON-MODE VOLTAGE ($V^+ = 4.5V$)

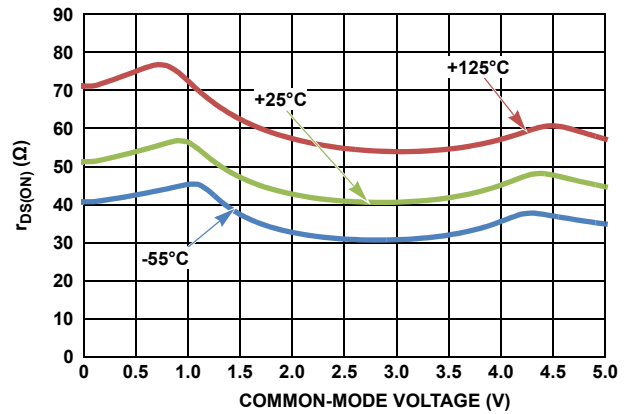


FIGURE 12. $r_{DS(ON)}$ vs COMMON-MODE VOLTAGE ($V^+ = 5V$)

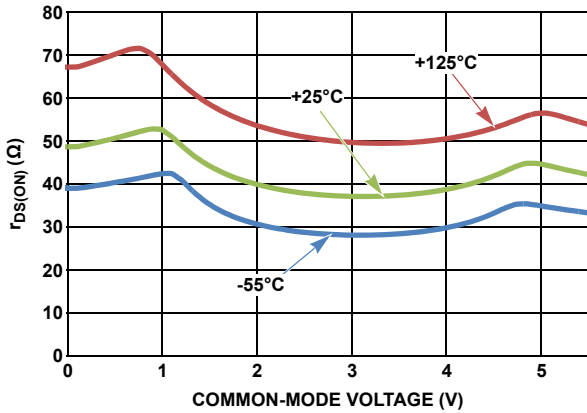


FIGURE 13. $r_{DS(ON)}$ vs COMMON-MODE VOLTAGE ($V^+ = 5.5V$)

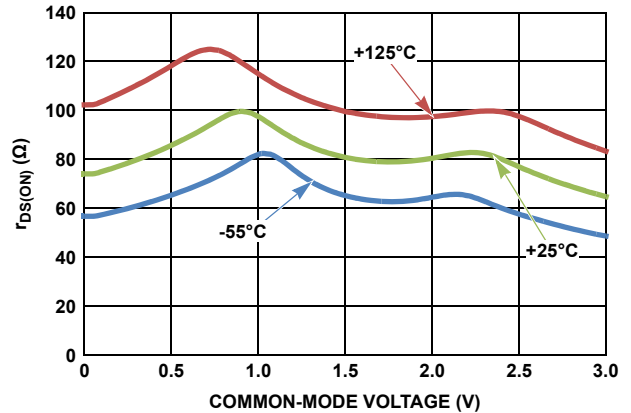


FIGURE 14. $r_{DS(ON)}$ vs COMMON-MODE VOLTAGE ($V^+ = 3V$)

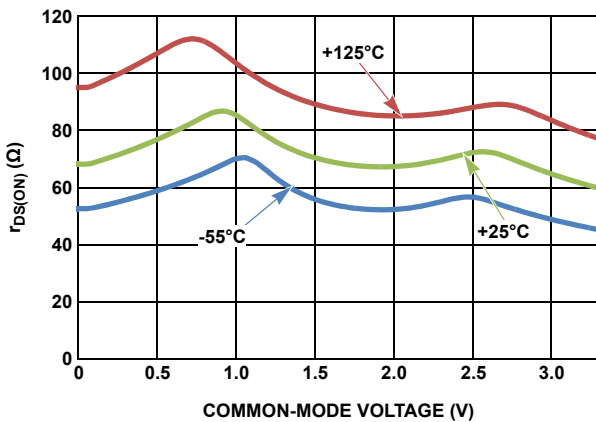


FIGURE 15. $r_{DS(ON)}$ vs COMMON-MODE VOLTAGE ($V^+ = 3.3V$)

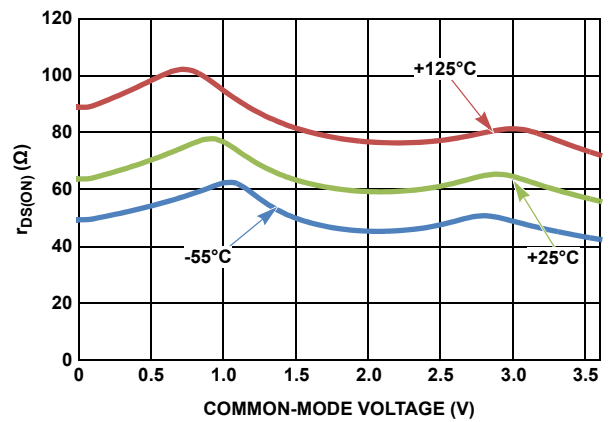


FIGURE 16. $r_{DS(ON)}$ vs COMMON-MODE VOLTAGE ($V^+ = 3.6V$)

Typical Performance Curves

unless otherwise specified. (Continued)

$V^+ = 5V, V_{REF} = 3.3V, V_{IN} = 0V, R_L = \text{Open}, T_A = +25^\circ\text{C}$,

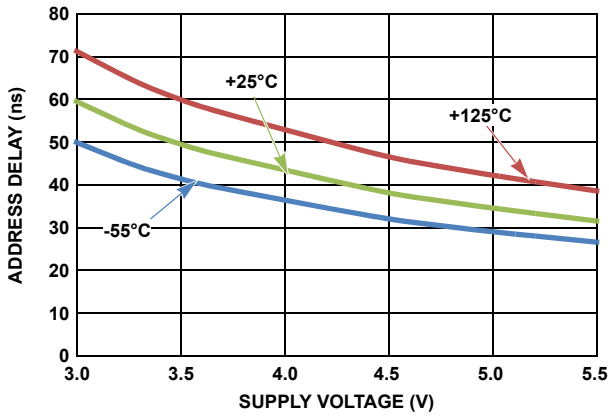


FIGURE 17. ADDRESS PROPAGATION DELAY (HIGH TO LOW)

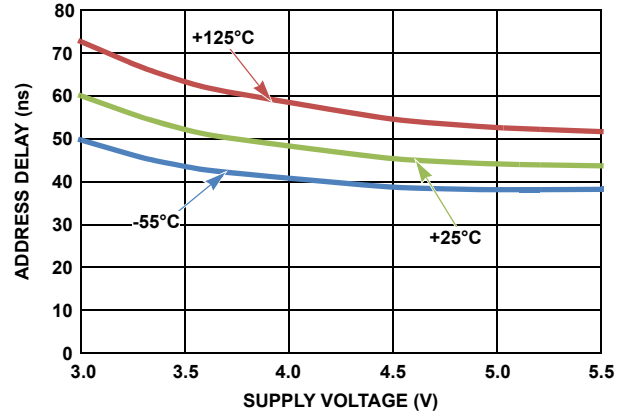


FIGURE 18. ADDRESS PROPAGATION DELAY (LOW TO HIGH)

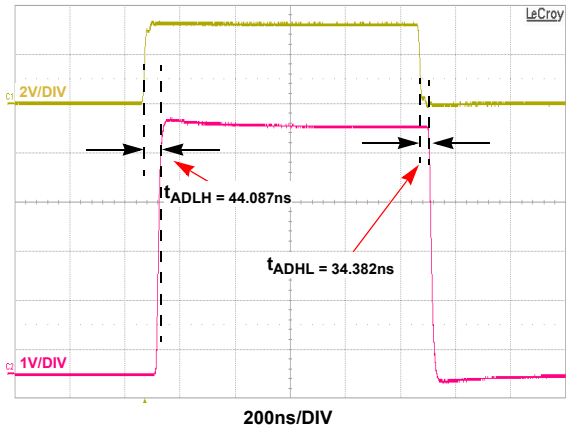


FIGURE 19. ADDRESS PROPAGATION DELAY

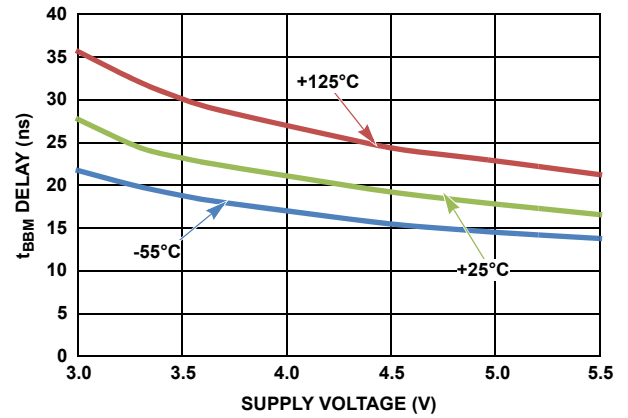


FIGURE 20. BREAK-BEFORE-MAKE DELAY

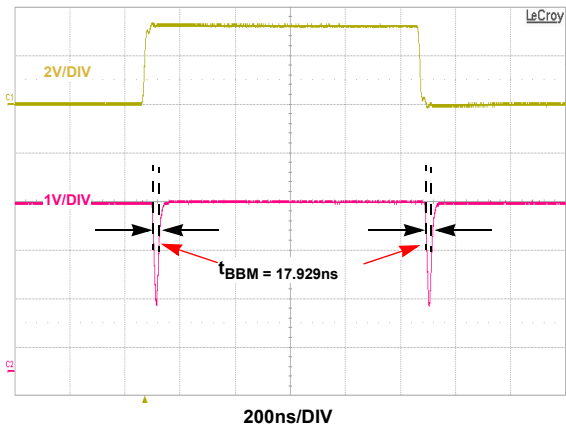


FIGURE 21. BREAK-BEFORE-MAKE DELAY

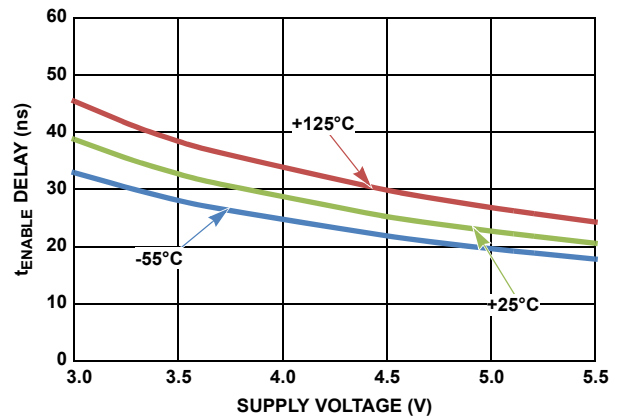


FIGURE 22. ENABLE TO OUTPUT PROPAGATION DELAY

Typical Performance Curves $V^+ = 5V, V_{REF} = 3.3V, V_{IN} = 0V, R_L = \text{Open}, T_A = +25^\circ\text{C}$, unless otherwise specified. (Continued)

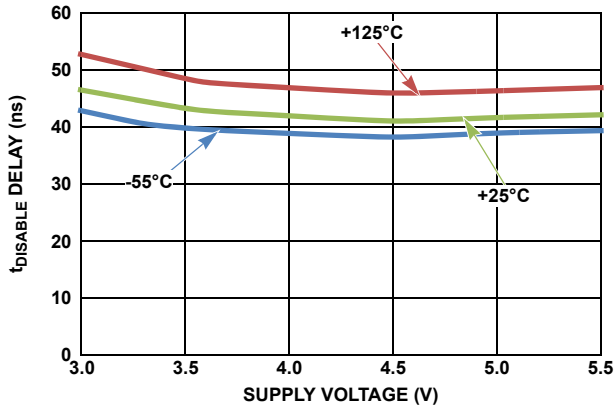


FIGURE 23. DISABLE TO OUTPUT PROPAGATION DELAY

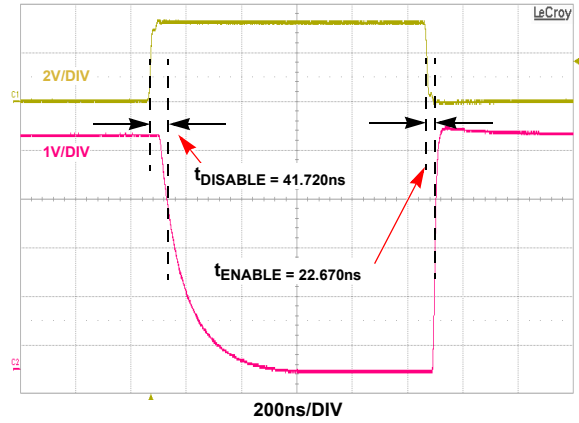


FIGURE 24. ENABLE/DISABLE PROPAGATION DELAY

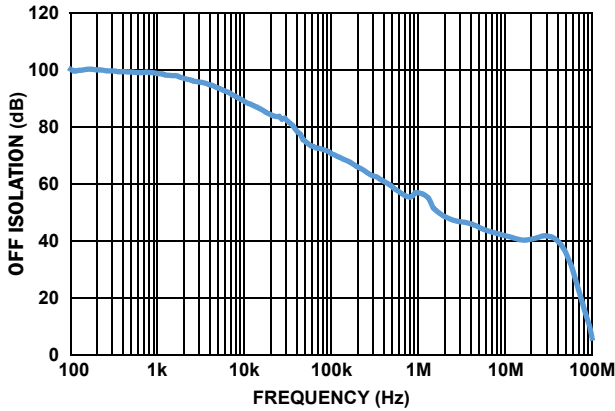


FIGURE 25. OFF ISOLATION ($V^+ = 5V, +25^\circ\text{C}, R_L = 511\Omega$)

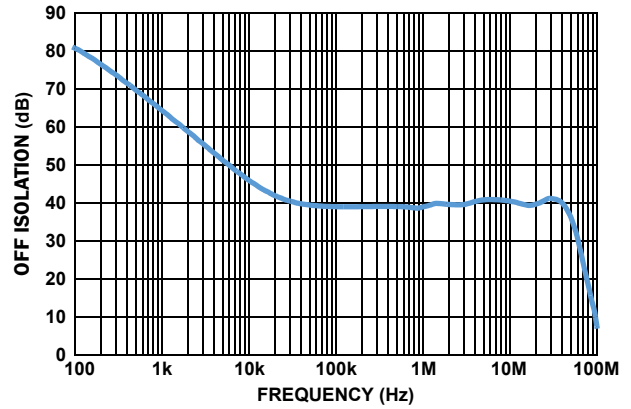


FIGURE 26. OFF ISOLATION ($V^+ = 5V, +25^\circ\text{C}, R_L = \text{OPEN}$)

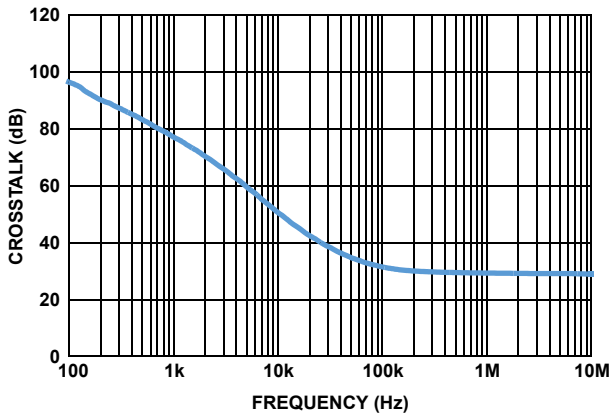


FIGURE 27. CROSSTALK ($V^+ = 5V, +25^\circ\text{C}, R_L = \text{OPEN}$)

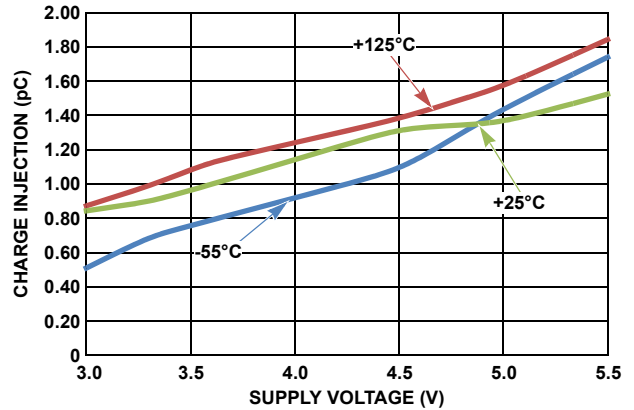


FIGURE 28. CHARGE INJECTION

Post Low Dose Rate Radiation Characteristics ($V^+ = 5V$)

Unless otherwise specified, $V^+ = 5V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25^\circ C$. This data is typical mean test data post radiation exposure at a low dose rate of $<10\text{mrad(Si)}/s$. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed.

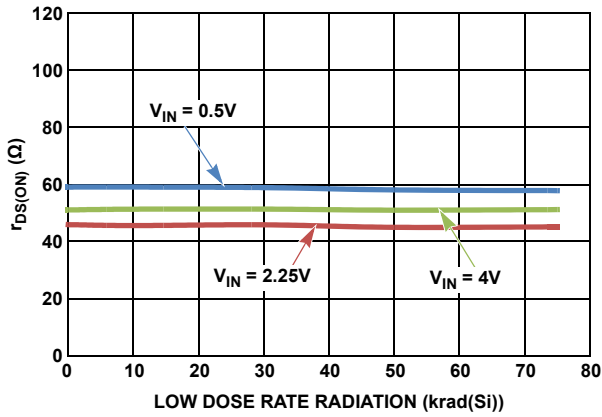


FIGURE 29. $r_{DS(ON)}$ ($V^+ = 4.5V$), BIASED

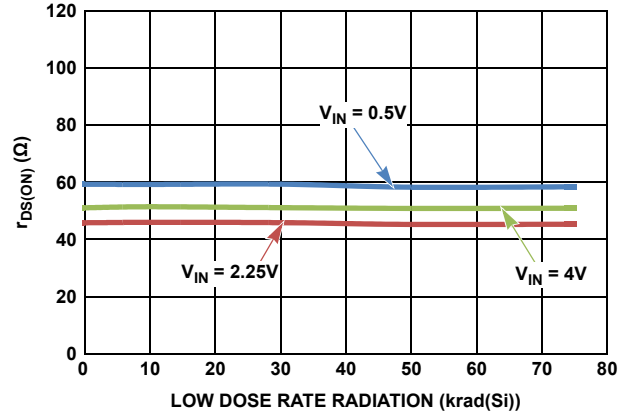


FIGURE 30. $r_{DS(ON)}$ ($V^+ = 4.5V$), GROUNDED

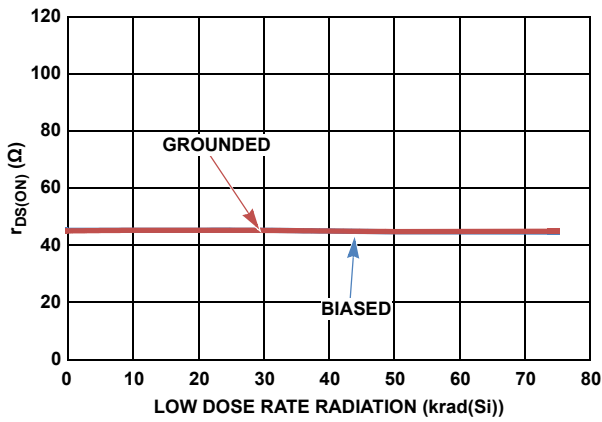


FIGURE 31. $r_{DS(ON)}$ MINIMUM ($V^+ = 4.5V$)

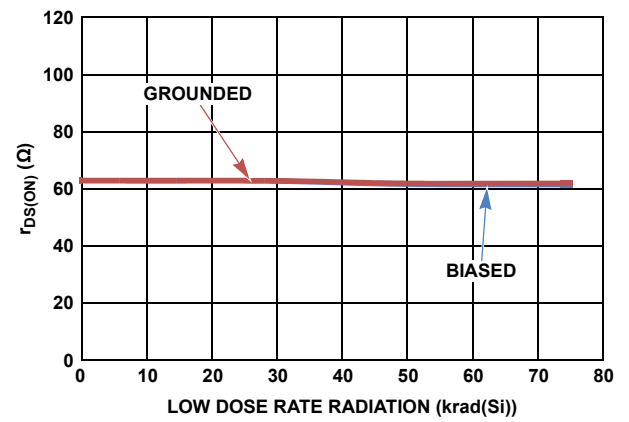


FIGURE 32. $r_{DS(ON)}$ MAXIMUM ($V^+ = 4.5V$)

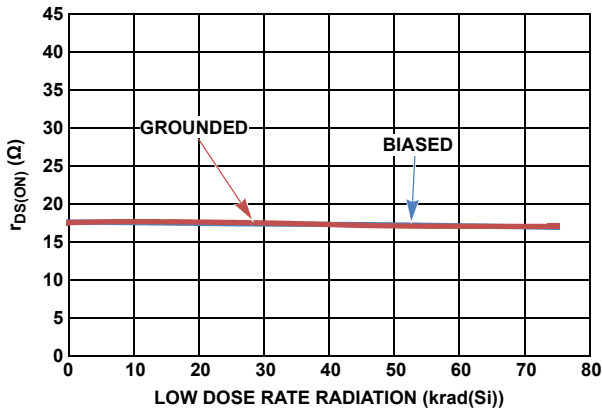


FIGURE 33. $r_{DS(ON)}$ FLATNESS ($V^+ = 4.5V$)

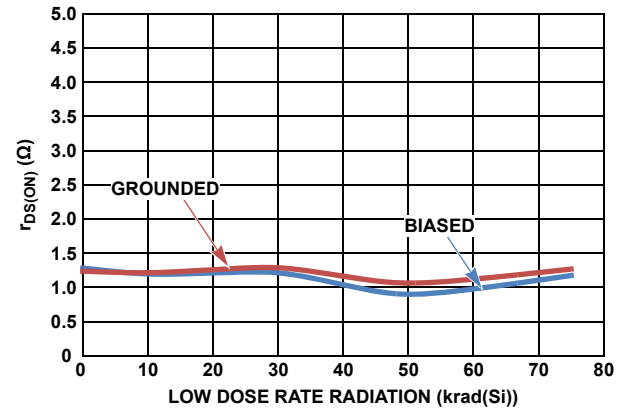


FIGURE 34. $r_{DS(ON)}$ MATCH ($V^+ = 4.5V$, $V_{IN} = 0.5V$)

Post Low Dose Rate Radiation Characteristics ($V^+ = 5V$)

Unless otherwise specified, $V^+ = 5V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25^\circ C$. This data is typical mean test data post radiation exposure at a low dose rate of $<10\text{mrad(Si)}/s$. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed. (Continued)

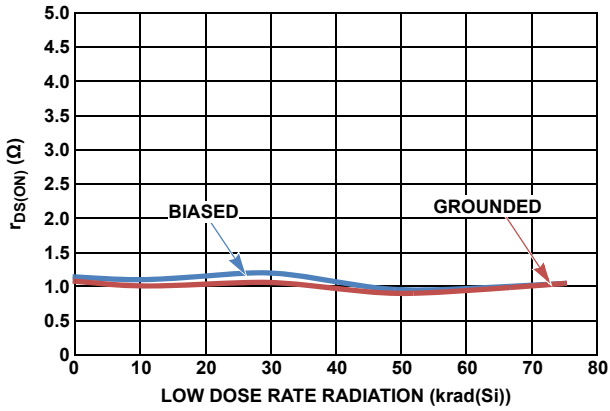


FIGURE 35. $r_{DS(ON)}$ MATCH ($V^+ = 4.5V$, $V_{IN} = 4V$)

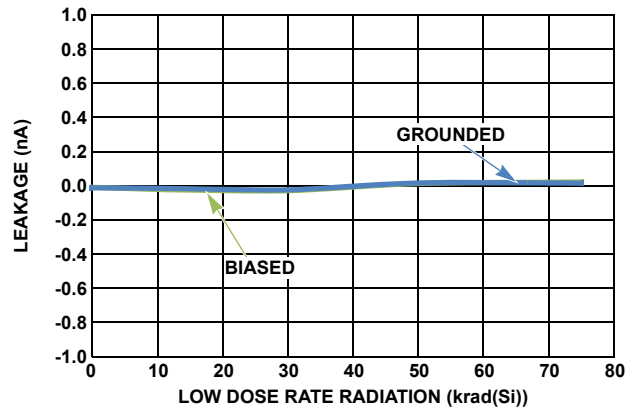


FIGURE 36. $I_{S(OFF)}$ ($V^+ = 5.5V$, $V_{IN} = 5V$)

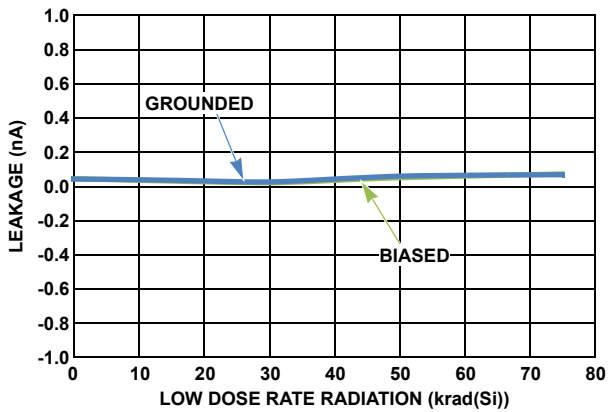


FIGURE 37. $I_{S(OFF)}$ ($V^+ = 5.5V$, $V_{IN} = 7V$)

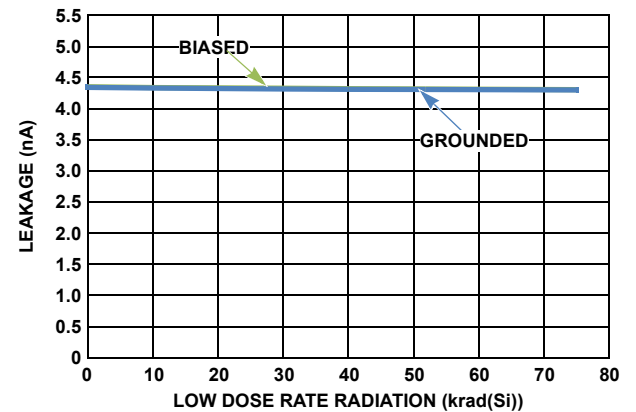


FIGURE 38. $I_{S(ON)}$ ($V^+ = 5.5V$, $V_{IN} = 5V$)

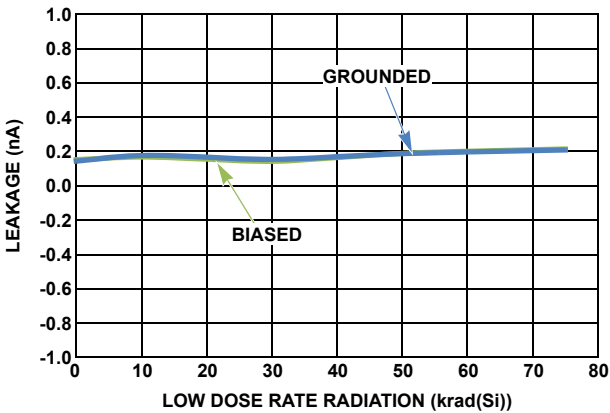


FIGURE 39. $I_{D(ON)}$ ($V^+ = 5.5V$, $V_{IN} = 5V$)

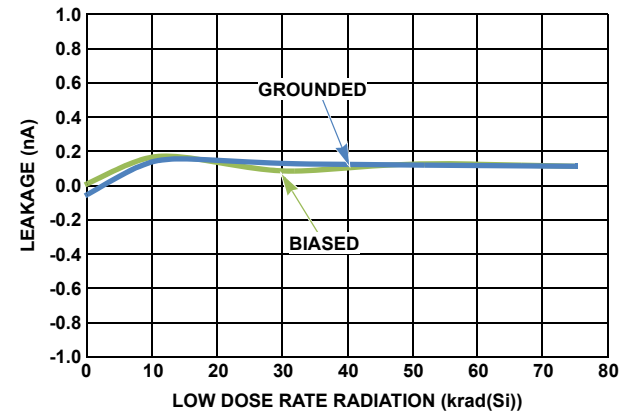


FIGURE 40. $I_{D(OFF)}$ ($V^+ = 3.6V$, $V_{IN} = 3.1V$)

Post Low Dose Rate Radiation Characteristics ($V^+ = 3.3V$) Unless otherwise specified, $V^+ = 3.3V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25^\circ C$. This data is typical mean test data post radiation exposure at a low dose rate of $<10\text{mrad(Si)/s}$. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed.

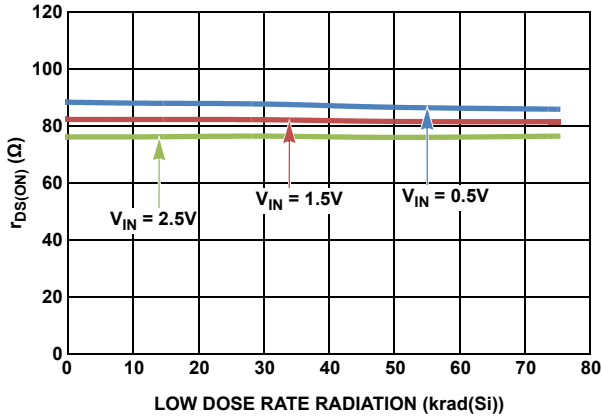


FIGURE 41. $r_{DS(ON)}$ ($V^+ = 3V$), BIASED

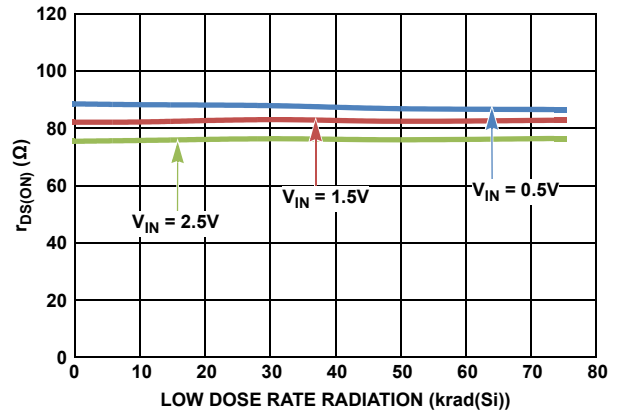


FIGURE 42. $r_{DS(ON)}$ ($V^+ = 3V$) - GROUND

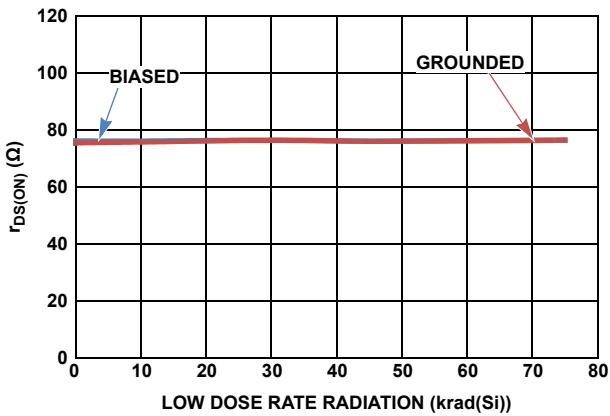


FIGURE 43. $r_{DS(ON)}$ MINIMUM ($V^+ = 3V$)

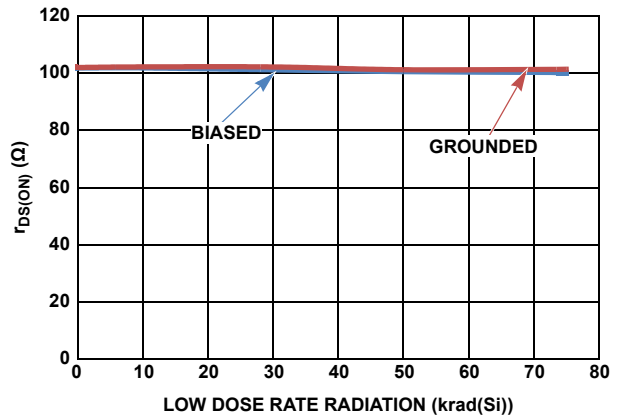


FIGURE 44. $r_{DS(ON)}$ MAXIMUM ($V^+ = 3V$)

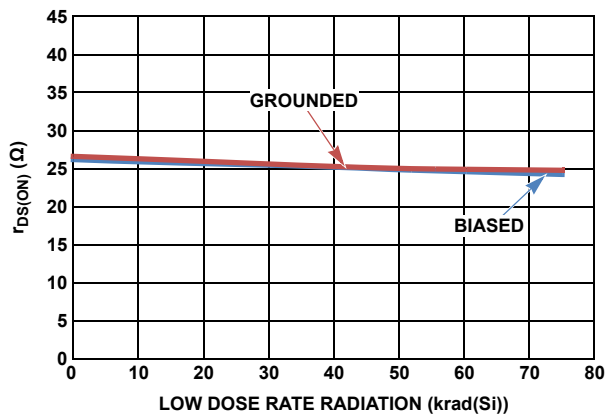


FIGURE 45. $r_{DS(ON)}$ FLATNESS ($V^+ = 3V$)

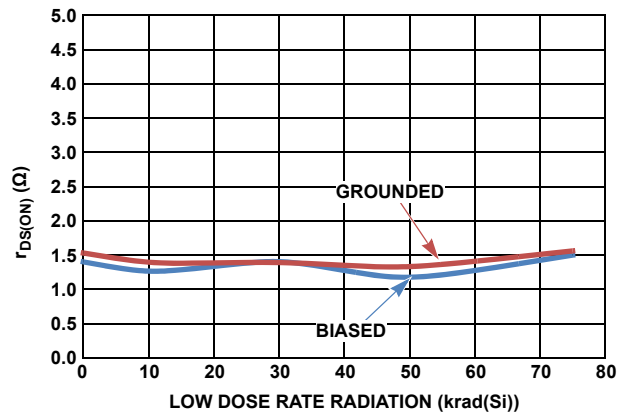


FIGURE 46. $r_{DS(ON)}$ MATCH ($V^+ = 3V$, $V_{IN} = 0.5V$)

Post Low Dose Rate Radiation Characteristics ($V^+ = 3.3V$) Unless otherwise specified, $V^+ = 3.3V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25^\circ C$. This data is typical mean test data post radiation exposure at a low dose rate of $<10\text{mrad(Si)}/\text{s}$. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed. **(Continued)**

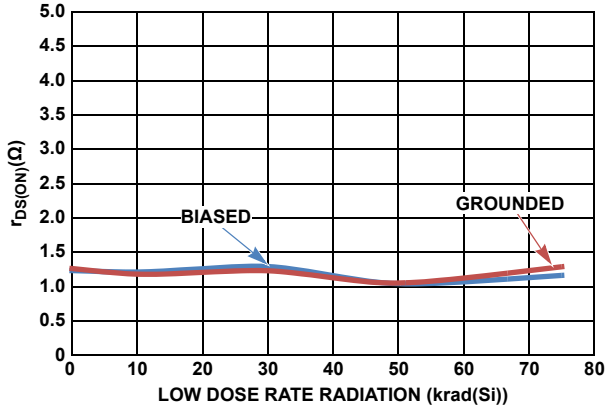


FIGURE 47. $r_{DS(ON)}$ MATCH ($V^+ = 3V$, $V_{IN} = 2.5V$)

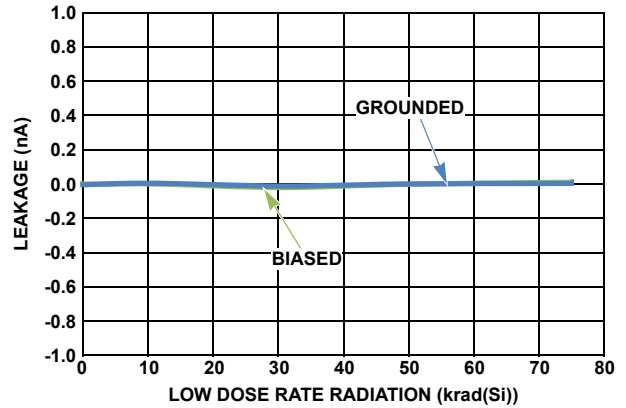


FIGURE 48. $I_{S(OFF)}$ ($V^+ = 3.6V$, $V_{IN} = 3.1V$)

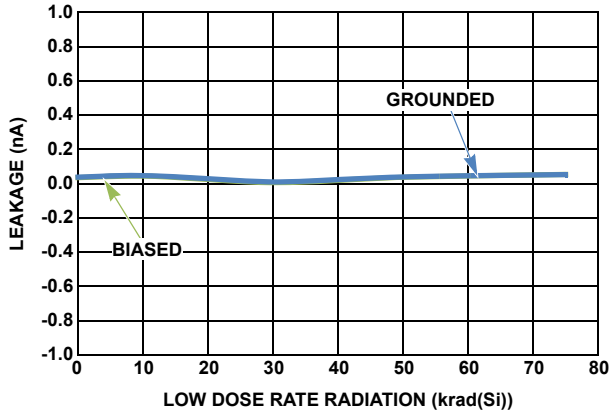


FIGURE 49. $I_{S(OFF)}$ ($V^+ = 3.6V$, $V_{IN} = 7V$)

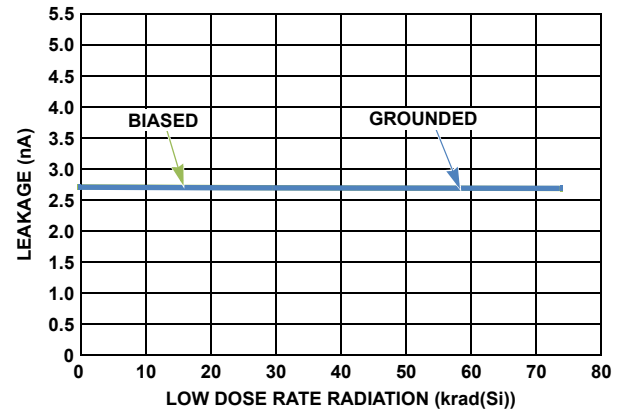


FIGURE 50. $I_{S(ON)}$ ($V^+ = 3.6V$, $V_{IN} = 7V$)

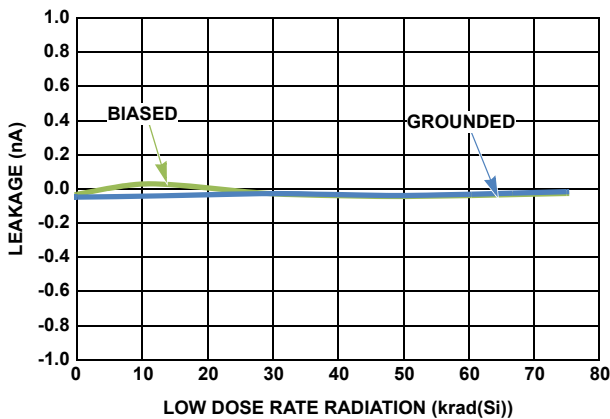


FIGURE 51. $I_{D(ON)}$ ($V^+ = 3.6V$, $V_{IN} = 3.1V$)

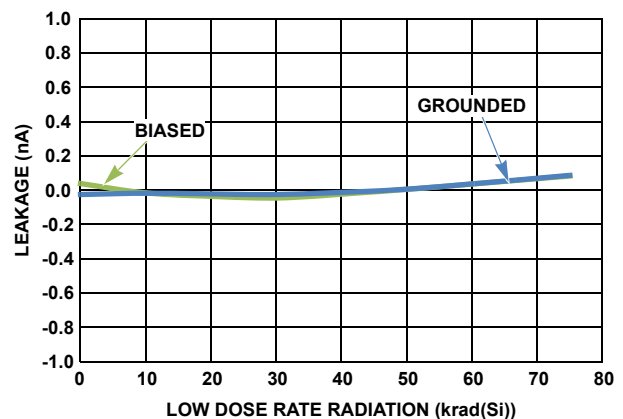


FIGURE 52. $I_{D(OFF)}$ ($V^+ = 3.6V$, $V_{IN} = 3.1V$)

Applications Information

Power-Up Considerations

The circuit is designed to be insensitive to any given power-up sequence between V+ and VREF, however, it is recommended that all supplies power-up relatively close to each other.

Overvoltage Protection

The ISL71831SEH has overvoltage protection on both the input as well as the output. On the output, the voltage is limited to a diode past the rails. Each of the inputs has independent overvoltage protection that works regardless of the switch being selected. If a switch experiences an overvoltage condition, the switch is turned off. As soon as the voltage returns within the rails, the switch returns to normal operation.

VREF and Logic Functionality

The VREF pin sets the logic threshold for the ISL71831SEH. The range for VREF is between 3V and 5.5V. The switching point is set to around 50% of the voltage presented to VREF. This switching point allows for both 5V and 3.3V logic control.

ISL71830SEH vs ISL71831SEH

A 16-channel version of the ISL71831SEH is available in a 28 Ld CDFP. In terms of performance specs, the parts are very similar in behavior. Apart from the apparent increase in channel density, the ISL71831SEH does have slightly higher output leakage compared to the ISL71830SEH due to having more channels connected to the output. The supply current for the ISL71831SEH is also a bit higher compared to the ISL71830SEH.

For additional products, see www.intersil.com/en/products.html

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ISL71831SEH

Die Characteristics

Die Dimensions

3102 μ m x 2800 μ m (122.1260 mils x 110.2362 mils)
Thickness: 483 μ m \pm 25 μ m (19 mils \pm 1 mil)

Interface Materials

GLASSIVATION

Type: 12k Å Silicon Nitride on 3k Å Oxide

TOP METALLIZATION

Type: 300 Å TiN on 2.8 μ m AlCu
In Bondpads, TiN has been removed.

BACKSIDE FINISH

Silicon

PROCESS

P6SOI

Assembly Related Information

SUBSTRATE POTENTIAL

Floating

Additional Information

WORST CASE CURRENT DENSITY

1.6 x 10⁵ A/cm²

TRANSISTOR COUNT

7734

Weight of Packaged Device

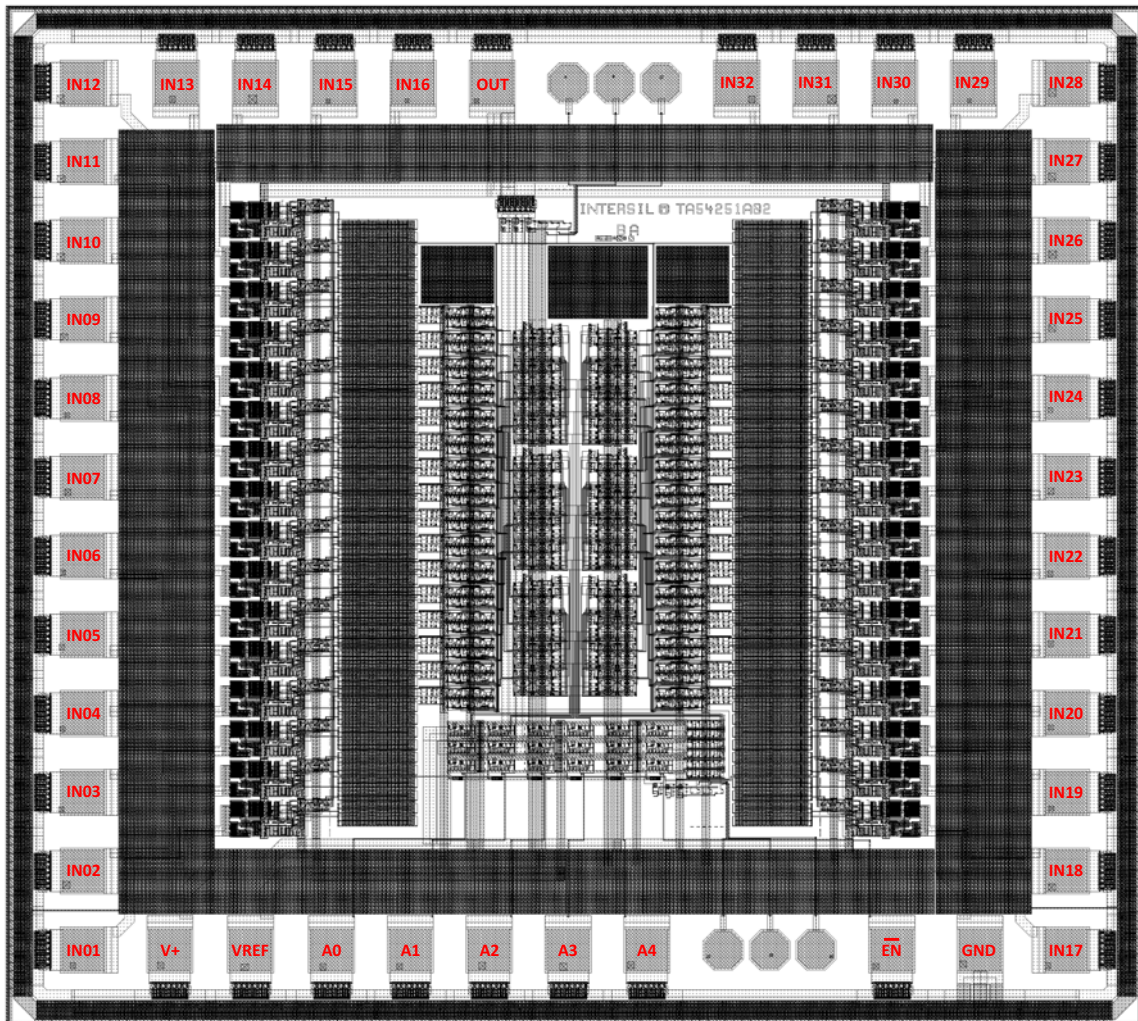
1.522 grams

Lid Characteristics

Finish: Gold

Potential: Grounded, tied to package pin 29

Metalization Mask Layout



ISL71831SEH

TABLE 3. ISL71831SEH DIE LAYOUT X-Y COORDINATES

PAD NUMBER	PAD NAME	PACKAGING PIN	ΔX (μm)	ΔY (μm)	X (μm)	Y (μm)
1	IN28	P42	110	110	2769.8	2467.8
2	IN29	P43	110	110	2526.8	2467.8
3	IN30	P44	110	110	2320.8	2467.8
4	IN31	P45	110	110	2114.8	2467.8
5	IN32	P46	110	110	1908.8	2467.8
9	OUT	P1	110	110	1268.8	2467.8
10	IN16	P3	110	110	1062.8	2467.8
11	IN15	P4	110	110	856.8	2467.8
12	IN14	P5	110	110	650.8	2467.8
13	IN13	P6	110	110	444.8	2467.8
14	IN12	P7	110	110	201.8	2467.8
15	IN11	P8	110	110	201.8	2261.8
16	IN10	P9	110	110	201.8	2055.8
17	IN9	P10	110	110	201.8	1849.8
18	IN8	P11	110	110	201.8	1643.8
19	IN7	P12	110	110	201.8	1437.8
20	IN6	P13	110	110	201.8	1231.8
21	IN5	P14	110	110	201.8	1025.8
22	IN4	P15	110	110	201.8	819.8
23	IN3	P16	110	110	201.8	613.8
24	IN2	P17	110	110	201.8	407.8
25	IN1	P18	110	110	201.8	201.8
26	V ⁺	P19	110	110	427.8	201.8
27	VREF	P20	110	110	638.8	201.8
28	A0	P21	110	110	849.8	201.8
29	A1	P22	110	110	1055.8	201.8
30	A2	P23	110	110	1261.8	201.8
31	A3	P24	110	110	1467.8	201.8
32	A4	P25	110	110	1673.8	201.8
36	$\overline{\text{EN}}$	P28	110	110	2313.8	201.8
37	GND	P29	110	110	2543.8	201.8
38	IN17	P31	110	110	2769.8	201.8
39	IN18	P32	110	110	2769.8	407.8
40	IN19	P33	110	110	2769.8	613.8
41	IN20	P34	110	110	2769.8	819.8
42	IN21	P35	110	110	2769.8	1025.8
43	IN22	P36	110	110	2769.8	1231.8
44	IN23	P37	110	110	2769.8	1437.8
45	IN24	P38	110	110	2769.8	1643.8
46	IN25	P39	110	110	2769.8	1849.8
47	IN26	P40	110	110	2769.8	2055.8
48	IN27	P41	110	110	2769.8	2261.8

NOTE: Origin of coordinates is the center of the die.

ISL71831SEH

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
November 18, 2016	FN8759.2	On page 1 - Updated Related Literature section On page 3 - Added Circuit 1 and Circuit 2 diagrams and ESD Circuit column in the pin description table.
December 10, 2015	FN8759.1	On page 1 Changed in Description, 2nd paragraph " r_{ON} " to " $r_{DS(ON)}$ " Changed in Description and Features supply voltage from "3.3V to 5V" to "3V to 5.5V". Updated Features "SEL/SEB LET _{TH} " by changing V^+ from 5V to 6.3V and value from 86.4 to 60MeV • cm ² /mg. Removed High Dose rate feature. Updated Low Dose value from 100 to 75krad(Si) on Feature bullet and Note. Made correction to package in last paragraph of description from "CQFP" to "CDFP" Made correction to SMD from "5962-1548" to "5962-15248" On page 4 - In the Abs Max Section, changed from "Maximum Supply Voltage (V+ to V-) (Note 5) 7V" to "Maximum Supply Voltage (V+ to GND) (Note 5) 6.3V" Updated Note 5 by changing value from 86.3 to 60MeV • cm ² /mg Electrical Spec changes - Updated heading on "Electrical Specifications (V ⁺ = 5V)" table. - Changed Parameter names from r_{ON} to $r_{DS(ON)}$. - Changed $r_{DS(ON)}$ typical from 60 to 40. - Removed MIN "15" from $\Delta r_{DS(ON)}$ - Added Leakage to description of $I_{IN(OFF-OV)}$ On page 5 - Changed t_{BBM} typical from "15" to "18" - Changed V_{CTE} typical from "2" to "1.4" - For V_{ISO} , - Updated Test Conditions from "VEN = 0V" to "VEN = VREF" - Moved typical values to MIN column. - For V_{CT} , - Updated Test Conditions from "VEN = VREF" to "VEN = 0V" - Moved typical values to MIN column. On page 6 - Changed Parameter names from r_{ON} to $r_{DS(ON)}$. - Changed $r_{DS(ON)}$ typical from 60 to 70. - Added Leakage to description of $I_{IN(OFF-OV)}$ On page 7 - Changed t_{BBM} typical from "15" to "25" On page 8 - Added Table 2 On page 9 - Updated Figure 7 by changing 1k Ω to 100 Ω . On page 11 through page 16 - Updated y-axis label on Figures 20, 22 and 23 - Updated y-axis label and title on Figures 29 through 35 and Figures 41 through 47 On page 18 - Replaced Metalization Mask Layout image. On page 19 - Updated the Pad Name for Pad 26 from "VDD" to "V+"
September 24, 2015	FN8759.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, see the respective product information page found at www.intersil.com.

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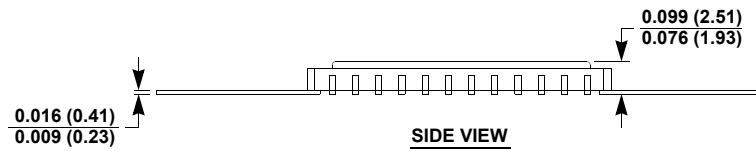
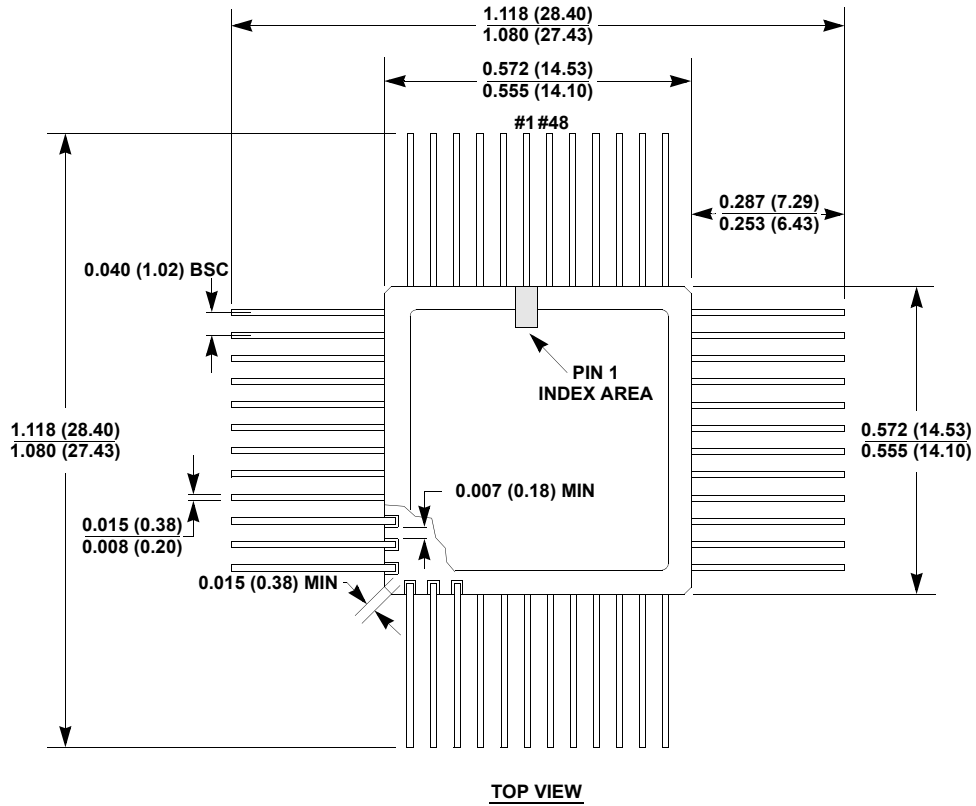
Package Outline Drawing

For the most recent package outline drawing, see [R48.A](#).

R48.A

48 CERAMIC QUAD FLATPACK PACKAGE (CQFP)

Rev 3, 10/12



NOTE:

1. All dimensions are in inches (millimeters).