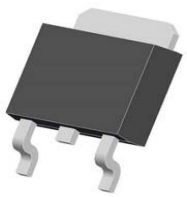
KERSEMI ELECTRONIC CO.,LTD.

IRLR3802
IRLU3802

Applications

- High Frequency 3.3V and 5V input Point-of-Load Synchronous Buck Converters
- Power Management for Netcom, Computing and Portable Applications.

D-Pak
IRLR3802



I-Pak
IRLU3802

Benefits

- Ultra-Low Gate Impedance
- Very Low $R_{DS(on)}$
- Fully Characterized Avalanche Voltage and Current

V_{DSS}	$R_{DS(on)}$ max	Q_g
12V	8.5mΩ	27nC

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V_{DS}	Drain-Source Voltage	12	V
V_{GS}	Gate-to-Source Voltage	± 12	V
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 4.5V	84 ④	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 4.5V	60④	
I_{DM}	Pulsed Drain Current①	320	
P_D @T_C = 25°C	Maximum Power Dissipation	88	W
P_D @T_C = 100°C	Maximum Power Dissipation	44	W
	Linear Derating Factor	0.59	mW/°C
T_J , T_{STG}	Junction and Storage Temperature Range	-55 to + 175	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	1.7	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	——	40	
$R_{\theta JA}$	Junction-to-Ambient	——	110	

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	12	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.009	—	V/°C	Reference to 25°C, I_D = 1mA ③
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	6.5	8.5	mΩ	V_{GS} = 4.5V, I_D = 15A ③
		—	—	30		V_{GS} = 2.8V, I_D = 12A
$V_{GS(th)}$	Gate Threshold Voltage	0.6	—	1.9	V	V_{DS} = V_{GS}, I_D = 250μA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-3.2	—	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	—	—	100	μA	V_{DS} = 9.6V, V_{GS} = 0V
		—	—	250		V_{DS} = 9.6V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	200	nA	V_{GS} = 12V
	Gate-to-Source Reverse Leakage	—	—	-200		V_{GS} = -12V
g_{fs}	Forward Transconductance	31	—	—	S	V_{DS} = 6.0V, I_D = 12A
Q_g	Total Gate Charge	—	27	41		
Q_{gs1}	Pre-Vth Gate-Source Charge	—	3.6	—		V_{DS} = 6.0V
Q_{gs2}	Post-Vth Gate-Source Charge	—	2.0	—		V_{GS} = 5.0V
Q_{gd}	Gate-to-Drain Charge	—	10	—	nC	I_D = 6.0A
Q_{godr}	Gate Charge Overdrive	—	11	—		See Fig.16
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	—	12	—		
Q_{oss}	Output Charge	—	28	—	nC	V_{DS} = 10V, V_{GS} = 0V
$t_{d(on)}$	Turn-On Delay Time	—	11	—		V_{DD} = 6.0V, V_{GS} = 4.5V③
t_r	Rise Time	—	14	—	ns	I_D = 12A
$t_{d(off)}$	Turn-Off Delay Time	—	21	—		Clamped Inductive Load
t_f	Fall Time	—	17	—		
C_{iss}	Input Capacitance	—	2490	—		V_{GS} = 0V
C_{oss}	Output Capacitance	—	2150	—	pF	V_{DS} = 6.0V
C_{rss}	Reverse Transfer Capacitance	—	530	—		f = 1.0MHz

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	300	mJ
I_{AR}	Avalanche Current①	—	20	A

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	84④	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	320		
V_{SD}	Diode Forward Voltage	—	0.81	1.2	V	T_J = 25°C, I_S = 12A, V_{GS} = 0V ③
		—	0.65	—		T_J = 125°C, I_S = 12A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	—	52	78	ns	T_J = 25°C, I_F = 12A, V_R=20V
Q_{rr}	Reverse Recovery Charge	—	54	81	nC	di/dt = 100A/μs ③
t_{rr}	Reverse Recovery Time	—	50	75	ns	T_J = 125°C, I_F = 12A, V_R=20V
Q_{rr}	Reverse Recovery Charge	—	50	75	nC	di/dt = 100A/μs ③

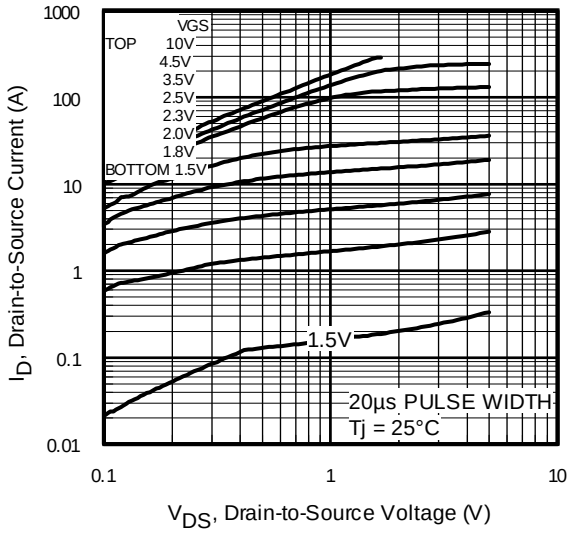


Fig 1. Typical Output Characteristics

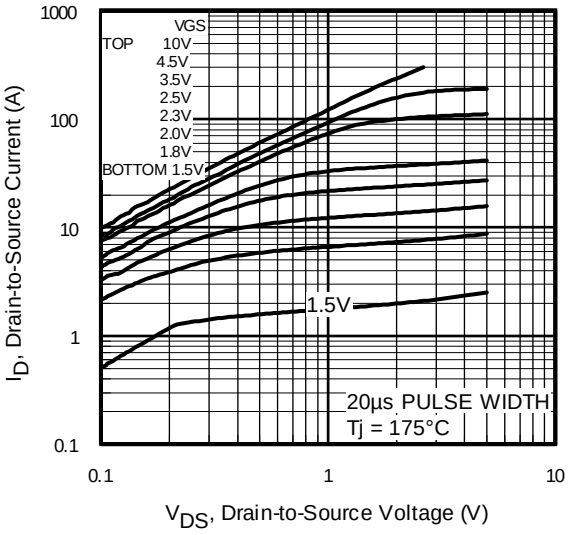


Fig 2. Typical Output Characteristics

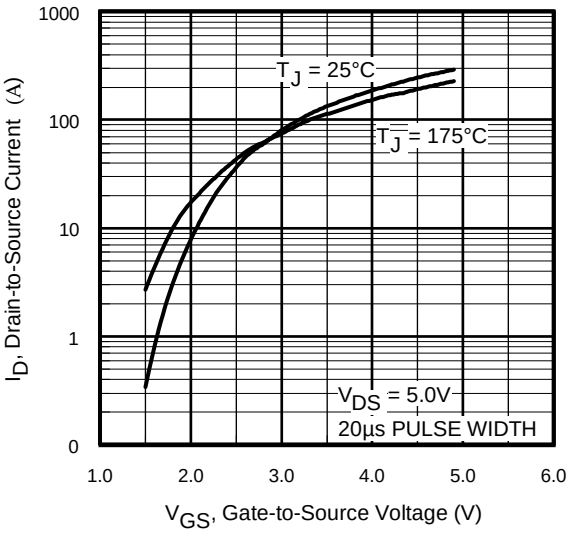


Fig 3. Typical Transfer Characteristics

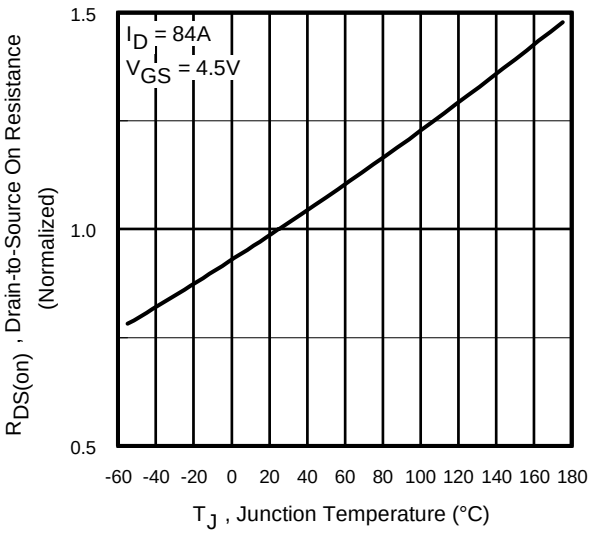


Fig 4. Normalized On-Resistance Vs. Temperature

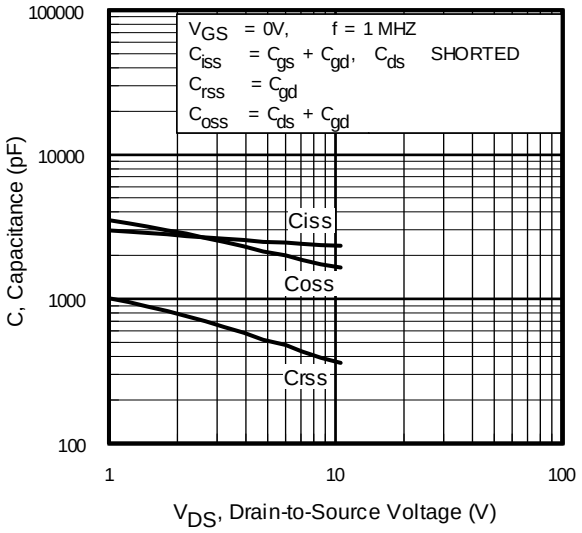


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

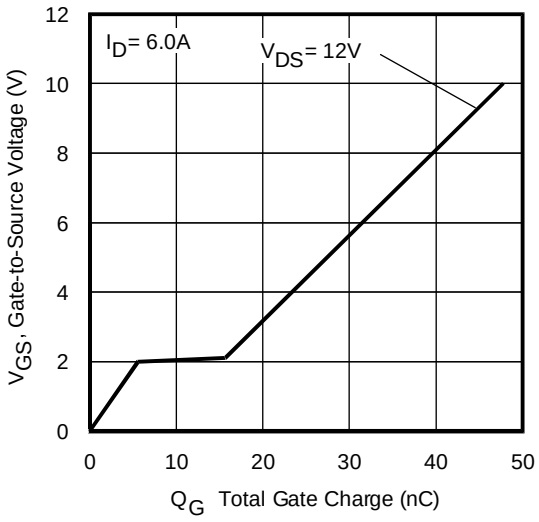


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

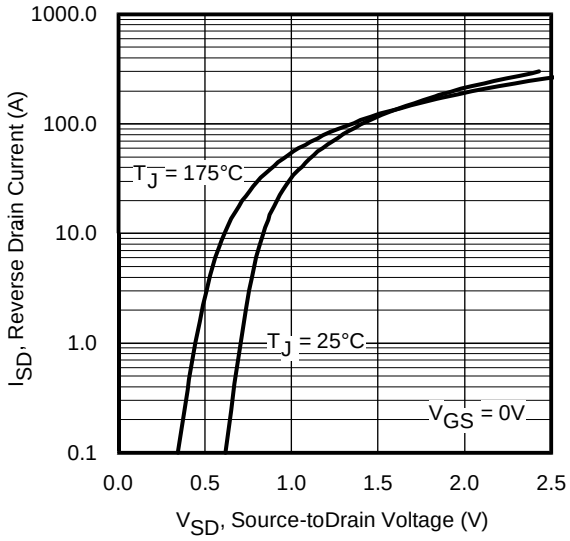


Fig 7. Typical Source-Drain Diode Forward Voltage

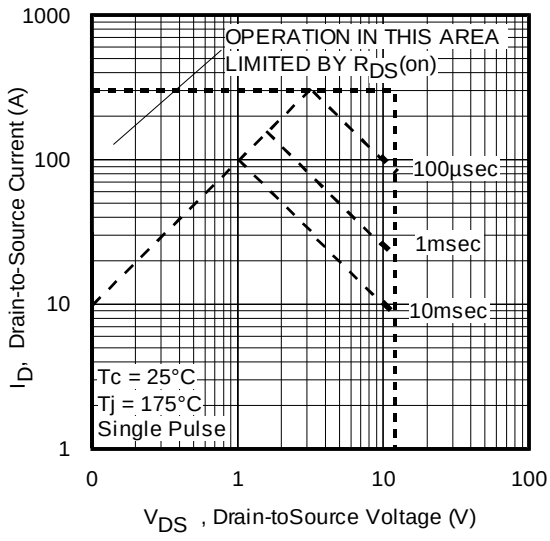


Fig 8. Maximum Safe Operating Area

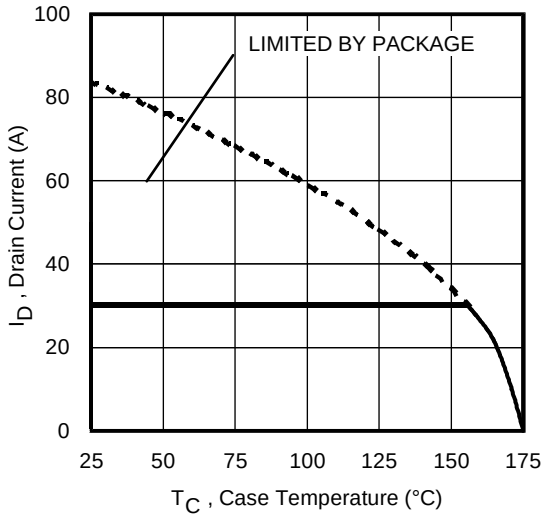


Fig 9. Maximum Drain Current Vs. Case Temperature

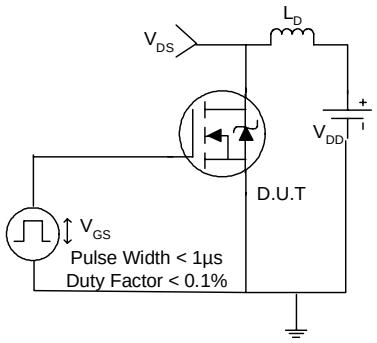


Fig 10a. Switching Time Test Circuit

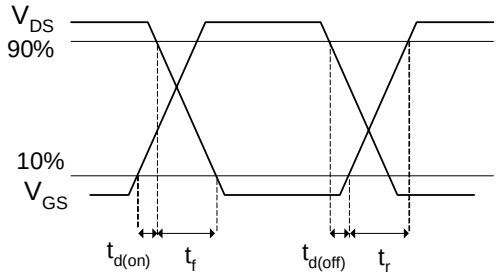


Fig 10b. Switching Time Waveforms

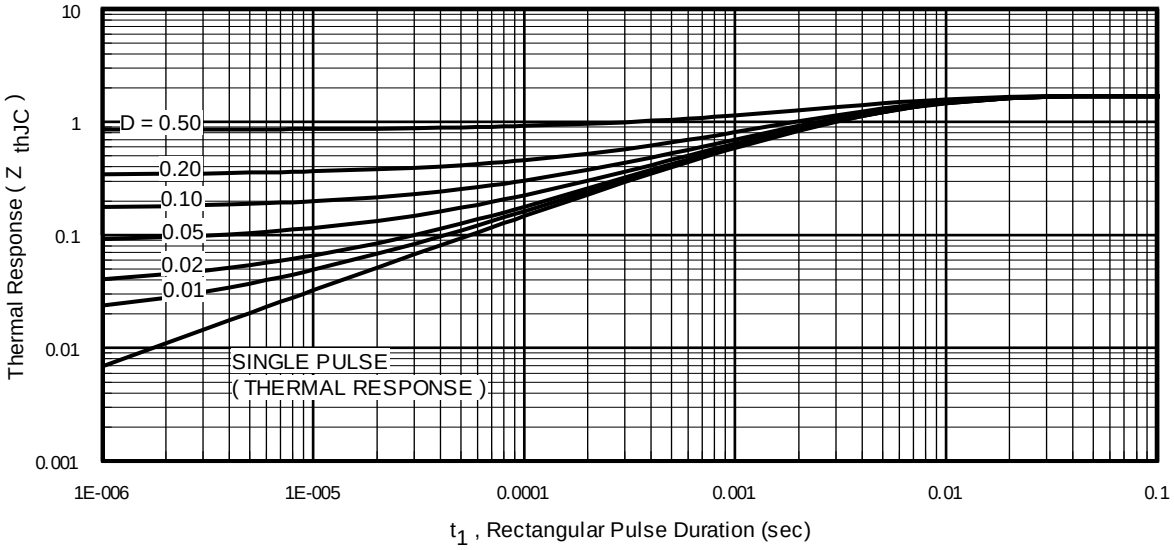


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

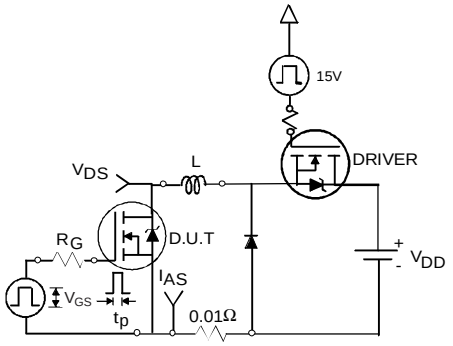


Fig 12a. Unclamped Inductive Test Circuit

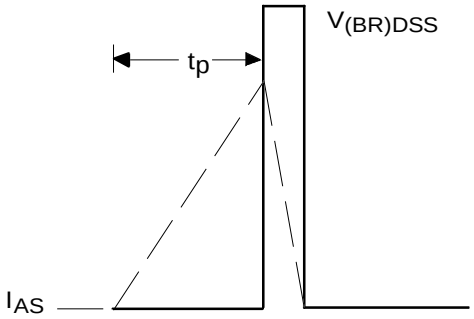


Fig 12b. Unclamped Inductive Waveforms

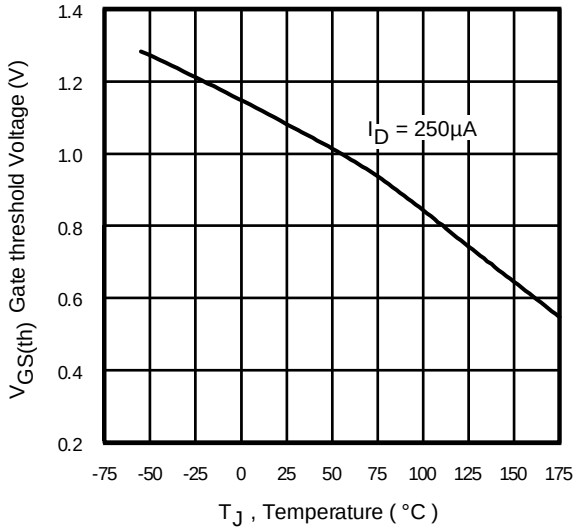


Fig 13. Threshold Voltage Vs. Temperature

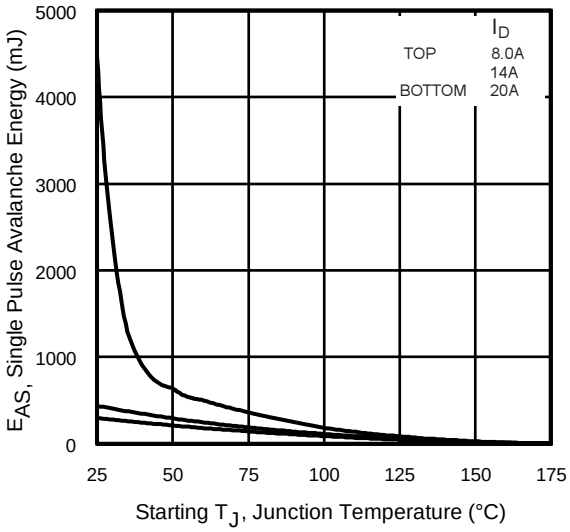


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

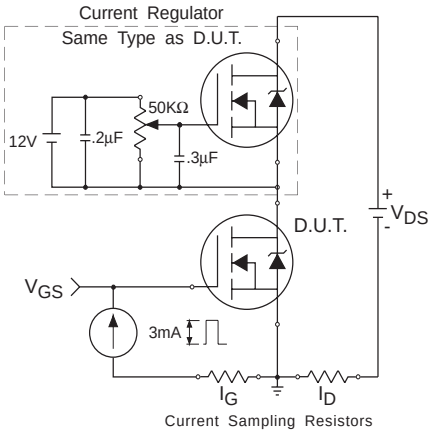


Fig 14. Gate Charge Test Circuit

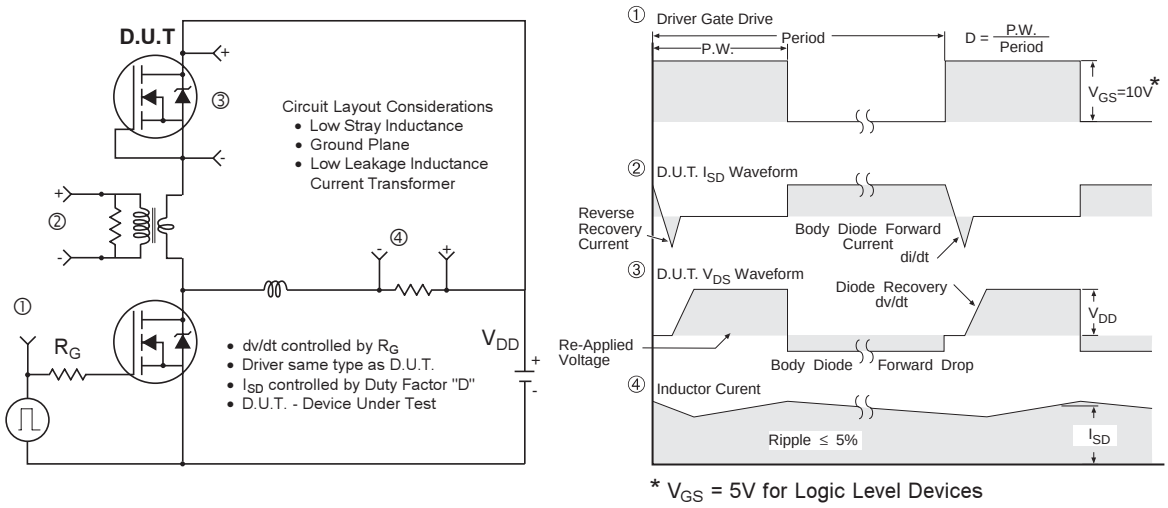


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

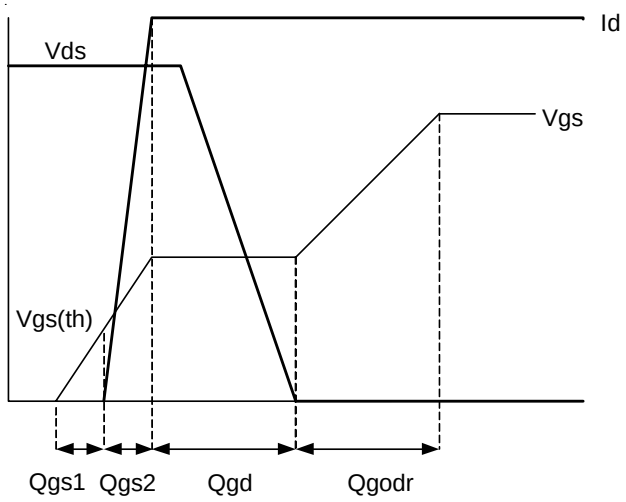
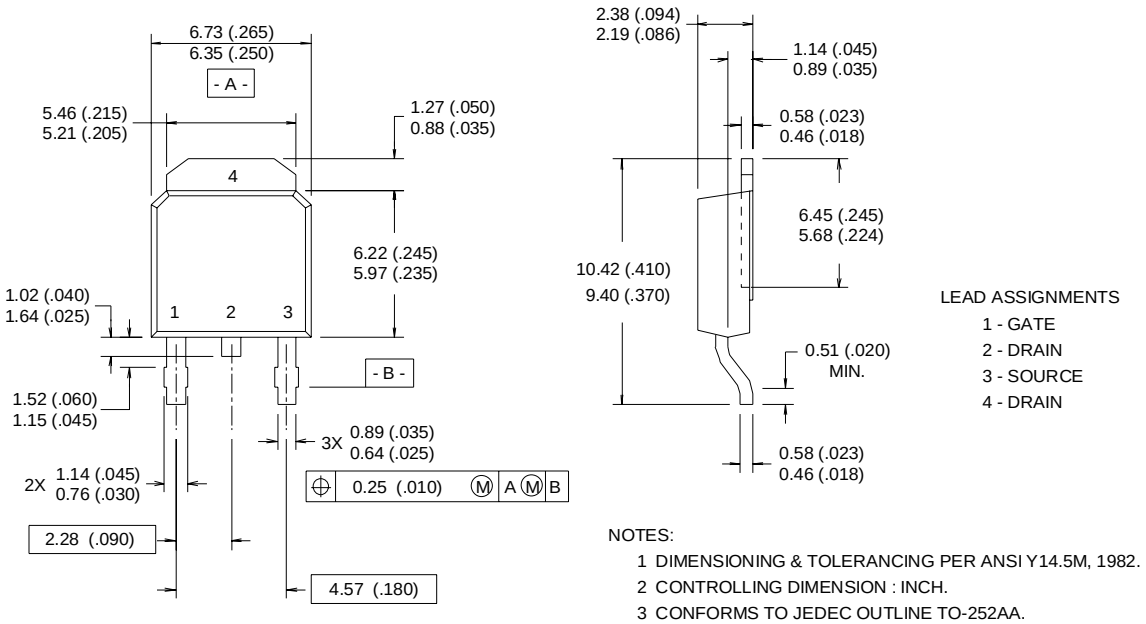


Fig 16. Gate Charge Waveform

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)

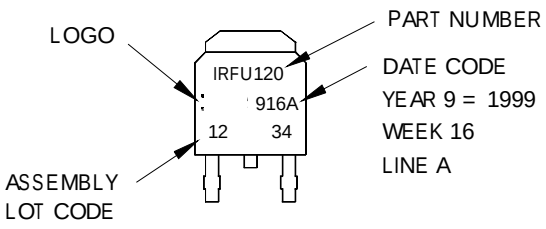


LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

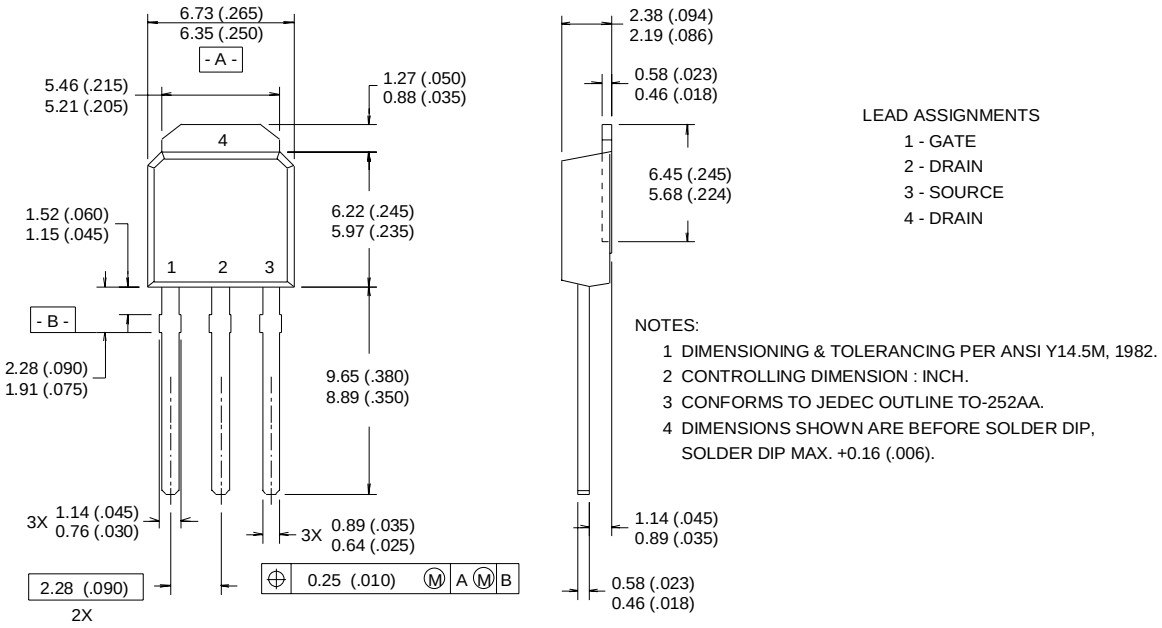
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"



I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)

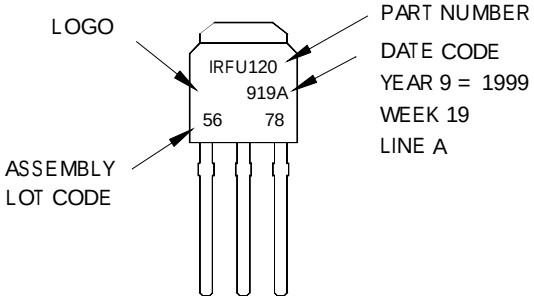


LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-252AA.
4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

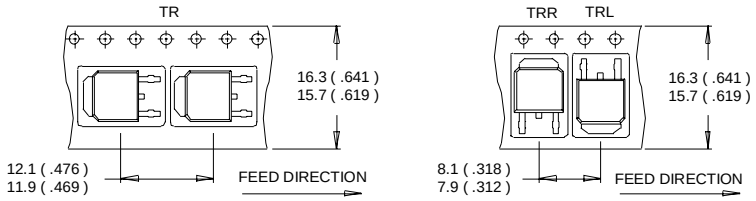
I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 1999
IN THE ASSEMBLY LINE "A"

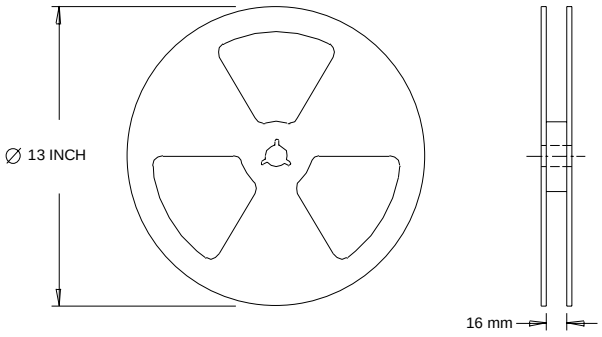


D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 1.4mH R_G = 25Ω, I_{AS} = 20A.

③ Pulse width ≤ 400μs; duty cycle ≤ 2%.

④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A.

* When mounted on 1" square PCB (FR-4 or G-10 Material).
For recommended footprint and soldering techniques refer to application note #AN-994.