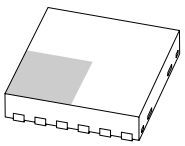


IP4791CZ12

HDMI ESD protection, level shifter and backdrive protection

Rev. 3 — 7 January 2011 Product data sheet

1. General description

The IP4791CZ12 is designed to protect mobile High-Definition Multimedia Interface (HDMI) transmitter interfaces. It includes level shifting for the Data Display Channel (DDC), Consumer Electronic Control (CEC), hot plug signal and backdrive protection. In addition, all signals are protected by high-level ElectroStatic Discharge (ESD) protection diodes.

The level shifting function is required to protect the I/Os against overvoltages when the transmitter operates at a supply voltage lower than the external devices. The IP4791CZ12 contains active buffers to provide the level shifting function, hot plug detect input and the CEC pull-up current source.

The ESD protection diodes provide protection from ESD voltages up to ±8 kV, according to IEC 61000-4-2, level 4.

2. Features and benefits

- HDMI 1.3 compliant
- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- Robust ESD protection without degradation after multiple ESD strikes
- Low leakage even after several hundred ESD discharges
- Bidirectional level shifting buffer provided for DDC clock and data channels
- Backdrive protection
- Power management
- CEC pull-up current source and level shifting buffer
- Hot plug detect module with pull-down resistor
- Matched 0.4 mm trace spacing for HDMI type C connector

3. Applications

The IP4791CZ12 can be used with a range of HDMI transmitter devices including:

- Personal computer
- Notebook
- Mobile phone
- DV camcorder
- Digital still camera
- MP3 player

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
IP4791CZ12	HXSON12	plastic, thermal enhanced extremely thin small outline package; no leads; 12 terminals; body 2.1 × 2.5 × 0.5 mm	SOT1156-1

5. Functional diagram

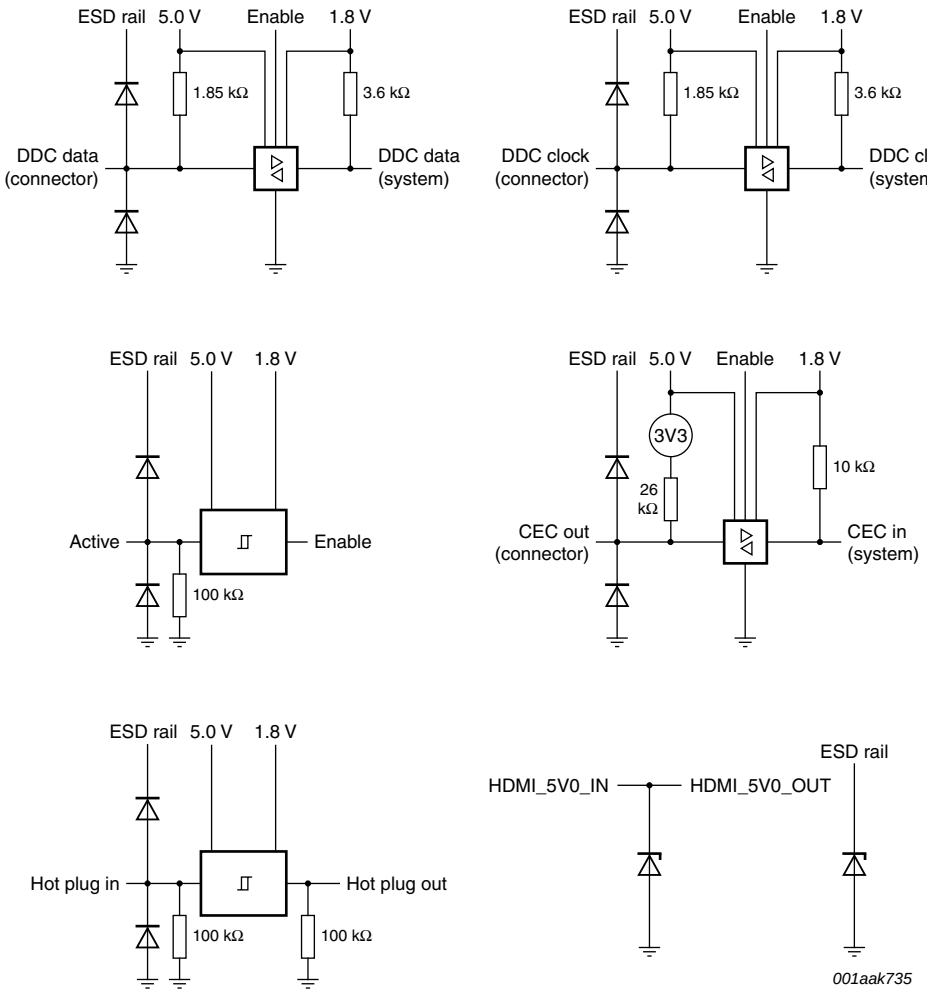


Fig 1. Functional diagram

6. Pinning information

6.1 Pinning

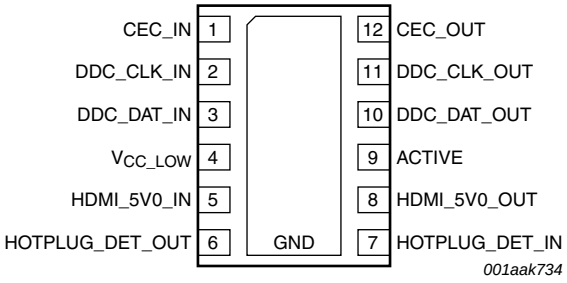


Fig 2. Pin configuration (transparent top view)

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
CEC_IN	1	CEC system side
DDC_CLK_IN	2	DDC clock system side
DDC_DAT_IN	3	DDC data system side
V_{CC_LOW}	4	supply voltage, low voltage side for level shifting
HDMI_5V0_IN	5	5 V line from main supply
HOTPLUG_DET_OUT	6	hot plug detect system side
HOTPLUG_DET_IN	7	hot plug detect connector side
HDMI_5V0_OUT	8	5 V line to HDMI connector
ACTIVE	9	power saving mode
DDC_DAT_OUT	10	DDC data connector side
DDC_CLK_OUT	11	DDC clock connector side
CEC_OUT	12	CEC connector side
GND	Pad	ground

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	signal pins to ground				
		at HDMI/DVI connector side	[1]	-	±10	kV
		all pins	[2]	-	±200	V
		all pins	[3]	-	±2	kV
V_{CC}	supply voltage			GND – 0.5	5.5	V
V_I	input voltage			GND – 0.5	5.5	V
P_{tot}	total power dissipation	ACTIVE = HIGH; DDC operating at 100 kHz, 50 % duty cycle; CEC operating at 1 kHz, 50 % duty cycle	[4]	-	30	mW
		disable: HDMI cable not connected; ACTIVE = LOW, DDC bus in Idle mode		-	0.2	mW
T_{stg}	storage temperature			–55	+125	°C
T_{amb}	ambient temperature			–40	+85	°C

[1] IEC 61000-4-2, level 4, contact discharge.

[2] Machine Model (MM) according to JESD22-A115-A.

[3] Human Body Model (HBM) according to JESD22-A-J114D.

[4] Including the current through the internal pull-up resistors.

8. Characteristics

Table 4. Supplies

GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(5V0)}$	supply voltage (5.0 V)		4.5	5.0	5.5	V
$V_{CC(1V8)}$	supply voltage (1.8 V)		1.62	1.8	3.63	V

Table 5. Static characteristics

$V_{CC(5V0)}$ = 5.0 V; $V_{CC(1V8)}$ = 1.8 V; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
HDMI_5V0_OUT							
R_{dyn}	dynamic resistance		[1]				
		positive transient		-	0.6	-	Ω
		negative transient		-	0.4	-	Ω
$V_{CL(ch)trt(pos)}$	positive transient channel clamping voltage	V_{ESD} = 8 kV, t_p = 100 ns	[2]	-	8.0	-	V
ACTIVE							
V_{IH}	HIGH-level input voltage		[3]	1.2	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
R_{pd}	pull-down resistance			60	100	140	kΩ

Table 5. Static characteristics *...continued*

$V_{CC(5V0)}$ = 5.0 V; $V_{CC(1V8)}$ = 1.8 V; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DDC buffer - connector side (pin 10 and pin 11) [3]							
V_{IH}	HIGH-level input voltage			0.5 × $V_{CC(5V0)}$	-	5.5	V
V_{IL}	LOW-level input voltage			−0.5	-	0.3 × $V_{CC(5V0)}$	V
V_{IK}	input clamping voltage	I_I = −18 mA		-	−1.0	-	V
V_{OL}	LOW-level output voltage	internal pull-down current		-	100	200	mV
V_{OH}	HIGH-level output voltage		[4]	$V_{CC(5V0)}$ − 0.02	-	$V_{CC(5V0)}$ + 0.02	V
C_{IO}	input/output capacitance	$V_{CC(5V0)}$ = 0 V; $V_{CC(1V8)}$ = 0 V; V_{bias} = 2.5 V; AC input = 3.5 $V_{(p-p)}$; f = 100 kHz	[4]	-	8	10	pF
R_{pu}	pull-up resistance			1.6	1.8	2.0	kΩ
DDC buffer - system side (pin 2 and pin 3) [3]							
V_{IH}	HIGH-level input voltage			0.26 × $V_{CC(1V8)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.20 × $V_{CC(1V8)}$	V
V_{IK}	input clamping voltage	I_I = −18 mA		-	−1.0	-	V
V_{OL}	LOW-level output voltage			-	-	0.28 × $V_{CC(1V8)}$	V
V_{OH}	HIGH-level output voltage		[4]	$V_{CC(1V8)}$ − 0.02	-	$V_{CC(1V8)}$ + 0.02	V
C_{IO}	input/output capacitance	$V_{CC(5V0)}$ = 0 V; $V_{CC(1V8)}$ = 0 V; V_{bias} = 2.5 V; AC input = 3.5 $V_{(p-p)}$; f = 100 kHz	[4]	-	6	8	pF
R_{pu}	pull-up resistance			3.2	3.65	4.1	kΩ
CEC_OUT [3]							
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.80	V
V_{OH}	HIGH-level output voltage			2.88	3.3	3.63	V
V_{OL}	LOW-level output voltage	I_{OL} = 1.5 mA		-	100	200	mV
C_{IO}	input/output capacitance	$V_{CC(5V0)}$ = 0 V; $V_{CC(1V8)}$ = 0 V; V_{bias} = 2.5 V; AC input = 3.5 $V_{(p-p)}$; f = 100 kHz	[4]	-	8	10	pF
R_{pu}	pull-up resistance			23.4	26.0	28.6	kΩ

Table 5. Static characteristics *...continued*

$V_{CC(5V0)}$ = 5.0 V; $V_{CC(1V8)}$ = 1.8 V; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
CEC_IN [3]							
V_{IH}	HIGH-level input voltage			0.26 × $V_{CC(1V8)}$	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.20 × $V_{CC(1V8)}$	V
V_{OH}	HIGH-level output voltage		[4]	$V_{CC(1V8)}$ − 0.02	-	$V_{CC(1V8)}$ + 0.02	V
V_{OL}	LOW-level output voltage			-	-	0.28 × $V_{CC(1V8)}$	V
C_{IO}	input/output capacitance	$V_{CC(5V0)}$ = 0 V; $V_{CC(1V8)}$ = 0 V; V_{bias} = 2.5 V; AC input = 3.5 $V_{(p-p)}$; f = 100 kHz	[4]	-	6	7	pF
R_{pu}	pull-up resistance			8.5	10.0	11.5	kΩ
HOTPLUG_DET_IN [3]							
V_{IH}	HIGH-level input voltage			2.0	-	-	V
V_{IL}	LOW-level input voltage			-	-	0.8	V
R_{pd}	pull-down resistance			60	100	140	kΩ
C_i	input capacitance	$V_{CC(5V0)}$ = 0 V; $V_{CC(1V8)}$ = 0 V; V_{bias} = 2.5 V; AC input = 3.5 $V_{(p-p)}$; f = 100 kHz	[4]	-	8	10	pF
HOTPLUG_DET_OUT [3]							
V_{OH}	HIGH-level output voltage	I_{OL} = 1 mA		0.7 × $V_{CC(1V8)}$	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = −1 mA		-	200	300	mV
R_{pd}	pull-down resistance			60	100	140	kΩ

[1] ANSI-ESDSP5.5.1-2004, ESD sensitivity testing TLP component level method 50 TDR.

[2] According to IEC 61000, level 4, contact discharge.

[3] The device is active if the input voltage at pin ACTIVE is above the HIGH level.

[4] This parameter is guaranteed by design.

Table 6. Dynamic characteristics

$V_{CC(5V0)}$ = 5.0 V; $V_{CC(1V8)}$ = 1.8 V; GND = 0 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
DDC_DAT_IN, DDC_CLK_IN, DDC_DAT_OUT, DDC_CLK_OUT							
t_{PLH}	LOW to HIGH propagation delay	system side to connector side Figure 3	[1]	-	80	-	ns
t_{PHL}	HIGH to LOW propagation delay	system side to connector side Figure 3	[1]	-	60	-	ns
t_{PLH}	LOW to HIGH propagation delay	connector side to system side Figure 4	[1]	-	120	-	ns
t_{PHL}	HIGH to LOW propagation delay	connector side to system side Figure 4	[1]	-	80	-	ns
t_{TLH}	LOW to HIGH transition time	connector side Figure 5	[1]	-	150	-	ns
t_{THL}	HIGH to LOW transition time	connector side Figure 5	[1]	-	100	-	ns
t_{TLH}	LOW to HIGH transition time	system side Figure 6	[1]	-	250	-	ns
t_{THL}	HIGH to LOW transition time	system side Figure 6	[1]	-	80	-	ns

[1] All dynamic measurements are done with a 50 pF load. Rise times are determined by internal pull-up resistors.

9. AC waveforms

9.1 DDC propagation delay

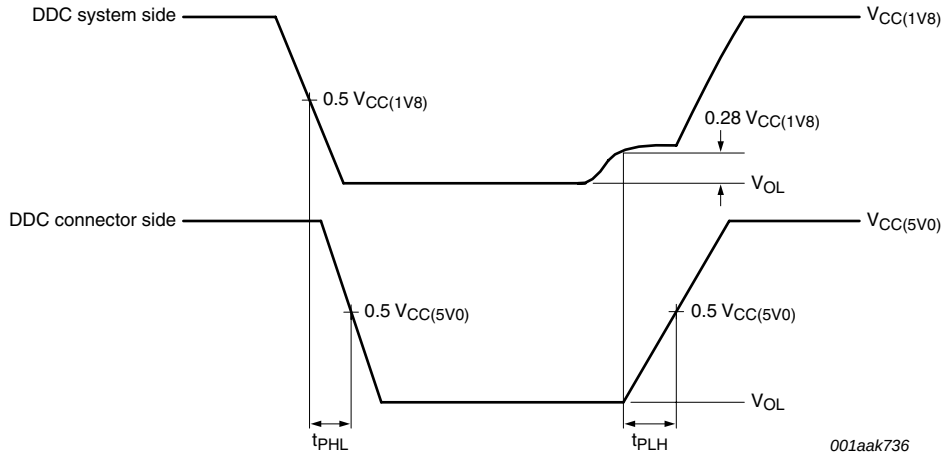


Fig 3. Propagation delay DDC, DDC system side to DDC connector side

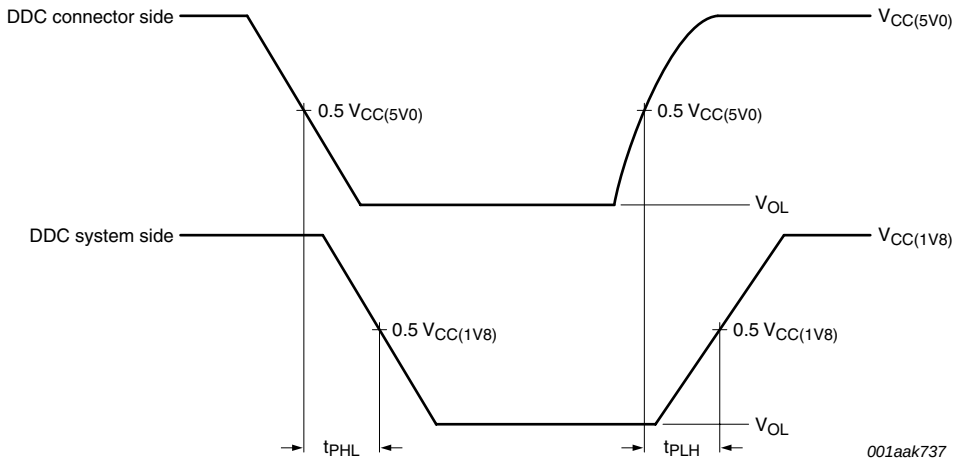


Fig 4. Propagation delay DDC, DDC connector side to DDC system side

9.2 DDC transition time

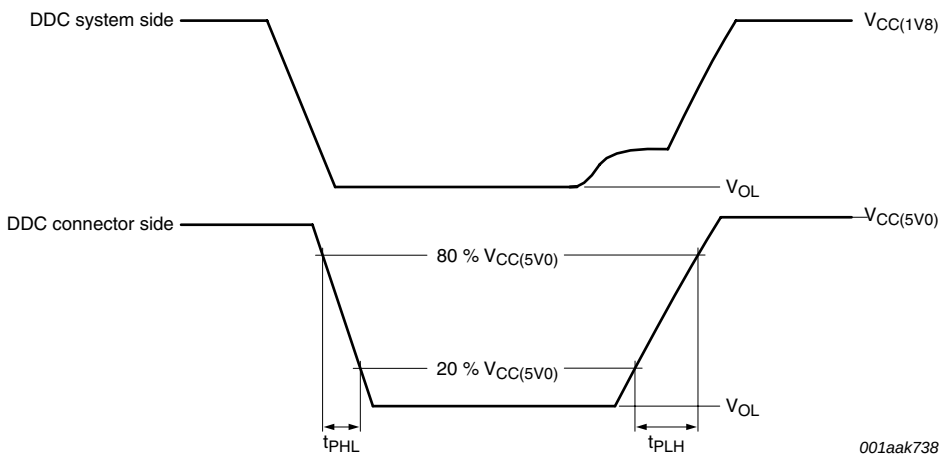


Fig 5. Transition time DDC connector side

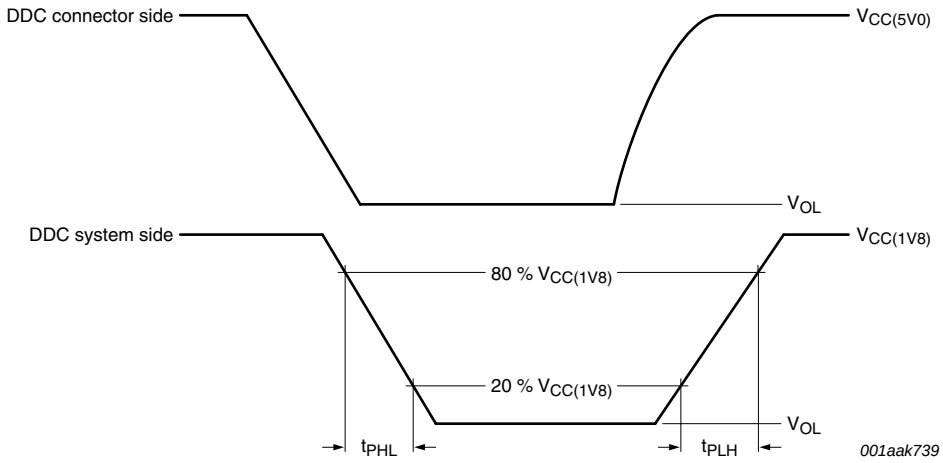


Fig 6. Transition time DDC system side

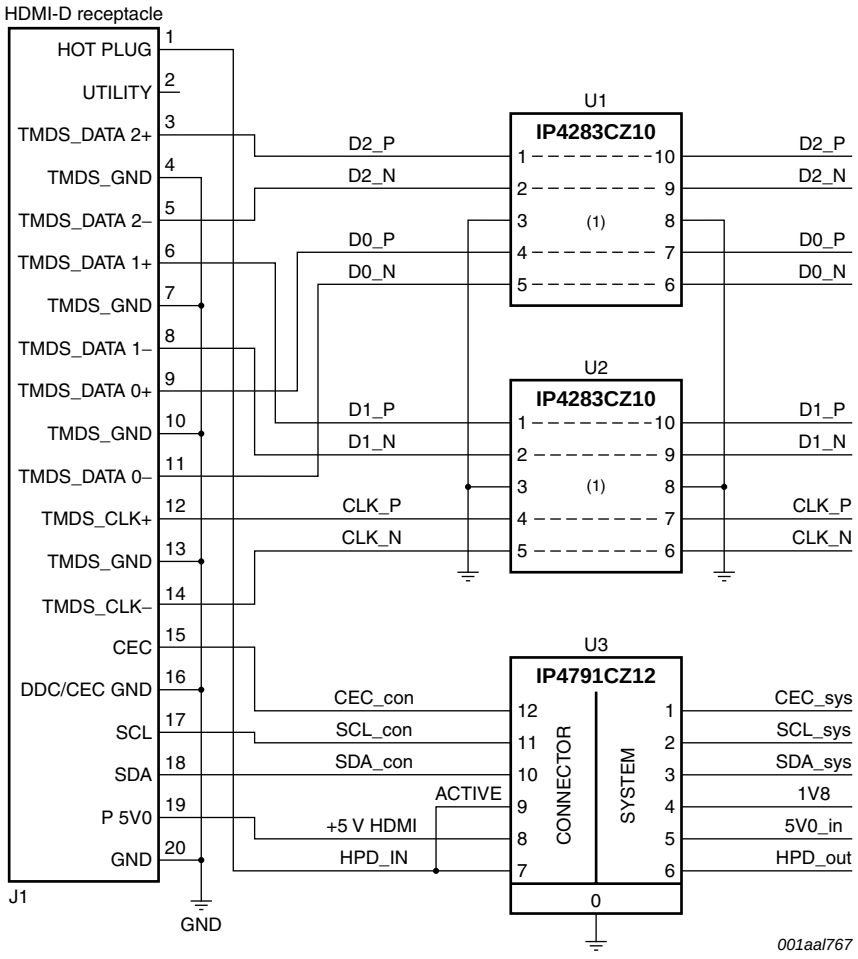
10. Application information

10.1 HDMI source

The IP4791CZ12 simplifies the application of a mobile HDMI source.

No external components are needed for the application to adapt the HDMI port to the HDMI transmitter.

Note: The 5 V supply voltage must be in the range 4.8 V to 5.3 V to pass the HDMI compliance test.



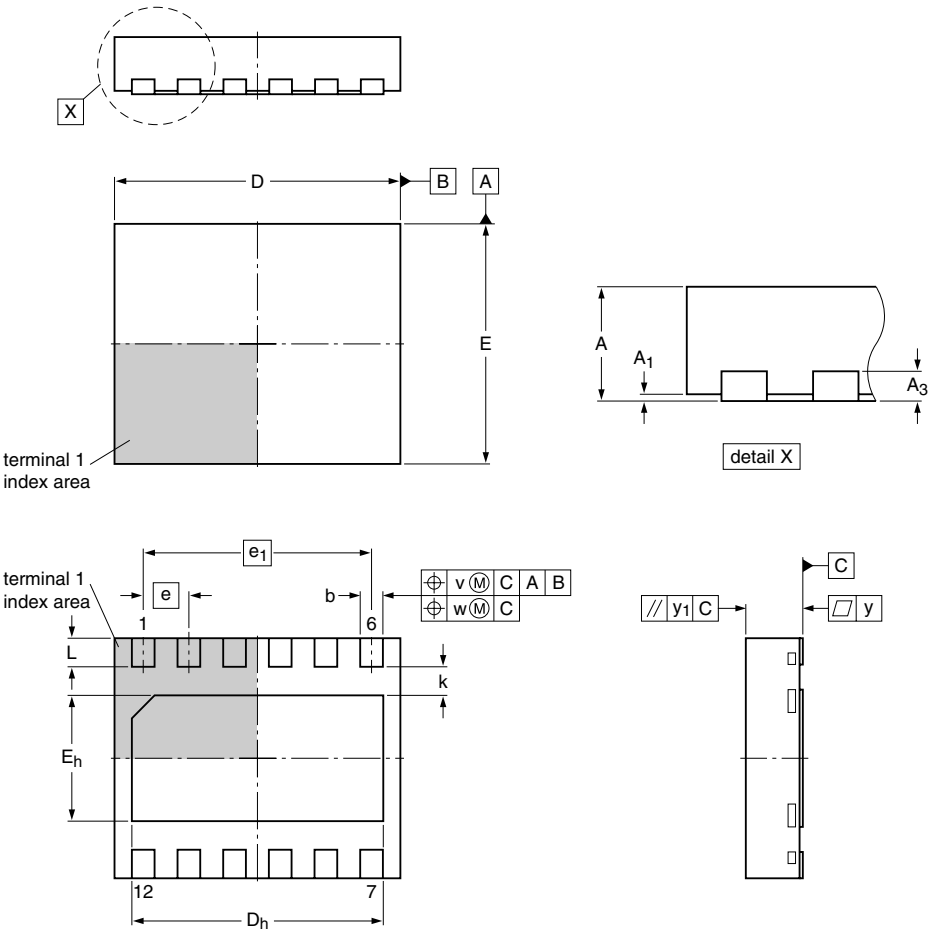
(1) The TDMS lines are 100 Ω differential impedance transmission lines which pass underneath the chip without being interrupted by it.

Fig 7. HDMI transmitter application

The ACTIVE pin is enabling the IP4791CZ12 with a voltage above 1.2 V. Connecting the ACTIVE pin to the HOT PLUG line will enable the IP4791CZ12 automatically if any HDMI sink is connected to the HDMI port and disable (switch to power-saving mode of the IP4791CZ12) when no HDMI sink is connecting to the HDMI port.

11. Package outline

HXSON12: plastic, thermal enhanced extremely thin small outline package; no leads; 12 terminals; body 2.1 x 2.5 x 0.5 mm **SOT1156-1**



Dimensions

Unit[1]		A	A_1	A_3	b	D	D_h	E	E_h	e	e_1	k	L	v	w	y	y_1
	max	0.5	0.05		0.25	2.6	2.25	2.2	1.15				0.30				
mm	nom			0.127	0.20	2.5	2.20	2.1	1.10	0.4	2		0.25	0.1	0.05	0.05	0.05
	min		0.00		0.15	2.4	2.15	2.0	1.05			0.2	0.20				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1156-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1156-1	- - -	- - -	- - -			~~10-01-21~~ 10-09-17

Fig 8. Package outline SOT1156-1 (HXSON12)

12. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

12.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

12.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

12.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

12.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 9) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 7 and 8

Table 7. SnPb eutectic process (from J-STD-020C)

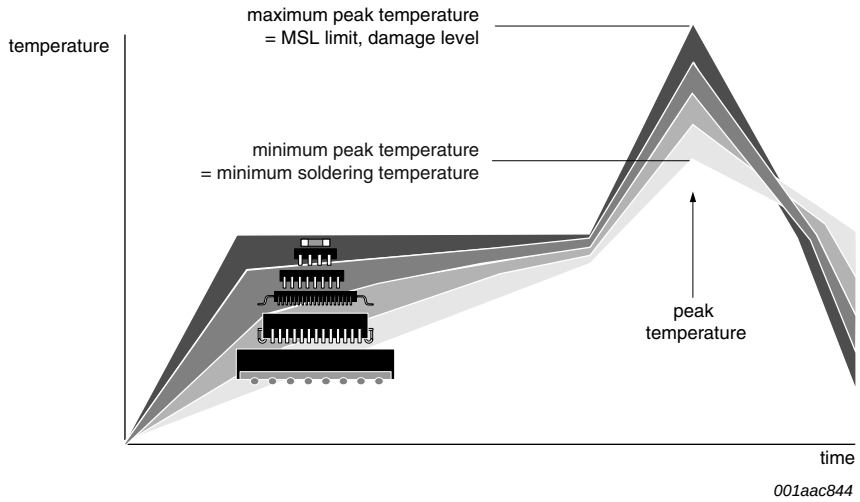
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 8. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 9.



MSL: Moisture Sensitivity Level

Fig 9. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CEC	Consumer Electronic Control
DDC	Data Display Channel
DVI	Digital Visual Interface
ESD	ElectroStatic Discharge
HDMI	High-Definition Multimedia Interface
RoHS	Restriction of Hazardous Substances
TDMS	Transition Minimized Differential Signalling
TDR	Time Domain Reflectometer
TLP	Transmission Line Pulse

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4791CZ12 v.3	20110107	Product data sheet	-	IP4791CZ12 v.2
Modifications:	• Table 3 “Limiting values”: P_{tot} maximum value updated. • Table 5 “Static characteristics”: V_{IK} updated. • Section 10.1 “HDMI source”: enhanced.			
IP4791CZ12 v.2	20101111	Preliminary data sheet	-	IP4791CZ12 v.1
IP4791CZ12 v.1	20100401	Objective data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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