![Texas Instruments logo] **TEXAS INSTRUMENTS**

Data sheet acquired from Harris Semiconductor
SCHS174

# CD74HC273, CD74HCT273

## High Speed CMOS Logic
## Octal D-Type Flip-Flop with Reset

February 1998

## Features

- **Common Clock and Asynchronous Master Reset**
- **Positive Edge Triggering**
- **Buffered Inputs**
- **Typical $f_{MAX}$ = 60MHz at $V_{CC}$ = 5V, $C_L$ = 15pF, $T_A$ = 25$^o$C**
- **Fanout (Over Temperature Range)**
  - **Standard Outputs . . . . . . . . . . . . . . . 10 LSTTL Loads**
  - **Bus Driver Outputs . . . . . . . . . . . . . 15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55$^o$C to 125$^o$C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity: $N_{IL}$ = 30%, $N_{IH}$ = 30% of $V_{CC}$ at $V_{CC}$ = 5V**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility, $V_{IL}$ = 0.8V (Max), $V_{IH}$ = 2V (Min)**
  - **CMOS Input Compatibility, $I_I \leq 1\mu A$ at $V_{OL}$, $V_{OH}$**

## Description

The Harris CD74HC273 and CD74HCT273 high speed octal D-Type flip-flops with a direct clear input are manufactured with silicon-gate CMOS technology. They possess the low power consumption of standard CMOS integrated circuits.

Information at the D inputis transferred to the Q outputs on the positive-going edge of the clock pulse. All eight flip-flops are controlled by a common clock (CP) and a common reset ($\overline{MR}$). Resetting is accomplished by a low voltage level independent of the clock. All eight Q outputs are reset to a logic 0.

## Ordering Information

| PART NUMBER | TEMP. RANGE ($^o$C) | PACKAGE | PKG. NO. |
|---|---|---|---|
| CD54HC273F | -55 to 125 | 20 Ld CERDIP | F20.3 |
| CD54HCT273F | -55 to 125 | 20 Ld CERDIP | F20.3 |
| CD74HC273E | -55 to 125 | 20 Ld PDIP | E20.3 |
| CD74HCT273E | -55 to 125 | 20 Ld PDIP | E20.3 |
| CD74HC273M | -55 to 125 | 20 Ld SOIC | M20.3 |
| CD74HCT273M | -55 to 125 | 20 Ld SOIC | M20.3 |
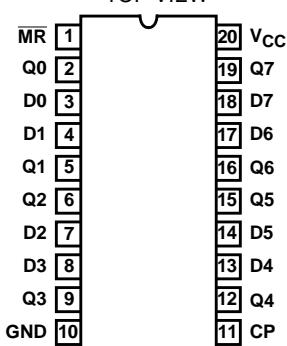
NOTES:
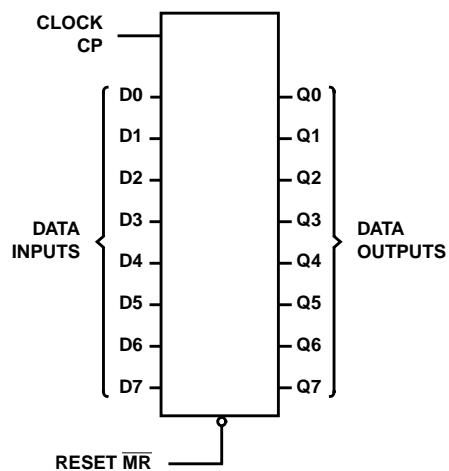
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

## Pinout

**CD54HC273, CD54HCT273, CD74HC273, CD74HCT273**
**(PDIP, SOIC, CERDIP)**
TOP VIEW

| Pin | | Pin |
|---|---|---|
| $\overline{MR}$ | 1 | 20 $V_{CC}$ |
| Q0 | 2 | 19 Q7 |
| D0 | 3 | 18 D7 |
| D1 | 4 | 17 D6 |
| Q1 | 5 | 16 Q6 |
| Q2 | 6 | 15 Q5 |
| D2 | 7 | 14 D5 |
| D3 | 8 | 13 D4 |
| Q3 | 9 | 12 Q4 |
| GND | 10 | 11 CP |

File Number **1479.2**

## *Functional Diagram*

```
         CLOCK
           CP ──┐  ┌──────────┐
                └──┤          │
          D0 ──────┤          ├────── Q0 ┐
          D1 ──────┤          ├────── Q1 │
          D2 ──────┤          ├────── Q2 │
          D3 ──────┤          ├────── Q3 │  DATA
 DATA               │          │              OUTPUTS
 INPUTS   D4 ──────┤          ├────── Q4 │
          D5 ──────┤          ├────── Q5 │
          D6 ──────┤          ├────── Q6 │
          D7 ──────┤          ├────── Q7 ┘
                   └────○─────┘
     RESET MR̄ ─────────┘
```

**TRUTH TABLE**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| **RESET ($\overline{MR}$)** | **CLOCK CP** | **DATA $D_n$** | **Q** |
| L | X | X | L |
| H | ↑ | H | H |
| H | ↑ | L | L |
| H | L | X | $Q_0$ |

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care, ↑ = Transition from Low to High Level, $Q_0$ = Level Before the Indicated Steady-State Input Conditions Were Established.

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# CD74HC273, CD74HCT273

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ . . . . . . . . . . . . . . . . . . . . . . . . . -0.5V to 7V
DC Input Diode Current, $I_{IK}$
  For $V_I$ < -0.5V or $V_I$ > $V_{CC}$ + 0.5V . . . . . . . . . . . . . . . . . . . . .±20mA
DC Output Diode Current, $I_{OK}$
  For $V_O$ < -0.5V or $V_O$ > $V_{CC}$ + 0.5V . . . . . . . . . . . . . . . . . . .±20mA
DC Drain Current, per Output, $I_O$
  For -0.5V < $V_O$ < $V_{CC}$ + 0.5V . . . . . . . . . . . . . . . . . . . . . . . . .±25mA
DC Output Source or Sink Current per Output Pin, $I_O$
  For $V_O$ > -0.5V or $V_O$ < $V_{CC}$ + 0.5V . . . . . . . . . . . . . . . . . . . .±25mA
DC $V_{CC}$ or Ground Current, $I_{CC}$ . . . . . . . . . . . . . . . . . . . . . . . . .±50mA

## Thermal Information

| Thermal Resistance (Typical, Note 3) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| PDIP Package . . . . . . . . . . . . . . . . . . . | 125 | N/A |
| CERDIP Package . . . . . . . . . . . . . . . . | 105 | 44 |
| SOIC Package . . . . . . . . . . . . . . . . . . . | 120 | N/A |

Maximum Junction Temperature . . . . . . . . . . . . . . . . . . . . . . . 150°C
Maximum Storage Temperature Range . . . . . . . . . .-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . . . . . . . . 300°C
  (SOIC - Lead Tips Only)

## Operating Conditions

Temperature Range, $T_A$ . . . . . . . . . . . . . . . . . . . . . . -55°C to 125°C
Supply Voltage Range, $V_{CC}$
  HC Types . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .2V to 6V
  HCT Types . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .4.5V to 5.5V
DC Input or Output Voltage, $V_I$, $V_O$ . . . . . . . . . . . . . . . . 0V to $V_{CC}$
Input Rise and Fall Time
  2V . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 1000ns (Max)
  4.5V. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 500ns (Max)
  6V . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 400ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

3. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.

## DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS $V_I$ (V) | TEST CONDITIONS $I_O$ (mA) | $V_{CC}$ (V) | 25°C MIN | 25°C TYP | 25°C MAX | -40°C TO 85°C MIN | -40°C TO 85°C MAX | -55°C TO 125°C MIN | -55°C TO 125°C MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **HC TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 2 | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | | | 4.5 | 3.15 | - | - | 3.15 | - | 3.15 | - | V |
| | | | | 6 | 4.2 | - | - | 4.2 | - | 4.2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 2 | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | | | 4.5 | - | - | 1.35 | - | 1.35 | - | 1.35 | V |
| | | | | 6 | - | - | 1.8 | - | 1.8 | - | 1.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 2 | 1.9 | - | - | 1.9 | - | 1.9 | - | V |
| | | | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| | | | -0.02 | 6 | 5.9 | - | - | 5.9 | - | 5.9 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| | | | -5.2 | 6 | 5.48 | - | - | 5.34 | - | 5.2 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 2 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| | | | 0.02 | 6 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| | | | 5.2 | 6 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ or GND | - | 6 | - | - | ±0.1 | - | ±1 | - | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 6 | - | - | 8 | - | 80 | - | 160 | µA |

## DC Electrical Specifications   (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | | | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
| | | $V_I$ (V) | $I_O$ (mA) | $V_{CC}$ (V) | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **HCT TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | - | - | 4.5 to 5.5 | 2 | - | - | 2 | - | 2 | - | V |
| Low Level Input Voltage | $V_{IL}$ | - | - | 4.5 to 5.5 | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | -0.02 | 4.5 | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| High Level Output Voltage TTL Loads | | | -4 | 4.5 | 3.98 | - | - | 3.84 | - | 3.7 | - | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 4.5 | - | - | 0.1 | - | 0.1 | - | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | - | - | 0.26 | - | 0.33 | - | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ to GND | 0 | 5.5 | - | - | ±0.1 | - | ±1 | - | ±1 | μA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | - | - | 8 | - | 80 | - | 160 | μA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4) | $\Delta I_{CC}$ | $V_{CC}$ -2.1 | - | 4.5 to 5.5 | - | 100 | 360 | - | 450 | - | 490 | μA |

NOTE:

4. For dual-supply systems theoretical worst case ($V_I$ = 2.4V, $V_{CC}$ = 5.5V) specification is 1.8mA.

### HCT Input Loading Table

| INPUT | UNIT LOADS |
|---|---|
| $\overline{MR}$ | 1.5 |
| Data | 0.4 |
| CP | 1.5 |

NOTE:  Unit Load is $\Delta I_{CC}$ limit specified in DC Electrical Specifications table, e.g., 360μA max at 25°C.

### Prerequisite For Switching Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | -40°C TO 85°C | | -55°C TO 125°C | | UNITS |
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **HC TYPES** | | | | | | | | | | | |
| Maximum Clock Frequency (Figure 1) | $f_{MAX}$ | - | 2 | 6 | - | - | 5 | - | 4 | - | MHz |
| | | | 4.5 | 30 | - | - | 25 | - | 20 | - | MHz |
| | | | 6 | 35 | - | - | 29 | - | 23 | - | MHz |
| $\overline{MR}$ Pulse Width (Figure 1) | $t_W$ | - | 2 | 60 | - | - | 75 | - | 90 | - | ns |
| | | | 4.5 | 12 | - | - | 15 | - | 18 | - | ns |
| | | | 6 | 10 | - | - | 13 | - | 15 | - | ns |

**Prerequisite For Switching Specifications**   (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C MIN | 25°C TYP | 25°C MAX | -40°C TO 85°C MIN | -40°C TO 85°C MAX | -55°C TO 125°C MIN | -55°C TO 125°C MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Clock Pulse Width (Figure 1) | $t_W$ | - | 2 | 80 | - | - | 100 | - | 120 | - | ns |
| | | | 4.5 | 16 | - | - | 20 | - | 24 | - | ns |
| | | | 6 | 14 | - | - | 17 | - | 20 | - | ns |
| Set-up Time Data to Clock (Figure 5) | $t_{SU}$ | - | 2 | 60 | - | - | 75 | - | 70 | - | ns |
| | | | 4.5 | 12 | - | - | 15 | - | 18 | - | ns |
| | | | 6 | 10 | - | - | 13 | - | 15 | - | ns |
| Hold Time, Data to Clock (Figure 5) | $t_H$ | - | 2 | 3 | - | - | 3 | - | 3 | - | ns |
| | | | 4.5 | 3 | - | - | 3 | - | 3 | - | ns |
| | | | 6 | 3 | - | - | 3 | - | 3 | - | ns |
| Removal Time, $\overline{MR}$ to Clock | $t_{REM}$ | - | 2 | 50 | - | - | 65 | - | 75 | - | ns |
| | | | 4.5 | 10 | - | - | 13 | - | 15 | - | ns |
| | | | 6 | 9 | - | - | 11 | - | 13 | - | ns |
| **HCT TYPES** | | | | | | | | | | | |
| Maximum Clock Frequency (Figure 2) | $f_{MAX}$ | - | 4.5 | 25 | - | - | 20 | - | 16 | - | MHz |
| $\overline{MR}$ Pulse Width (Figure 2) | $t_W$ | - | 4.5 | 12 | - | - | 15 | - | 18 | - | ns |
| Clock Pulse Width (Figure 2) | $t_W$ | - | 4.5 | 20 | - | - | 25 | - | 30 | - | ns |
| Set-up Time Data to Clock (Figure 6) | $t_{SU}$ | - | 4.5 | 12 | - | - | 15 | - | 18 | - | ns |
| Hold Time, Data to Clock (Figure 6) | $t_H$ | - | 4.5 | 3 | - | - | 3 | - | 3 | - | ns |
| Removal Time, $\overline{MR}$ to Clock | $t_{REM}$ | - | 4.5 | 10 | - | - | 13 | - | 15 | - | ns |

**Switching Specifications**   Input $t_r$, $t_f$ = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C TYP | 25°C MAX | -40°C TO 85°C MAX | -55°C TO 125°C MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **HC TYPES** | | | | | | | | |
| Propagation Delay, Clock to Output (Figure 3) | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | - | 150 | 190 | 225 | ns |
| | | | 4.5 | - | 30 | 38 | 45 | ns |
| | | | 6 | - | 26 | 30 | 38 | ns |
| | | $C_L$ = 15pF | 5 | 12 | - | - | - | ns |
| Propagation Delay, $\overline{MR}$ to Output (Figure 3) | $t_{PHL}$ | $C_L$ = 50pF | 2 | - | 150 | 190 | 225 | ns |
| | | | 4.5 | - | 30 | 38 | 45 | ns |
| | | | 6 | - | 26 | 30 | 38 | ns |
| Output Transition Time (Figure 3) | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 2 | - | 75 | 95 | 110 | ns |
| | | | 4.5 | - | 15 | 19 | 22 | ns |
| | | | 6 | - | 13 | 16 | 19 | ns |
| Input Capacitance | $C_I$ | - | - | - | 10 | 10 | 10 | pF |
| Maximum Clock Frequency | $f_{MAX}$ | $C_L$ = 15pF | 5 | 60 | - | - | - | MHz |

**Switching Specifications** Input $t_r$, $t_f$ = 6ns **(Continued)**
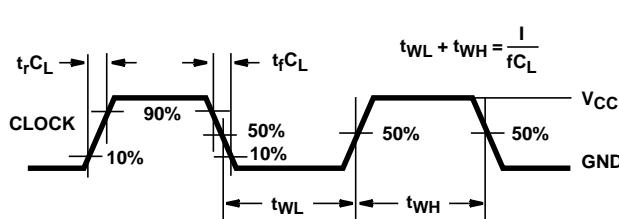
| PARAMETER | SYMBOL | TEST CONDITIONS | V$_{CC}$ (V) | 25°C | | -40°C TO 85°C | -55°C TO 125°C | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | | TYP | MAX | MAX | MAX | |
| Power Dissipation Capacitance (Notes 5, 6) | C$_{PD}$ | - | 5 | 25 | - | - | - | pF |
| **HCT TYPES** | | | | | | | | |
| Propagation Delay, Clock to Output (Figure 4) | t$_{PLH}$, t$_{PHL}$ | C$_L$ = 50pF | 4.5 | - | 30 | 38 | 45 | ns |
| | | C$_L$ = 15pF | 5 | 12 | - | - | - | ns |
| Propagation Delay, $\overline{MR}$ to Output (Figure 4) | t$_{PHL}$ | C$_L$ = 50pF | 4.5 | - | 32 | 40 | 48 | ns |
| Output Transition Time | t$_{TLH}$, t$_{THL}$ | C$_L$ = 50pF | 4.5 | - | 15 | 19 | 22 | ns |
| Input Capacitance | C$_{IN}$ | - | - | - | 10 | 10 | 10 | pF |
| Maximum Clock Frequency | f$_{MAX}$ | C$_L$ = 15pF | 5 | 50 | - | - | - | MHz |
| Power Dissipation Capacitance (Notes 5, 6) | C$_{PD}$ | - | 5 | 25 | - | - | - | pF |

NOTES:

5. C$_{PD}$ is used to determine the dynamic power consumption, per flip-flop.
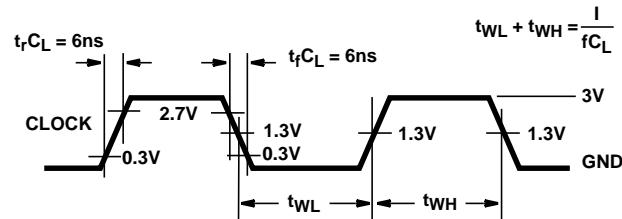
6. $P_D = C_{PD} V_{CC}^2 f_i + \Sigma (C_L V_{CC}^2 + f_O)$ where $f_i$ = Input Frequency, $f_O$ = Output Frequency, $C_L$ = Output Load Capacitance, $V_{CC}$ = Supply Voltage.

## *Test Circuits and Waveforms*
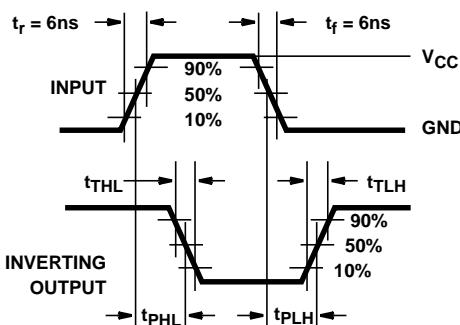


NOTE: Outputs should be switching from 10% V$_{CC}$ to 90% V$_{CC}$ in accordance with device truth table. For f$_{MAX}$, input duty cycle = 50%.

**FIGURE 1. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**
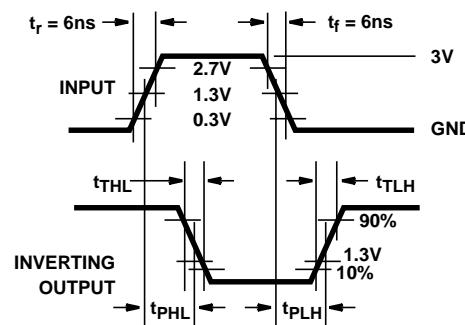


NOTE: Outputs should be switching from 10% V$_{CC}$ to 90% V$_{CC}$ in accordance with device truth table. For f$_{MAX}$, input duty cycle = 50%.

**FIGURE 2. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH**
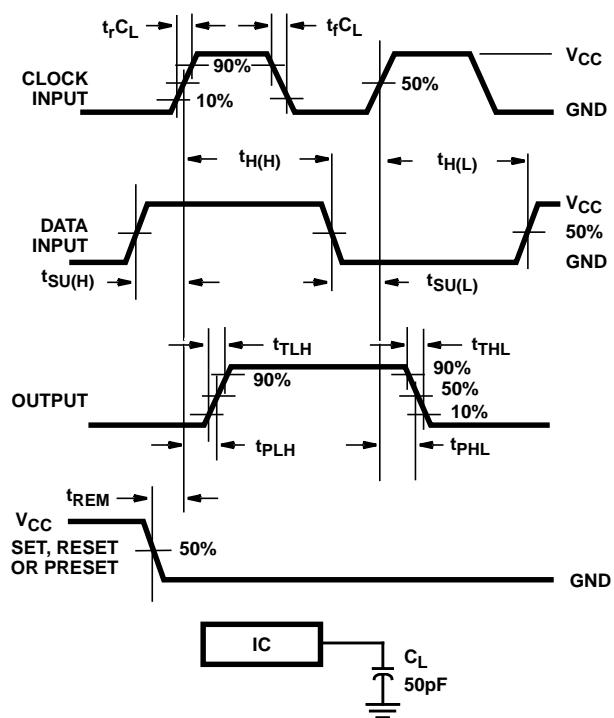


**FIGURE 3. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**
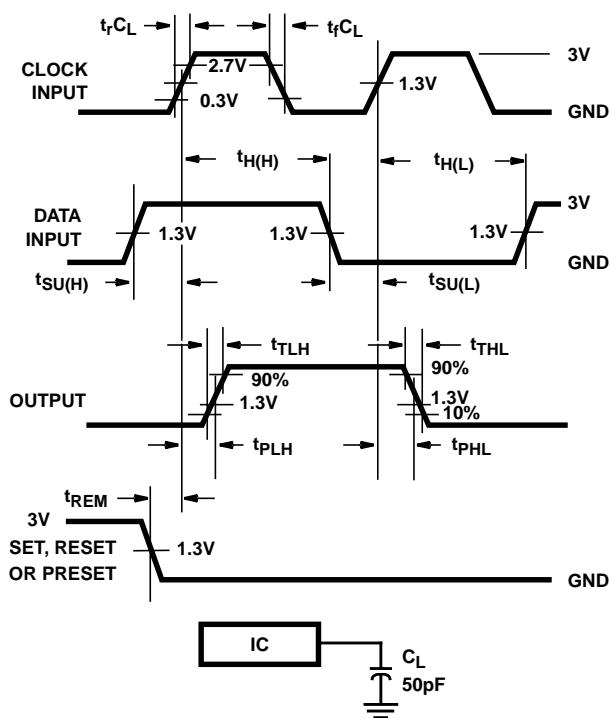


**FIGURE 4. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC**

## *Test Circuits and Waveforms* (Continued)



**FIGURE 5. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**



**FIGURE 6. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS**

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