AS5410

3D-Hall Absolute Linear Position Sensor

General Description

The chip can measure magnetic field components in two different orientation directions and converts the magnetic field information into absolute position information. The AS5410 supports absolute linear position measurement applications.

Only a simple 2-pole magnet is required as the magnetic field source.

Using two 3D-Hall cells allows both absolute as well as differential 3D magnetic field measurement.

The differential measurement makes the AS5410 ideal for use in rough industrial position sensing applications that include not only dust, dirt or moisture but also unwanted magnetic stray fields.

All the signal conditioning, including compensation of temperature effects, linearization of the output is included in the IC.

The absolute position information of the magnet is directly accessible over a SPI interface and PWM output. A cycle redundancy check (CRC) allows verification of the received data.

The AS5410 is available in a 14-pin TSSOP package and is qualified for an ambient temperature range from -40°C to 105°C.

It operates at a supply voltage of 3.3V ±10%.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS5410, 3D-Hall Absolute Linear Position Sensor are listed below:

Figure 1:
Added Value of Using AS5410

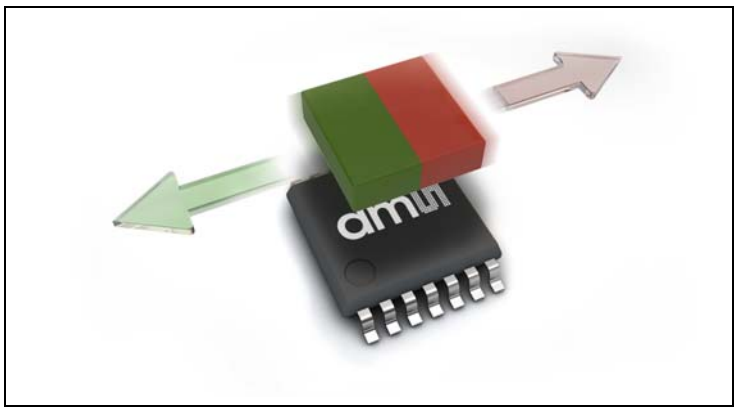
Benefits	Features
• High flexibility in magnet selection	• Wide magnetic input range
• Suppression against magnetic stray fields	• Dual 3D sensor pixel principle
• Flexibility in choice of interface	• SPI and PWM output
• Contactless position sensing	• Absolute linear position sensing
• Flexible mechanical arrangement of magnet	• Flexible configuration registers
• External calculations of raw data	• Bx and Bz raw data assessment possible
• High linearity after teaching	• 33 linearization points to achieve high precision
• Ideal for applications in harsh environments	• Integrated diagnostic functions • Temperature range from -40°C to 105°C (ambient)

Applications

AS5410 is ideal for:

- Plunger position
- Pedal position
- Pneumatic and hydraulic cylinder position
- Automation with linear position stages through cascading of several AS5410 devices.

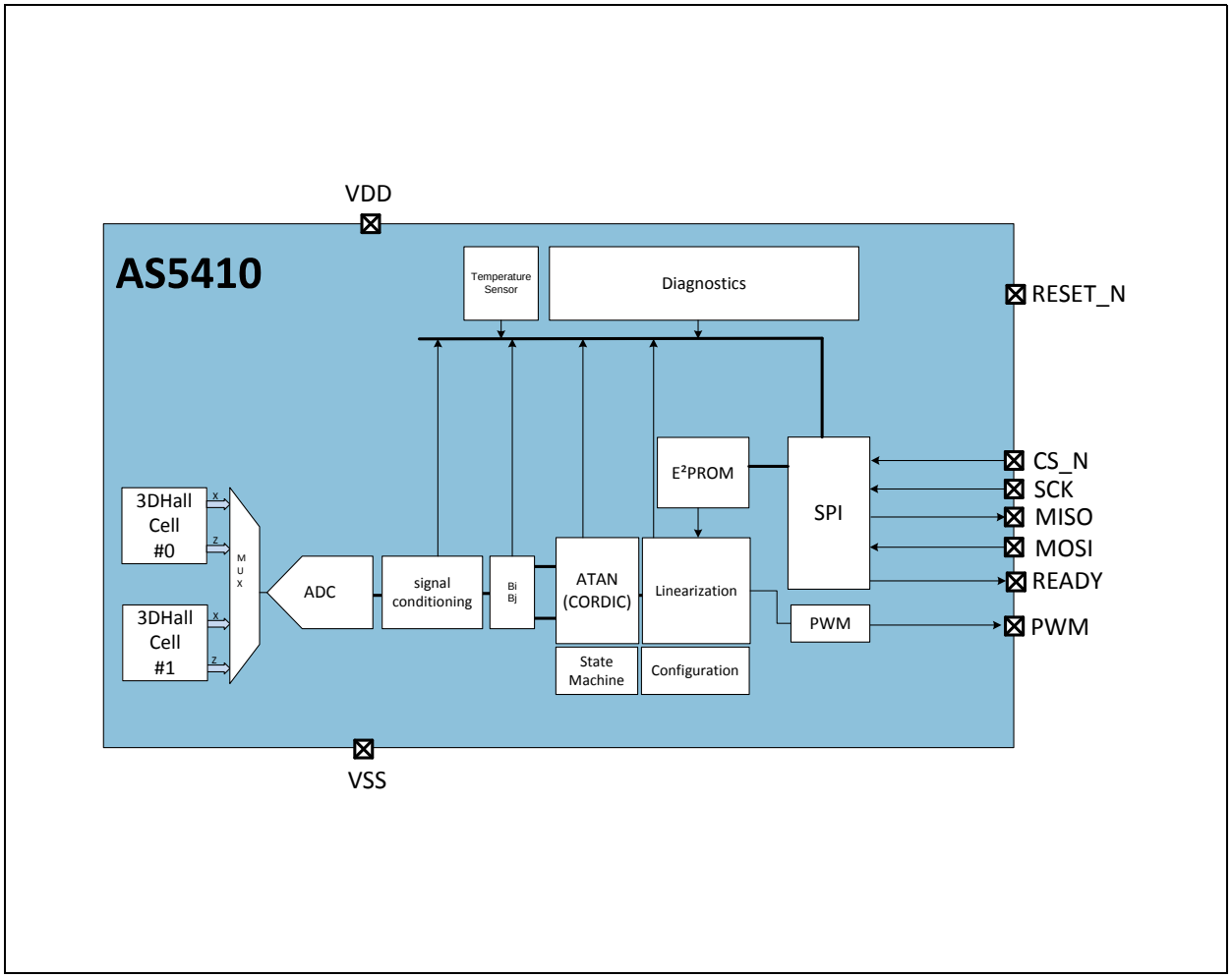
Figure 2:
AS5410 Linear Position Sensing of the Magnet



Block Diagram

The functional blocks of this device are shown below.

Figure 3:
AS5410 Block Diagram

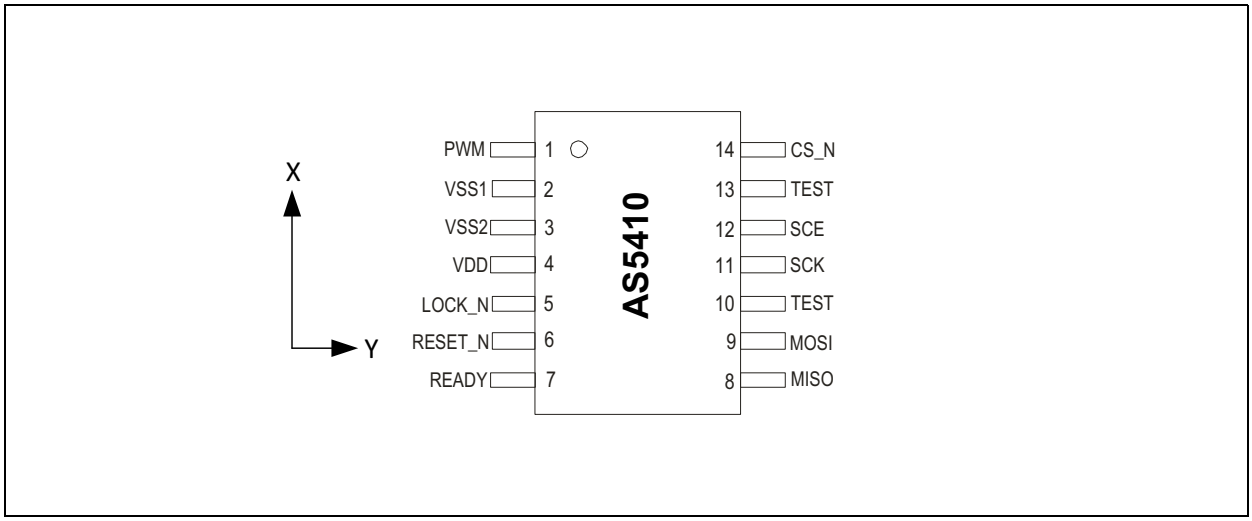


3D Hall cells:	The AS5410 contains two 3D Hall cells, spaced 2.5mm apart.
MUX:	The multiplexer selects two magnetic field components Bx and Bz as the inputs for the CORDIC. The selected inputs can either be absolute sensor signals or differential sensor signals.
ADC:	The Sigma-Delta ADC samples the Hall sensors signals selected by the MUX. The sampling of the sensors is done sequentially.
Signal conditioning:	This block includes offset and temperature compensation as well as amplitude matching.
Bi/Bj values:	This block represents the registers containing the input sensor signals of the CORDIC inputs.
ATAN:	Coordinate to Rotation Digital Computer: This block converts rectangular coordinates (sine and cosine signals from the Hall sensors) into polar coordinates (angle/distance and magnitude).
Linearization:	A 33-point linearization of the CORDIC output data is available to accommodate a variety of different magnet sizes and applications.
Temperature sensor:	An on-chip temperature sensor is available. It can be read over the SPI interface. This sensor is also used for signal conditioning.
PWM interface:	The linearized measurement data is available over a single pin in the form of a pulse width modulated (PWM) signal.
SPI interface:	A bi-directional SPI interface allows communication with the chip, including reading measurement data, E^2PROM contents or writing configuration data.
E^2PROM:	The on-chip E^2PROM contains the configuration data of the chip.
State machine:	The state machine (sequencer) controls the automatic sequencing of measurements. Once it is configured for a certain measurement, the state machine executes all necessary steps to perform a complete measurement cycle.
Configuration:	The configuration is pre-defined in the AS5410. Mode selection.

Pin Assignment

Pin Diagram

Figure 4:
AS5410 Pin Configuration, TSSOP-14 Package (Top View)



Note(s) and/or Footnote(s):

1. X indicates the axis of lateral position measurement; z axis is perpendicular to the package surface

Pin Description

Figure 5:
Pin Description

Pin TSSOP	Symbol	Type	Description
1	PWM	DO	PWM output. The linearized output data is available on this pin.
2	VSS2	S	Ground (0V) (1)
3	VSS1	S	Ground (0V)(1)
4	VDD	S	Positive supply voltage (3.0V to 3.6V)
5	LOCK_N	DI_ST	Test pin, must be connected to VSS in normal operation
6	RESET_N	DIO_ST	Reset input (active low) to be connected with open drain driver. In case of output application leave open
7	READY	DO	Measurement ready signal is set high when a measurement cycle is completed and the results in the output registers are valid
8	MISO	DO_T	Master in / Slave out (SPI interface data output)
9	MOSI	DI_ST	Master out / Slave in (SPI interface data input)
10	TEST	DIO	Must be connected to VSS.

Pin TSSOP	Symbol	Type	Description
11	SCK	DI_ST	SPI interface clock input (max. 1 MHz)
12	SCE	DI_ST	Test pin, must be connected to VSS in normal operation
13	TEST	DI_ST	Test pin, must be connected to VSS in normal operation
14	CS_N	DI_ST	Chip select (active low)

Note(s) and/or Footnote(s):

1. Both VSS1 and VSS2 must be connected.
2. CS_N is active low and activates data transmission. If only a single device is used, CS_N may remain low for several commands, for example while reading the output registers.

Abbreviations for Pin Types in Figure 5:

DO : Digital output

DIO : Digital input & output

DI_ST : Digital Schmitt-Trigger input

DO_T : Digital output /tri-state

S : Supply pin

DIO_ST : Digital Schmitt-Trigger input & output

Electrical Characteristics

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings

Parameter	Min	Max	Unit	Comments
DC supply voltage at pin VDD		5	V	
Input pin voltage	-0.3	VDD +0.3	V	
Input current (latchup immunity)	-100	100	mA	Norm: JEDEC 78
Electrostatic discharge	± 2		kV	Norm: MIL 883 E method 3015
Storage temperature	-55	150	°C	Min – 67°F; Max 257°F
Body temperature		260	°C	IPC/JEDEC J-Std-020 Lead finish 100% Sn “matte tin”
Relative humidity (non-condensing)	5	85	%	
Moisture sensitivity level (MSL)	3			Represents a maximum floor time of 168h
EEPROM read/write cycles		100	cycles	

Operating Conditions

Operating conditions: operating temperature = -40°C to 105°C, VDD = 3.0-3.6V unless otherwise noted.

Figure 7:
Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Note
VDD	Positive supply voltage	3.0	3.3	3.6	V	
Isupp	Supply current		15		mA	Active operation, continuous mode
T_{AMB}	Operating ambient temperature	-40		105	°C	-40°F to 221°F
twu	Wake up time		2		ms	From cold start
twlp				200	µs	From standby; see Single Loop Mode

System Performance Specifications

Operating conditions: magnet placement as specified in Figure 2, operating temperature = -40°C to 105°C, VDD = 3.0V to 3.6V, unless otherwise noted.

Figure 8:
System Parameters

Symbol	Parameter	Min	Typ	Max	Unit	Note
B_{IR_x}	Magnetic Range X	±5 (1)		±60	mT	
B_{IR_z}	Magnetic Range Z	±5 (1)		±50	mT	
S_{var_x}	Sensitivity Variation absolute X			±1.85(2)	%	
S_{var_z}	Sensitivity Variation absolute Z			±1.05(2)	%	
dSx/dSz	Sensitivity Ratio Drift X/Z			±1.00(3)	%	
T_{S0}	Sampling rate configuration 0(4)		1	1.08	ms	
T_{S1}	Sampling rate configuration 1(4)		2	2.15	ms	

Note(s) and/or Footnote(s):

1. Minimum condition is valid if both input components are above 5mT.
2. Maximum value of 1 sigma (static variation). Sensitivity variation absolute from part to part. Better performance can be reached with linearization step at end of line.
3. Over temperature. Value in % (1 sigma).
4. Configurable in register 000Bh.

DC Characteristics for Digital Inputs and Outputs

CMOS Schmitt-Trigger Inputs: LOCK_N, RESET_N, CLK, MOSI, SCK, CS_N

Operating conditions: operating temperature = -40°C to 105°C, VDD = 3.0V to 3.6V unless otherwise noted.

Figure 9:
CMOS Schmitt-Trigger Inputs

Symbol	Parameter	Min	Max	Unit	Note
VIH	High level input voltage	1.77	1.87	V	VDD = 3.0V
		2.07	2.23		VDD = 3.6V
VIL	Low level input voltage	1.12	1.27	V	VDD = 3.0V
		1.42	1.52		VDD = 3.6V
I_{in}	Input current		10	mA	for Vin >VDD (1)

Note(s) and/or Footnote(s):

1. Input pin voltages higher than VDD (e.g. 5V TTL levels) must be limited by a series resistor to ensure that the maximum input current (Iin) is not exceeded.

CMOS Outputs: READY, MISO, PWM

Operating conditions: operating temperature = -40°C to 105°C, VDD = 3.0V to 3.6V unless otherwise noted.

Figure 10:
CMOS Outputs: READY, MISO, PWM

Symbol	Parameter	Min	Max	Unit	Note
VO_H	Output high level	2.5	VDD	V	
IO_H	Output current, source		8	mA	
VO_L	Output low level	0	0.4	V	
IO_L	Output current, sink		8	mA	

Power On Reset

Operating conditions: operating temperature = -40°C to 105°C

Figure 11:
Power On Reset

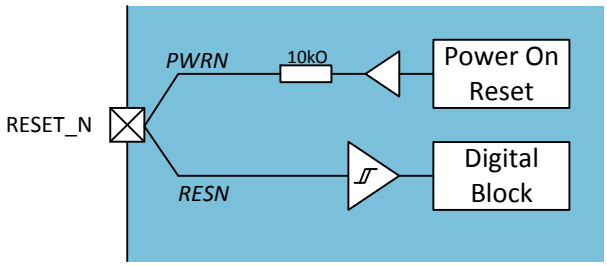
Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{ON}	Reset threshold; VDD level rising	1.4	2.38	2.97	V	
V_{OFF}	Reset threshold; VDD level falling	1.18	2.2	2.79	V	
Tpwrmin	Minimum reset pulse duration	1.8		7.1	µs	

RESET_N

The RESET_N pin can work as an output to monitor the internal power on reset signal (see Figure 12).

The RESET_N can also work as an input and trigger an internal reset. While power on cycle is not finished, communication is not allowed until the READY pin is high.

Figure 12:
Power On Reset



On-Chip Temperature Measurement

The AS5410 provides a linear on-chip temperature sensor which is use for automatic compensation of sensitivity and offset drifts for the Hall-In-One sensors.

The measured chip temperature is available in a register (0110h) and can be used for monitoring purposes.

Operating conditions: operating temperature = -40°C to 105°C

Figure 13:
Temperature Sensor

Symbol	Parameter	Min	Typ	Max	Unit	Note
D_{temp}	Temperature signal at 25°		0		LSB	
Res_{temp}	Resolution	185	200	210	LSB/K	

Detailed Description

Power Modes

The AS5410 can be configured for two power modes:

- Continuous mode
- Single loop mode

Continuous Mode

In this mode, the AS5410 is always active. The chip continuously updates the output registers. The completion of a new measurement is signalled with pin READY.

Single Loop Mode

The AS5410 features an automatic power down mode. After completion of a measurement, the chip automatically suspends to standby. The SPI interface remains active. The control of this mode is possible over register 000Eh (see Register Description). A high on the Ready output indicates that a measurement is completed. The AS5410 suspends to stand-by state after the Ready output has been set.

Serial Interface (SPI)

The SPI interface provides data transfer between AS5410 and the external microcontroller.

The minimum number of connections between microcontroller and AS5410 is three:

1. MOSI: Master Out – Slave In; data transfer from microcontroller to AS5410 (Write)
2. MISO: Master In – Slave Out; data transfer from AS5410 to microcontroller (Read)
3. SCK: Serial clock; Data is written and read with the rising edge of SCK

Optionally, two further connections may be used:

1. CS_N: Chip select; this connection is mandatory when multiple AS5410 devices are connected in parallel. In electrically “noisy” environment it is recommended to use the CS_N connection in order to maintain safe data transfer.
   For a single unit, this connection is optional as the data transmission is synchronized automatically by the number of SCK cycles. In this case it is recommended to verify the synchronization by CRC, Data readback or repeated reading and cross-checking of subsequent measurements.
2. Ready: this output indicates when data is ready, it is cleared by reading data from address 0100h or 0122h.

Figure 14:
Hardware Connection Between AS5410 and Microcontroller

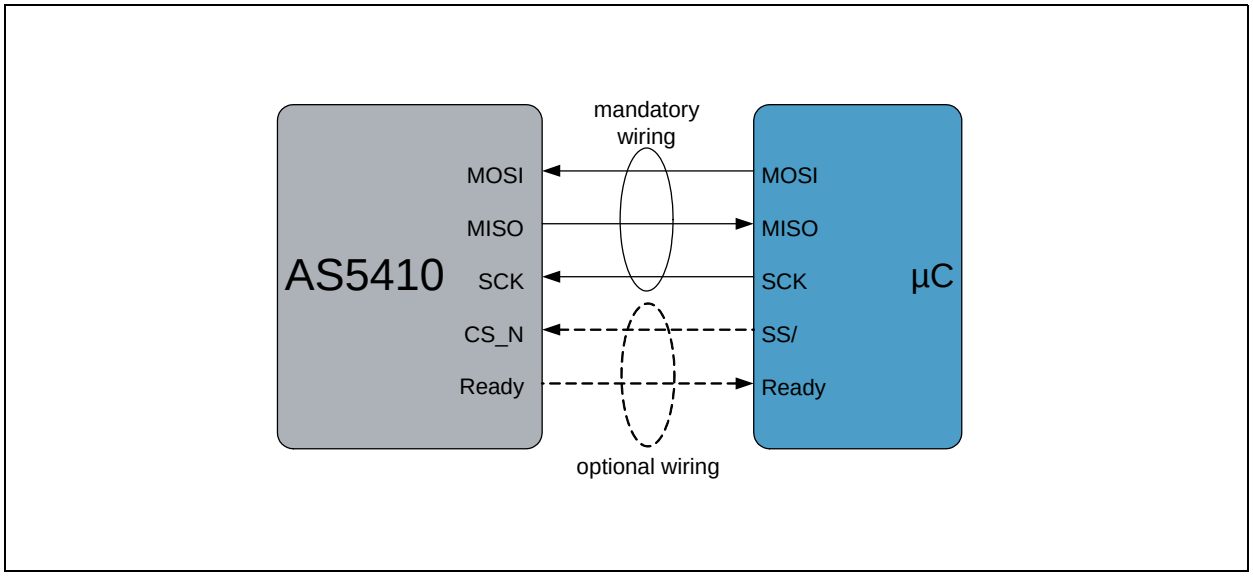
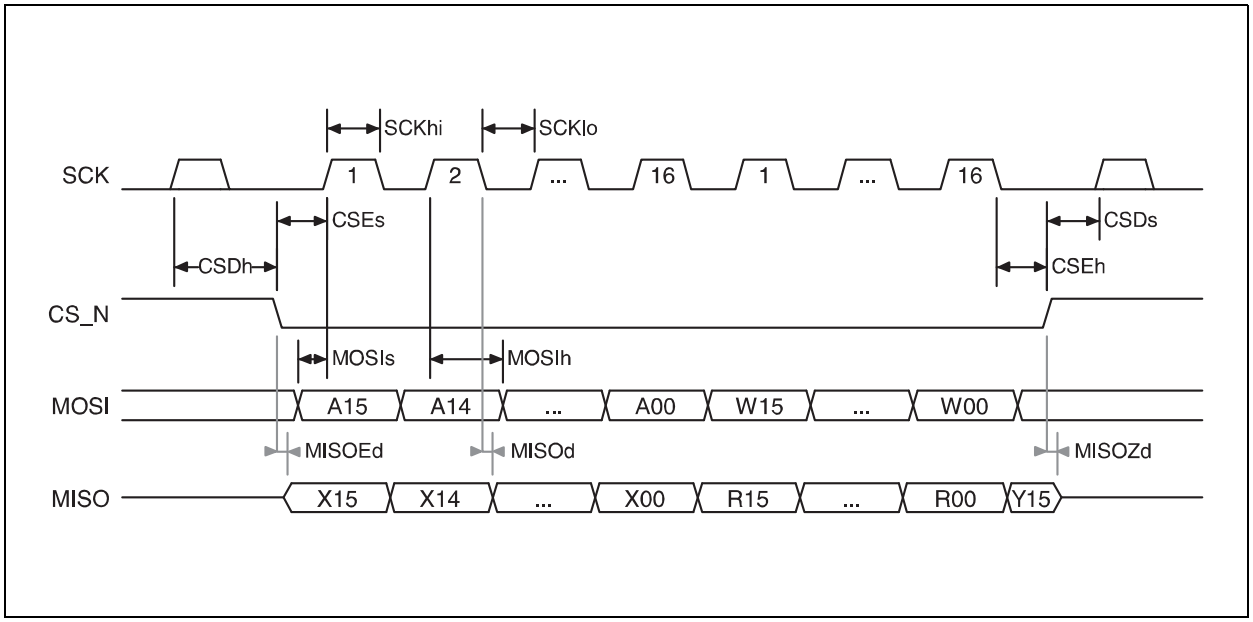


Figure 15:
SPI Timing Diagram



The data bits sent to the chip via MOSI and the data bits received from the chip via MISO are defined as follows (see also Figure 15):

A15 … A00	: 16-bit register address
W15 … W00	: 16-bit write data (in write mode)
X15 … X00, Y15	: 16-bit read data or previous command (depending on mode)
R15 … R0	: 16-bit read data in read mode or previous data in write mode

Figure 16:
SPI Timing

Symbol	Parameter	Min	Typ	Max	Unit	Note
f_{sck}	SCK frequency			1	MHz	
t_{SCKhi}	SCK pulse width HI	15			ns	
t_{SCKlo}	SCK pulse width LO	15			ns	
t_{CSEs}	CS_N enable setup time before SCK	10			ns	
t_{CSEh}	CS_N enable hold time after SCK	10			ns	
t_{CSDs}	CS_N disable setup time before SCK	10			ns	
t_{CSDh}	CS_N disable hold time after SCK	10			ns	
t_{MOSIs}	MOSI setup time before SCK	10			ns	
t_{MOSIh}	MOSI hold time after SCK	10			ns	
t_{MISOd}	MISO delay after SCK			10	ns	
t_{MISOEd}	MISO enable delay after CS_N			10	ns	
t_{MISOZd}	MISO high Z delay after CS_N			10	ns	
t_{Or}	Output edge rise time			3	ns	
t_{Of}	Output edge fall time			3	ns	

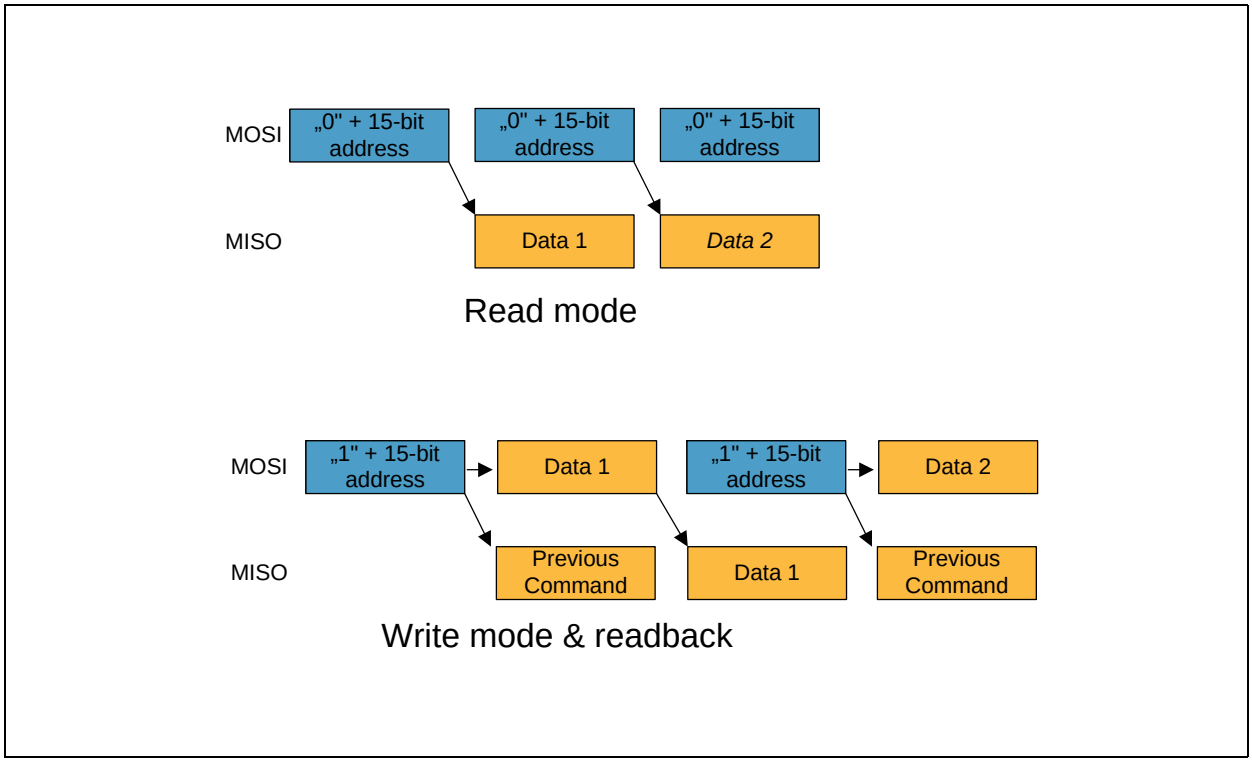
Data Transfer Between AS5410 and Microcontroller

Data is transferred to the AS5410 via the MOSI pin (Master Out – Slave In) with the rising edge of SCK.
Data is read from the AS5410 from the MISO pin (Master In – Slave Out) with the rising edge of SCK.

The data format consists of data streams with 32 bit in length. The first 16 bits define a 16-bit address and the subsequent 16 bits contain read or write data.

The MSB of the address word A<15> defines the direction of data transfer:
A<15> = 0 READ; data transfer from AS5410 to microcontroller; read measurement data
A<15> = 1 WRITE; data transfer from microcontroller to AS5410; write configuration data

Figure 17:
Data Transfer Between AS5410 and Microcontroller



Read Mode

For reading a register, the 16-bit Read address (with A<15>=0) is sent to the MOSI pin. After 16 SCK cycles, data of the specified address is read from the MISO pin (see Figure 17). At the same time, the new address may be clocked into the MOSI pin.

Continuous Measurement

It is possible to continuously read data from the AS5410 even if a new measurement is not yet finished. In this case, the last measurement data will be read. As soon as a new measurement is completed, it will be available at the SPI interface.

Write Mode and Readback

For additional safety and detection of communication errors, the actual contents of a register may be read at the same time as new data is written to this register.
In case of a Write command, the 16-bit Write address (with A<15>=1) is sent to the MOSI pin. After 16 SCK cycles, data following the address bits is written to the specified address via MOSI in (see Figure 17) At the same time, the present data of that register may be read from the MISO pin. Following the 16-bit of data (Data 1 in Figure 17), a new address may be written to the AS5410. While the new address is written, the address from the previous command is available at the MISO output.

Checksum

To avoid reading errors, the IC calculates a Checksum at every read cycle from the register content. The Checksum value is built by an XOR operation of the previous Checksum value and the read register content. The CRC is calculated every time a register is read.

By choosing how often the Checksum is read and rechecked by the master it is possible to adjust the communication speed and safety level.

The Checksum value is stored in register 0108h (see Register Description).

PWM Data Transmission

In addition to the SPI interface, the AS5410 offers a PWM output that provides data transmission of the linearized output data over a single wire. The base frequency of the PWM is the system clock frequency, so one PWM digit always corresponds to approx. 125ns. The PWM resolution is set by 3 bits (PWMPreScale) which shift the 16 bit wide angle value by 0 to 7 digits.

The duty cycle of the PWM signal lies between 0% to 100%. In case of an error, the duty cycle is 0%.

If register 0122h value increases the duty cycle decreases. If register 0122h value decreases the duty cycle increases.

Figure 18:
Register 000Dh

Register	Access	Bit	Function	Default	Note
000Dh: PWM settings	R/W	D15-10	PWMLimitHi <5:0>	0	PWM Limit High, Limits the PWM duty cycle to a maximum value
		D9-4	PWMLimitLo <5:0>	0	PWM Limit Low, Limits the PWM duty cycle to a minimum value
		D3	PWMEn	0	PWM Enable, Enables the PWM output
		D2-0	PWMPreScale <2:0>	0	PWM PreScale, Sets PWM frequency and resolution

Figure 19:
Single Pin Data Transmission Connection Diagram

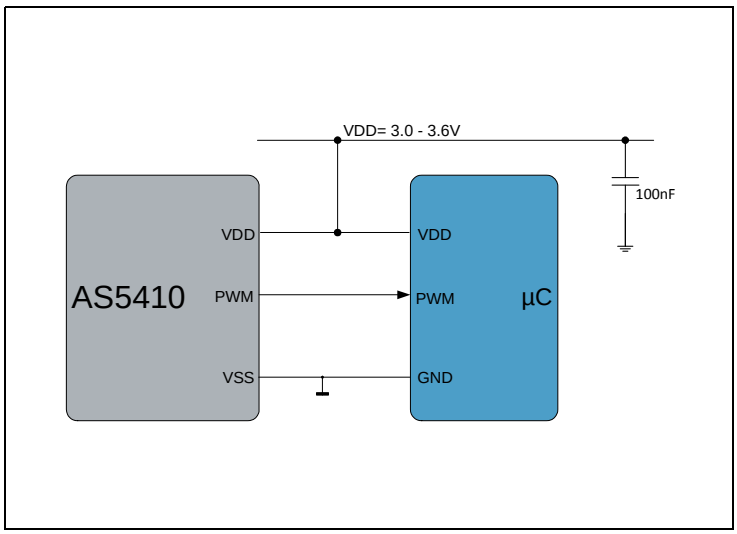


Figure 20:
PWM Duty Cycle Information

PWM Duty Cycle [%]	Register 122h (Linear Angle) [LSB]
0	32767
50	0
100	-32768

Between 0% to 100% the duty cycle is linear to the Linear Angle.

PWM Enable: Must be set high to enable the PWM mode.

PWMPreScale0 to PWMPreScale3: The PWM resolution is set by those 3 Bits.

Figure 21:
PWM Resolution

PWMPreScale0 to PWMPreScale3	Resolution (bit)	PWM (kHz)
000	16	0.122
001	15	0.244
010	14	0.488
011	13	0.977
100	12	1.953
101	11	3.906
110	10	7.813
111	9	15.63

PWMLimitHi5 to PWMLimitHi0: Limits the PWM duty cycle.

Figure 22:
PWM Upper Clamping Limits

Duty Cycle	PWMLimitHi0 to PWMLimitHi5
Minimum 50%	000000
Minimum 0%	111111

Between 0% to 50% the duty cycle limit is linear to the binary values selected by PWMLimitHi5 to PWMLimitHi0.
The limits are clamping limits (by selecting limits the resolution decreases).

PWMLimitLo5 to PWMLimitLo0: Limits the PWM duty cycle.

Figure 23:
PWM Lower Clamping Limits

Duty Cycle	PWMLimitLo0 to PWMLimitLo5
Maximum 50%	111111
Maximum 100%	000000

Between 50% to 100% the duty cycle limit is linear to the binary values selected by PWMLimitLo5 to PWMLimitLo0. The limits are clamping limits (by selecting limits the resolution decreases).

Figure 24:
PWM Setting Example

Clamping Range	0% – 100% PWM Duty Cycle	10% – 90% PWM Duty Cycle	50% – 50% PWM Duty Cycle
PWMLimitHi5	1	1	0
PWMLimitHi4	1	1	0
PWMLimitHi3	1	0	0
PWMLimitHi2	1	0	0
PWMLimitHi1	1	1	0
PWMLimitHi0	1	0	0
PWMLimitLo5	0	0	1
PWMLimitLo4	0	0	1
PWMLimitLo3	0	1	1
PWMLimitLo2	0	1	1
PWMLimitLo1	0	0	1
PWMLimitLo0	0	1	1

Register Description

The following registers can be addressed by the user via the SPI interface. Each register is 16-bit wide.

Registers not listed in the table below must not be modified from their factory programmed setting.

Note(s): "r" are reserved bits, they must not be modified (unless otherwise noted)

Register 000Bh

This register controls the sequencer

Figure 25:
Register 000Bh

Register	Access	Bit	Function	Default	Note
000Bh: Sequencer control	R/W	D15 (MSB)	r	0	
		D14	r	0	
		D13	r	0	
		D12	r	0	
		D11	MgRangExt	0	"Magnet Range Extension" Enable the algorithm for an extended position range. 1 = Magnet Range Extension enabled 0 = Magnet Range Extension disabled
		D10	CoordSel	0	"Coordinate System Selection" 1 = The sign of the Lin Ang (Register 0122h) gets changed if MagDir (Register 000Bh) = 1 0 = Lin Ang (Register 0122h) gets not changed
		D9	r	0	
		D8	r	0	
		D7	Table Select 0	0	These bits allow the selection of 4 different operating modes, stored in 4 individual sequencer tables
		D6	Table Select 1	0	
		D5	MagDir	0	This bit allows to switch the magnet direction MagDir = 0: North pole must point in +x direction (pin 7 to pin1) Default/powerup mode. MagDir = 1: North pole must point in -x direction (pin1 to pin7). Preferred orientation to permit use of CoordSel bit.

Register	Access	Bit	Function	Default	Note
000Bh: Sequencer control	R/W	D4	DiffMd	0	Differential mode: 0 = Absolute measurement of Hall cells, 1 = Differential measurement of Hall cells
		D3	r	0	
		D2	r	0	
		D1	RdyHZ	0	READY Tri-State: 0: The READY pin is always active. It must NOT be connected in parallel 1: The READY output may be connected in parallel. It is normally in high Z and only active (high) if the IC is selected. (1)
		D0 (LSB)	r	0	

Note(s) and/or Footnote(s):

1. A 10k pull down resistor is mandatory at the common READY signal line if RdyHz = 1.

Figure 26:
Possible Table Selection

	Table 0	Table 1	Table 2	Table 3
	Differential Mode		Absolute Pixel1	
	1kHz Sample Rate	0.5kHz Sample Rate	1kHz Sample Rate	0.5kHz Sample Rate
CORDIC Input Values	Pixelcell0, Bz0 = 0x112h -Pixelcell1, Bz1 = 0x111h Pixelcell0, Bx0 = 0x114h -Pixelcell1, Bx1 = 0x113h	Pixelcell0, Bz0 = 0x112h -Pixelcell1, Bz1 = 0x111h Pixelcell0, Bx0 = 0x114h -Pixelcell1, Bx1 = 0x113h	Pixelcell1, Bz1 = 0x111h Pixelcell1, Bx1 = 0x113h	Pixelcell1, Bz1 = 0x111h Pixelcell1, Bx1 = 0x113h
Register B Settings	Table Select 1… Table Select 0 = 00 (mandatory) DiffMd = 1 (mandatory) MgRangExt = 0 or 1 depending on application	Table Select 1… Table Select 0 = 01 (mandatory) DiffMd = 1 (mandatory) MgRangExt = 0 or 1 depending on application	Table Select 1… Table Select 0 = 10 (mandatory) DiffMd = 0 (mandatory) MgRangExt = 0 (mandatory)	Table Select 1… Table Select 0 = 11 (mandatory) DiffMd = 0 (mandatory) MgRangExt = 0 (mandatory)

Register 000Dh

Figure 27:
Register 000Dh

Register	Access	Bit	Function	Default	Note
000Dh:	R/W	D15 (MSB)	PWMLimitHi 5	1	PWM Limit High, Limits the PWM duty cycle to a maximum value
		D14	PWMLimitHi 4	1	
		D13	PWMLimitHi 3	0	
		D12	PWMLimitHi 2	0	
		D11	PWMLimitHi 1	1	
		D10	PWMLimitHi 0	1	
		D9	PWMLimitLo 5	0	PWM Limit Low, Limits the PWM duty cycle to a minimum value
		D8	PWMLimitLo 4	0	
		D7	PWMLimitLo 3	1	
		D6	PWMLimitLo 2	1	
		D5	PWMLimitLo 1	0	
		D4	PWMLimitLo 0	1	
		D3	PWMEn	0	PWM Enable, Enables the PWM output
		D2	PWM PreScale 2	0	PWM PreScale, Sets PWM frequency and resolution
		D1	PWM PreScale 1	1	
		D0 (LSB)	PWM PreScale 0	1	

Register 000Eh

This register holds the sequencer control bits.

Figure 28:
Register 000Eh

Register	Access	Bit	Function	Default	Note
000Eh: Sequencer control	R/W	D15 (MSB) – D2	r	0	
		D1	Seq	1	1 = Sequencer enabled (to be set to activate the state machine) 0 = Sequencer disabled
		D0 (LSB)	SL	0	1 = Single loop mode enabled 0 = Single loop mode disabled

Register 000Fh

This register holds the threshold and hysteresis of the CORDIC magnitude value (see Register 0120h), at which the "Magnet Lost" flag in register 0107h is set/cleared.

Figure 29:
Register 000Fh

Register	Access	Bit	Function	Default	Note
000Fh:	R/W	D15 (MSB)	r	0	Reserved
		D14	r	0	
		D13	r	0	
		D12	r	0	
		D11	r	0	
		H2	Hyst	0	Hysteresis for "magnet lost"
		H1	Hyst	0	
		H0	Hyst	1	
		V7	MgnLostLmt	0	Magnet lost threshold value compared to register 0121h
		V6	MgnLostLmt	0	
		V5	MgnLostLmt	0	
		V4	MgnLostLmt	0	
		V3	MgnLostLmt	0	
		V2	MgnLostLmt	0	
		V1	MgnLostLmt	1	
		V0 (LSB)	MgnLostLmt	1	

Note(s) and/or Footnote(s):

1. **V7 to V0:** The minimum allowed Magnitude of CORDIC can be selected. The binary number, represented by V7 to V0 must be multiplied with 64 to calculate the minimum allowed Magnitude of CORDIC.

Figure 30:
Example: Select V0 and V1.

Binary								Decimal
V7	V6	V5	V4	V3	V2	V1	V0	
0	0	0	0	0	0	1	1	3

The corresponding dual number to 00000011 is 3 this number multiplied with 64 is the minimum allowed magnitude of CORDIC.
64 * 3 = 192 = Threshold limit
If the magnitude of CORDIC turns under 192 the MagLost bit in register 0107h will turn form 0 to 1.

H2...H0: The hysteresis around the minimum allowed magnitude of CORDIC can be selected.

The hysteresis ***Hystd*** is calculated by the formula

Hyst : Hysteresis value in Register 000Fh

Hystd : Decimal hysteresis value around the minimum allowed magnitude of CORDIC

MgnLostLmt : The threshold limit as calculated in the example above.

(EQ1) $$\mathrm{Hystd} = \mathrm{MgnLostLmt} \times \frac{1}{2^{\mathrm{Hyst}}}$$

Figure 31:
Example: Select H0

Binary			Decimal
H2	H1	H0	
0	0	1	1

(EQ2) $$\mathrm{Hystd} = \mathrm{MgnLostLmt} \times \frac{1}{2^{\mathrm{Hyst}}} = 192 \times \frac{1}{2^{1}} = 96$$

Now the MagLost bit in register 0107h will turn form 0 to 1 at a magnitude of CORDIC value lower than 192. After the MagLost bit is 0 it turns back to 1 at a value higher than 288, because 192 + 96 = 288.

Register 0030h

E²PROM address

Figure 32:
Register 0030h

Register	Access	Bit	Function	Note
0030h: E²PROM address	R/W	D15 (MSB)	A15	To read/write E²PROM contents, the selected E²PROM address must be specified in this register. The corresponding data is available in register 0031h. For write operations, status bit ED in register 0107h which indicates the completion of a write operation must be verified before starting a new write cycle. Writing 16 bits of data requires ~10ms
		D14	A14	
		D13	A13	
		D12	A12	
		D11	A11	
		D10	A10	
		D9	A9	
		D8	A8	
		D7	A7	
		D6	A6	
		D5	A5	
		D4	A4	
		D3	A3	
		D2	A2	
		D1	A1	
		D0 (LSB)	A0	

Note(s) and/or Footnote(s):

1. 1LSB=4mT.

Register 0031h

E²PROM data

Figure 33:
Register 0031h

Register	Access	Bit	Function	Note
0031h: E²PROM data	R/W	D15 (MSB)	D15	This register holds the E²PROM contents of the address selected in register 0030h
		D14	D14	
		D13	D13	
		D12	D12	
		D11	D11	
		D10	D10	
		D9	D9	
		D8	D8	
		D7	D7	
		D6	D6	
		D5	D5	
		D4	D4	
		D3	D3	
		D2	D2	
		D1	D1	
		D0 (LSB)	D0	

Register 0032h

Figure 34:
Register 0032h

Register	Access	Bit	Function	Note
0032h: Page WRITE E^2PROM address	R/W	D15 (MSB)	A15	To page write E^2PROM contents, the selected E^2PROM address must be specified in this register.
		D14	A14	
		D13	A13	
		D12	A12	
		D11	A11	
		D10	A10	
		D9	A9	
		D8	A8	
		D7	A7	
		D6	A6	
		D5	A5	
		D4	A4	
		D3	A3	
		D2	A2	
		D1	A1	
		D0 (LSB)	A0	

Register 0033h

Figure 35:
Register 0033h

Register	Access	Bit	Function	Note
0033h: Page WRITE E^2PROM data	R/W	D15 (MSB)	D15	To page write E^2PROM contents, the E^2PROM data must be specified in this register.
		D14	D14	
		D13	D13	
		D12	D12	
		D11	D11	
		D10	D10	
		D9	D9	
		D8	D8	
		D7	D7	
		D6	D6	
		D5	D5	
		D4	D4	
		D3	D3	
		D2	D2	
		D1	D1	
		D0 (LSB)	D0	

Register 0107h

Status register; this register holds various status flags

Figure 36:
Register 0107h

Register	Access	Bit	Function	Note
0107h: Status	R	D15 (MSB)	RDY	Indicates completion of a new measurement; same function as the "Ready" output pin. 0 = calculation is in progress or chip not ready 1 = measurement completed, new measurement data is stored in register 0110h-0114h and 0120h-0122h
		D14	MagLost	1 = Magnetic field values are too low for position measurement; the threshold level can be selected at Register 000Fh Bit D7 to D0
		D13	CorrOvfl	Ambiguous angle correction overflow
		D12	NormOvfl	Normalizing scale overflow
		D11	SensOvfl	Overflow during sensitivity correction over temperature
		D10	RngWarn	ADC overflow
		D9	HistWarn	Histogram failure during ADC operation
		D8	CalcError	Or wired combination of RngWarn, HistWarn, NormOvfl, SensOvfl
		D7	D7	Reserved
		D6	D6	Reserved
		D5	D5	Reserved
		D4	D4	Reserved
		D3	D3	Reserved
		D2	D2	Reserved
		D1	MagDir	Detected or chosen orientation of magnet
		D0 (LSB)	ED	E^2PROM write cycle: 0 = E^2PROM write cycle in progress 1= E^2PROM write cycle completed

Register 0108h

Cycle Redundancy Check (CRC):

Figure 37:
Register 0108h

Register	Access	Bit	Function	Note
0108h: CRC	R	D15 (MSB)	CRC15	Checksum reading check
		D14	CRC14	
		D13	CRC13	
		D12	CRC12	
		D11	CRC11	
		D10	CRC10	
		D9	CRC9	
		D8	CRC8	
		D7	CRC7	
		D6	CRC6	
		D5	CRC5	
		D4	CRC4	
		D3	CRC3	
		D2	CRC2	
		D1	CRC1	
		D0 (LSB)	CRC0	

Register 0110h

On-chip temperature sensor

Figure 38:
Register 0110h

Register	Access	Bit	Function	Note
0110h: Temperature	R	D15 (MSB)	T15	On-chip temperature sensor Temperature [°C] = (Register 0110h / 200) + 25
		D14	14	
		D13	T13	
		D12	T12	
		D11	T11	
		D10	T10	
		D9	T9	
		D8	T8	
		D7	T7	
		D6	T6	
		D5	T5	
		D4	T4	
		D3	T3	
		D2	T2	
		D1	T1	
		D0 (LSB)	T0	

Register 0111h

Magnetic field of Pixel cell 1; Z field sensor cell

Figure 39:
Register 0111h

Register	Access	Bit	Function	Note
0111h: Magnetic field value	R	D15 (MSB)	Bz1	Magnetic field Bz of Pixel-cell 1 (1LSB=~4mT)
		D14		
		D13		
		D12		
		D11		
		D10		
		D9		
		D8		
		D7		
		D6		
		D5		
		D4		
		D3		
		D2		
		D1		
		D0 (LSB)		

Register 0112h

Magnetic field of Pixel cell 0; Z field sensor cell

Figure 40:
Register 0112h

Register	Access	Bit	Function	Note
0112h: Magnetic field value	R	D15 (MSB)	Bz0	Magnetic field Bz of Pixel-cell 0 (1LSB=~4mT)
		D14		
		D13		
		D12		
		D11		
		D10		
		D9		
		D8		
		D7		
		D6		
		D5		
		D4		
		D3		
		D2		
		D1		
		D0 (LSB)		

Register 0113h

Magnetic field of Pixel cell 1; X field sensor cell

Figure 41:
Register 0113h

Register	Access	Bit	Function	Note
0113h: Magnetic field value	R	D15 (MSB)	Bx1	Magnetic field Bx of Pixel-cell 1 (1LSB=~4mT)
		D14		
		D13		
		D12		
		D11		
		D10		
		D9		
		D8		
		D7		
		D6		
		D5		
		D4		
		D3		
		D2		
		D1		
		D0 (LSB)		

Register 0114h

Magnetic field of Pixel cell 0; X field sensor cell

Figure 42:
Register 0114h

Register	Access	Bit	Function	Note
0114h: Magnetic field value	R	D15 (MSB)	Bx0	Magnetic field Bx of Pixel-cell 0 (1LSB=~4mT)
		D14		
		D13		
		D12		
		D11		
		D10		
		D9		
		D8		
		D7		
		D6		
		D5		
		D4		
		D3		
		D2		
		D1		
		D0 (LSB)		

Register 0120h

CORDIC magnitude value; this is representing the strength of the magnetic field, as calculated by the CORDIC.
These values may for example be used to check the magnet for out-of-range conditions, or to issue a “weak magnetic field” warning when the value gets below a certain threshold.

(EQ3) $$0120\text{h} = 0.82338 \times \sqrt{0111\text{h}^2 + 0113\text{h}^2}$$

(EQ4) $$0120\text{h} = 0.82338 \times \sqrt{(0112\text{h} - 0111\text{h})^2 + (0114\text{h} - 0113\text{h})^2}$$

Figure 43:
Register 0120h

Register	Access	Bit	Function	Note
0120h: Magnitude	R	D15 (MSB)	Mag	Magnitude value of CORDIC Calculation in absolute mode (DiffMd = 0) See EQ 3 Calculation in differential mode (DiffMd = 1) See EQ 4
		D14		
		D13		
		D12		
		D11		
		D10		
		D9		
		D8		
		D7		
		D6		
		D5		
		D4		
		D3		
		D2		
		D1		
		D0 (LSB)		

Register 0121h

CORDIC angle value; this is representing the (non-linearized) angle or direction of the magnetic field, as calculated by the CORDIC.

(EQ5) $$\text{Ang}[^\circ] = \frac{360}{65536} \times 0121\text{h}$$

(EQ6) $$\text{Ang}[^\circ] = \frac{576}{65536} \times 0121\text{h}$$

Figure 44:
Register 0121h

Register	Access	Bit	Function	Note
0121h: Angle	R	D15 (MSB)	Ang	Ang [°]…angle value of CORDIC [°] 0121*h* … angle value of CORDIC [LSB] MgRangExt = 0: See EQ 5 MgRangExt = 1: See EQ 6
		D14		
		D13		
		D12		
		D11		
		D10		
		D9		
		D8		
		D7		
		D6		
		D5		
		D4		
		D3		
		D2		
		D1		
		D0 (LSB)		

Register 0122h

This register holds the final, calculated and linearized position information

(EQ7) $$\mathrm{LinAng}[^\circ] = \frac{360}{65536} \times 0122\mathrm{h}$$

(EQ8) $$\mathrm{LinAng}[^\circ] = \frac{576}{65536} \times 0122\mathrm{h}$$

Figure 45:
Register 0122h

Register	Access	Bit	Function	Note
0122h: Position	R	D15 (MSB)	LinAng	This register holds the linearized 16-bit position information. LinAng [°]…linearized 16-bit position information [°] 0121*h* … linearized 16-bit position information [LSB] MgRangExt = 0: See EQ 7 MgRangExt = 1: See EQ 8
		D14		
		D13		
		D12		
		D11		
		D10		
		D9		
		D8		
		D7		
		D6		
		D5		
		D4		
		D3		
		D2		
		D1		
		D0 (LSB)		

E²PROM

AS5410 is equipped with a 1kx8 E²PROM memory to store the factory settings and the customer configuration data. The device can be configured using the 4wire Serial Peripheral Interface (SPI).

Figure 46:
E²PROM Memory Map

Address (hex)	E²PROM Location Name	Notes
000Bh	Sequencer control	
000Dh	PWM configuration	
000Fh	Magnet lost threshold and hysteresis	
005Fh	Angle linearization Table entry 16	Applied to CORDIC output
0060h	Angle linearization Table entry 0	
0061h	Angle linearization Table entry 1	
0062h	Angle linearization Table entry 2	
0063h	Angle linearization Table entry 3	
0064h	Angle linearization Table entry 4	
0065h	Angle linearization Table entry 5	
0066h	Angle linearization Table entry 6	
0067h	Angle linearization Table entry 7	
0068h	Angle linearization Table entry 8	
0069h	Angle linearization Table entry 9	
006Ah	Angle linearization Table entry 10	
006Bh	Angle linearization Table entry 11	
006Ch	Angle linearization Table entry 12	
006Dh	Angle linearization Table entry 13	
006Eh	Angle linearization Table entry 14	
006Fh	Angle linearization Table entry 15	
0070h	Angle linearization Table entry -16	
0071h	Angle linearization Table entry -15	
0072h	Angle linearization Table entry -14	
0073h	Angle linearization Table entry -13	

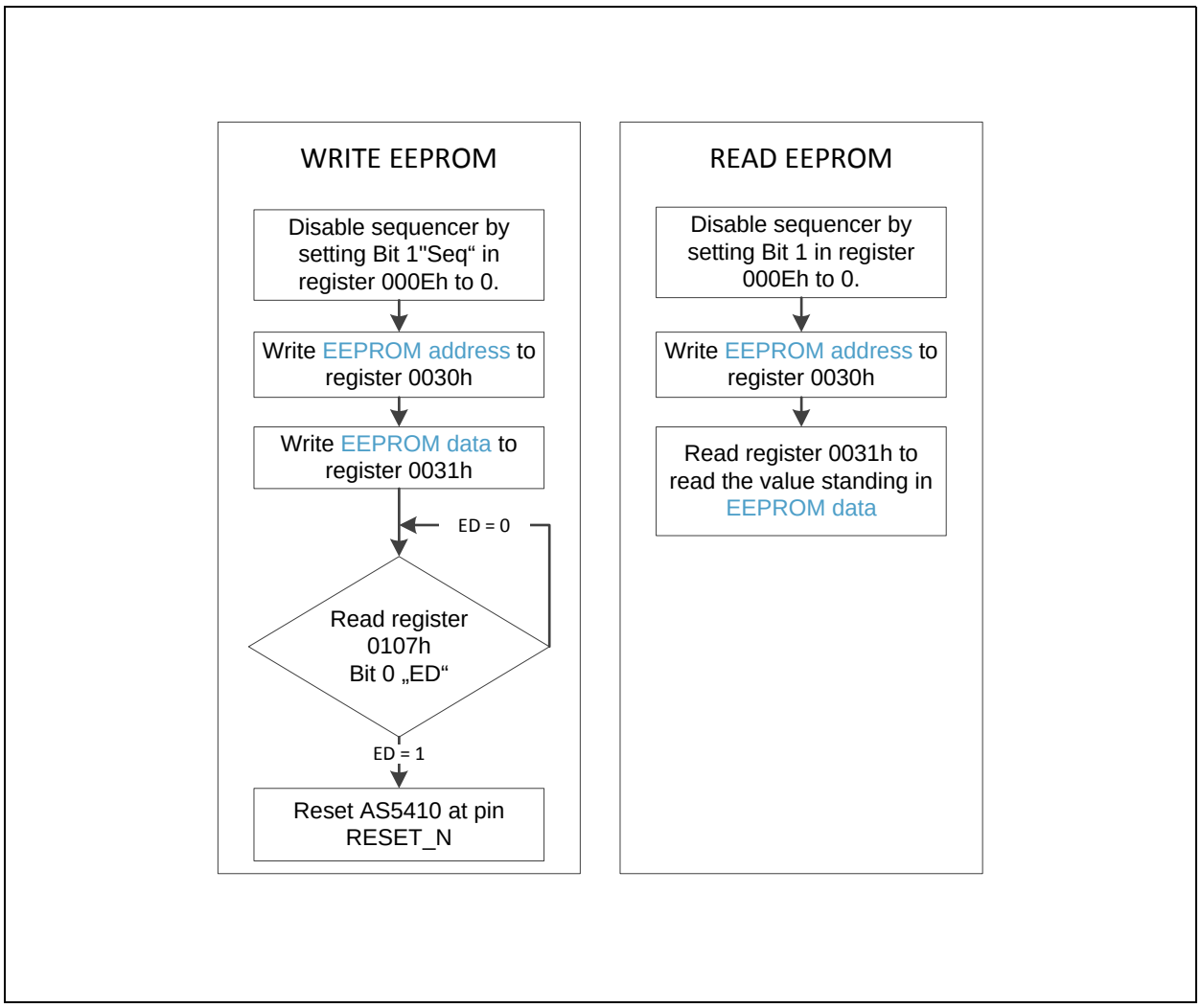
Address (hex)	E²PROM Location Name	Notes
0074h	Angle linearization Table entry -12	Applied to CORDIC output
0075h	Angle linearization Table entry -11	
0076h	Angle linearization Table entry -10	
0077h	Angle linearization Table entry -9	
0078h	Angle linearization Table entry -8	
0079h	Angle linearization Table entry -7	
007Ah	Angle linearization Table entry -6	
007Bh	Angle linearization Table entry -5	
007Ch	Angle linearization Table entry -4	
007Dh	Angle linearization Table entry -3	
007Eh	Angle linearization Table entry -2	
007Fh	Angle linearization Table entry -1	

Note(s) and/or Footnote(s):

1. The Angle linearization points can be used to achieve higher precision at the angle output.

E²PROM WRITE/READ

Figure 47:
E²PROM WRITE/READ Cycle



For reading from the E²PROM the E²PROM address is written to register 0030h and the stored E²PROM data can be read from register 0031h.

For writing to the E²PROM the E²PROM address is written to register 0030h and the E²PROM data can be written to register 0031h. The write cycle is completed when the ED (E²PROM Done) bit is set to 1.

E²PROM Page WRITE

Figure 48:
Page E²PROM WRITE Cycle

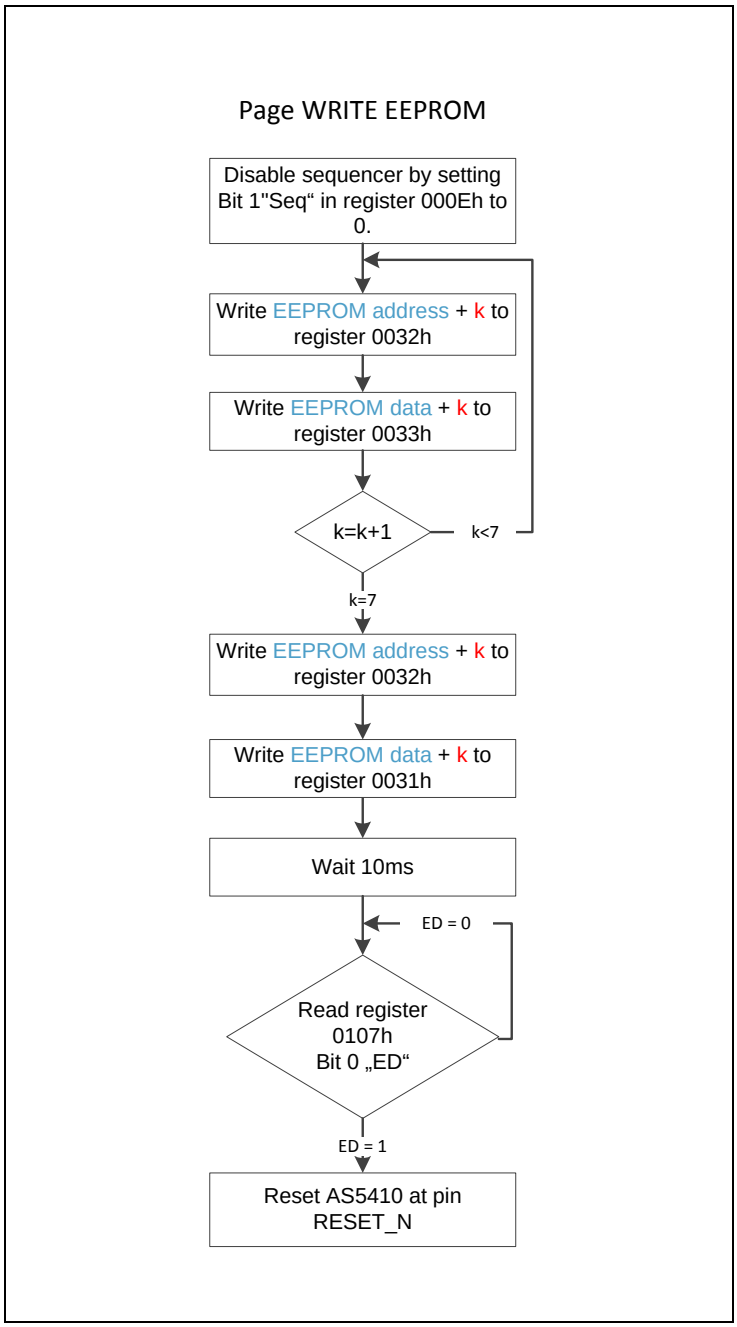


Figure 49:
E²PROM Page Index

PAGE	ADDRESS
0	0000h-0007h
1	0008h-000Fh
2	0010h-0017h
…	…
64	01F8h-01FFh

In order to write E²PROM content faster it is possible to use page WRITE. A page is 8 words of 16bit width tall and can be stored in the E²PROM during one WRITE cycle.

For page writing to the E²PROM the first 7 E²PROM addresses of one page are written to register 0032h and the appropriate E²PROM data can be written to register 0033h. The 8th EEPROM address of the page is written to register 0032h and the appropriate E²PROM data can be written to register 0031h.

(Note: First 7th data parts are stored to the volatile memory. Only a write to register 0031h initiates the load cycle and the data is stored in the E²PROM.)

The write cycle is completed when the ED (E²PROM Done) bit is set to 1.

Magnet Features

Magnet Range Extension

If the magnet is far away from the sensor, the field vectors in the sensor position can generate false angle information. By exploiting the magnetic field behavior it is still possible to calculate correct position information. As absolute field values are used during this calculation external disturbance fields must not exceed a maximum of approximately ten times the terrestrial magnetic field. The position range extending calculation method can be disabled if large disturbance fields occur during operation.

MgRangExt = 0: Angles between -180° and +180° can be measured

MgRangExt = 1: Angles between -288° and +288° can be measured

Figure 50:
Register 000Bh

Register	Access	Bit	Function	Note
000Bh: Sequencer control	R/W	D11	MgRangExt	"**Mag**net **Rang**e **Ext**ension" Enable the algorithm for an extended position range.
		D10	CoordSel	"**Coord**inate System **Sel**ection" 1 = The sign of the LinAng (Register 0122h) gets changed if MagDir (Register 000Bh) = 1 0 = LinAng (Register 0122h) gets not changed

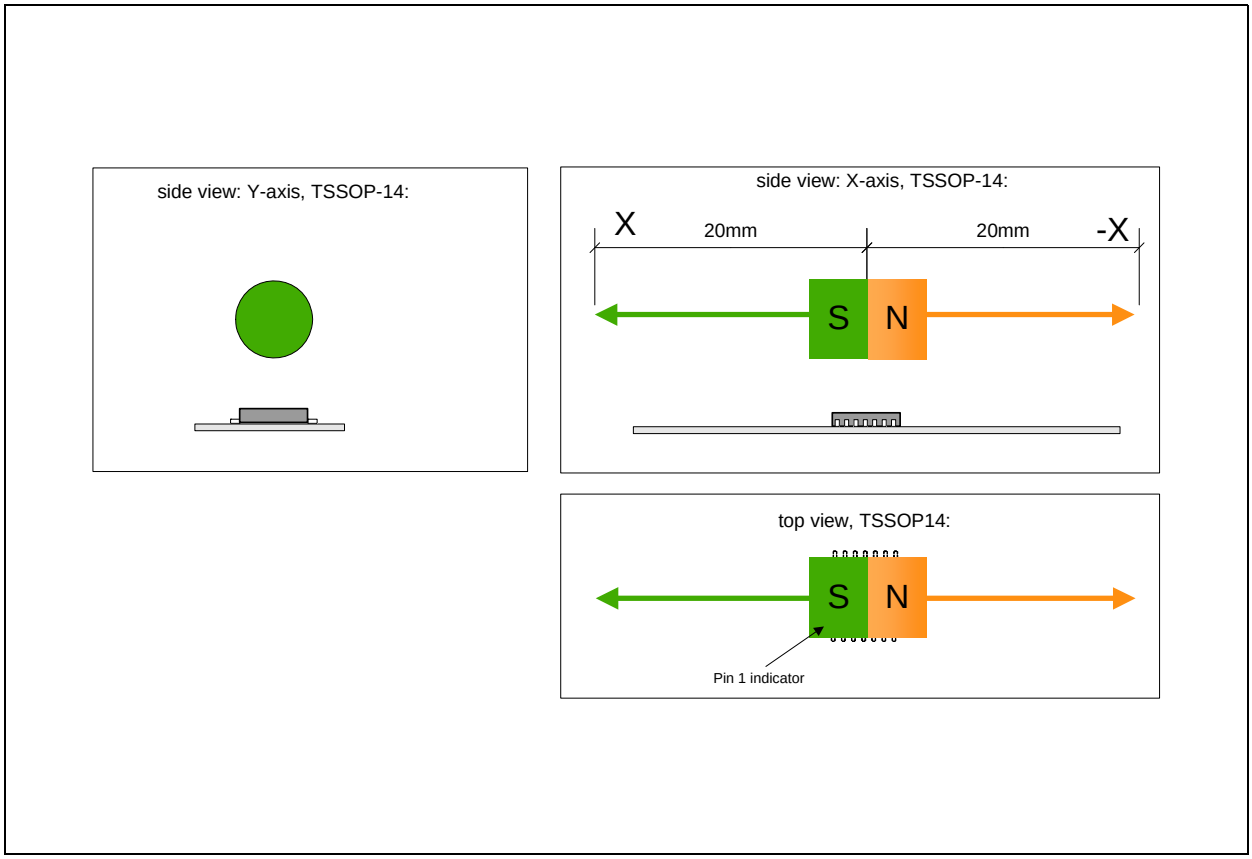
Note(s) and/or Footnote(s):

1. Pins LOCK_N and SCE are test pins for factory testing. They must be connected to VSS in normal operation to prevent accidental enabling of a test mode
2. Output READY is set high when a measurement cycle is completed and the results in the output registers are valid. It is cleared by reading data from address 0100h or 0122h
3. CLK allows monitoring of the internal clock or applying an external clock.
4. Output MISO is only activated when CS_N is low. It is in high impedance state otherwise, this allows parallel operation of multiple ICs.
5. CS_N is active low and activates data transmission. If only a single device is used, CS_N may remain low for several commands, for example while reading the output registers.

Application Information

The AS5410 can be used in linear sensing applications.

Figure 51:
Reference Setup for Absolute Linear Displacement Measurement



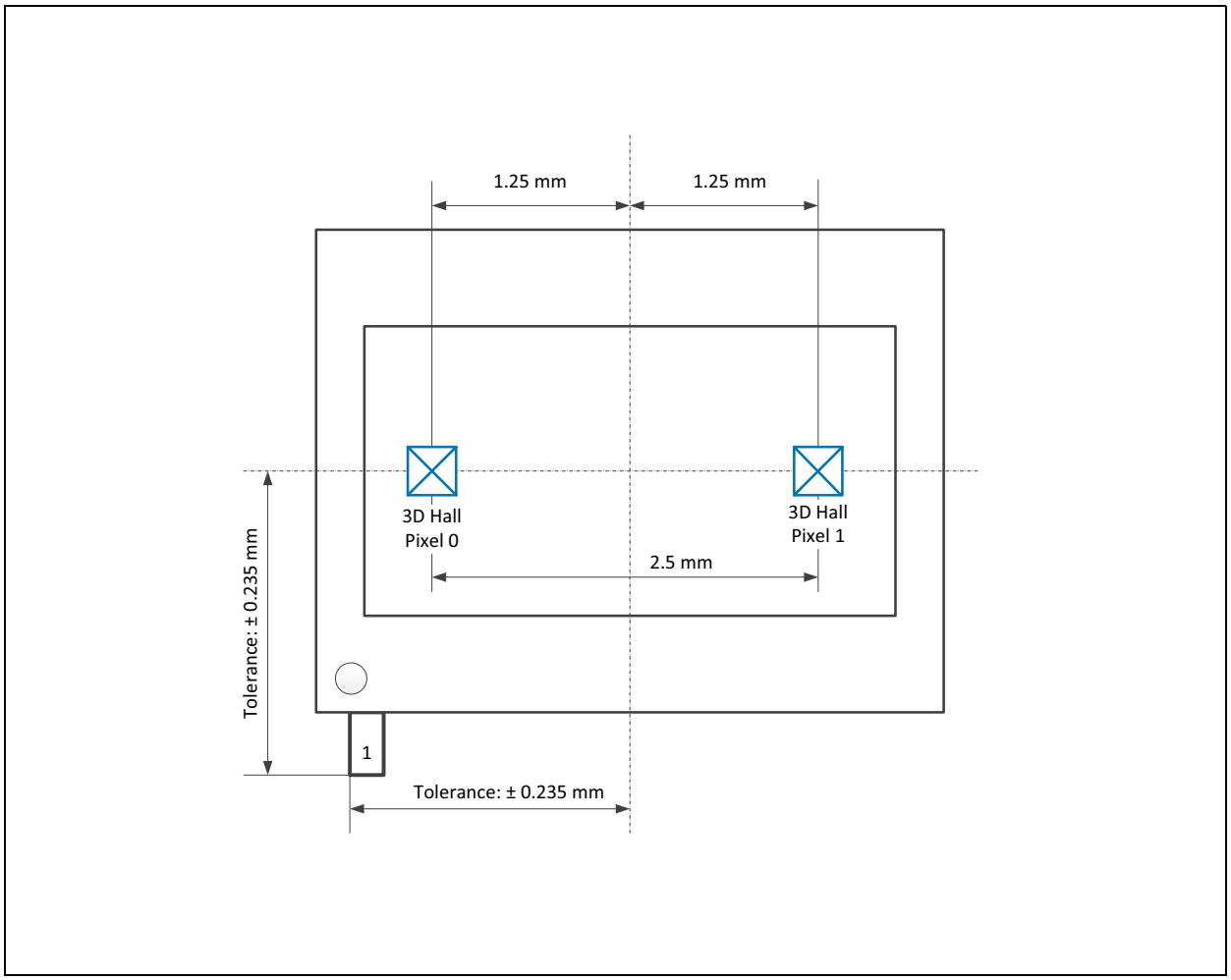
Sensor Placement

Two pixel cells each with an X-/Z-Sensor are arranged in a line on the X Axis parallel to the chip edge, 2.5mm distant from each other. Pixel positions relative to chip centre are:

Pixel 0: -1250 µm

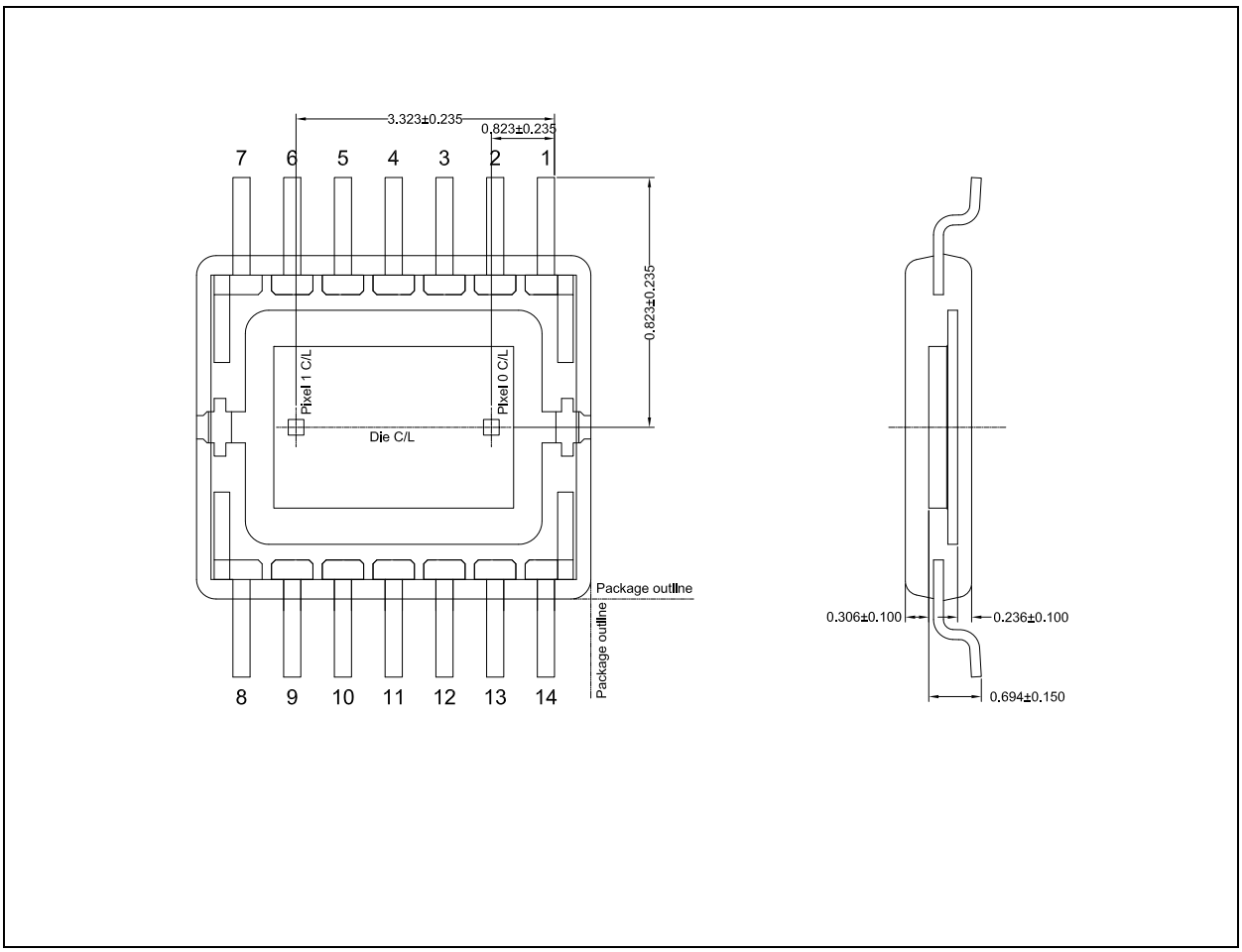
Pixel 1: 1250 µm

Figure 52:
Pixel Cell Arrangement



Package Drawings & Markings

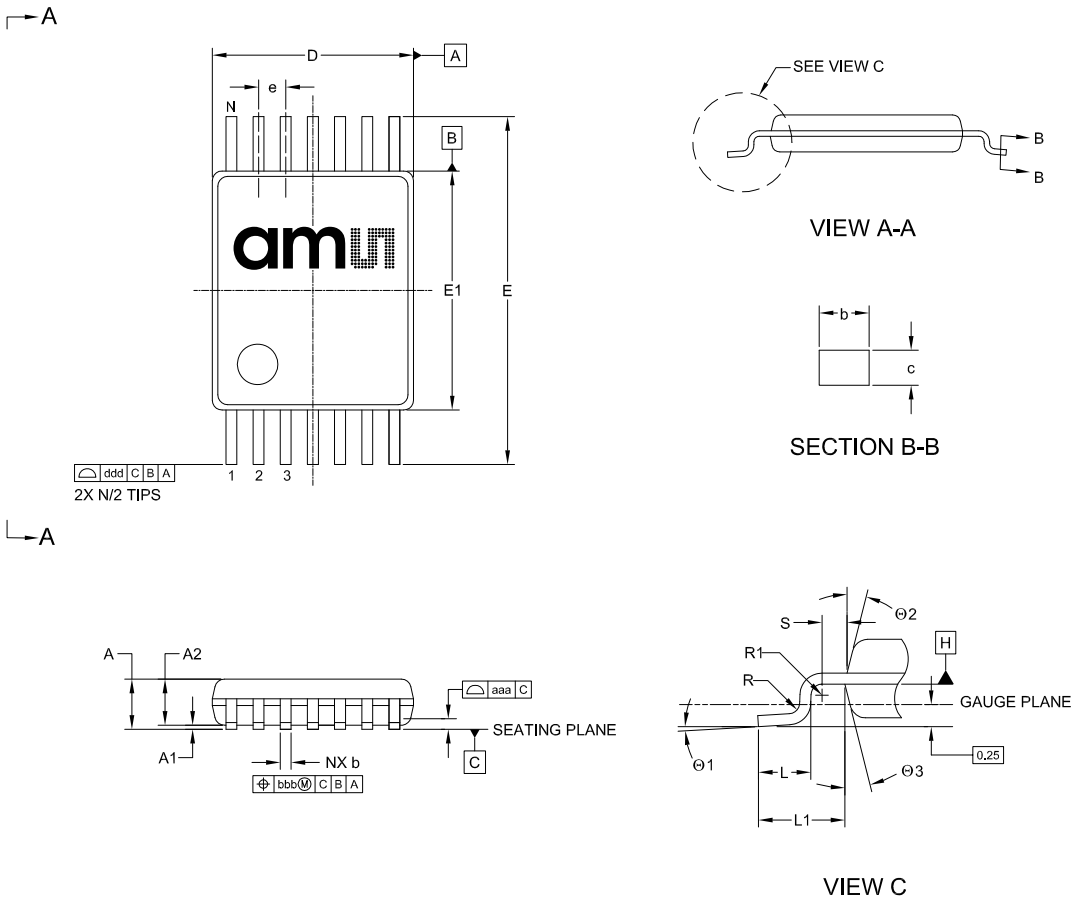
Figure 53:
Pixel Cell Placement



Note(s) and/or Footnote(s):

1. All dimensions in mm.
2. Die thickness 203µm nom.
3. Adhesive thickness 30 ± 15µm.
4. Leadframe downest 152 ± 25µm.
5. Leadframe thickness 125 ± 8µm.

Figure 54:
14-Lead Thin Shrink Small Outline Package TSSOP-14



Symbol	Min	Typ	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	5.00	5.10
E		6.40 BSC	
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	

Symbol	Min	Typ	Max
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
Θ1	0°	-	8°
Θ2		12 REF	
Θ3		12 REF	
aaa	-	0.10	-
bbb	-	0.10	-
ccc	-	0.05	-
ddd	-	0.20	-
N		14	

Note(s) and/or Footnote(s):

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters (angles are in degrees).
3. N is the total number of terminals.

Figure 55:
AS5410 Marking

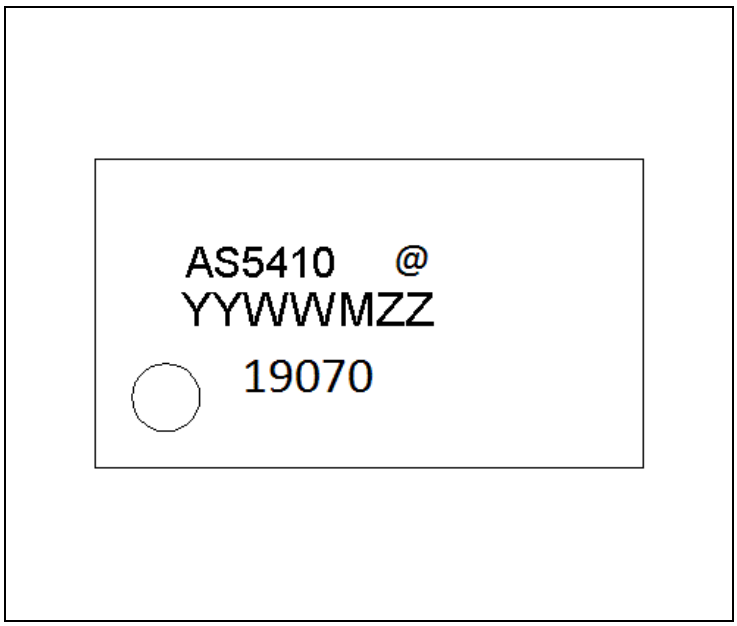


Figure 56:
Packaging Code: YYWWMZZ@

YY	WW	M	ZZ	@
Year	Manufacturing week	Plant identifier	Free choice/traceability code	Sublot identifier

Ordering & Contact Information

The devices are available as standard products, shown in Figure 57.

Figure 57:
Ordering Information

Model	Package	Marking	Delivery Form	Delivery Quantity
AS5410-ZTST	TSSOP-14	AS5410	13" Tape & Reel in dry pack	4500
AS5410-ZTSM	TSSOP-14	AS5410	7" Tape & Reel in dry pack	500

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Document Status

Document Status	Product Status	Definition
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Revision Information

Changes from 2.1 (2015-Aug-15) to current revision 2-04 (2015-Oct-07)	Page
2.1 (2015-Aug-15) to 2-01 (2015-Aug-28)	
Content was updated to the latest **ams** design, altered content structure	
Added figures 53 and 54	49
2-01 (2015-Aug-28) to 2-02 (2015-Sep-18)	
Removed E^2PROM Linearization Table 005Fh to 007Fh	
Updated General Description section	1
Updated Pin Assignment section	5
Updated Electrical Characteristics section	7
Updated Figure 14	13
Updated Figure 17	15
Updated Figure 18	17
Updated Figure 19	17
Updated Figure 32 and added note under it	25
Added Registers 0032h and 0033h	27; 28
Updated Figure 39	32
Updated Figure 40	33
Updated Figure 41	34
Updated Figure 42	35
Added E^2PROM section	39
2-02 (2015-Sep-18) to 2-03 (2015-Sep-30)	
Updated Figure 6	7
2-03 (2015-Sep-30) to 2-04 (2015-Oct-07)	
Updated Figure 15	13
Updated Figure 16	14
Updated Figure 19	17

Note(s) and/or Footnote(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision
2. Correction of typographical errors is not explicitly mentioned.

Content Guide