TPS62801 1.8-V to 5.5-V, 1-A, 2.3-µA I_Q Step Down Converter in a 6-Pin, 0.35-mm Pitch WCSP Package

1 Features

- Input Voltage Range from 1.8 V to 5.5 V
- 2.3-µA Operating Quiescent Current
- Up to 4 MHz Switching Frequency
- Output Current 1 A
- 1% Output Voltage Accuracy
- Selectable Power Save / Forced PWM Mode
- R2D converter for flexible V_{OUT} setting
- 16 Selectable + 1 Fixed Output Voltages
  - TPS62801: 0.8V to 1.55V in 50mV steps
- Smart Enable Pin
- Optimized Pinout to Support 0201 Components
- DCS-Control™ Topology
- Output Discharge
- 100% Duty Cycle Operation
- Tiny 6-pin, 0.35 mm Pitch WCSP package
- Supports < 0.6 mm Solution Height

2 Applications

- Wearable Electronic
- Smart Phones
- IoT Applications
- 2xAA Battery Powered Applications

3 Description

The TPS6280x device family is a step down converter with 2.3-µA typical quiescent current featuring highest efficiency and smallest solution size. TI's DCS-Control™ topology enables the device to operate with tiny inductors and capacitors up to a 4 MHz switching frequency. At light load conditions, it seamlessly enters Power Save Mode to reduce switching cycles and maintaining high efficiency.

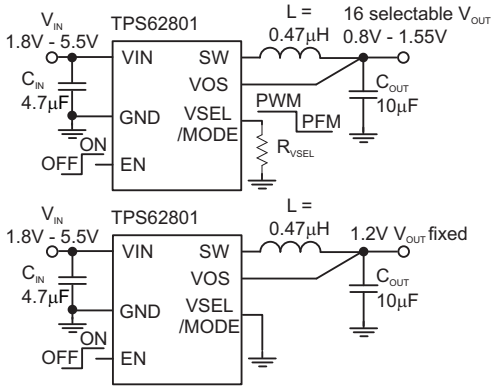
Connecting the VSEL/MODE pin to GND selects a 1.2-V fixed output voltage. With only one external resistor connected to VSEL/MODE pin, 16 internally set output voltages can be selected. An integrated R2D (resistor to digital) converter reads out the external resistor and sets the output voltage. The same device part number can be used for different applications and voltage rails just by changing a single resistor. Furthermore, the internally set output voltage provides better accuracy compared to a traditional external resistor divider network. Once the device has started up, the DC/DC converter enters Forced PWM Mode by applying a high level at the VSEL/MODE pin. In this operating mode, the device runs at typically 4-MHz switch frequency enabling lowest output voltage ripple. The TPS6280x device series comes in a tiny 6-pin WCSP package with 0.35-mm pitch.

Device Information[1]

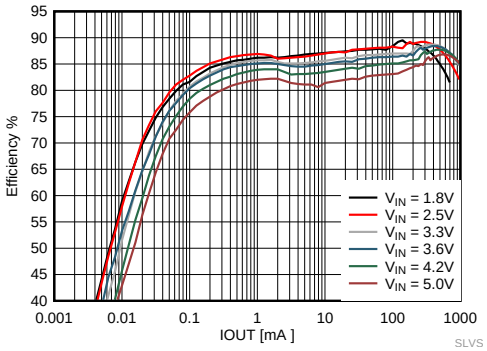
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS6280x	DSBGA (6)	1.05 mm × 0.70 mm x 0.4mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application



Efficiency vs. IOUT @ 1.2 V V_{OUT}



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2017) to Revision A	Page
• Production Data release	1

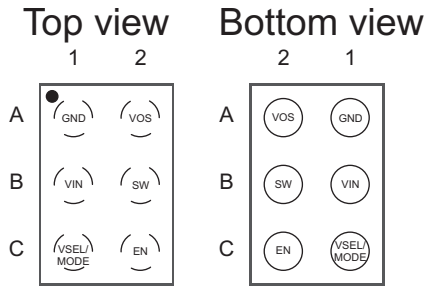
5 Device Comparison Table

Device	Function VSEL/MODE	Fixed VOUT	Selectable Output Voltages with R_{VSEL}	f_{SW} [MHz]	I_{OUT} [A]	Soft Start t_{SS}	Output Discharge
TPS62801	VSEL + MODE	1.20V (VSEL / MODE = GND)	0.8V - 1.55V in 50mV steps	4	1	125 µs	Yes
TPS62802(1)	VSEL + MODE	1.8V (VSEL / MODE = GND)	1.8V - 3.3V in 100mV steps	4	1	400 µs	Yes

(1) Planned device options, in development

6 Pin Configuration and Functions

YKA Package
6-Pin DSBGA



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	A1	PWR	GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor.
VIN	B1	PWR	V_{IN} power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A ceramic capacitor of 4.7 µF is required.
VSEL/MODE	C1	IN	This pin has two functions depending on the device option: Digital input only, or R2D converter + digital input. Connecting a resistor selects a pre defined output voltage. Once the device has started up, the R2D converter is disabled and the pin operates as an input. Applying a high level selects forced PWM mode operation, a low level power save mode operation. For the fixed output voltage options, this pin operates as input only to select between Power Save Mode and Forced PWM mode.
VOS	A2	IN	Output voltage sense pin for the internal feedback divider network and regulation loop. This pin also discharges V_{OUT} when the converter is disabled by an internal MOSFET. Connect this pin directly to the output capacitor with a short trace.
SW	B2	OUT	The switch pin is connected to the internal MOSFET switches. Connect the inductor to this terminal.
EN	C2	IN	High level enables the devices, low level turns the device off. The pin features an internal pulldown resistor, which is disabled once the device has started up.

Table 1. Output Voltage Setting (VSEL/MODE Pin)

Output voltage setting V_{OUT} [V]		R_{VSEL} Resistance [kΩ], E96 Resistor Series, 1% Accuracy, Temperature Coefficient better or equal +/-200ppm/°C
TPS62801	TPS62802 (1)	
1.2	1.8	Connected to GND (no resistor needed)
0.8	1.8	10.0
0.85	1.9	12.1
0.9	2.0	15.4
0.95	2.1	18.7
1.0	2.2	23.7
1.05	2.3	28.7
1.1	2.4	36.5
1.15	2.5	44.2
1.2	2.6	56.2
1.25	2.7	68.1
1.3	2.8	86.6
1.35	2.9	105.0
1.4	3.0	133.0
1.45	3.1	162.0
1.5	3.2	205.0
1.55	3.3	249.0 or larger

(1) Planned device options

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN	–0.3	6	V
	SW (DC)	–0.3	V_{IN} +0.3V	V
	SW (AC), less than 10ns (3)	–2.5	9	V
	EN, VSEL/MODE	–0.3	6	V
	VOS	–0.3	5	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal GND.
(3) while switching

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage V_{IN}	1.8		5.5	V
I_{OUT}	Output current, V_{IN} >/= 2.3V(1)			1	A
	Output current, V_{IN} < 2.3V(1)			0.7	
L	Effective inductance	0.19		0.82	µH
C_{OUT}	Effective output capacitance	3		26	µF
C_{IN}	Effective input capacitance	0.5	4.7		µF
$C_{VSEL/MODE}$	External parasitic capacitance at VSEL/MODE pin			30	pF
R_{VSEL}	Resistance range for external resistor at VSEL/MODE pin (E96 1% resistor values)	10		249	kΩ
	External resistor tolerance E96 series at VSEL/MODE pin			1%	
	E96 resistor series temperature coefficient (TCR)	-200		+200	ppm/°C
T_J	Operating junction temperature range	-40		125	°C

(1) Depending on thermal performance of PCB, maximum output current may be reduced.

7.4 Thermal Information

THERMAL METRIC(1)		TPS6280x YKA (DSBGA) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	147.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	47.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

V_{IN} = 3.6 V, T_J = –40°C to 125°C typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Operating quiescent current (Power Save Mode)	EN = V_{IN}, VSEL/MODE = GND, I_{OUT} = 0µA, V_{OUT} = 1.2 V, device not switching, T_J = -40°C to +85°C		2.3	4	µA
		EN = V_{IN}, VSEL/MODE = GND, I_{OUT} = 0µA, V_{OUT} = 1.2 V, device switching		2.5		µA
	Operating quiescent current (PWM Mode)	EN = V_{IN}, VSEL/MODE = V_{IN} (after power up), device switching, I_{OUT} = 0mA, V_{OUT} = 1.2V		8		mA
I_{SD}	Shutdown current	EN = GND, shutdown current into VIN, VSEL/MODE = GND, T_J = -40°C to +85°C		120	250	nA
V_{TH_UVLO+}	Undervoltage lockout threshold	Rising V_{IN}		1.65	1.8	V
$V_{TH\_UVLO–}$		Falling V_{IN}		1.56	1.7	V
INPUT EN						
$V_{IH\ TH}$	High level input voltage		0.8			V
$V_{IL\ TH}$	Low level input voltage				0.4	V
I_{IN}	Input bias current	T_J = -40°C to +85°C, EN = high		10	25	nA
R_{PD}	Internal pulldown resistance	EN = low		500		kΩ
INPUT VSEL/MODE						
$V_{IH\ TH}$	High level input voltage		0.8			V
$V_{IL\ TH}$	Low level input voltage				0.4	V
I_{IN}	Input bias Current	EN = high, T_J = -40°C to +85°		10	25	nA
POWER SWITCHES						
I_{LKG_SW}	Leakage current into SW pin	V_{SW} = 1.2V, T_J = -40°C to +85°C		10	25	nA
$R_{DS(ON)}$	High side MOSFET on-resistance	I_{OUT} = 500 mA		120	170	mΩ
	Low side MOSFET on-resistance	I_{OUT} = 500 mA		80	115	mΩ
I_{LIMF}	High side MOSFET switch current limit		1.2	1.4	1.6	A
	Low side MOSFET switch current limit		1.1	1.3	1.5	A
OUTPUT VOLTAGE DISCHARGE						
R_{DSCH_VOS}	MOSFET on-resistance	EN = GND, I_{VOS} = –10 mA into VOS pin, T_J = -40°C to +85°C		7	11	Ω
I_{IN_VOS}	Bias current into VOS pin	EN = V_{IN}, V_{OUT} = 1.2 V (internal 12MΩ resistor divider), T_J = -40°C to +85°C		100	400	nA

Electrical Characteristics (continued)

V_{IN} = 3.6 V, T_J = –40°C to 125°C typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL PROTECTION						
T_{SD}	Thermal shutdown temperature	Rising Junction Temperature, PWM mode		160		°C
	Thermal shutdown hysteresis			20		°C
OUTPUT						
V_{OUT}	Output voltage range	TPS62801, 50mV steps	0.8		1.55	V
V_{OUT}	Output voltage range	TPS62802, 100mV steps	1.8		3.3	V
V_{OUT}	Output voltage accuracy	Power Save Mode		0%		
V_{OUT}	Output voltage accuracy	PWM Mode, I_{OUT} = 0 mA, T_J = 25°C to +85°C	-1%	0%	1%	
V_{OUT}	Output voltage accuracy	PWM Mode, I_{OUT} = 0 mA, T_J = -40°C to +125°C	-2%	0%	1.7%	
V_{OUT}	DC output voltage load regulation			0.1		%/A
V_{OUT}	DC output voltage line regulation			0		%/V
t_{ONmin}	Minimum ON time	V_{IN} = 3.6V, V_{OUT} = 1.2V		85		ns
t_{ONmin}	Minimum ON time	V_{IN} = 3.6V, V_{OUT} = 1.8V,	100	120	140	ns
t_{OFFmin}	Minimum OFF time			40		ns
f_{SW}	Switching frequency	V_{IN} = 3.6V, V_{OUT} = 1.2V, PWM operation		4		MHz
$t_{Startup\_delay}$	Regulator start up delay time	From EN = low to high until device starts switching, fixed output voltage options		220	850	µs
$t_{Startup\_delay}$	Regulator start up delay time	From EN = low to high until device starts switching, TPS62801, R_{VSEL} = 249kΩ		500	1100	µs
t_{SS}	Soft start time	TPS62801, from V_{OUT} = 0V to 95% of V_{OUT} nominal,		125	170	µs
t_{SS}	Soft start time	TPS62802, from V_{OUT} = 0V to 95% of V_{OUT} nominal		400	500	µs

7.6 Typical Characteristics

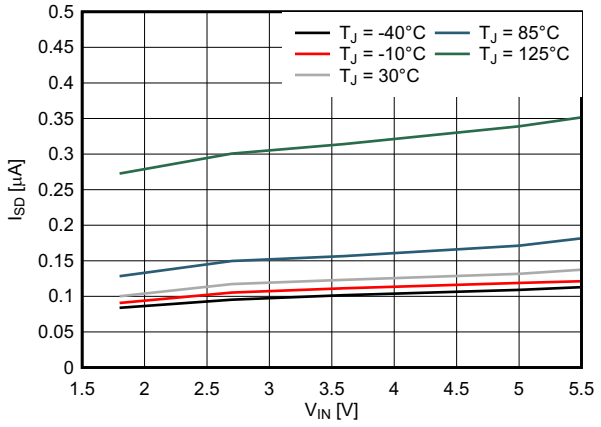


Figure 1. Shutdown Current I_{SD}

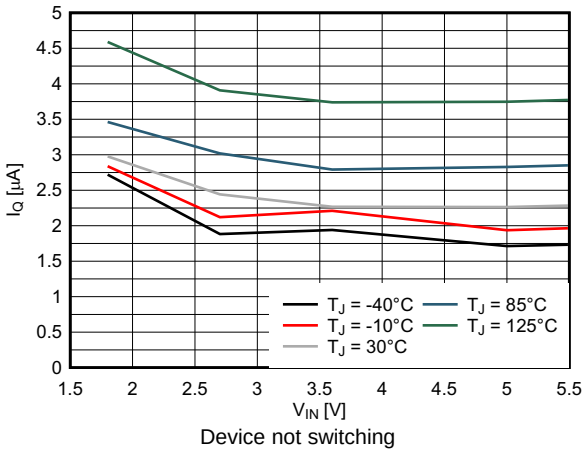


Figure 2. Quiescent Current I_Q

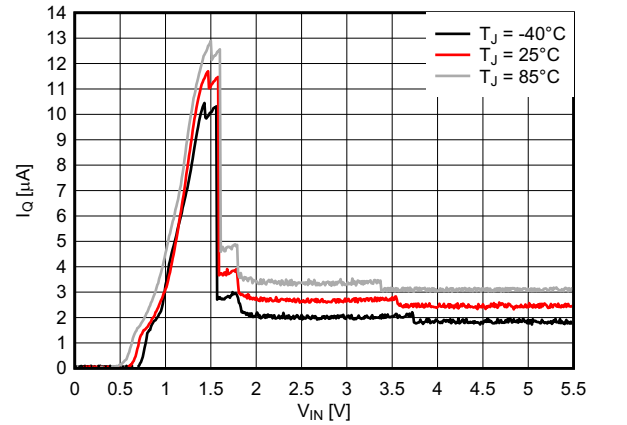


Figure 3. Operating Quiescent Current I_Q

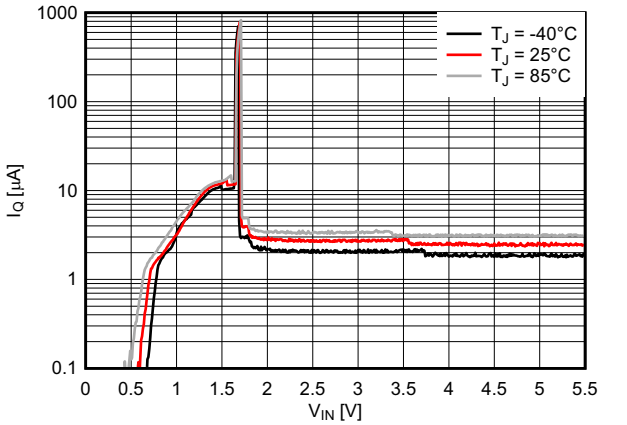


Figure 4. Operating Quiescent Current I_Q

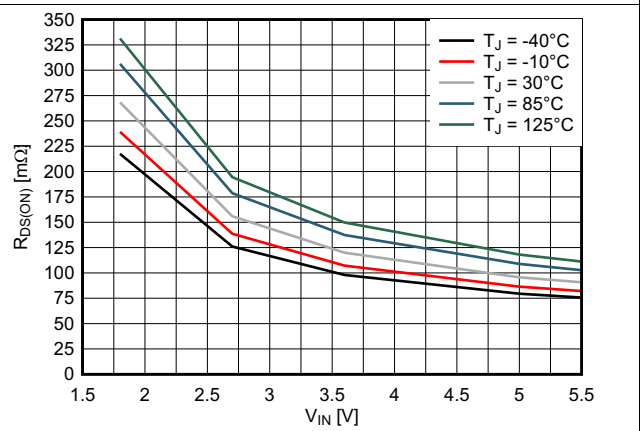


Figure 5. High Side Switch Drain Source Resistance $R_{DS(ON)}$

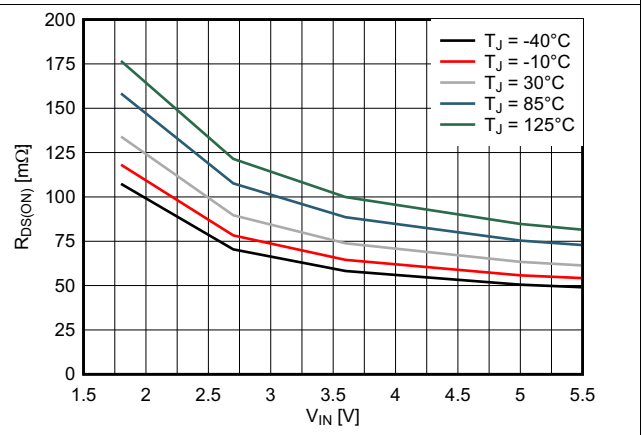


Figure 6. Low Side Switch Drain Source Resistance $R_{DS(ON)}$

Typical Characteristics (continued)

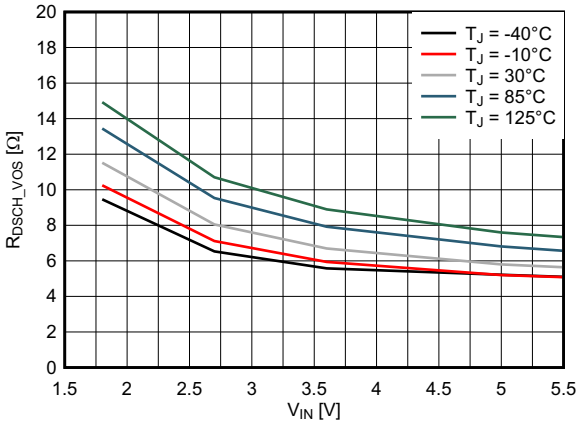


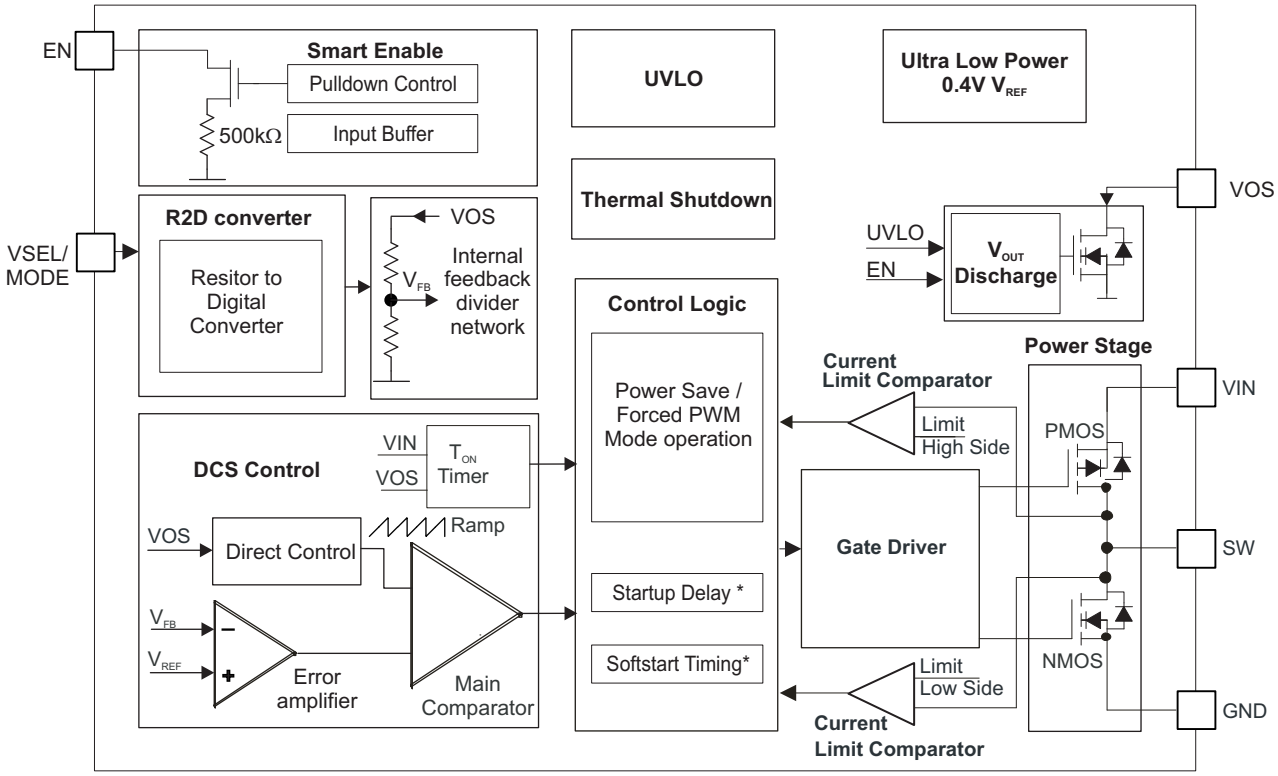
Figure 7. VOS Discharge Switch Drain Source Resistance R_{DSCH_VOS}

8 Detailed Description

8.1 Overview

The TPS6280x is a high frequency synchronous step down converter with ultra low quiescent current consumption. Using TI's DCS-Control™ topology, the device extends the high efficiency operation area down to microamperes of load current during Power Save Mode Operation. TI's DCS-Control™ (Direct Control with Seamless Transition into Power Save Mode) is an advanced regulation topology, which combines the advantages of hysteretic and voltage mode control. Characteristics of DCS-Control™ are excellent AC load regulation and transient response, low output ripple voltage and a seamless transition between PFM and PWM mode operation. DCS-Control™ includes an AC loop which senses the output voltage (VOS pin) and directly feeds the information to a fast comparator stage. This comparator sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. In order to achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Smart Enable and Shutdown (EN)

An internal 500kΩ resistor pulls the EN pin to GND and avoids the pin to be floating. This prevents an uncontrolled start up of the device in case the EN pin cannot be driven to low level safely. With EN low, the device is in shutdown mode. The device is turned on with EN set to a high level. The pulldown control circuit disconnects the pulldown resistor on the EN pin once the internal control logic and the reference have been powered up successfully. With EN set to a low level the device enters shutdown mode and the pulldown resistor is activated again.

Feature Description (continued)

8.3.2 Softstart

Once the device has been enabled with EN high, it initializes and powers up its internal circuits. This occurs during the regulator start up delay time $t_{Startup\_delay}$. Once $t_{Startup\_delay}$ expires, the internal soft start circuitry ramps up the output voltage within the Soft start time t_{SS}.

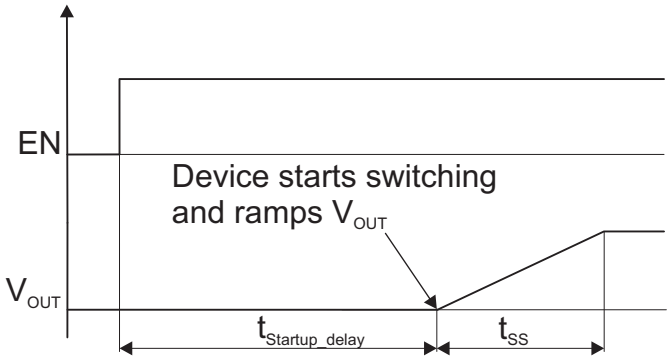


Figure 8. Device Startup

8.3.3 VSEL/MODE Pin

This pin has multiple functions, depending on the device option. See table. In device options with only one fixed output voltage, the R2D function is disabled and the pin just operates as a digital input for Mode selection.

8.3.3.1 Output Voltage Selection (R2D Converter)

The output voltage is set with a single external resistor connected between the VSEL/MODE pin and GND. Once the device has been enabled and the control logic as well the internal reference has been powered up, a R2D (resistor to digital) conversion is started to detect the external resistor R_{VSEL}. An internal current source applies current through the external resistor and an internal ADC reads back the resulting voltage level. Depending on the level, an internal feedback divider network is selected to set the correct output voltage. Once this R2D conversion is finished within the regulator start up delay time $t_{Startup\_delay}$, the current source is turned off to avoid current flow through the external resistor.

After power up, the pin is configured as an input for Mode Selection. Therefore, the output voltage is set only once. If the Mode selection function is used in combination with the VSEL function, ensure that there is no additional current path or capacitance greater than 30pF total to GND, during R2D conversion. Otherwise the additional current to GND is interpreted as a lower resistor value and a false output voltage will be set. Table 1 lists the correct resistor values for R_{VSEL} to set the appropriate output voltages. The R2D converter is designed to operate with resistor values out of the E96 table and requires 1% resistor value accuracy. Ensure that there is no other leakage path than the R_{VSEL} resistor at the VSEL/MODE pin during an undervoltage lockout event. Otherwise a false voltage will be set.

Connecting VSEL/MODE to GND selects a pre-defined output voltage (TPS62801 = 1.2V, TPS62802 = 1.8V). In this case, no external resistor is needed and enables a smaller solution size.

8.3.3.2 Mode Selection: Power Save Mode / Forced PWM Operation

A low level at this pin selects Power Save Mode operation, and a high level selects forced PWM operation. The Mode can be changed during operation after the device has been powered up. In device options with output voltage selection (VSEL) function (TPS62801, TPS62802), the Mode selection function is only available after the R2D converter has read out the external resistor.

Feature Description (continued)

8.3.4 Undervoltage Lockout (UVLO)

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) comparator monitors the supply voltage. The UVLO comparator shuts down the device at an input voltage of 1.7V (max) with falling V_{IN}. The device starts at an input voltage of 1.8V (max) rising V_{IN}. Once the device re-enters operation out of an undervoltage lockout condition, it behaves like being enabled. The internal control logic is powered up and the external resistor at the VSEL/MODE pin is read out.

8.3.5 Switch Current Limit / Short Circuit Protection

The TPS6280x integrates a current limit on the high side, as well on the low side MOSFETs to protect the device against overload or short circuit conditions. The current in the switches is monitored cycle by cycle. If the high side MOSFET current limit I_{LIMF} trips, the high side MOSFET is turned off and the low side MOSFET is turned on to ramp down the inductor current. Once the inductor current through the low side switch decreases below the low side MOSFET current limit I_{LIMF}, the low side MOSFET is turned off and the high side MOSFET turns on again.

8.3.6 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds the thermal shutdown temperature T_{SD} of 160°C (typ), the device enters thermal shutdown. Both the high side and low side power FETs are turned off. When T_J decreases below the hysteresis amount of typically 20°C, the converter resumes normal operation, beginning with a soft start. The thermal shutdown is not active in Power Save Mode.

8.3.7 Output Voltage Discharge

The purpose of the output discharge function is to ensure a defined down-ramp of the output voltage when the device is disabled and to keep the output voltage close to 0 V. The output discharge feature is only active once the device has been enabled at least once since the supply voltage was applied. The output discharge function is not active if the device is disabled and the supply voltage is applied the first time.

The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is disabled. The minimum supply voltage required to keep the discharge function active is $V_{IN} > V_{TH\_UVLO-}$.

8.4 Device Functional Modes

8.4.1 Power Save Mode Operation

The DCS-Control™ topology supports Power Save Mode operation. At light loads the device operates in PFM (Pulse Frequency Modulation) mode that generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shutdown to achieve lowest operating quiescent current. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current. During the sleep periods, the current consumption is reduced to typically 2.3 µA. This low quiescent current consumption is achieved by an ultra low power voltage reference, an integrated high impedance feedback divider network and an optimized Power Save Mode operation.

In PFM Mode, the switching frequency varies linearly with the load current. At medium and high load conditions, the device enters automatically PWM (Pulse Width Modulation) mode and operates in continuous conduction mode with a nominal switch frequency f_{sw} of typically 4MHz. The switching frequency in PWM mode is controlled and depends on V_{IN} and V_{OUT}. The boundary between PWM and PFM mode is when the inductor current becomes discontinuous.

If the load current decreases, the converter seamlessly enters PFM mode to maintain high efficiency down to very light loads. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to PFM Mode is seamless with minimum output voltage ripple.

8.4.2 Forced PWM Mode Operation

After the device has powered up and ramped up V_{OUT}, the VSEL/MODE pin acts as an input. With a high level on VSEL/MODE pin, the device enters forced PWM Mode and operates with a constant switching frequency over the entire load range, even at very light loads. This reduces or eliminates interference with RF and noise sensitive circuits, but lowers efficiency at light loads.

8.4.3 100% Mode Operation

The duty cycle of the buck converter operating in PWM mode is given as $D = V_{OUT}/V_{IN}$. The duty cycle increases as the input voltage comes close to the output voltage. In 100% duty cycle mode, it keeps the high side switch on continuously. The high side switch stays turned on as long as the output voltage is below the internal set point. This allows the conversion of small input to output voltage differences.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

9.2 Typical Application

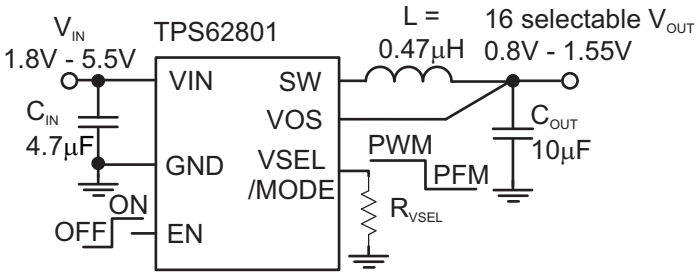


Figure 9. TPS62801 Adjustable V_{OUT} Application Circuit

Additional circuits are shown in the *System Examples* section.

9.2.1 Design Requirements

Table 2 shows the list of components for the application circuit and the characteristic application curves

Table 2. Components for Application Characteristic Curves

Reference	Description	Value	Size [L x W X T]	Manufacturer(1)
TPS6280x	Step down converter		1.05mm x 0.70mm x 0.4mm max.	Texas Instruments
C_{IN}	Ceramic capacitor, GRM155R60J475ME47D	4.7 µF	0402 (1mm x 0.5mm x 0.6mm max.)	Murata
C_{OUT}	Ceramic capacitor, GRM155R60J106ME15D	10 µF	0402 (1mm x 0.5mm x 0.65mm max.)	Murata
L	Inductor DFE18SANR47MG0L	0.47 µH	0603 (1.6mm x 0.8mm x 1.0mm max.)	Murata

(1) See *Third-party Products Disclaimer*

9.2.2 Detailed Design Procedure

The inductor and output capacitor together provide a low-pass filter. To simplify this process, Table 3 outlines possible inductor and capacitor value combinations.

Table 3. Recommended LC Output Filter Combinations

Inductor Value [µH](1)	Output Capacitor Value [µF](2)		
	4.7µF	10µF	22µF
0.47	√	√(3)	√

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and -20%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance varies by +20% and –50%.
(3) Typical application configuration. Other check marks indicate alternative filter combinations.

9.2.2.1 Inductor Selection

The inductor value affects the peak-to-peak ripple current, the PWM-to-PFM transition point, the output voltage ripple and the efficiency. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_{IN} or V_{OUT} and can be estimated according to Equation 1.

Equation 2 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current, as calculated with Equation 2. This is recommended because during a heavy load transient the inductor current rises above the calculated value. A more conservative way is to select the inductor saturation current according to the high side MOSFET switch current limit, I_{LIMF}.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (1)$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (2)$$

where

- f = Switching Frequency
- L = Inductor Value
- ΔI_L = Peak to Peak inductor ripple current
- I_{Lmax} = Maximum Inductor current

The table below shows a list of possible inductors.

Table 4. List of Possible Inductors(1)

INDUCTANCE [µH]	INDUCTOR TYPE	SIZE IMPERIAL (METRIC)	DIMENSIONS L x W X T	SUPPLIER(1)
0.47	DFE18SAN_G0	0603 (1608)	1.6mm x 0.8mm x 1.0mm max	Murata
0.47	HTEB16080F	0603 (1608)	1.6mm x 0.8mm x 0.6mm max.	Cyntec
0.47	HTET1005FE	0402 (1005)	1.0mm x 0.5mm x 0.65mm max.	Cyntec
0.47	TFM160808ALC	0603 (1608)	1.6mm x 0.8mm x 0.8mm max.	TDK

(1) See *Third-party Products Disclaimer*

9.2.2.2 Output Capacitor Selection

The DCS-Control™ scheme of the TPS6280x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. A larger output capacitors can be used reducing the output voltage ripple.

9.2.2.3 Input Capacitor Selection

Because the buck converter has a pulsating input current, a low ESR input capacitor is required for best input voltage filtering to minimize input voltage spikes. For most applications a 4.7-µF input capacitor is sufficient. When operating from a high impedance source, a larger input buffer capacitor is recommended avoiding voltage drops during start-up and load transients. The input capacitor can be increased without any limit for better input voltage filtering. Table 5 shows a selection of input and output capacitors.

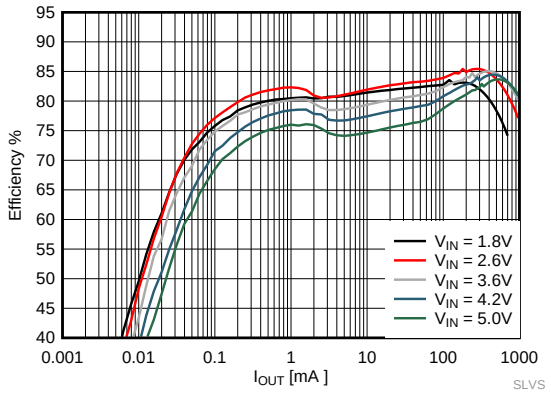
Table 5. List of Possible Capacitors(1)

CAPACITANCE [µF]	CAPACITOR TYPE	SIZE IMPERIAL (METRIC)	DIMENSIONS L x W X T	SUPPLIER(1)
4.7	GRM155R60J475ME47D	0402 (1005)	1.0mm x 0.5mm x 0.6mm max.	Murata
4.7	GRM035R60J475ME15	0201(0603)	0.6mm x 0.3mm x 0.55mm max	Murata
10	GRM155R60J106ME15D	0402 (1005)	1.0mm x 0.5mm x 0.65mm max.	Murata

(1) See *Third-party Products Disclaimer*

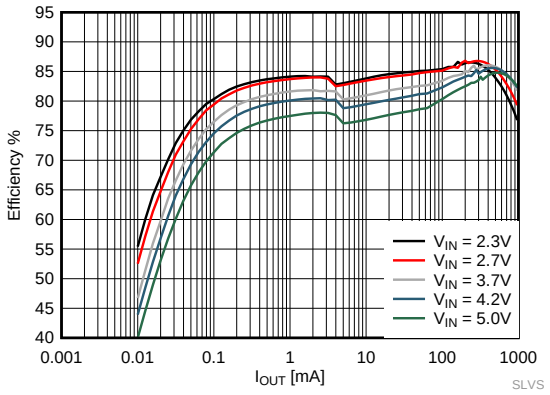
9.2.3 Application Curves

The conditions for below application curves are V_{IN} = 3.6 V, V_{OUT}= 1.2 V and the components listed in Table 2, unless otherwise noted.



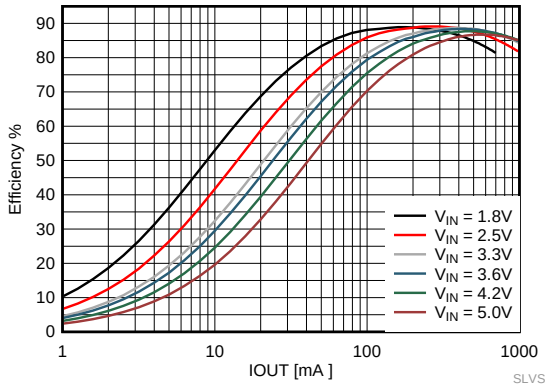
TPS62801 R_{VSEL} = 10 kΩ to GND

Figure 10. Efficiency Power Save Mode V_{OUT} = 0.8 V



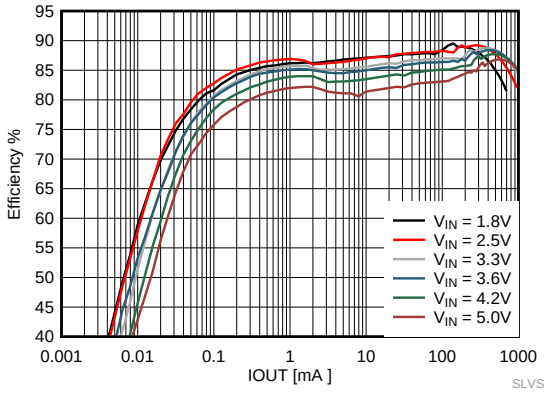
TPS62801 R_{VSEL} = 15.4 kΩ to GND

Figure 11. Efficiency Power Save Mode V_{OUT} = 0.9 V



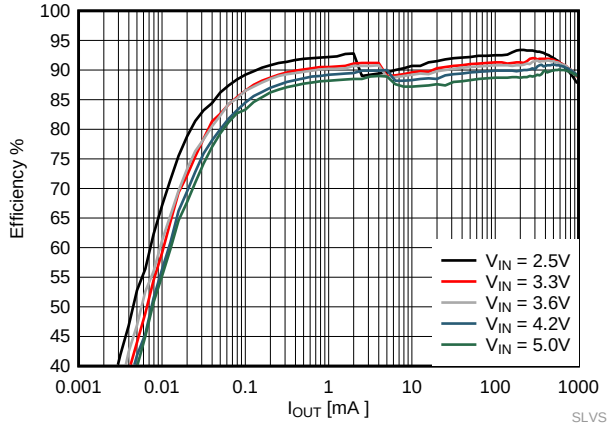
TPS62801 R_{VSEL} = 56.2 kΩ, VSEL/MODE pin = high after startup

Figure 12. Efficiency Forced PWM Mode V_{OUT} = 1.2 V



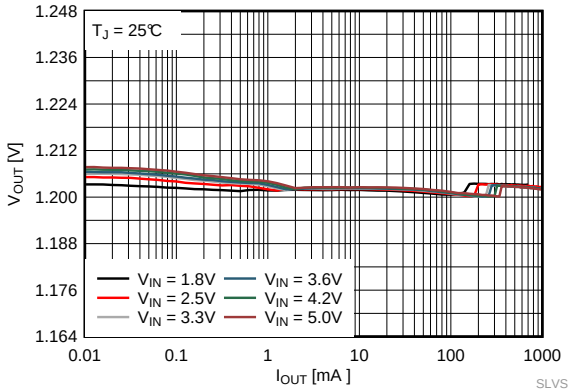
TPS62801 VSEL/MODE = GND

Figure 13. Efficiency Power Save Mode V_{OUT} = 1.2 V



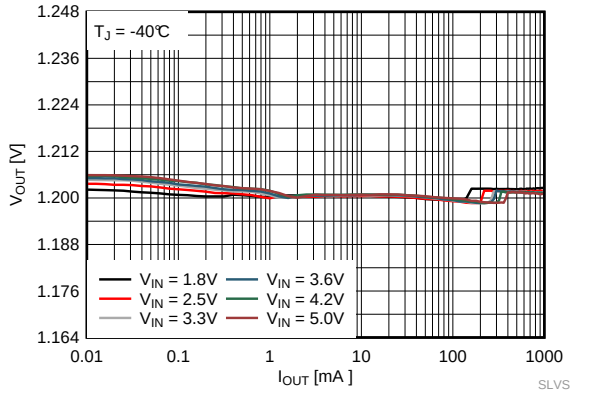
TPS62802 VSEL/MODE = GND

Figure 14. Efficiency Power Save Mode V_{OUT} = 1.8 V



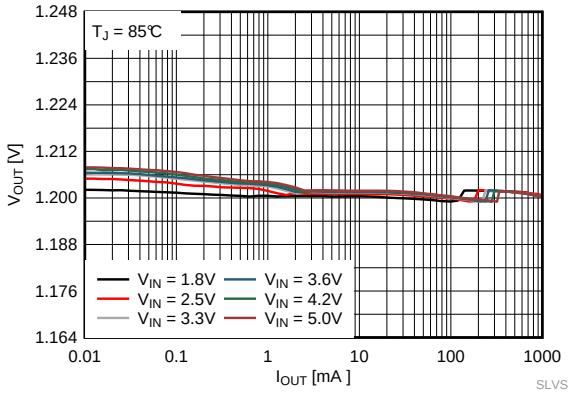
TPS62801 VSEL/MODE = GND
V_{OUT} = 1.2 V PFM/PWM Mode T_J = 25°C

Figure 15. Output Voltage vs. Output Current



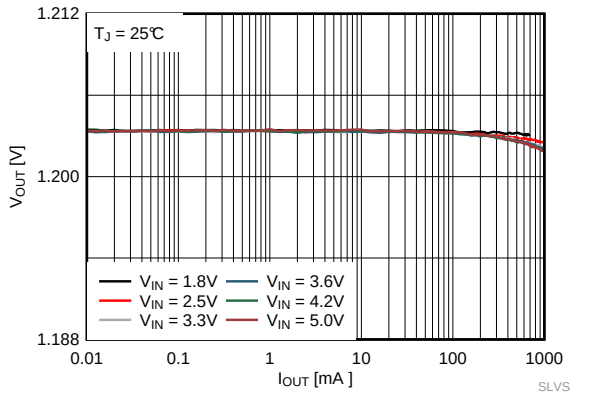
TPS62801 VSEL/MODE = GND
V_{OUT} = 1.2 V PFM/PWM Mode T_J = –40°C

Figure 16. Output Voltage vs. Output Current



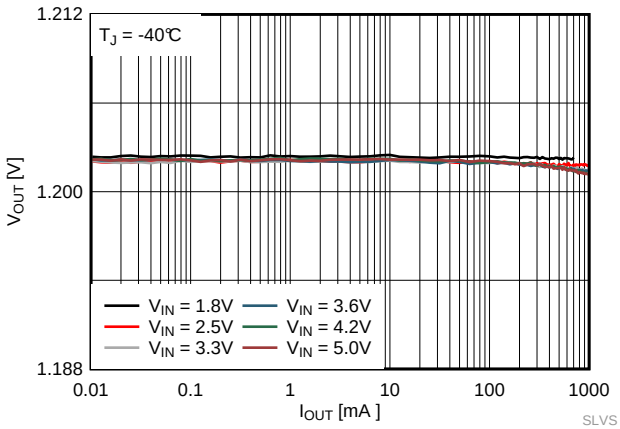
TPS62801 VSEL/MODE = GND
V_{OUT} = 1.2 V PFM/PWM Mode T_J = 85°C

Figure 17. Output Voltage vs. Output Current



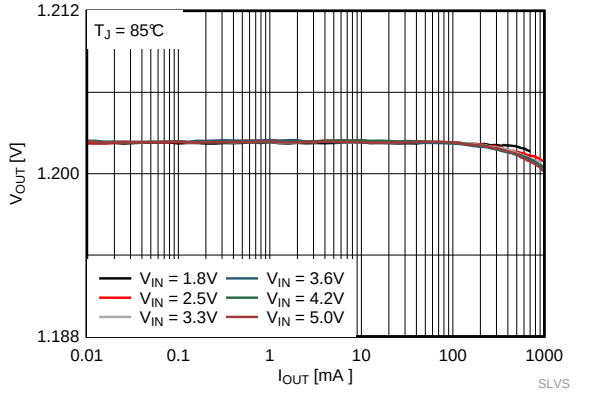
TPS62801 VSEL/MODE = high after startup
V_{OUT} = 1.2 V Forced PWM Mode T_J = 25°C

Figure 18. Output Voltage vs. Output Current



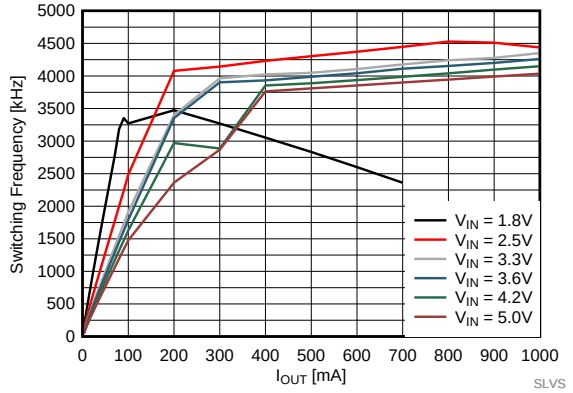
TPS62801 VSEL/MODE = high after startup
V_{OUT} = 1.2 V Forced PWM Mode T_J = –40°C

Figure 19. Output Voltage vs. Output Current



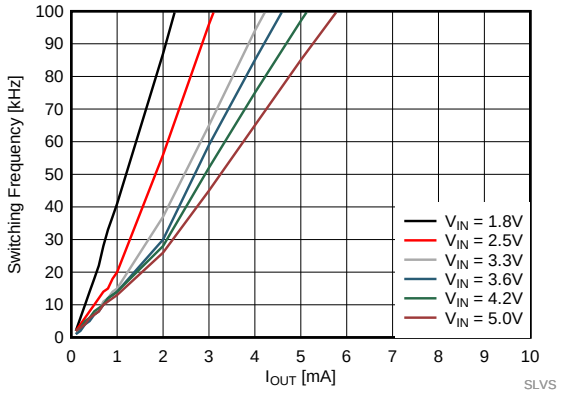
TPS62801 VSEL/MODE = high after startup
V_{OUT} = 1.2 V Forced PWM Mode T_J = 85°C

Figure 20. Output Voltage vs. Output Current



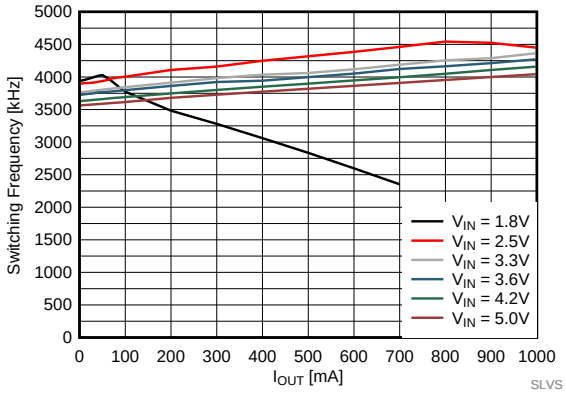
TPS62801 VSEL/MODE = GND
V_{OUT} = 1.2 V PFM/PWM Mode T_J = 25°C

Figure 21. Switching Frequency vs. Output Current



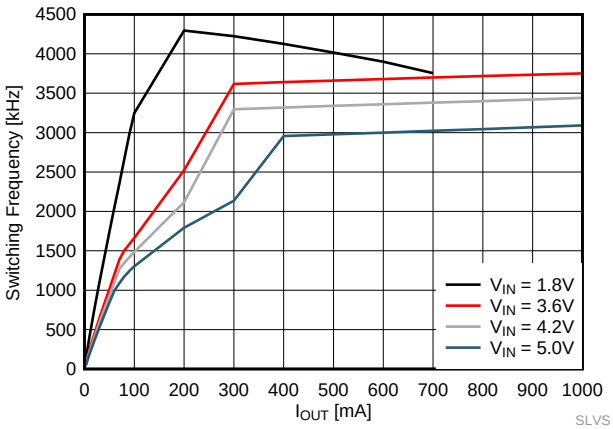
TPS62801 VSEL/MODE = GND
V_{OUT} = 1.2 V PFM/PWM Mode T_J = 25°C

Figure 22. Switching Frequency (zoom in)



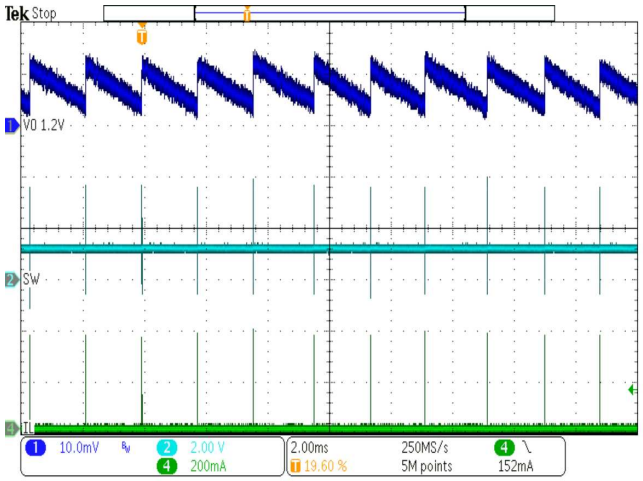
TPS62801 VSEL/MODE = high after startup
V_{OUT} = 1.2 V Forced PWM Mode T_J = 25°C

Figure 23. Switching Frequency vs. Output Current



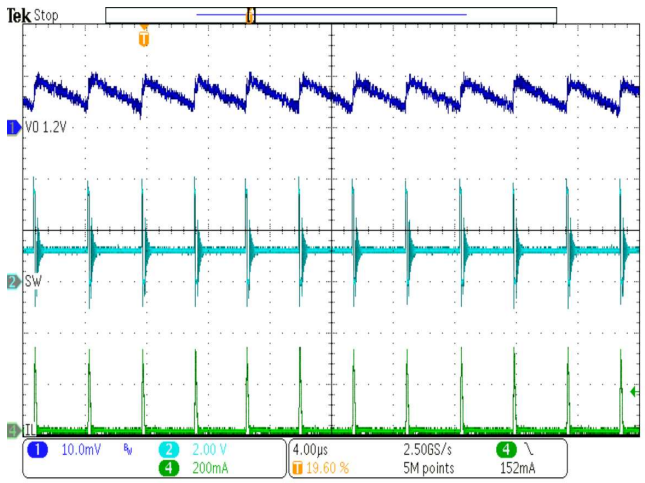
TPS62801 VSEL/MODE = 10 kΩ to GND
V_{OUT} = 0.8 V PFM/PWM Mode T_J = 25°C

Figure 24. Switching Frequency vs. Output Current



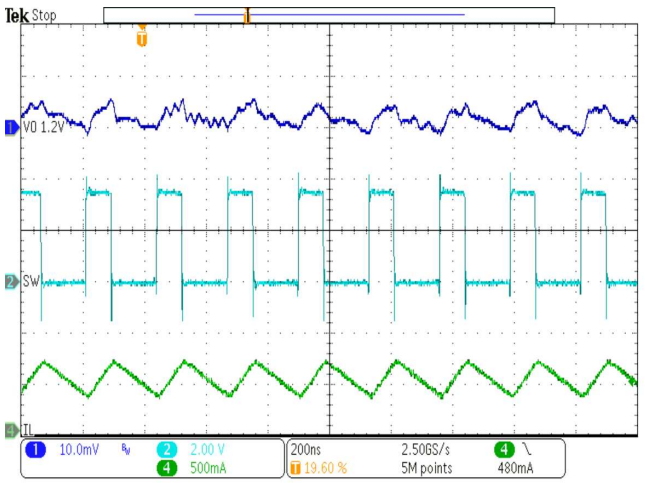
TPS62801 V_{OUT} = 1.2 V VSEL/MODE = GND
I_{OUT} = 25 µA PFM Mode

Figure 25. Typical Operation Power Save Mode



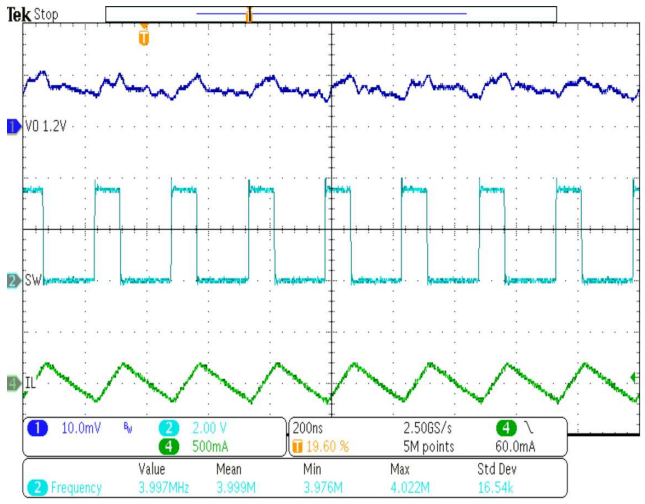
TPS62801 V_{OUT} = 1.2 V VSEL/MODE = GND
I_{OUT} = 10 mA PFM Mode

Figure 26. Typical Operation Power Save Mode



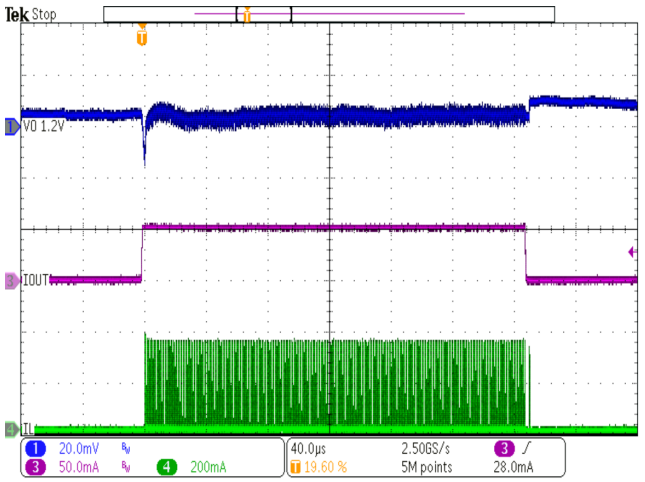
TPS62801 V_{OUT} = 1.2 V VSEL/MODE = GND
I_{OUT} = 500 mA PWM Mode

Figure 27. Typical Operation PWM Mode



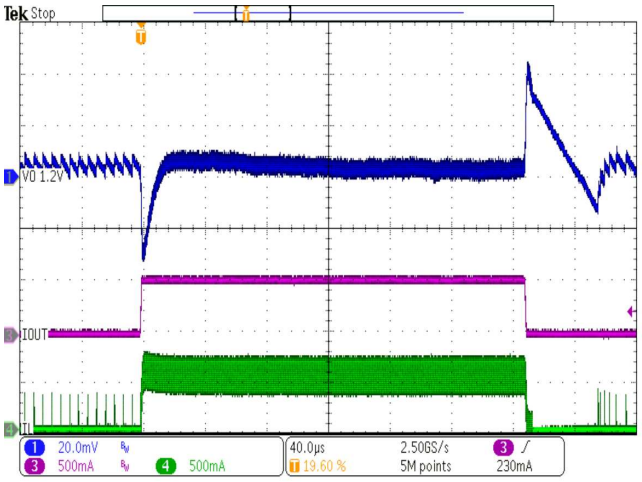
TPS62801 V_{OUT} = 1.2 V I_{OUT} = 0 mA
Forced PWM Mode VSEL/MODE = VIN (after startup)

Figure 28. Typical Operation Forced PWM Mode



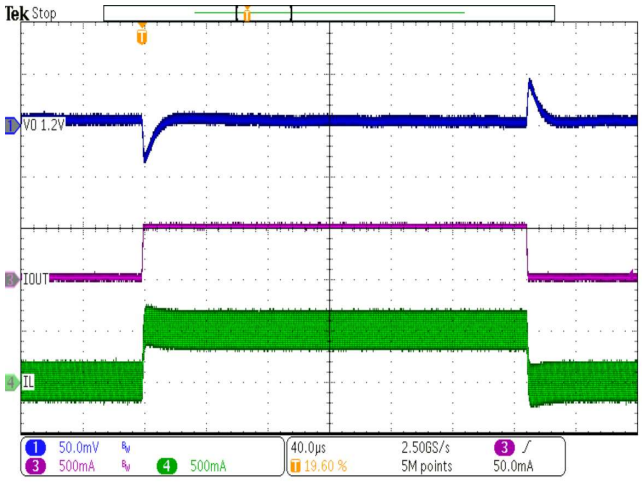
TPS62801 V_{OUT} = 1.2 V VSEL/MODE = GND
rise / fall time < 1 µs I_{OUT} = 0 mA to 50 mA, PFM Mode

Figure 29. Load Transient Power Save Mode



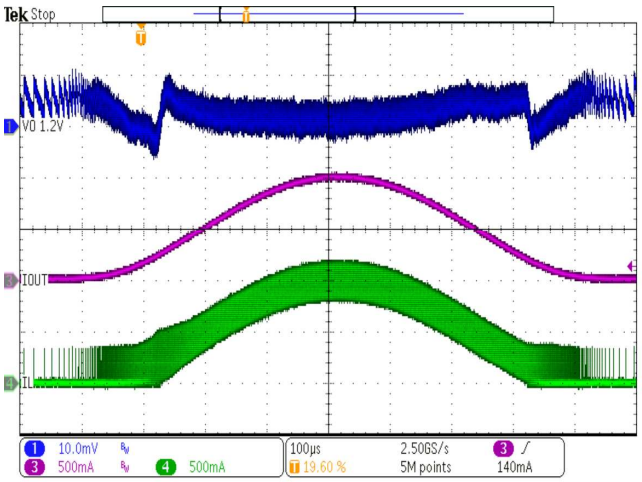
TPS62801 V_{OUT} = 1.2 V VSEL/MODE = GND
rise / fall time < 1 µs PFM / PWM Mode
I_{OUT} = 5 mA to 500 mA

Figure 30. Load Transient Power Save Mode



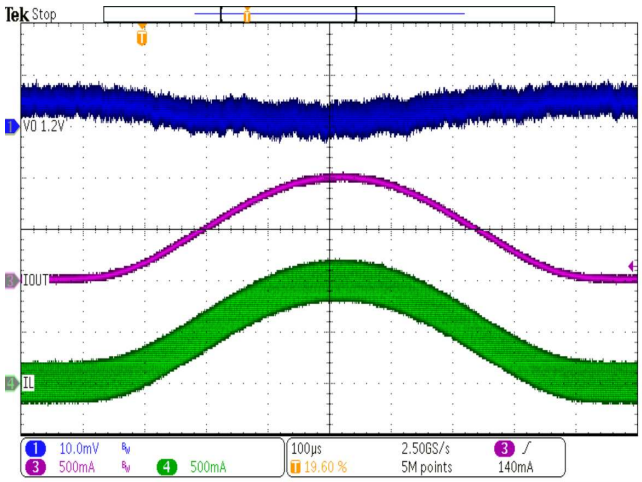
TPS62801 V_{OUT} = 1.2 V VSEL/MODE = VIN
rise / fall time < 1 µs (after startup)
Forced PWM Mode
I_{OUT} = 5 mA to 500 mA

Figure 31. Load Transient Forced PWM Mode



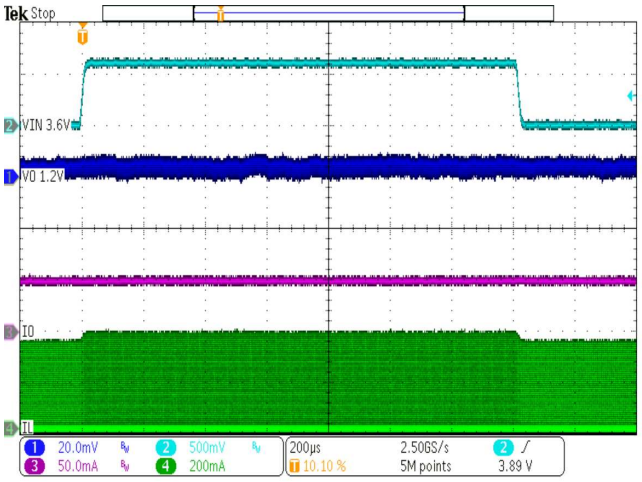
TPS62801 V_{OUT} = 1.2 V VSEL/MODE = GND
I_{OUT} = 1 mA to 1 A 1 kHz PFM/PWM Mode

Figure 32. AC Load Sweep Power Save Mode



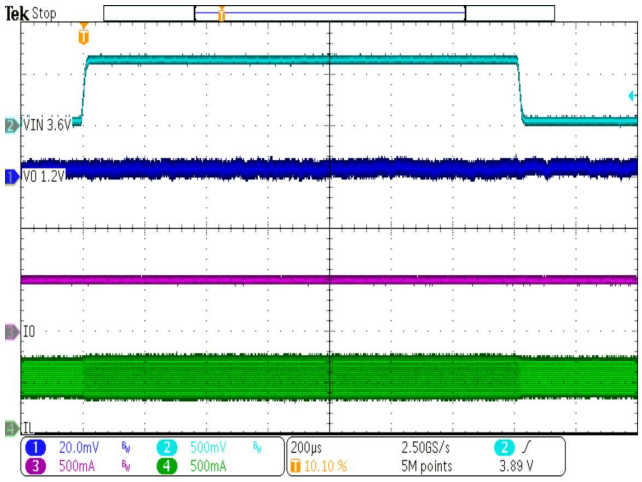
TPS62801 V_{OUT} = 1.2 V VSEL/MODE = VIN
I_{OUT} = 1 mA to 1 A, 1 kHz (after start up)
Forced PWM Mode

Figure 33. AC Load Sweep Forced PWM Mode



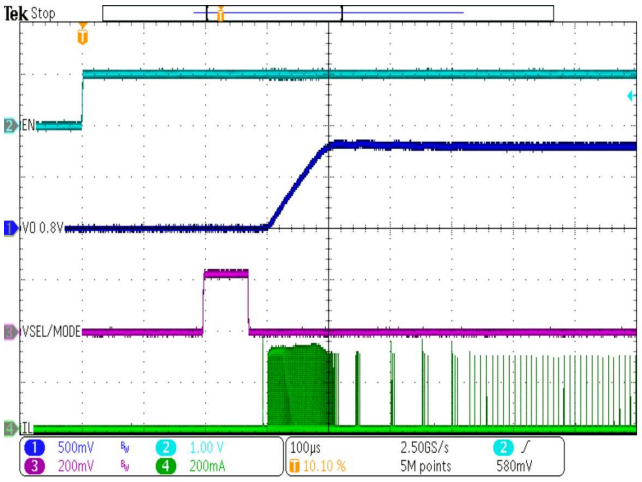
TPS62801 V_{OUT} = 1.2 V V_{IN} = 3.6 V to 4.2 V
rise / fall time = 10 µs I_{OUT} = 50 mA

Figure 34. Line Transient PFM Mode



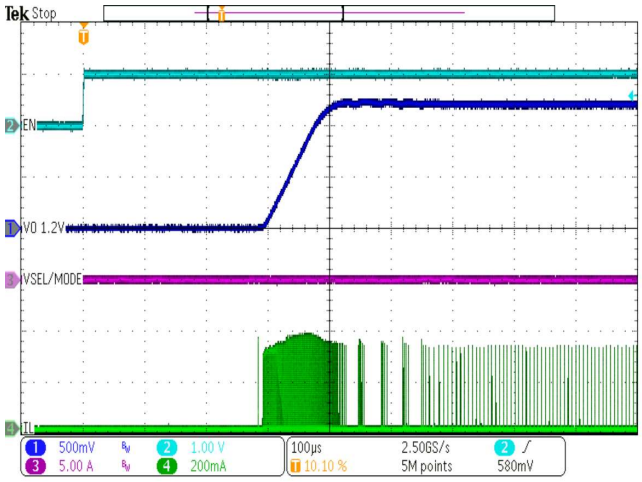
TPS62801 V_{OUT} = 1.2 V V_{IN} = 3.6 V to 4.2 V
rise / fall time = 10 µs I_{OUT} = 500 mA

Figure 35. Line Transient PWM Mode



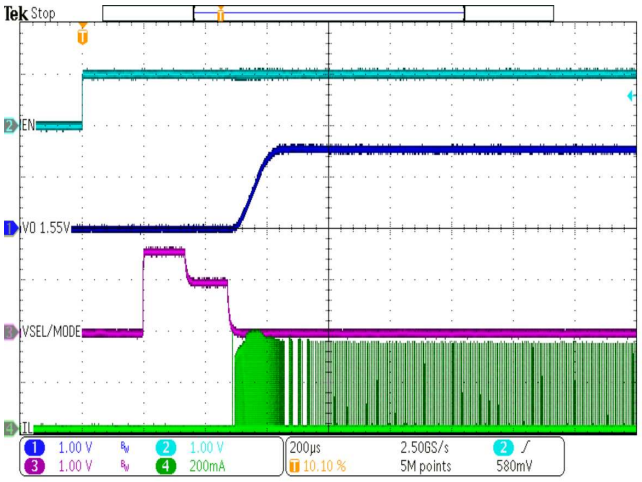
TPS62801 V_{OUT} = 0.8 V VSEL/MODE = Low
R_{VSEL} = 10 kΩ (via R_{VSEL})
R_{Load} = 220 Ω

Figure 36. Start up V_{OUT} = 0.8 V



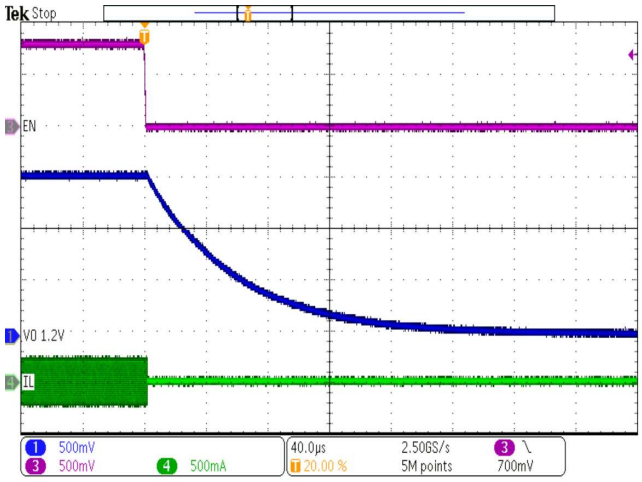
TPS62801 V_{OUT} = 1.2 V VSEL/MODE = GND
R_{Load} = 220 Ω

Figure 37. Start up V_{OUT} = 1.2 V



TPS62801 V_{OUT} = 1.55 V
R_{VSEL} = 249 kΩ
VSEL/MODE = Low
(via R_{VSEL})
R_{Load} = 220 Ω

Figure 38. Start up V_{OUT} = 1.55 V



TPS62801 V_{OUT} = 1.2 V
EN = high to low
VSEL/MODE = V_{IN}
No Load

Figure 39. Output Discharge

9.3 System Examples

This section shows additional circuits for various output voltages.

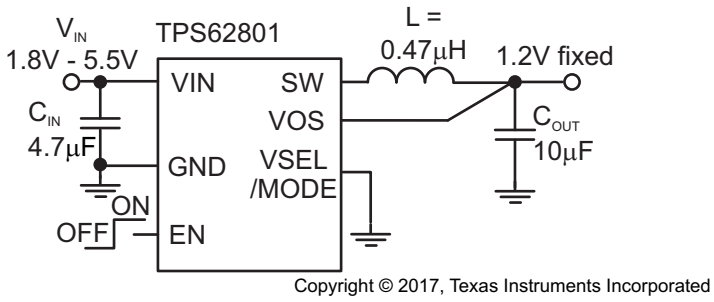


Figure 40. TPS62801 VSEL Connected to GND for 1.2V Fixed V_{OUT}

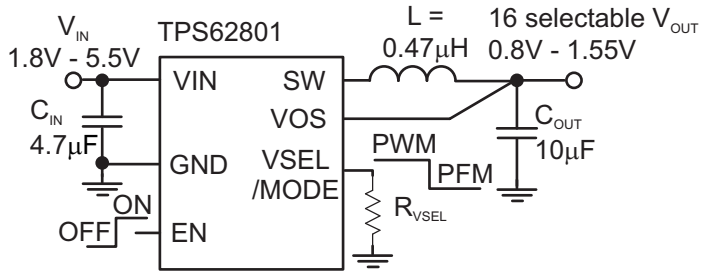


Figure 41. TPS62801 Adjustable V_{OUT} Application Circuit

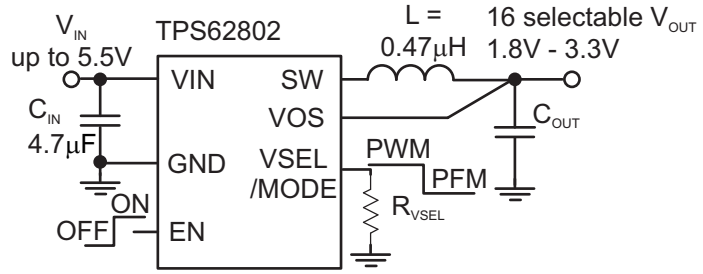


Figure 42. TPS62802 Adjustable V_{OUT} Application Circuit

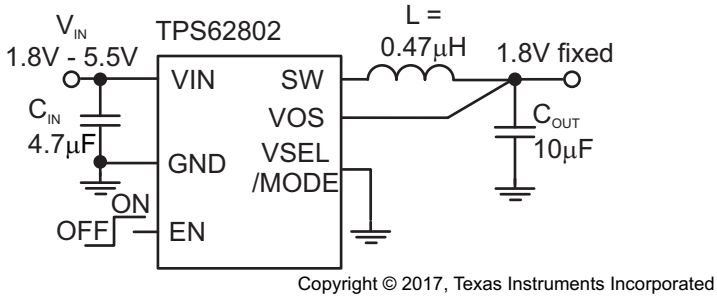


Figure 43. TPS62802 VSEL Connected to GND for 1.8V Fixed V_{OUT}

10 Power Supply Recommendations

The power supply must provide a current rating according to the supply voltage, output voltage and output current of the TPS6280x.

11 Layout

11.1 Layout Guidelines

- As for all switching power supplies, the layout is an important step in the design. Care must be taken in board layout to get the specified performance.
- It is critical to provide a low inductance, low impedance ground path. Therefore, use wide and short traces for the main current paths.
- The input capacitor should be placed as close as possible to the IC's VIN and GND pins. This is the most critical component placement.
- The VOS line is a sensitive, high impedance line and should be connected to the output capacitor and routed away from noisy components and traces (e.g. SW line) or other noise sources.

11.2 Layout Example

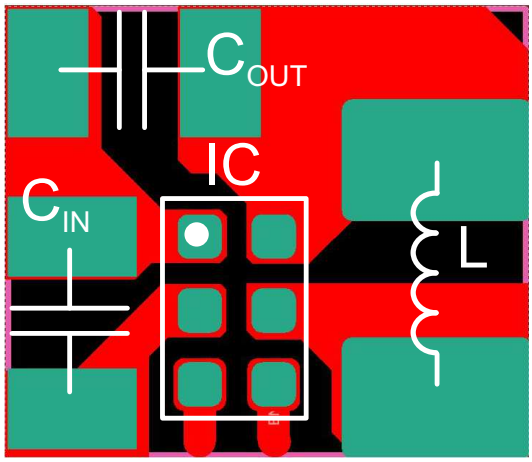


Figure 44. PCB Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

DCS-Control, E2E are trademarks of Texas Instruments.
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12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Chip Scale Package Dimensions

The TPS62801 device is available in a 6-bump chip scale package (DSBGA). See the attached package drawing. The YKA package D and E dimensions are given as:

D	E
1054 µm ±30 µm	704 µm ±30 µm

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62801YKAR	ACTIVE	DSBGA	YKA	6	3000	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 125	+	Samples
TPS62801YKAT	ACTIVE	DSBGA	YKA	6	250	Green (RoHS & no Sb/Br)	SAC396	Level-1-260C-UNLIM	-40 to 125	+	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

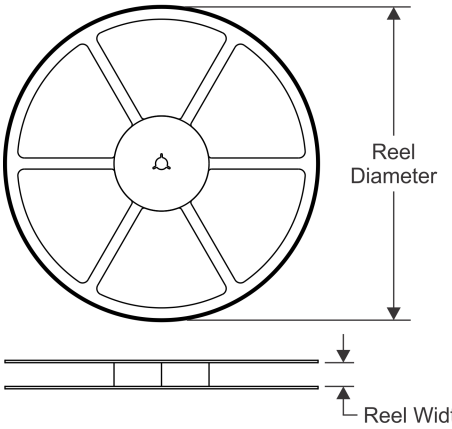
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

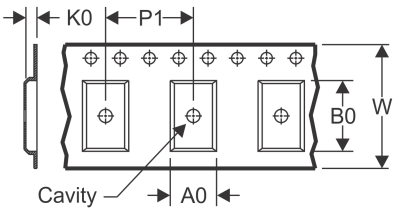
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

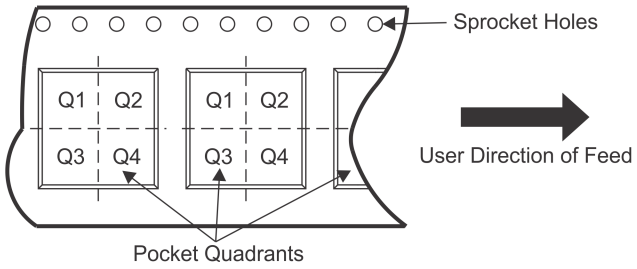


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

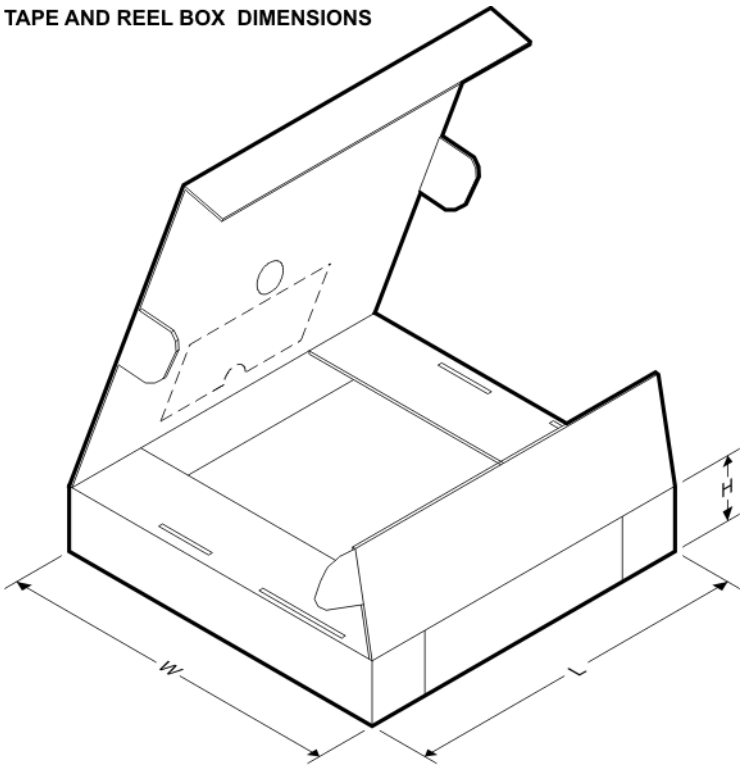
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62801YKAR	DSBGA	YKA	6	3000	178.0	8.4	0.81	1.16	0.46	4.0	8.0	Q1
TPS62801YKAT	DSBGA	YKA	6	250	178.0	8.4	0.81	1.16	0.46	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

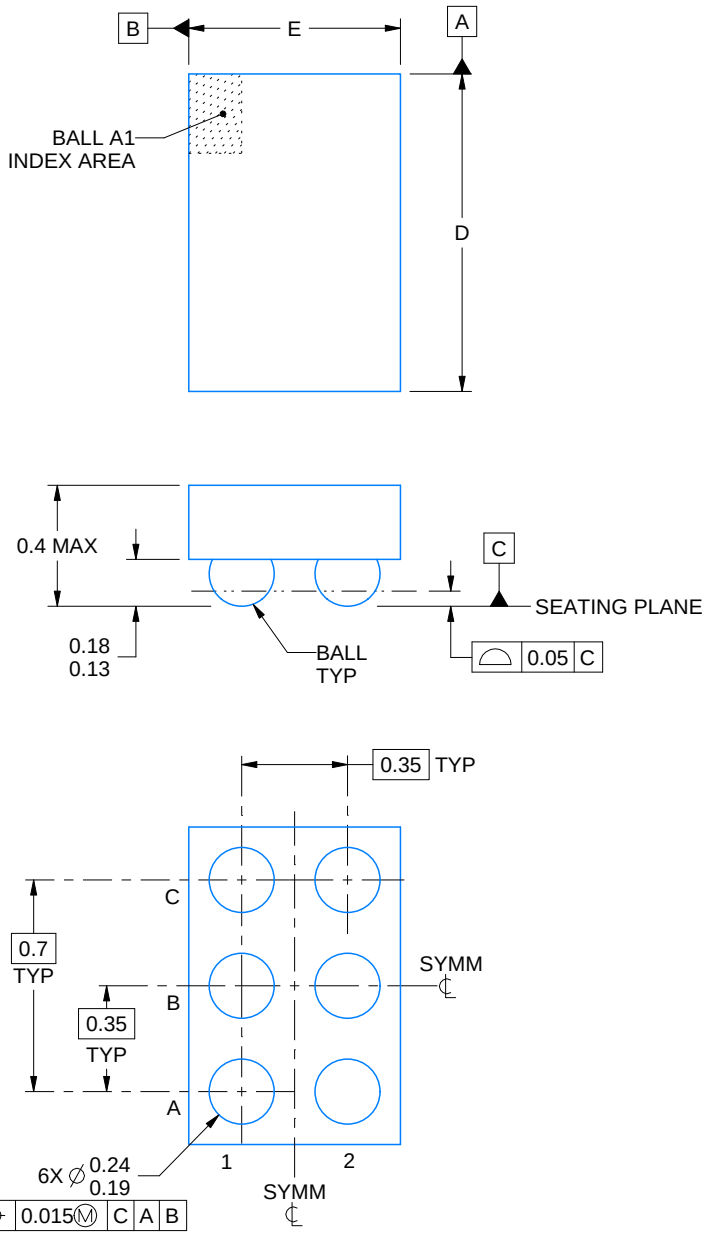
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62801YKAR	DSBGA	YKA	6	3000	220.0	220.0	35.0
TPS62801YKAT	DSBGA	YKA	6	250	220.0	220.0	35.0

PACKAGE OUTLINE

YKA0006

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



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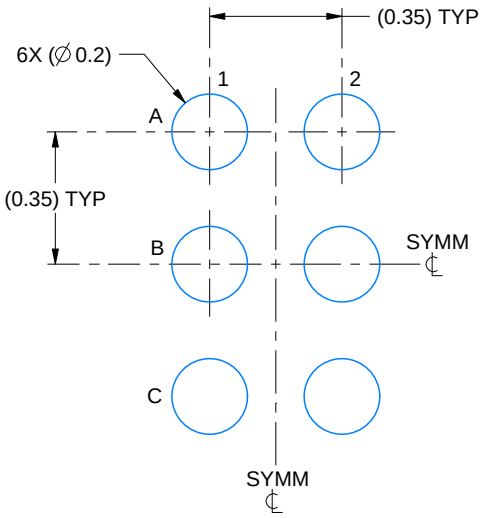
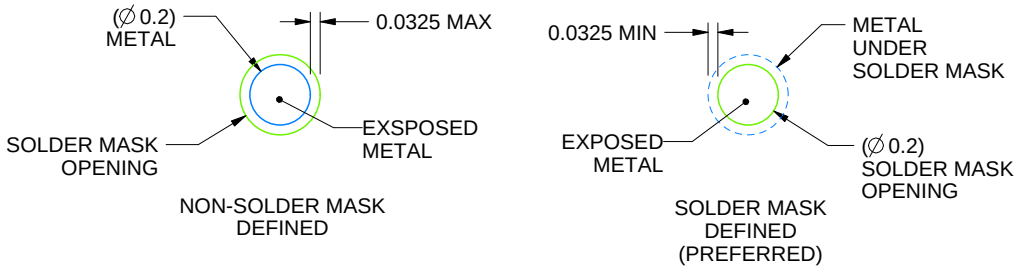
NanoFree Is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

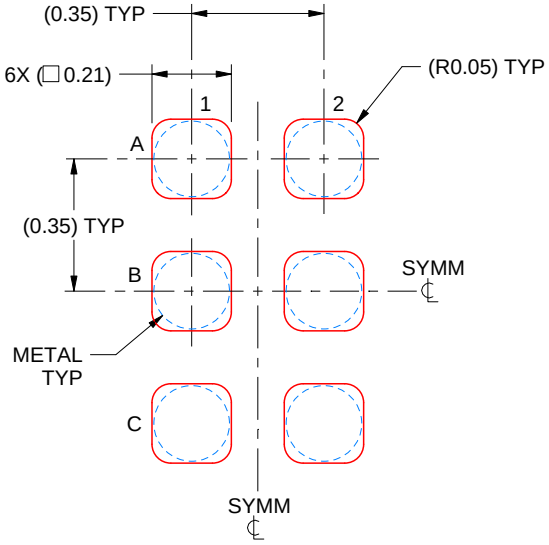
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YKA0006

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm - 0.1 mm THICK STENCIL
SCALE:50X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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