force TECHNOLOGIES

FT28C16

Parallel EEPROM 16K (2Kx8)

Features

- **Fast Read Access Time - 150 ns**
- **Fast Byte Write - 200 µs or 1 ms**
- **Self-Timed Byte Write Cycle**
  - **–Internal Address and Data Latches**
  - **–Internal Control Timer**
  - **–Automatic Clear Before Write**
- **Direct Microprocessor Control**
  - **–$\overline{\text{DATA}}$ POLLING**
- **Low Power**
  - **–30 mA Active Current**
  - **–100 µA CMOS Standby Current**
- **High Reliability**
  - **–Endurance: 10^4 or 10^5 Cycles**
  - **–Data Retention: 10 Years**
- **5V ± 10% Supply**
- **CMOS & TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte Wide Pinout**
- **Commercial, Industrial and Military Temperature Ranges**

Description

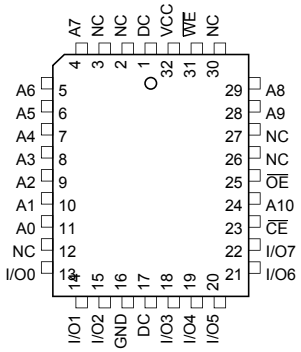
The FT28C16 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The FT28C16 is a 16K memory organised as 2,048 words by 8 bits. The device is manufactured with reliable Atmel die.

(continued)

Pin Configurations

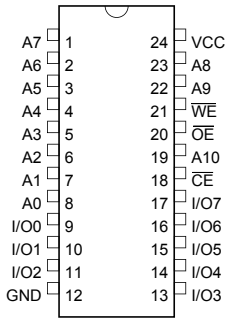
Pin Name	Function
A0 - A10	Addresses
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
$\overline{\text{WE}}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

LCC/"J"LCC
Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

CDIL/FP
Top View

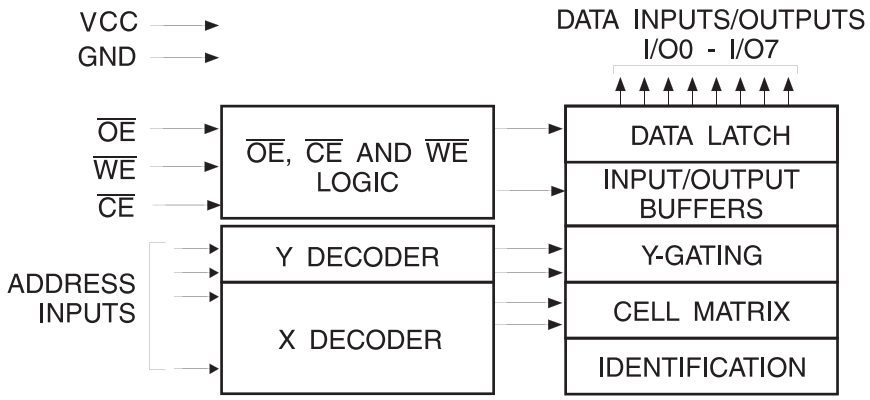


The FT28C16 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The end of a write cycle can be determined by $\overline{\text{DATA}}$ POLLING of I/O_7. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

The CMOS technology offers fast access times of 150 ns at low power dissipation. When the chip is deselected the standby current is less than 100 µA.

Force's 28C16 has additional features to ensure high quality and manufacturability. The device utilises error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of EEPROM are available for device identification or tracking.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including NC Pins) with Respect to Ground	-0.6V to +6.25V
All Output Voltages with Respect to Ground	-0.6V to V_{CC} + 0.6V
Voltage on $\overline{OE}$ and A9 with Respect to Ground	-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Device Operation

READ: The FT28C16 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the FT28C16 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

FAST BYTE WRITE: The FT28C16E offers a byte write time of 200 µs maximum. This feature allows the entire device to be rewritten in 0.4 seconds.

$\overline{\text{DATA}}$ POLLING: The FT28C16 provides $\overline{\text{DATA}}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways: (a) V_{CC} sense—if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power on delay—once V_{CC} has reached 3.8V the device will automatically time out 5 ms (typical) before allowing a byte write; and (c) write inhibit—holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the FT28C16 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

DEVICE IDENTIFICATION: An extra 32 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12 ± 0.5V and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

DC and AC Operating Range

		FT28C16
Operating Temperature (Case)	Com.	0°C - 70°C
	Ind.	-40°C - 85°C
	Mil	-55°C - 125°C
Vcc Power Supply		5V ± 10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL} H	igh Z

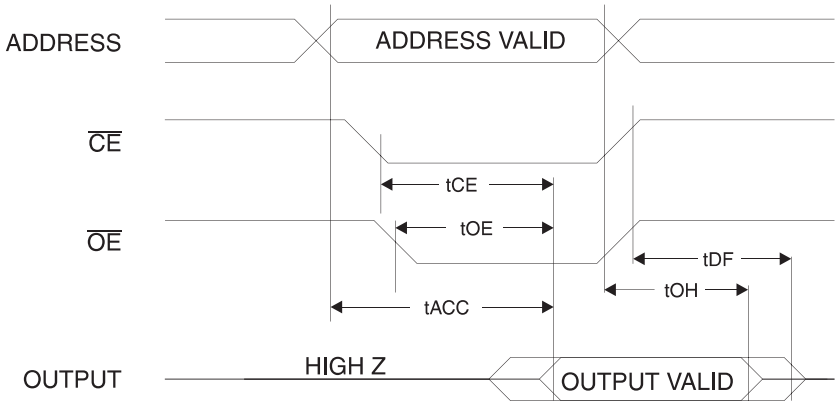
DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC} + 1.0V			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC} + 1.0V	Com.		2	mA
			Ind.		3	mA
I_{CC}	V_{CC} Active Current AC	f = 5 MHz; I_{OUT} = 0 mA $\overline{CE}$ = V_{IL}	Com.		30	mA
			Ind.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			.4	V
V_{OH}	Output High Voltage	I_{OH} = -400 µA		2.4		V

AC Read Characteristics

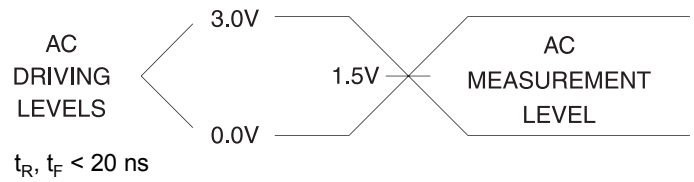
Symbol	Parameter	FT28C16-15		FT28C16-20		FT28C16-25		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	10	70	10	80	10	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first.	0		0		0		ns

AC Read Waveforms(1)(2)(3)(4)



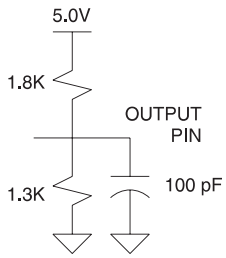
Notes:
1. $\overline{CE}$ may be delayed up to t_{ACC} - t_{CE} after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{CE} or by t_{ACC} - t_{OE} after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterised and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20 ns

Output Test Load



Pin Capacitance

f = 1 MHz, T = 25°C(1)

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

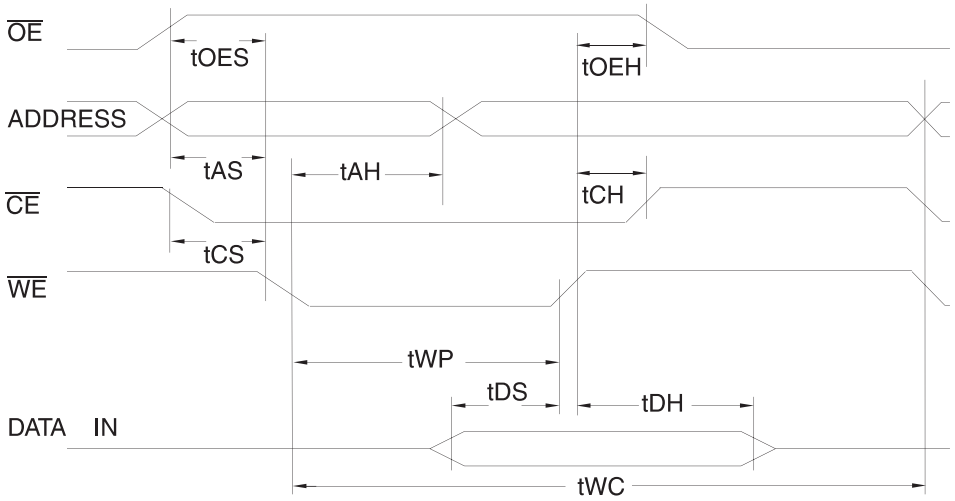
Note: 1. This parameter is characterised and is not 100% tested.

AC Write Characteristics

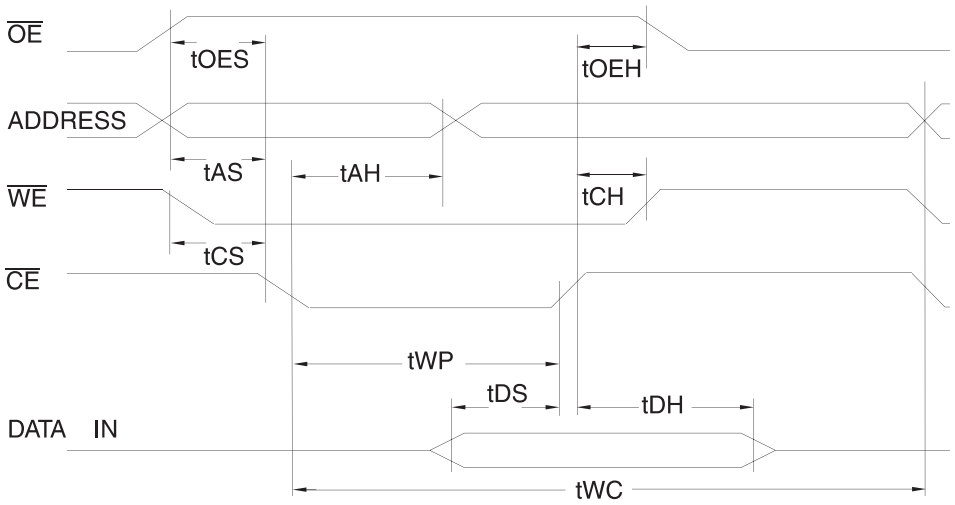
Symbol	Parameter		Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time		10			ns
t_{AH}	Address Hold Time		50			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100		1000	ns
t_{DS}	Data Set-up Time		50			ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time		10			ns
t_{CS}, t_{CH}	$\overline{CE}$ to $\overline{WE}$ and $\overline{WE}$ to $\overline{CE}$ Set-up and Hold Time		0			ns
t_{WC}	Write Cycle Time	FT28C16		0.5	1.0	ms
		FT28C16E		100	200	µs

AC Write Waveforms

$\overline{WE}$ Controlled



$\overline{CE}$ Controlled

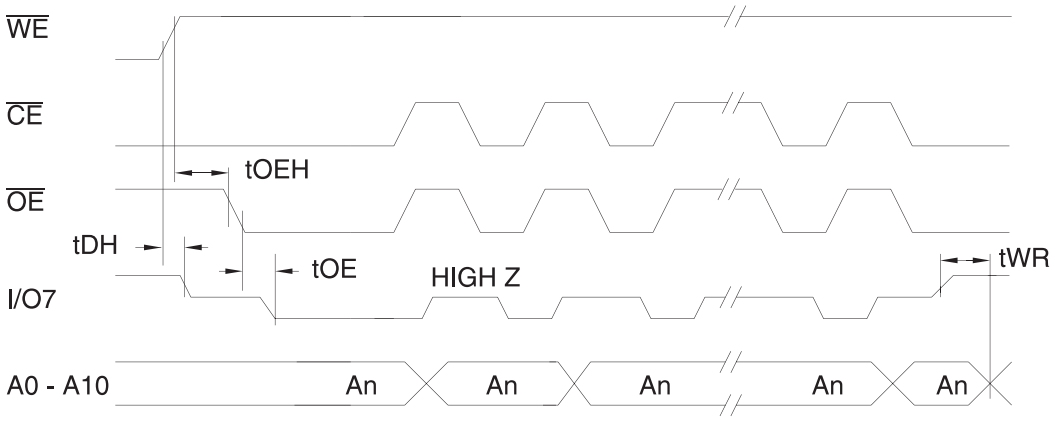


$\overline{\text{Data}}$ Polling Characteristics(1)

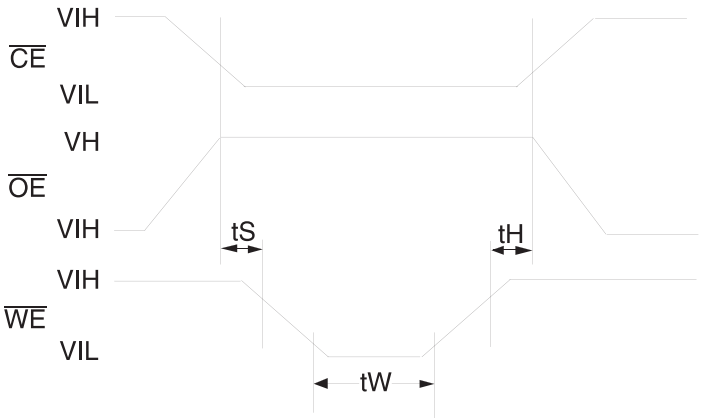
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay(2)				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterised and not 100% tested.
2. See AC Characteristics.

$\overline{\text{Data}}$ Polling Waveforms

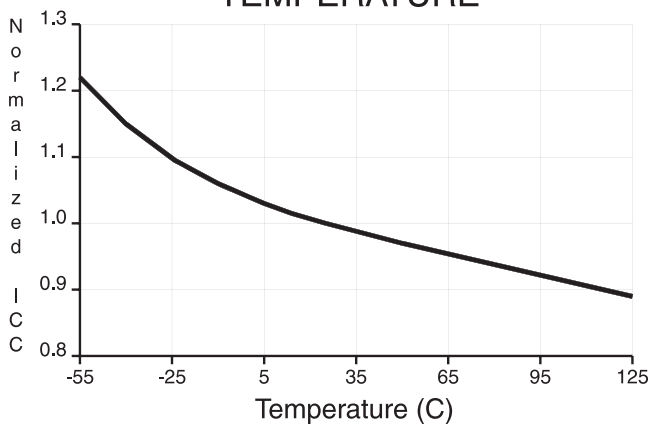


Chip Erase Waveforms

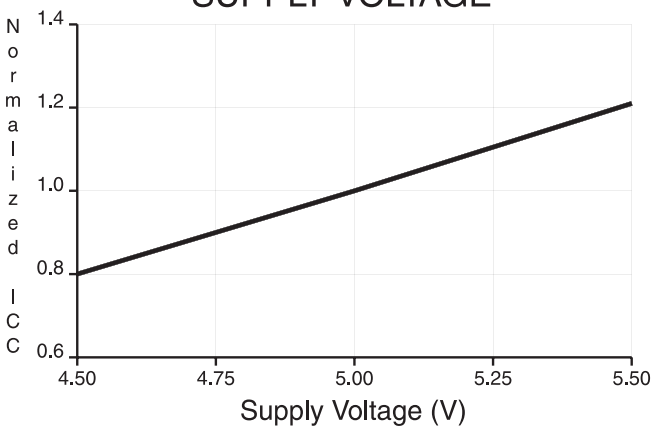


$t_S = t_H = 1$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0V \pm 0.5V$

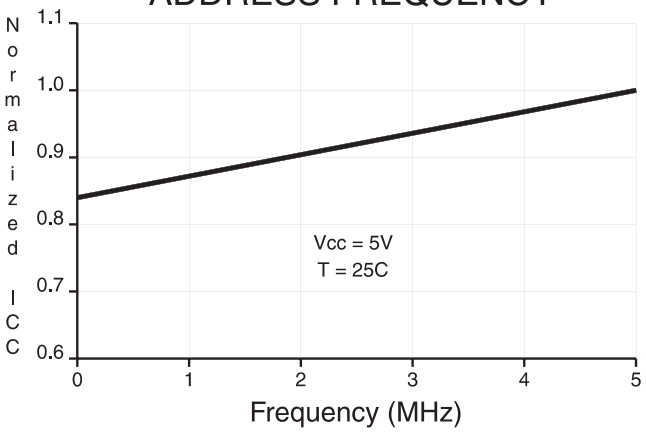
NORMALISED SUPPLY CURRENT vs. TEMPERATURE



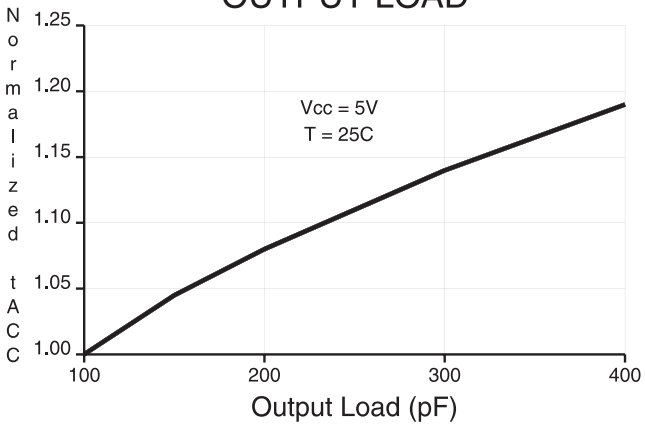
NORMALISED SUPPLY CURRENT vs. SUPPLY VOLTAGE



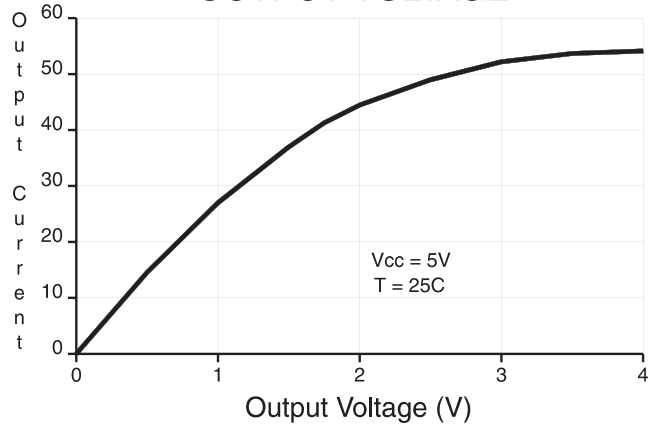
NORMALISED SUPPLY CURRENT vs. ADDRESS FREQUENCY



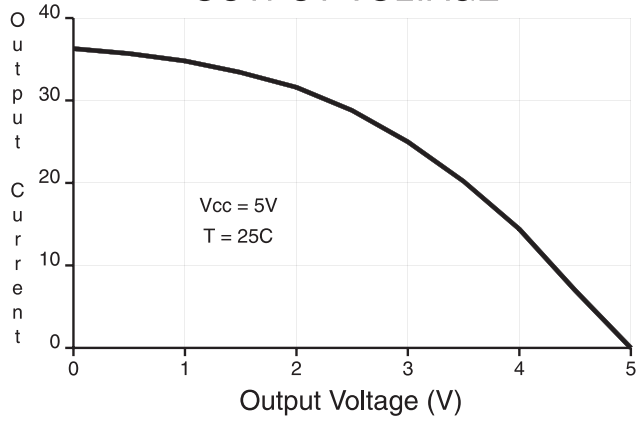
NORMALISED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



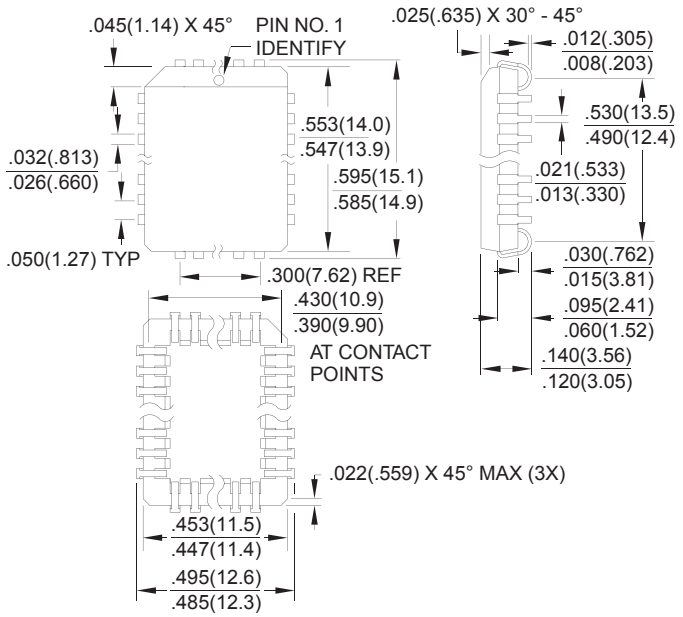
Ordering Information (1)

t_{ACC} (ns)	I_{CC} (mA) Active	I_{CC} (mA) Standby	Ordering Code	Package	Operation Range
150	30	0.1	FT28C16(E)-15DC FT28C16(E)-15JC FT28C16(E)-15PC FT28C16(E)-15SC	24D6 32J 24P6 24S	Commercial (0°C to +70°C)
150	45	0.1	FT28C16(E)-15DI FT28C16(E)-15JI FT28C16(E)-15PI FT28C16(E)-15SI	24D6 32J 24P6 24S	Industrial (-40°C to +85°C)
			FT28C16(E)-15DM	24D6	Military (-55°C to +125°C)
			FT28C16(E)-15DMB	24D6	Military (-55°C to +125°C) Mil-Std-883 M5004
200	30	0.1	FT28C16(E)-20DC FT28C16(E)-20JC FT28C16(E)-20PC FT28C16(E)-20SC	24D6 32J 24P6 24S	Commercial (0°C to +70°C)
200	45	0.1	FT28C16(E)-20DI FT28C16(E)-20JI FT28C16(E)-20PI FT28C16(E)-20SI	24D6 32J 24P6 24S	Industrial (-40°C to +85°C)
			FT28C16(E)-20DM	24D6	Military (-55°C to +125°C)
			FT28C16(E)-20DMB	24D6	Military (-55°C to +125°C) Mil-Std-883 M5004
250	30	0.1	FT28C16(E)-25DC FT28C16(E)-25JC FT28C16(E)-25PC FT28C16(E)-25SC	24D6 32J 24P6 24S	Commercial (0°C to 70°C)
250	45	0.1	FT28C16(E)-25DI FT28C16(E)-25JI FT28C16(E)-25PI FT28C16(E)-25SI	24D6 32J 24P6 24S	Industrial (-40°C to +85°C)
			FT28C16(E)-25DM	24D6	Military (-55°C to +125°C)
			FT28C16(E)-25DMB	24D6	Military (-55°C to +125°C) Mil-Std-883 M5004

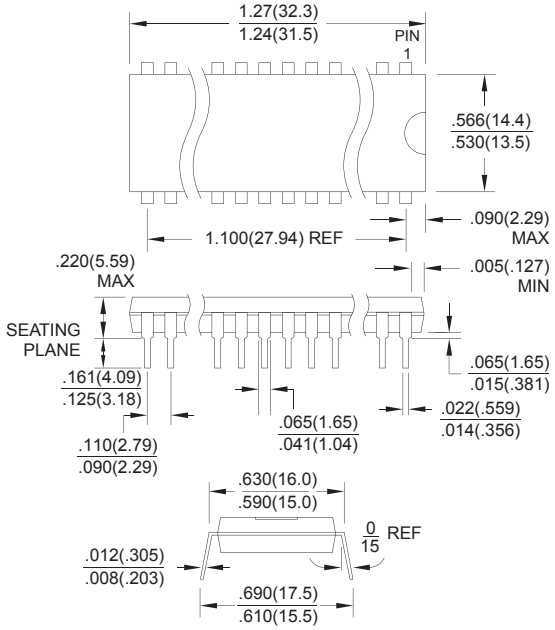
Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
24S	24 Lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
24D6	24-lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
	Options
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles;

Packaging Information

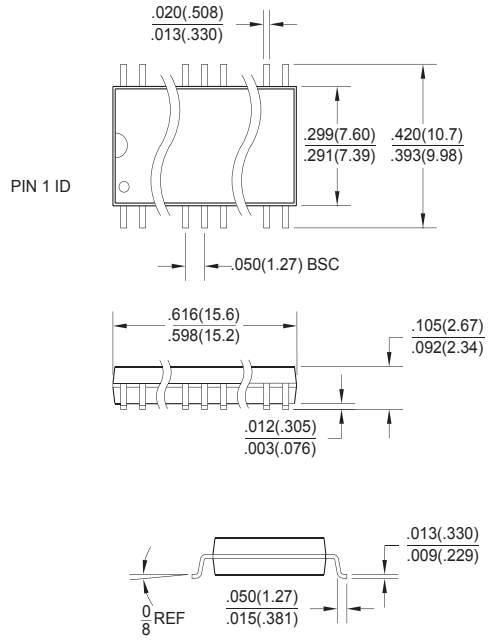
32J, 32-Lead, Plastic J-Leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AA



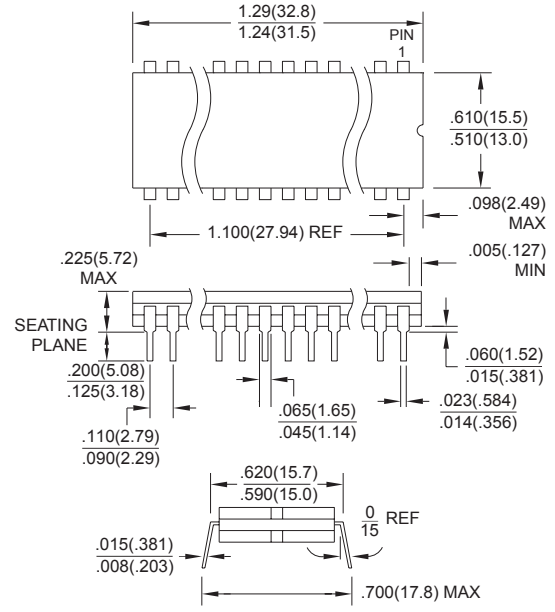
24P6, 24-Lead, 0.600” Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-011 AA



24S, 24-Lead, 0.300” Wide, Plastic Gull Wing Small Outline (SOIC)
Dimensions in Inches and (Millimeters)



24D6, 24-lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)



Revision History

Rev 1	12/04/05	Original
Rev 2	07/09/11	Removed 200 µs Write Time option

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