8 Channel Serial Interface Low-Side Driver

Check for Samples: DRV8860

FEATURES

- **8-Channel Protected Low-side Driver**
  - **Eight NMOS FETs with Overcurrent Protection**
  - **Integrated Inductive Catch Diodes**
  - **Open/Short Load Detection**
  - **Configurable 100% Output Timing**
  - **Configurable PWM Duty Cycle**
- **Continuous Current Driving Capability**
  - **560mA (Single Channel on)**
  - **280mA (Quad Channels on)**
  - **200mA (Oct Channels on)**
  - **Support Parallel Configuration**
- **8V to 38V Supply Voltage Range**
- **Input Digital Noise Filter for Noise Immunity**
- **Internal Data Read Back Capability for Reliable Control**
- **Programmable Current Profile**
  - **Configurable 100% Output Timing. Fast Activation of Solenoid.**
  - **Configurable PWM Duty Cycle in Chopping Mode. Reducing Power Consumption and Thermal Dissipation in Hold-mode of Solenoid.**
- **Serial Interface**
  - **Daisy Chain Connection**
- **16-pin TSSOP Package**
- **Protection and Diagnostic Features**
  - **Overcurrent Protection (OCP)**
  - **Open Load Detection (OL)**
  - **Over-Temperature Shutdown (OTS)**
  - **Under-Voltage Lockout (UVLO)**
  - **Individual Channel Status Report**
  - **Fault Condition Alarm**

APPLICATIONS

- **Relays**
- **Unipolar Stepper Motors**
- **Solenoids**
- **Electromagnetic Drivers**
- **General Low-side Switch Applications**

DESCRIPTION

The DRV8860 provides an 8-channel low side driver with overcurrent protection and open/shorted load detection. It has built-in diodes to clamp turn-off transients generated by inductive loads, and can be used to drive unipolar stepper motors, DC motors, relays, solenoids, or other loads.

DRV8860 can supply up to 200mA × 8 channel continuous output current. The current driving capability increased with lower PWM duty cycle. A single channel can deliver up to 560mA continuous output current. Refer to the OUTPUT CURRENT RECOMMENDATION section for details.

A serial interface is provided to control the DRV8860 output drivers, configure internal setting register and read the fault status of each channel. Multiple DRV8860 devices can be daisy-chained together to use a single serial interface. Energizing-Time and Holding-PWM-Duty cycles are configurable through serial interface as well. These functions allow for lower temperature operation rather than traditional always-on solutions.

Internal shutdown functions are provided for over current protection, short circuit protection, under voltage lockout, and over temperature. DRV8860 can diagnosis the open load condition. Fault information for each channel can be read out through serial interface and indicated by an external fault pin.

The DRV8860 is packaged in a 16 pin TSSOP package (Eco-friendly: RoHS and no Sb/Br).

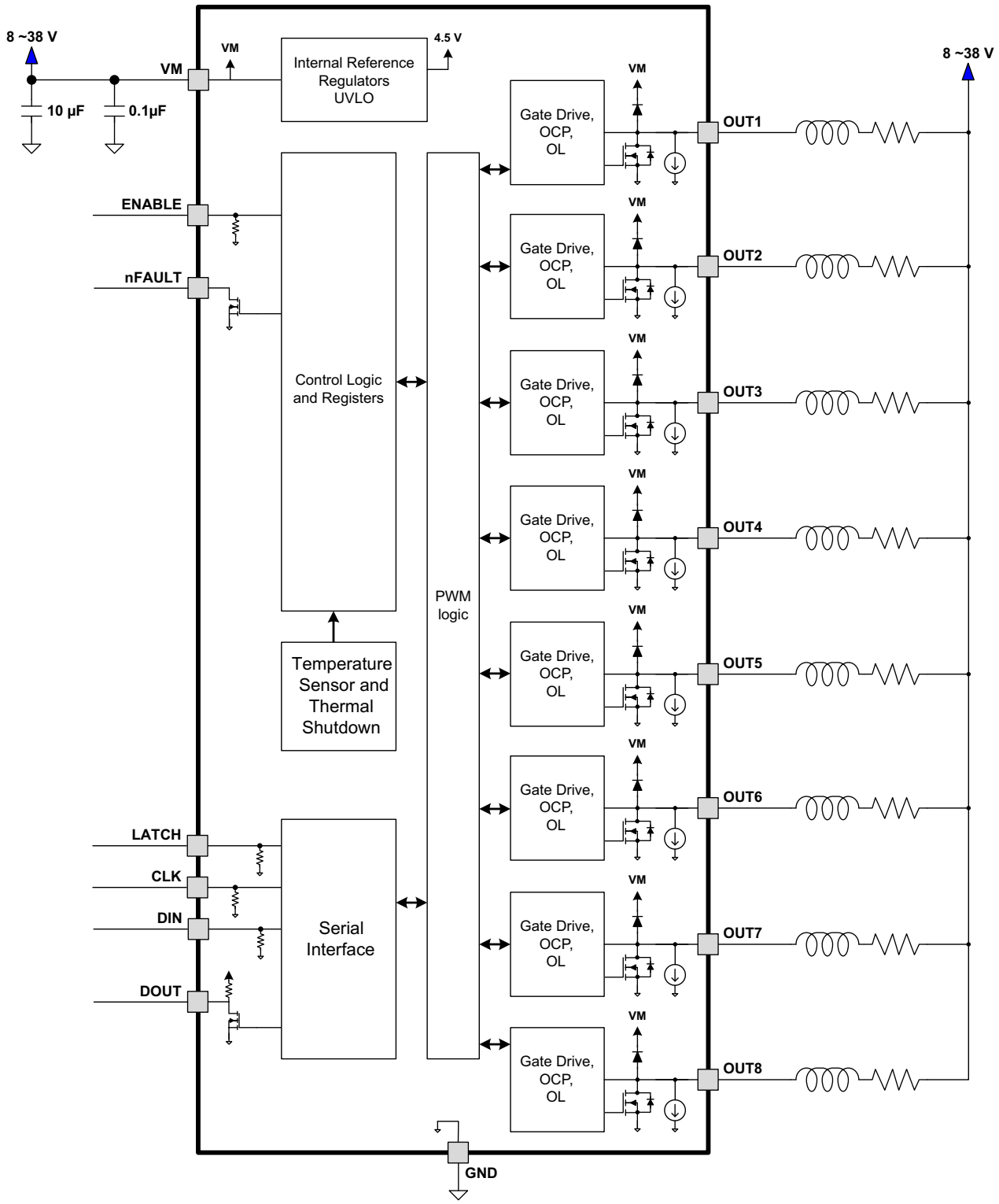
Ordering Information

For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

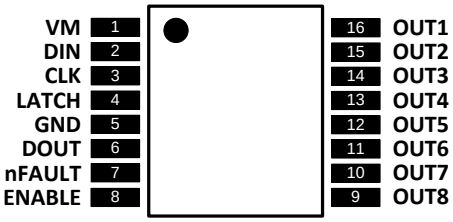
The package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Functional Block Diagram



PW (TSSOP) PACKAGE
(TOP VIEW)



Pin Functions

NAME	PIN	I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
POWER AND GROUND				
GND	5	—	Device ground	All pins must be connected to ground
VM	1	—	Motor power supply	Connect to motor supply voltage. Bypass to GND with a 0.1µF ceramic capacitor plus a 10µF electrolytic capacitor.
CONTROL AND SERIAL INTERFACE				
ENABLE	8	I	Output stage enable control input	Logic high to enable outputs, logic low to disable outputs. Internal logic and registers can be read and written to when ENABLE is logic low. Internal pulldown.
LATCH	4	I	Serial latch signal	Refer to serial communication waveforms. Internal pulldown.
CLK	3	I	Serial clock input	Rising edge clocks data into part for write operations. Falling edge clocks data out of part for read operations. Internal pulldown.
DIN	2	I	Serial data input	Serial data input from controller. Internal pulldown.
DOUT	6	O	Serial data output	Serial data output to controller. Open-drain output with internal pullup.
STATUS				
nFAULT	7	OD	Fault	Logic low when in fault condition. Open-drain output requires external pullup. Faults: OCP, OL, OTS, UVLO
OUTPUT				
OUT1	16	O	Low-side output 1	NFET output driver. Connect external load between this pin and VM
OUT2	15	O	Low-side output 2	NFET output driver. Connect external load between this pin and VM
OUT3	14	O	Low-side output 3	NFET output driver. Connect external load between this pin and VM
OUT4	13	O	Low-side output 4	NFET output driver. Connect external load between this pin and VM
OUT5	12	O	Low-side output 5	NFET output driver. Connect external load between this pin and VM
OUT6	11	O	Low-side output 6	NFET output driver. Connect external load between this pin and VM
OUT7	10	O	Low-side output 7	NFET output driver. Connect external load between this pin and VM
OUT8	9	O	Low-side output 8	NFET output driver. Connect external load between this pin and VM

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

Critical Components

PIN	NAME	COMPONENT
1	VM	10µF electrolytic rated for VM voltage to GND, 0.1µF ceramic rated for VM voltage to GND
7	nFAULT	Requires external pullup to logic supply

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

	DRV8860		UNIT
	MIN	MAX	
Power supply voltage range (VM)	–0.3	40	V
Digital input pin current range (ENABLE, LATCH, CLK, DIN)	0	20	mA
Digital output pin voltage range (DOUT, nFAULT)	–0.5	7	V
Digital output pin current (DOUT, nFAULT)	–0.5	7	V
Output voltage range (OUTx)	–0.3	40	V
Output current range (OUTx)	Internally limited		A
Operating virtual junction temperature range, T_J	–40	150	°C
Storage temperature range, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed

Thermal Information(1)

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC		DRV8860	UNITS
		PW (16 PINS)	
Θ_{JA}	Junction-to-ambient thermal resistance (2)	103	°C/W
$\Theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(3)	37.9	
Θ_{JB}	Junction-to-board thermal resistance(4)	48	
Ψ_{JT}	Junction-to-top characterization parameter(5)	3	
Ψ_{JB}	Junction-to-board characterization parameter(6)	47.4	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard 30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, Ψ_{JT}, estimates the junction temperature of the device in a real system and is extracted from the simulation data for obtaining Θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, Ψ_{JB}, estimates the junction temperature of the device in a real system and is extracted from the simulation data for obtaining Θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage range	8.2		38	V
I_{OUT}	Low-side driver current capability			560	mA
T_A	Operating ambient temperature range	–40		85	°C

Electrical Characteristics

T_A = 25°C, over operating free-air temperature range (unless otherwise noted)

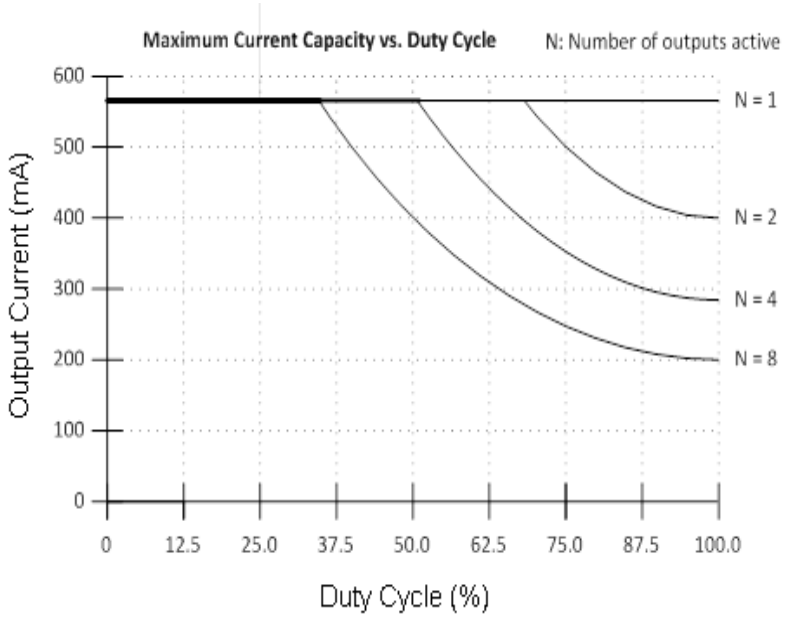
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	VM operating supply current	VM = 24V		3		mA
V_{UVLO}	VM undervoltage lockout voltage	VM rising			8.2	V
LOGIC-LEVEL INPUTS (DIN, CLK, LATCH, ENABLE)						
V_{IL}	Input low voltage			0.6	0.7	V
V_{IH}	Input high voltage		2			V
V_{HYS}	Input hysteresis			0.45		V
I_{IL}	Input low current	VIN = 0	–20		20	µA
I_{IH}	Input high current	VIN = 3.3V			100	µA
R_{PD}	Input pulldown resistance			100		kΩ
nFAULT, DOUT OUTPUTS (OPEN-DRAIN OUTPUTS)						
V_{OL}	Output low voltage	I_O = 5mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3V, nFAULT	–1		1	µA
R_{PU}	Input pullup resistance	DOUT only (Pull up to internal 5.7V)		1.4		kΩ
LOW-SIDE FET DRIVERS						
$R_{ds(on)}$	FET on resistance	V_M = 24V, I_O = 150mA, T_J = 25°C		1.5		Ω
		V_M = 24V, I_O = 150mA, T_J = 85°C		1.8		
I_{OFF}	Off-state leakage current	V_M = 24V, T_J = 25°C	0	30		µA
HIGH-SIDE FREE-WHEELING DIODES						
V_F	Diode forward voltage	V_M = 24V, I_O = 150mA, T_J = 25°C		0.9		V
OUTPUTS						
t_R	Rise time	I_O = 150mA, VM = 24V, resistive load	50		300	ns
tF	Fall time		50		300	ns
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level	Each channel separately monitored		620		mA
t_{OCP}	Overcurrent protection deglitch time	VM = 24V	2.7	3.5	3.85	µs
IOL	Open load detect pull-down current	Each channel separately monitored		30		µA
V_{OL}	Open load detect threshold voltage	Each channel separately monitored		1.2		V
t_{OL}	Open load detect deglitch time	Each channel separately monitored	14	17	20	µs
T_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C
T_{HYS}	Thermal shutdown hysteresis	Die temperature		35		°C
PWM CHOPPING FREQUENCY						
f_{PWM}	PWM chopping frequency	Duty cycle is > 25%	45	50	55	kHz
		Duty cycle is 25%	22	25	28	
		Duty cycle is 12.5%	11	12.5	14	

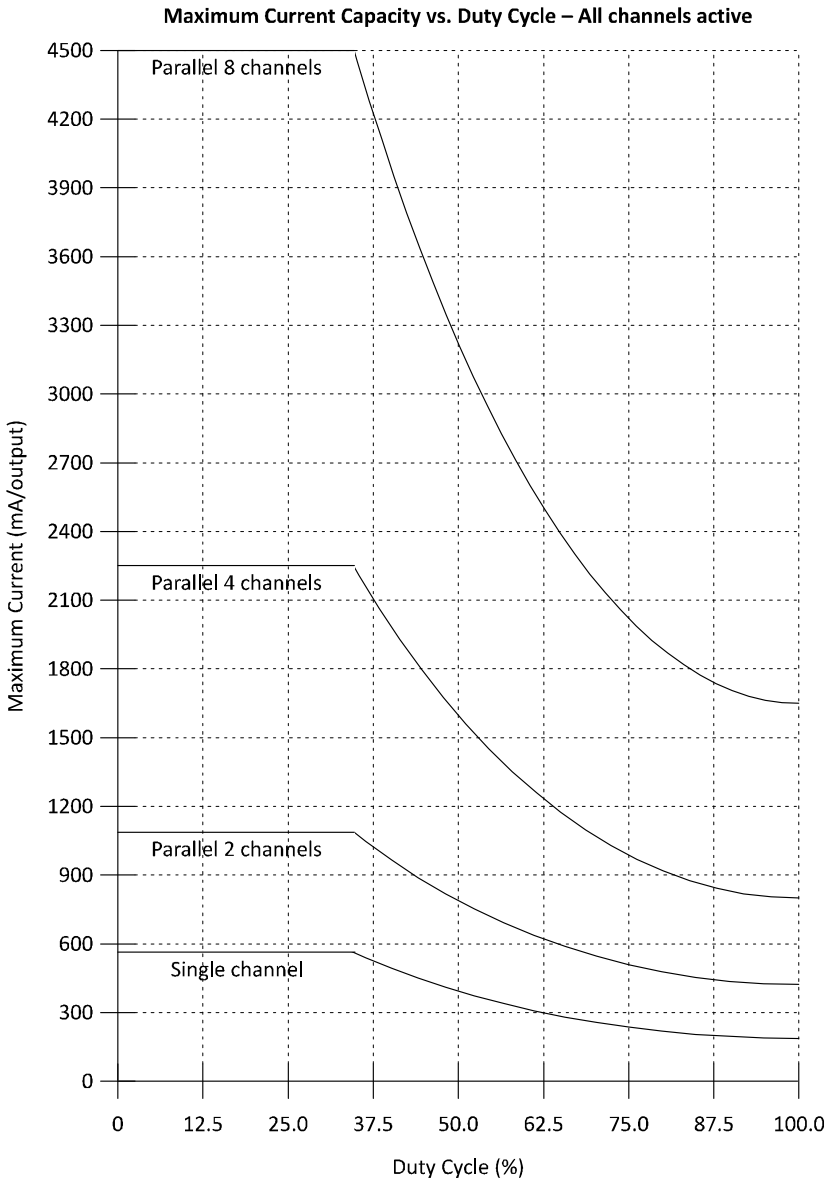
Output Current Recommendation

DRV8860 current capability will depend on several system application parameters:

- System ambient temperature
- Maximum case temperature
- Overall output current duty cycle
- Output channel configuration

OUTPUT CURRENT RECOMMENDATION (PW PACKAGE) T_A = 25°C	
CONFIGURATION	**OUTPUT CURRENT CAPACITY**
1x output on (100% duty cycle)	566mA
2x outputs on (100% duty cycle)	400mA per output
4x outputs on (100% duty cycle)	283mA per output
8x outputs on (100% duty cycle)	200mA per output



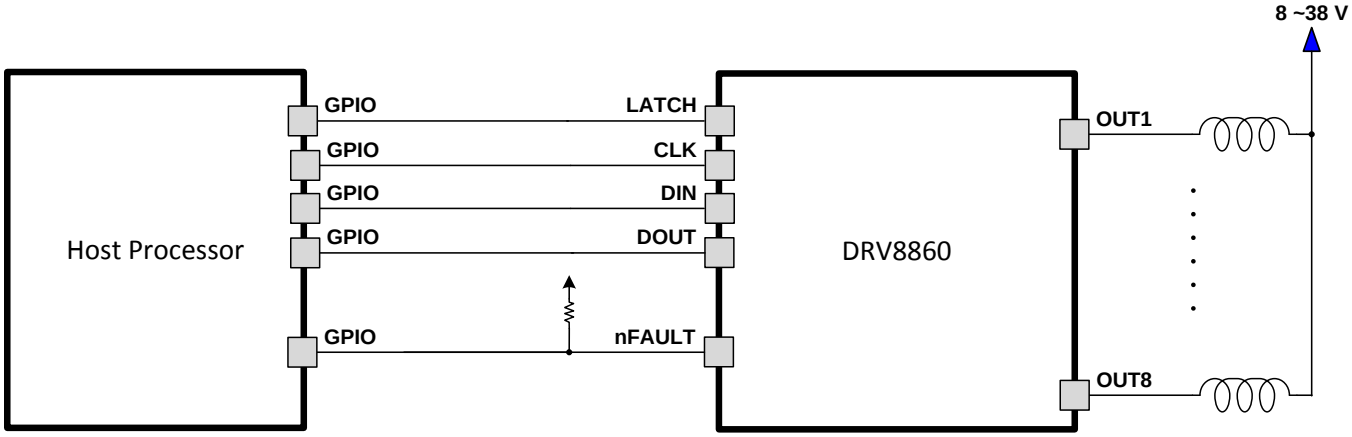

Maximum Current Capacity vs. Duty Cycle – All channels active
Parallel 8 channels
Parallel 4 channels
Parallel 2 channels
Single channel
Maximum Current (mA/output)
4500
4200
3900
3600
3300
3000
2700
2400
2100
1800
1500
1200
900
600
300
0
0
12.5
25.0
37.5
50.0
62.5
75.0
87.5
100.0
Duty Cycle (%)

Daisy Chain Connection

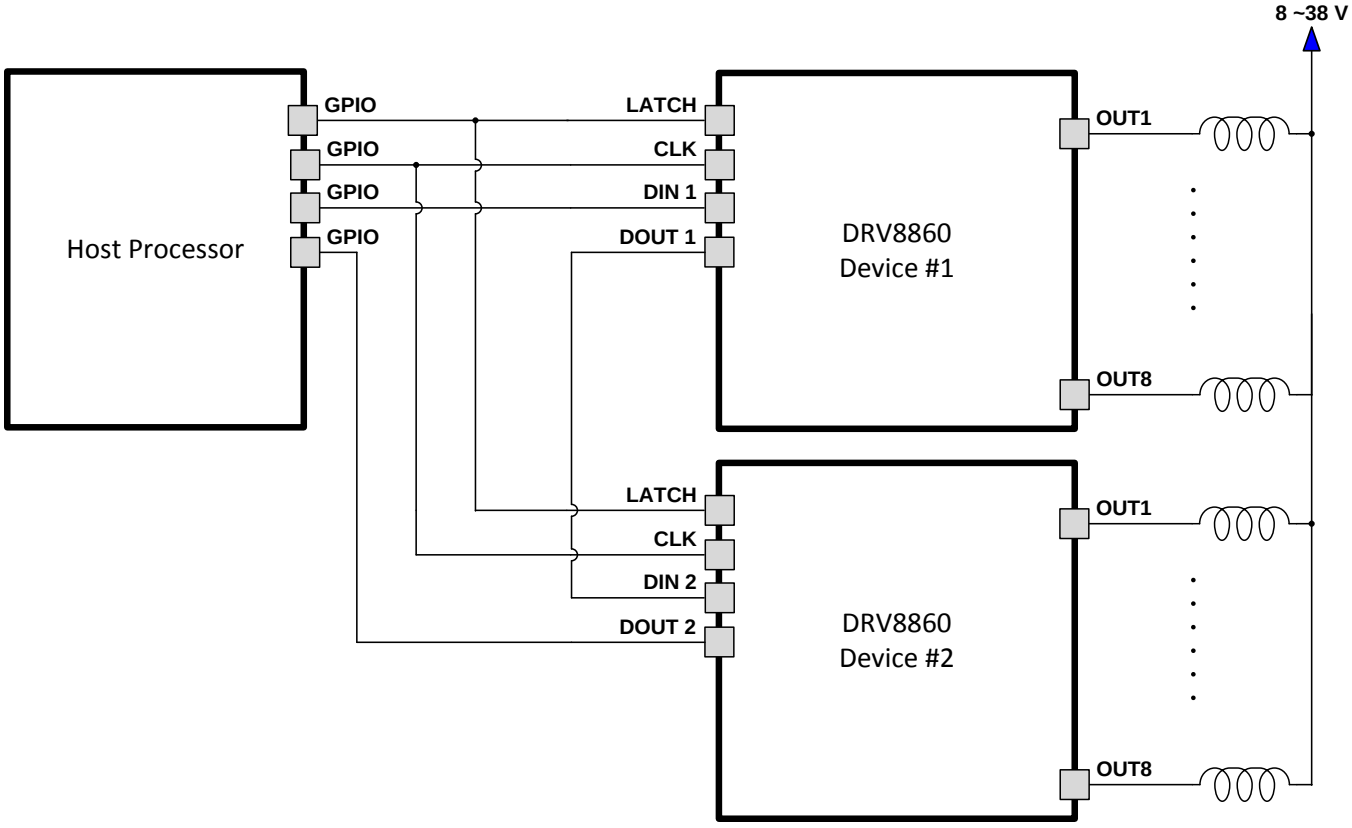
Two or more DRV8806 devices may be connected together to use a single serial interface. The DOUT pin of the first device in the chain is connected to the DIN pin of the next device. The SCLK, LATCH, RESET, and nFAULT pins are connected together.

Timing diagrams are shown on the following pages for the configuration of single devices, as well as two devices in daisy-chain connection.

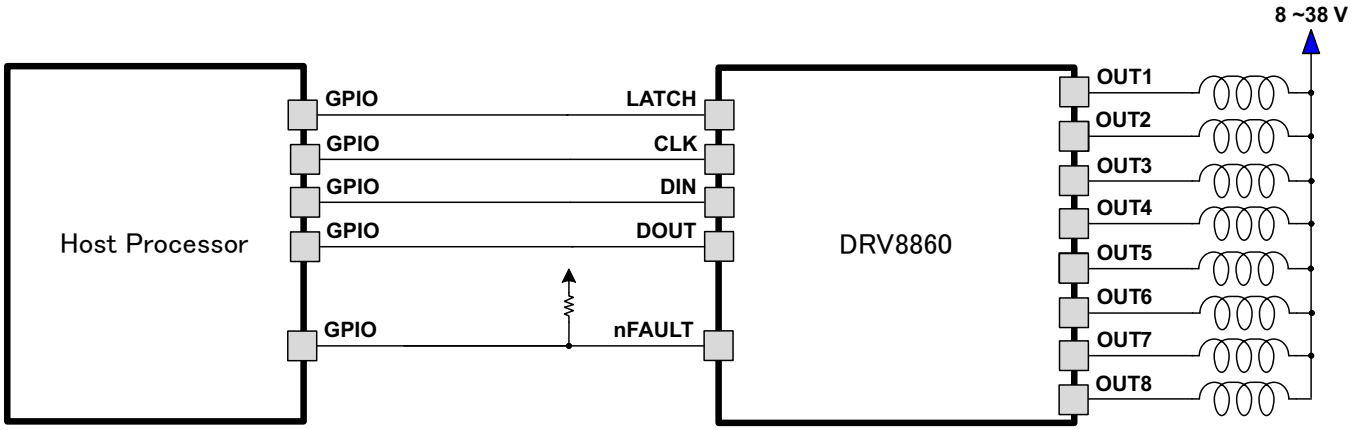
Single Device Connection



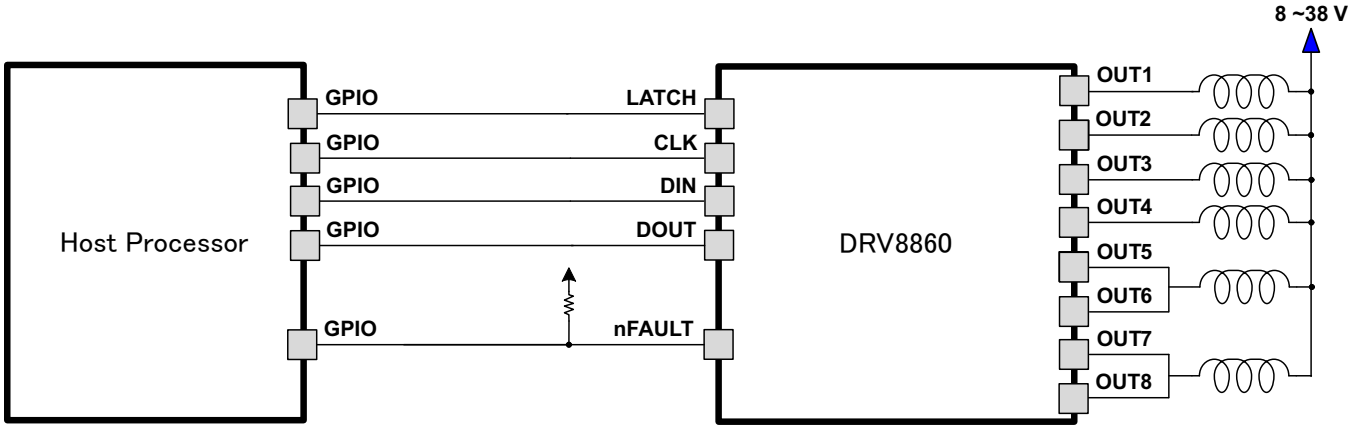
Daisy-Chain Connection



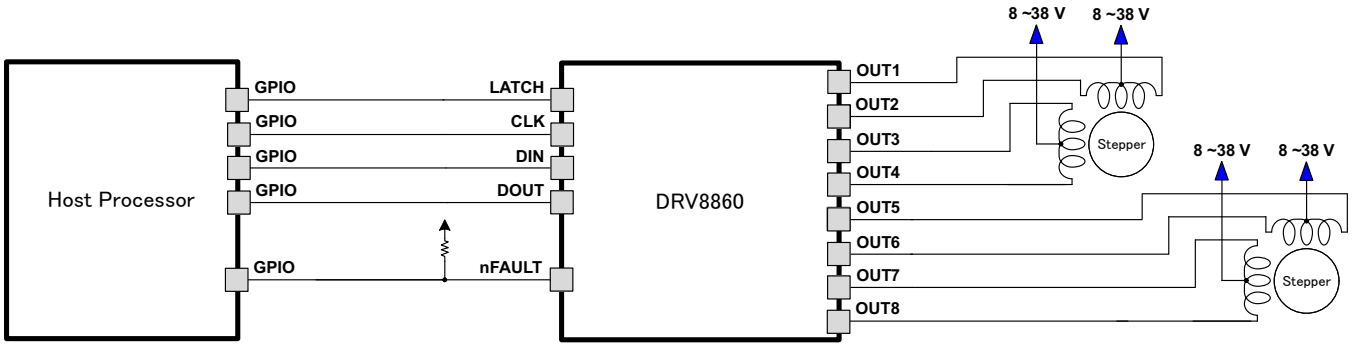
Example Output Configuration



Example Configuration 1: DRV8860 Drives 8 Low Side Loads



Example Configuration 2: DRV8860 Drives Multiple Low Side Loads With Parallel Configuration



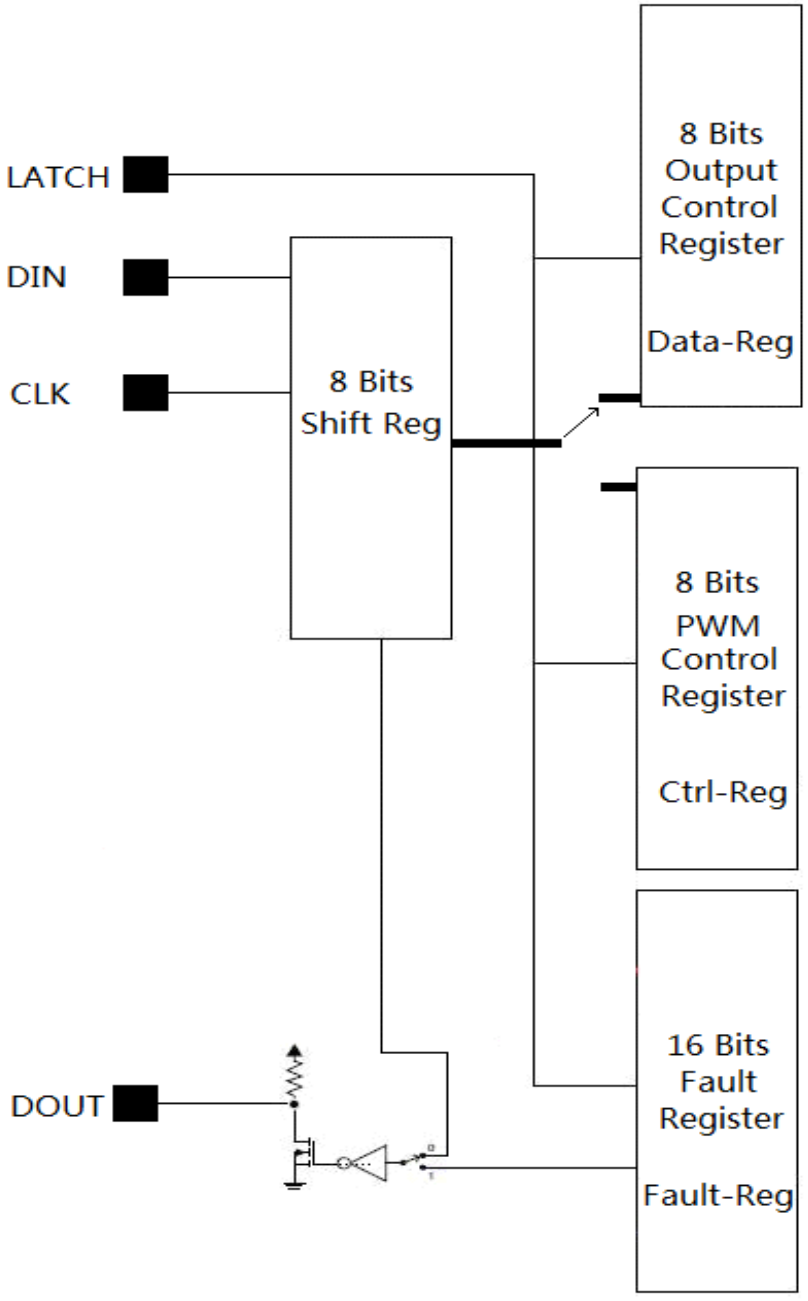
Example Configuration 3: DRV8860 Drives Two Unipolar Stepper Motors

Functional Description

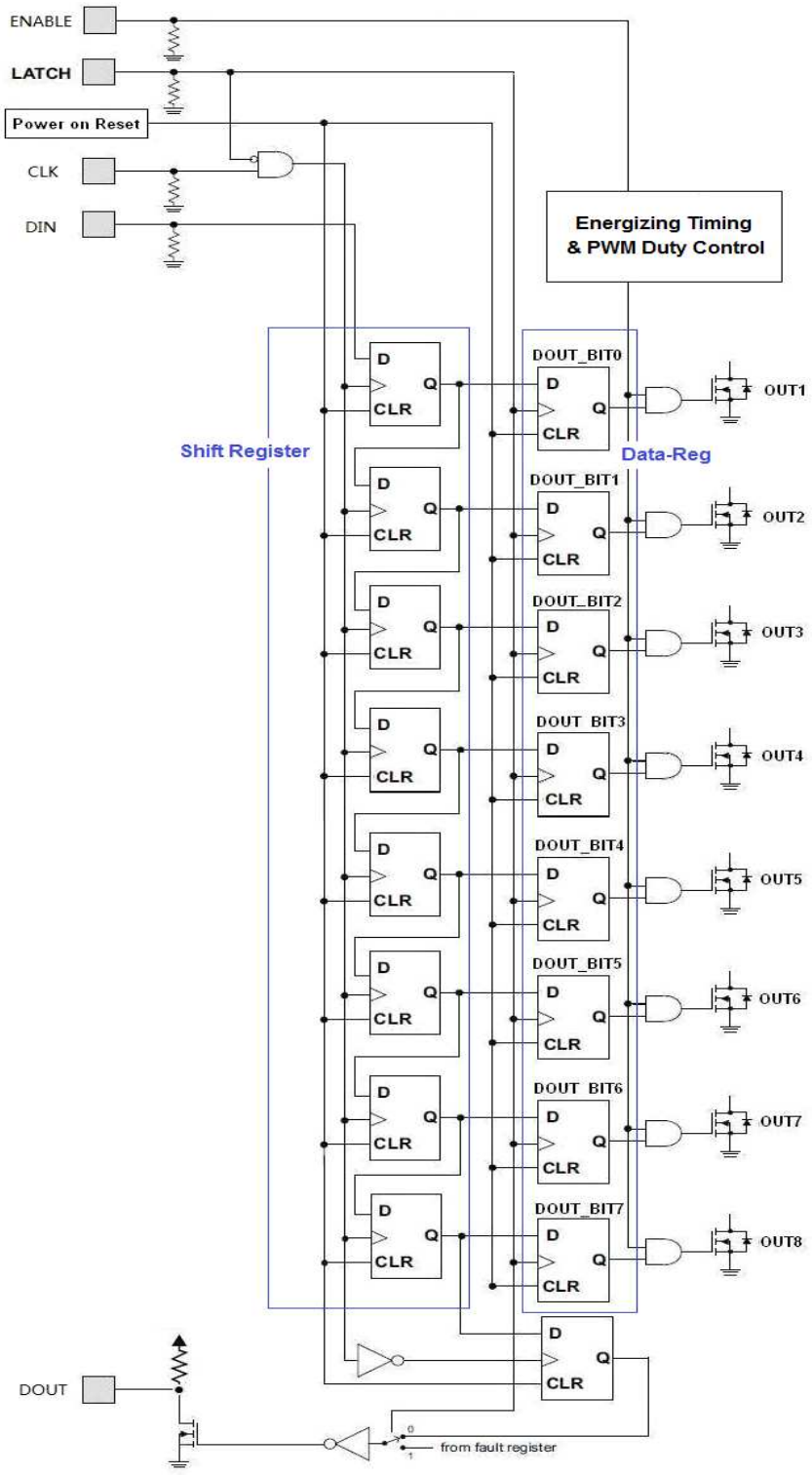
Internal Registers

The DRV8860 is controlled with a simple serial interface. There are three register banks that are used during operation: the Data register, the Control register, and the Fault register.

Register data movement flow and direction will be affected by special command.



In default condition, 8 Bit shift register data moves into output control register DATA-REG


ENABLE
LATCH
Power on Reset
CLK
DIN
Energizing Timing & PWM Duty Control
Shift Register
Data-Reg
D
Q
CLR
DOUT_BIT0
DOUT_BIT1
DOUT_BIT2
DOUT_BIT3
DOUT_BIT4
DOUT_BIT5
DOUT_BIT6
DOUT_BIT7
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT8
DOUT
from fault register

Data Register

The Data register is used to control the status of each of the eight outputs:

DATA REGISTER							
D8	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**
OUT8	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1

When any bit is '1', the corresponding output will be active. When any bit is '0', the output will be inactive.

The data register is the default write location for the serial interface. In order to read back data from this register, the Data Register Readout special command is used.

Fault Register

The Fault register can be read to determine if any channel exist fault condition. OCP is an over current fault and OL is an open load fault.

FAULT REGISTER							
F16	**F15**	**F14**	**F13**	**F12**	**F11**	**F10**	**F9**
OUT8 OCP	OUT7 OCP	OUT6 OCP	OUT5 OCP	OUT4 OCP	OUT3 OCP	OUT2 OCP	OUT1 OCP
F8	**F7**	**F6**	**F5**	**F4**	**F3**	**F2**	**F1**
OUT8 OL	OUT7 OL	OUT6 OL	OUT5 OL	OUT4 OL	OUT3 OL	OUT2 OL	OUT1 OL

When any fault occurs, nFAULT pin will be driven low and corresponding Fault register bit will be set up as '1'. OCP is a flag indicating over current fault. OL is a flag indicating open load fault.

Fault bits can be reset by two approaches:

1. Special command 'FAULT RESET' clear all fault bits.
2. Setting Data register to ON will clear corresponding OL bits.
   Setting Data register to OFF will clear corresponding OCP bits.

Control Register

The Control register is used to adjust the Energizing Time and PWM Duty Cycle of outputs:

CONTROL REGISTER							
C8	**C7**	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**
Over All Enable	PWM Duty Cycle control			Energizing Time control			

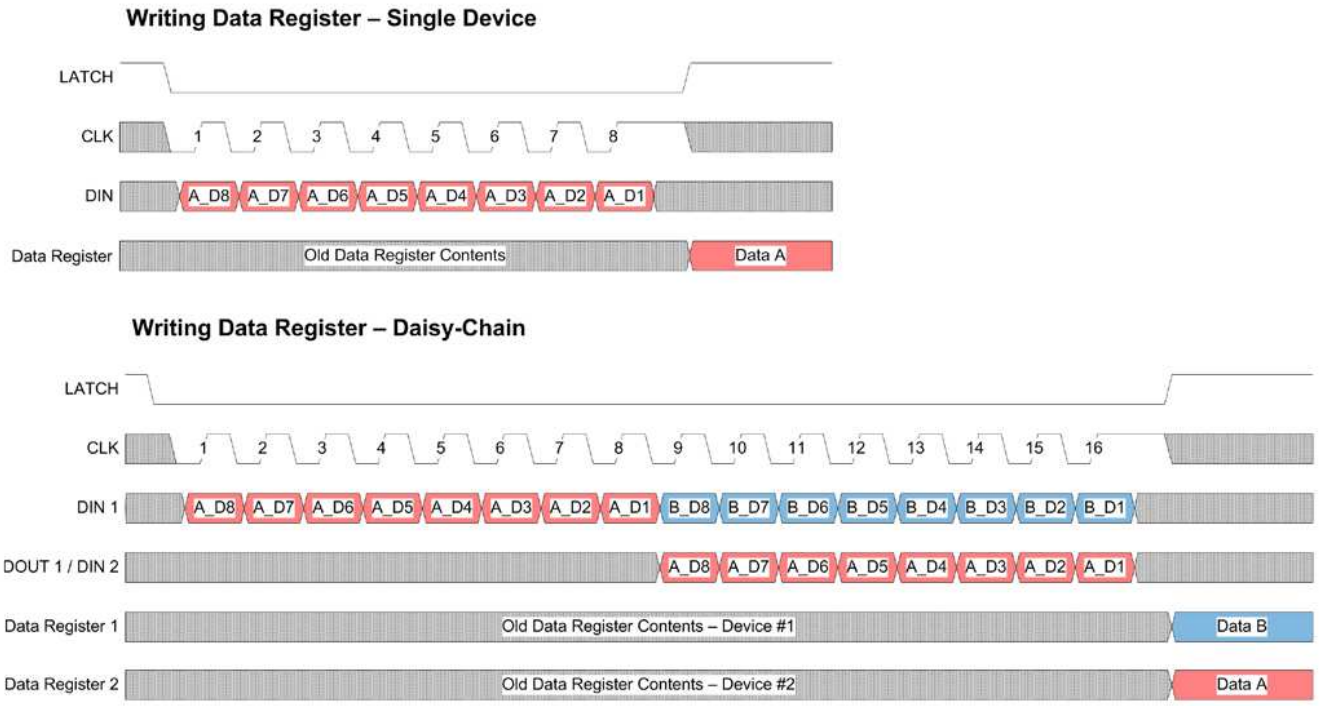
Special command 'WRITE CONTROL REGISTER' is used to program control register.

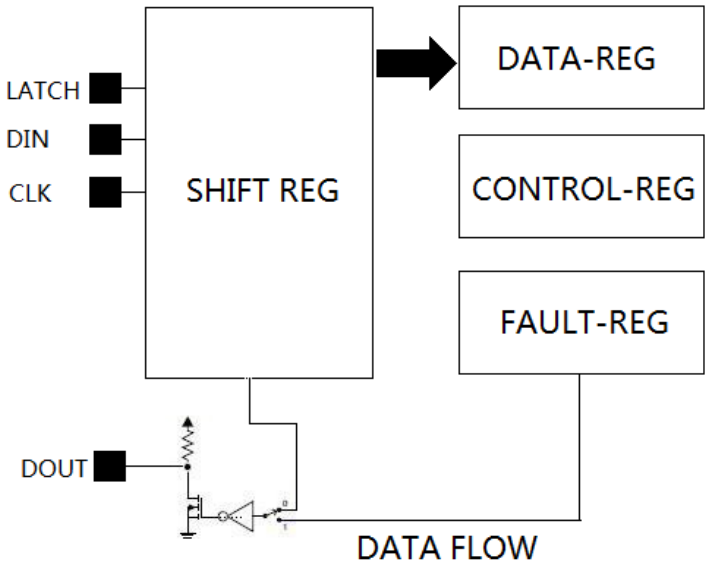
Special command 'READ CONTROL REGISTER' is used to read back control register content.

Serial Control Interface

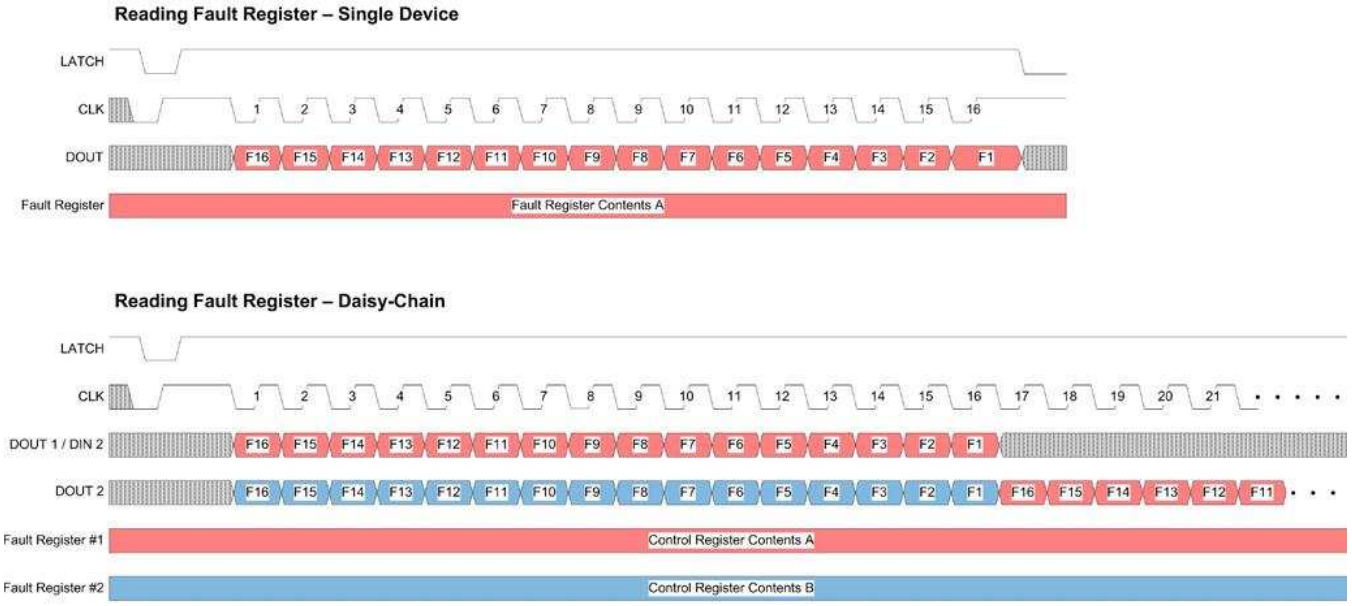
DRV8860 is using a daisy chain serial interface. Data shifting control is enabled by a falling edge of LATCH pin. Data is latched into the register on the rising edge of the LATCH pin. Data is clocked in on the rising edge of CLK when writing, and data is clocked out on the falling edge of CLK when reading.

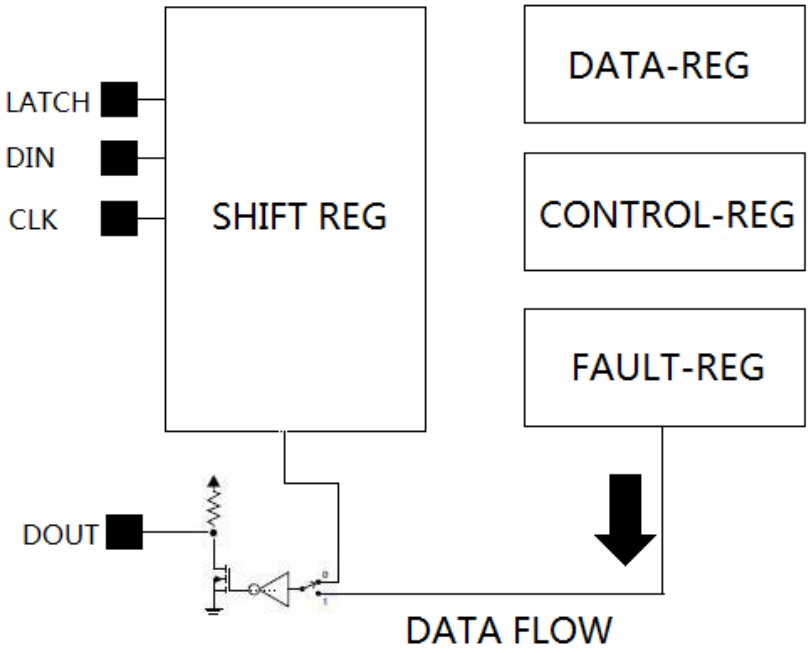
Data Writing Waveform





Fault Register Reading Waveform





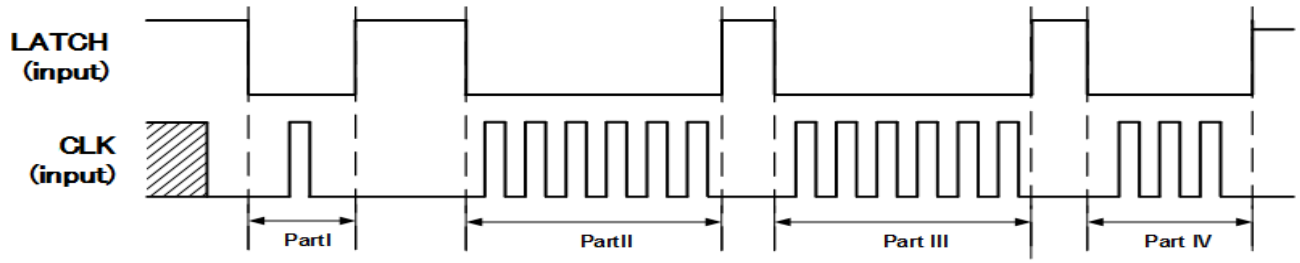
Special Command

Besides output ON/OFF control and fault status reading back, DRV8860 has special functions to make system more robust or power efficient. These functions will need special command to initiate the device or configure the internal registers.

There are 5 Special Commands:

1. Write Control Register command
2. Read Control Register command
3. Read Data Register command
4. Fault Register Reset command
5. PWM Start command

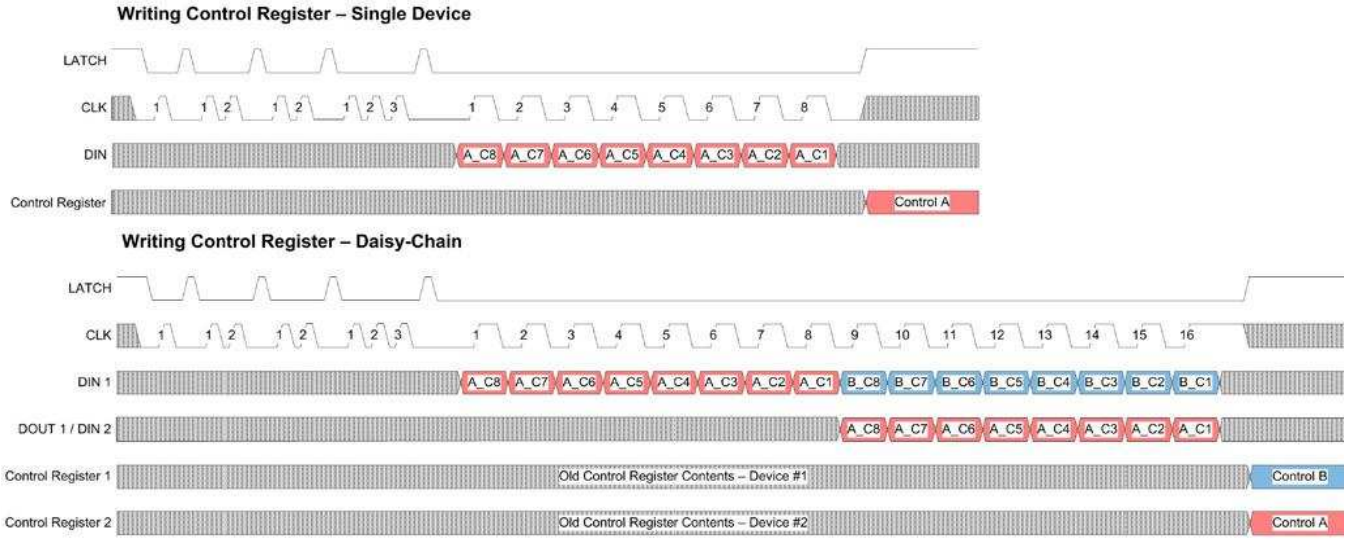
Special wave form pattern on CLK and LATCH pin will issue the special command, as below

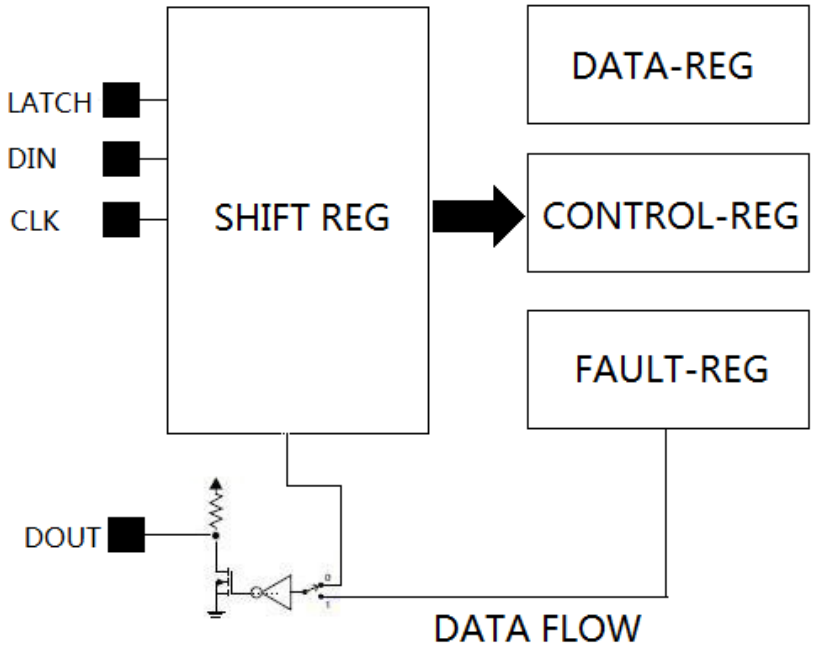


SPECIAL COMMAND	CLK CYCLES IN EACH PART			
	Part I	Part II	Part III	Part IV
Write Control Register	1	2	2	3
Read Control Register	1	4	2	3
Read Data Register	1	4	4	3
Fault Register Reset	1	2	4	3
PWM Start	1	6	6	3

Special command: Write Control Register

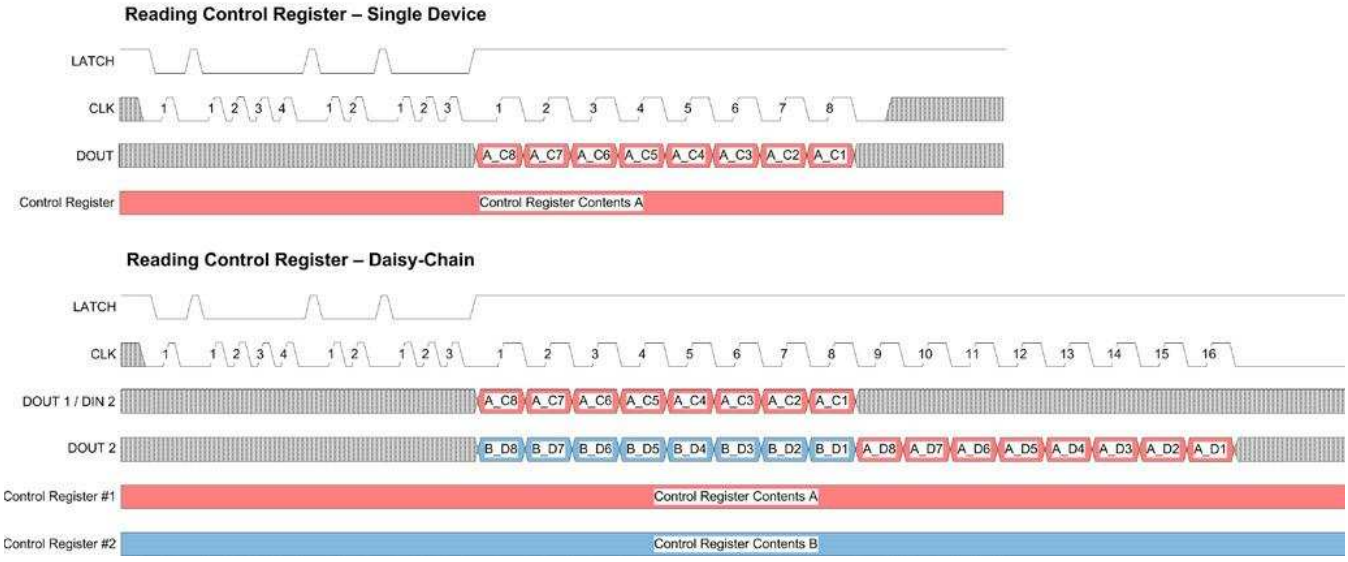
When Write-Control-Register command is issued, the following serial data will be latched into timing and duty control register.

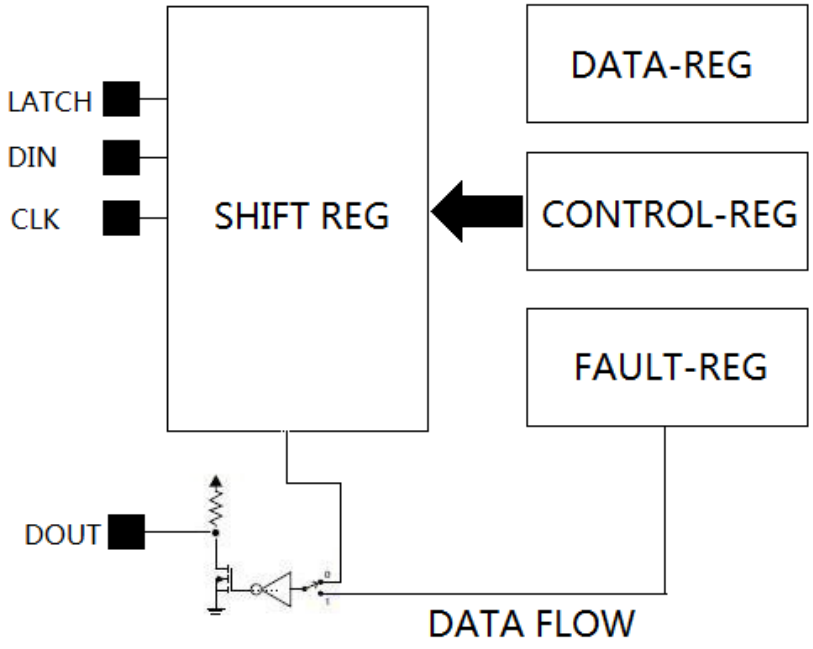




Special command: Read Control Register

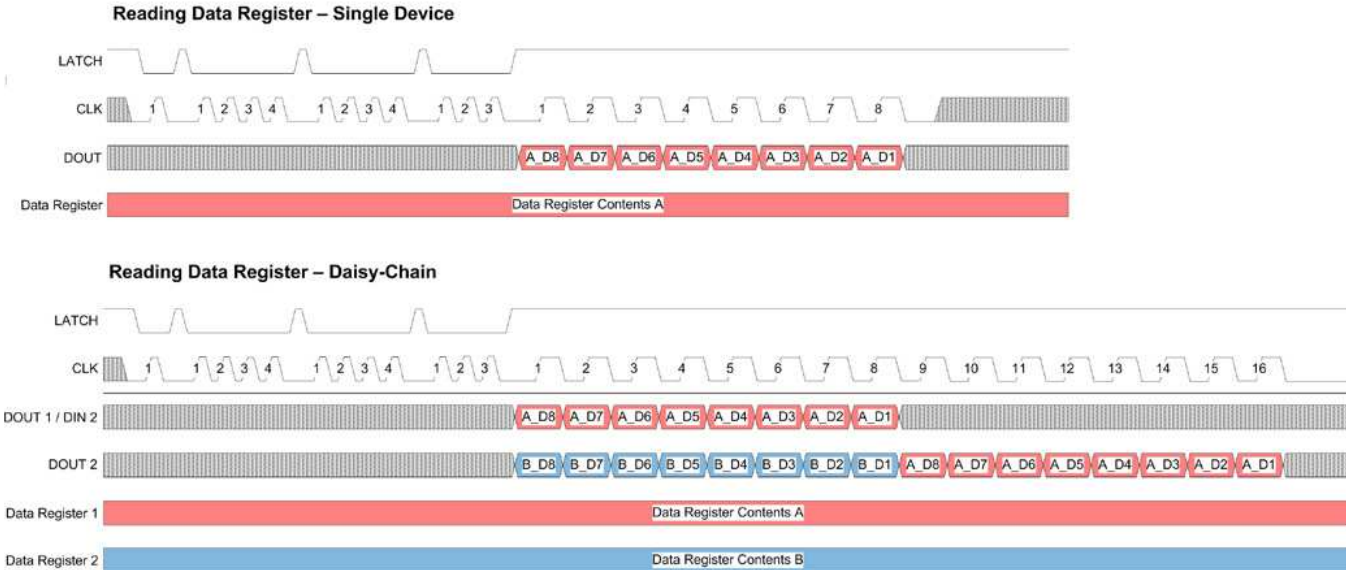
When Read-Control-Register command is issued, control register content will be copied to internal shift register and following CLK will shift this content out from DOUT pin. This provides a mechanism for system to verify the control register is correctly programmed.

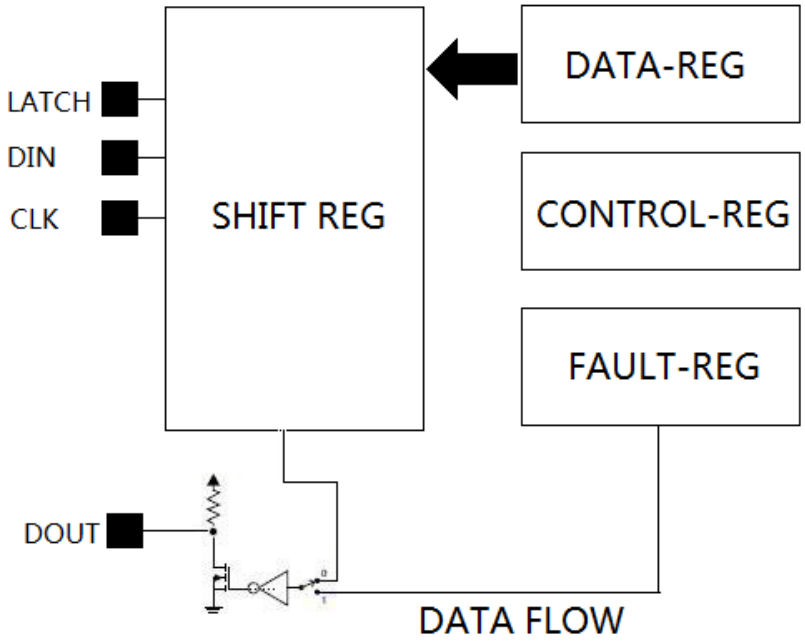




Special command: Read Data Register

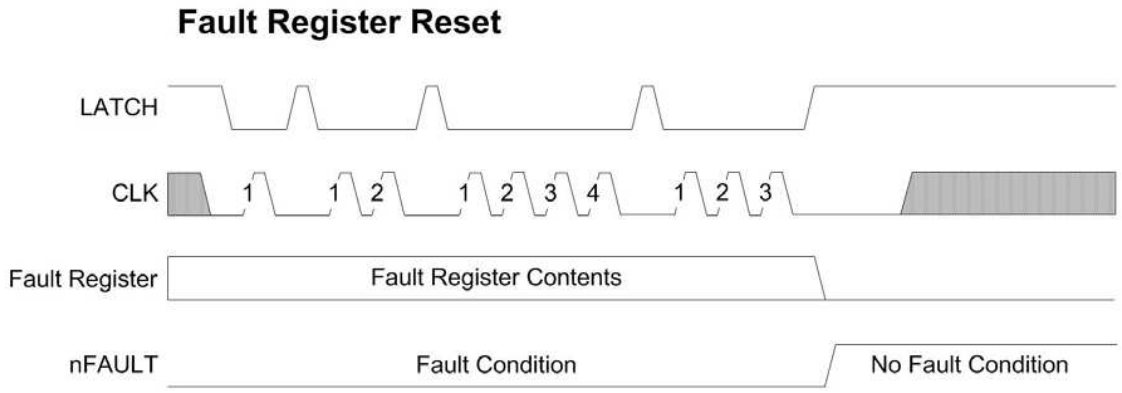
When Read-Data-Register command is issued, internal output data register content will be copied to internal shift register and following CLK will shift this content out from DOUT pin. This provides a mechanism for system to verify the output data is correctly programmed. It makes system more robust in noisy system.





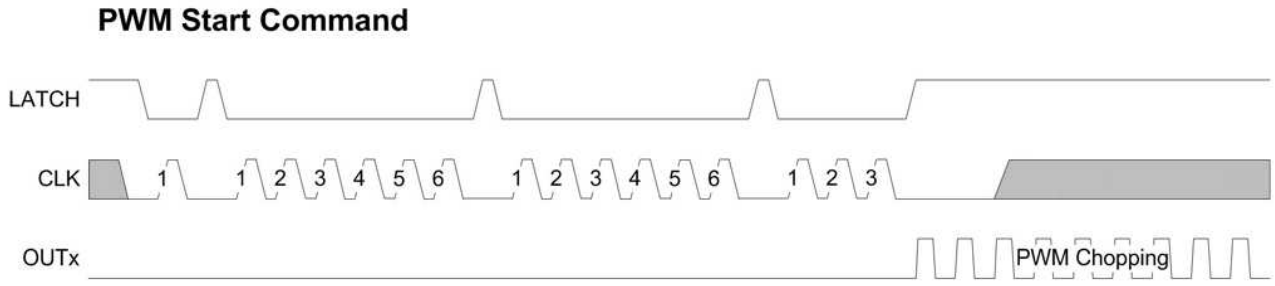
Special command: Fault Register Reset

When Fault-Register-Reset command is issued, internal 16bit fault register will be cleared. System can use this method to clear out all fault condition in every chained device at once.



Special command: PWM Start

When Fault-Register-Reset command is issued, output channel will ignore energizing time and directly enter into PWM mode following the setting in control register.



Output Energizing and PWM Control

The device output is defined by two stages: Energizing Phase and PWM Phase.

This special feature is designed to save energy and reduce heat for electromagnetic armature loads. It as well can be used to adjust average output voltage for resistance load.

During the Energizing phase, the channel is turned on with 100% duty cycle for a duration set by Control register bits C4:C1.

In PWM chopping phase, with the PWM Duty Cycle defined by Control register bits C7:C5.

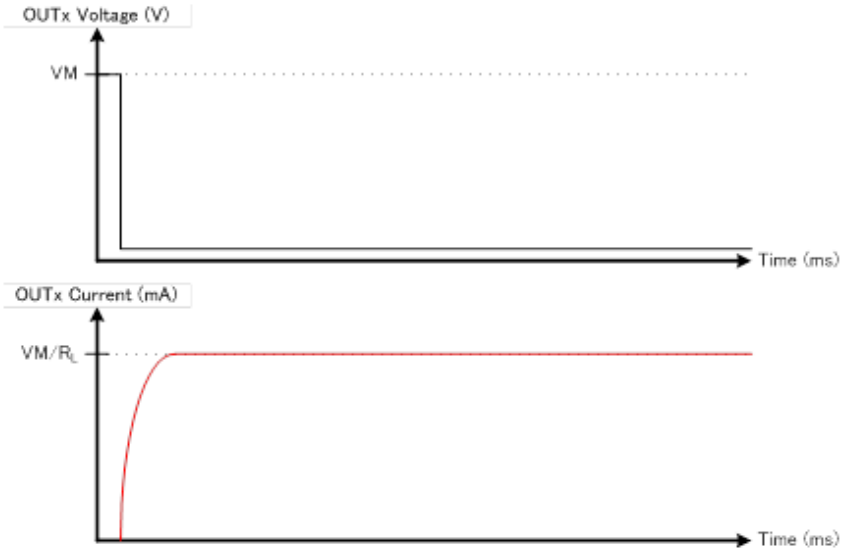
The behavior of each bit in the Control Register is described in the table below:

CONTROL REGISTER SETTINGS										
C8	**C7**	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**Value**	**DESCRIPTION**	
0	X	X	X	X	X	X	X	N/A	Outputs always in Energizing mode	
1	X	X	X	0	0	0	0	0 ms	No Energizing, starts in PWM chopping	
1	X	X	X	0	0	0	1	3 ms	Sets the Energizing Time (100% duty cycle) before switching to PWM Phase	
1	X	X	X	0	0	1	0	5 ms		
1	X	X	X	0	0	1	1	10 ms		
1	X	X	X	0	1	0	0	15 ms		
1	X	X	X	0	1	0	1	20 ms		
1	X	X	X	0	1	1	0	30 ms		
1	X	X	X	0	1	1	1	50 ms		
1	X	X	X	1	0	0	0	80 ms		
1	X	X	X	1	0	0	1	110 ms		
1	X	X	X	1	0	1	0	140 ms		
1	X	X	X	1	0	1	1	170 ms		
1	X	X	X	1	1	0	0	200 ms		
1	X	X	X	1	1	0	1	230 ms		
1	X	X	X	1	1	1	0	260 ms		
1	X	X	X	1	1	1	1	300 ms		
1	0	0	0	X	X	X	X	0%	Output is off after Energizing Phase	
1	0	0	1	X	X	X	X	12.50%	12.5 kHz	Sets PWM chopping duty cycle. DC is the duty cycle that the low-side FET is on.
1	0	1	0	X	X	X	X	25.00%	25 kHz	
1	0	1	1	X	X	X	X	37.50%	50 kHz	
1	1	0	0	X	X	X	X	50.00%		
1	1	0	1	X	X	X	X	62.50%		
1	1	1	0	X	X	X	X	75.00%		
1	1	1	1	X	X	X	X	87.50%		

Different operation cases with inductive load are described in following pages.

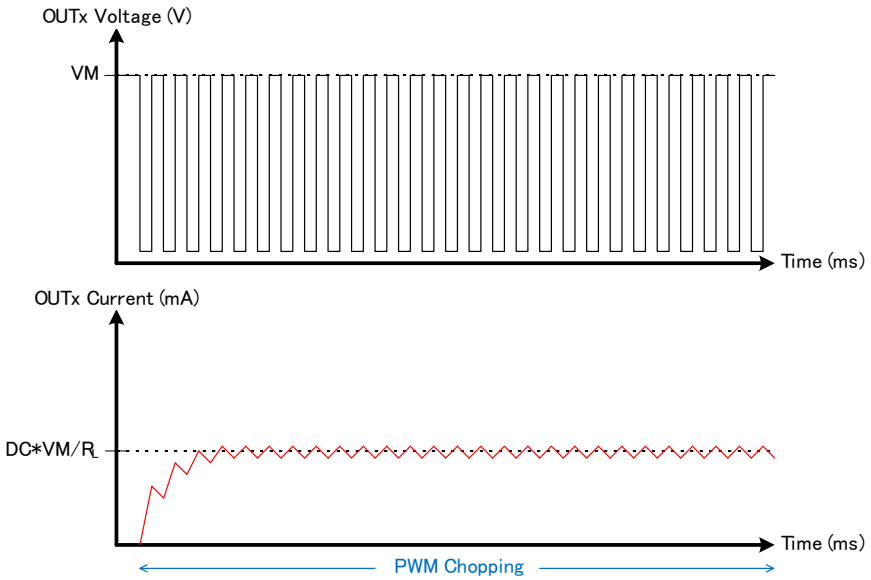
Case 1: Timer enable bit (C8) is 0 (Default value)

The output is turned on with 100% duty cycle.



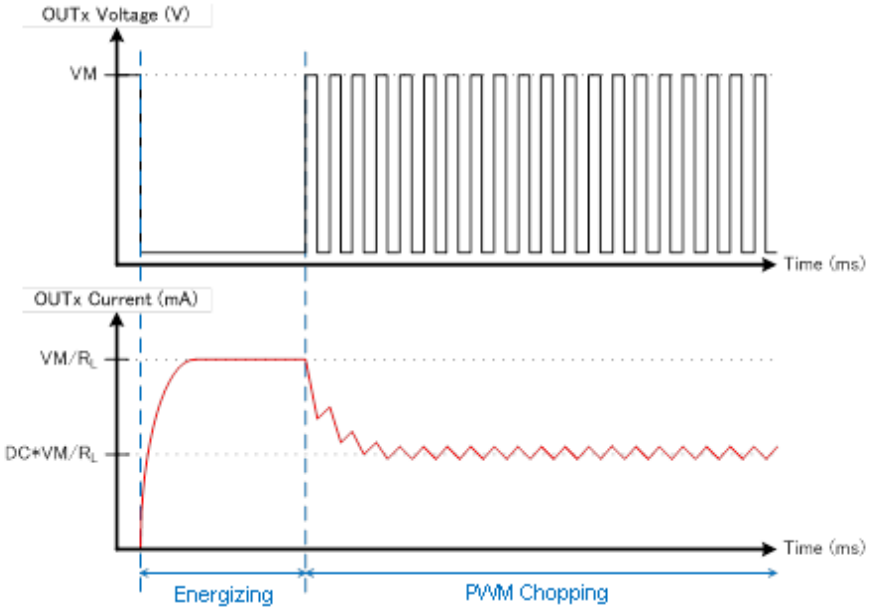
Case 2: Timer enable bit (C8) is 1 and Energizing Timing bits (C4:C1) are 0000

The output is turned on in PWM chopping mode with duty cycle defined by Control register bits C7:C5.



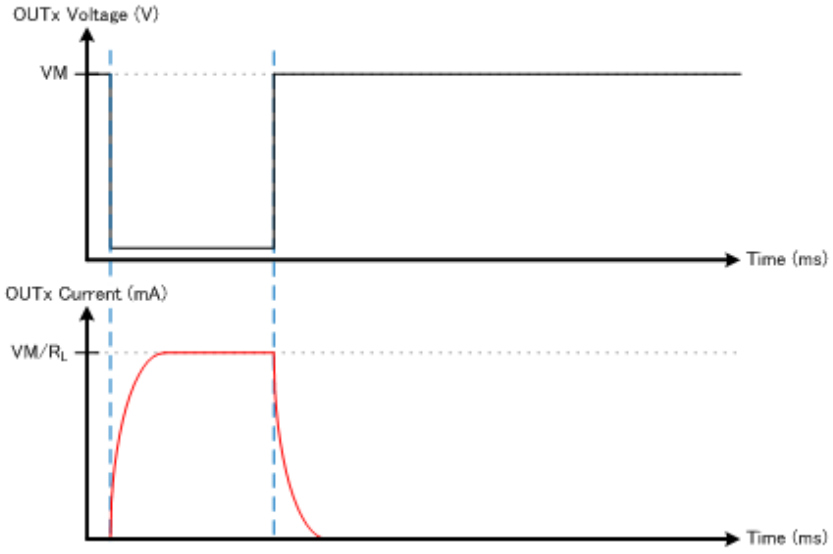
Case 3: Timer enable bit (C8) is 1, Energizing Timing bits (C4:C1) are NOT 0000, and PWM Duty bits (C7:C5) are NOT 000

The output is turned on in Energizing mode with 100% duty cycle for a duration set by Control register bits C4:C1. After the timer expires, the output switches to PWM chopping mode with PWM Duty Cycle defined by Control register bits C7:C5.



Case 4: Timer enable bit (C8) is 1, Energizing Timing bits (C4:C1) are NOT 0000, and PWM Duty bits (C7:C5) are 000

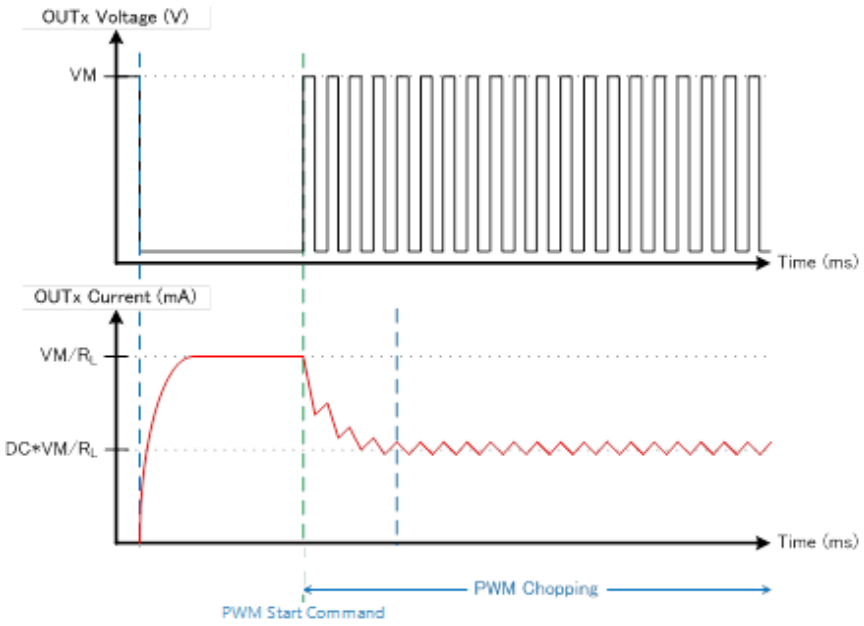
The output is turned on in Energizing mode with 100% duty cycle for a duration set by Control register bits C4:C1. After the timer expires, the output is turned off.



Case 5: Timer enable bit (C8) is 0, Energizing Timing bits (C4:C1) are NOT 0000, and PWM Duty bits (C7:C5) are NOT 000

PWM Start Special Command Used

The output is turned on in Energizing mode with 100% duty cycle, and a timer is enabled with duration set by Control register bits C4:C1. If the PWM Start special command is received before the timer expires, then the output switches to PWM chopping mode with PWM Duty Cycle defined by Control register bits C7:C5. If the timer expires and no PWM Start is received, then the device will stay in Energizing mode regardless of other PWM Start commands.



Protection Circuits

The DRV8860 is fully protected against undervoltage, overcurrent and overtemperature events.

Overcurrent Protection (OCP)

When output current exceeds OCP trigger level, corresponding channel will be automatically turned off. nFault pin will be set low and corresponding OCP flag in fault register will be set to 1.

Over current faults are automatically cleared whenever the corresponding output is turned off by setting the Data register bit to '0'. Alternatively, a Fault Reset special command will also clear this value. In either case, once all bits in the Fault register are clear, nFAULT is released.

Open Load Detection (OL)

When any output is in off status (the corresponding Data Register bit is set to '0'), a current sink pulls the node down with approximately 30 µA. If the voltage on the pin is sensed to be less than 1.2 V, then an open load condition is reported. nFAULT is driven low and the OL bit of the fault register (F8:F1) corresponding to the specific channel is set.

Open load faults are automatically cleared whenever the corresponding output is turned on by setting the Data register bit to '1'. Alternatively, a Fault Reset special command will also clear this value. In either case, once all bits in the Fault register are clear, nFAULT is released.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all outputs will be disabled, and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level, operation will automatically resume. The nFAULT pin will be released after operation has resumed.

Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled and internal logic will be reset. Operation will resume when VM rises above the UVLO threshold. nFAULT will not be asserted in this condition.

Digital Noise Filter

The DRV8860 features an internal noise filter on all digital inputs. In a noisy system, noise may disturb the serial daisy-chain interface. Without an input filter, this noise may result in an unexpected behavior or output state. The digital input filter is capable of removing unwanted noise frequencies while allowing fast communication over the serial interface.

REVISION HISTORY

Changes from Original (September 2013) to Revision A **Page**

- Added additional features. 1
- Updated MIN value for V_M in the Recommended Operating Conditions table. 4
- Added Example Output Configuration section. 9

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8860PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	8860	Samples
DRV8860PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	8860	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

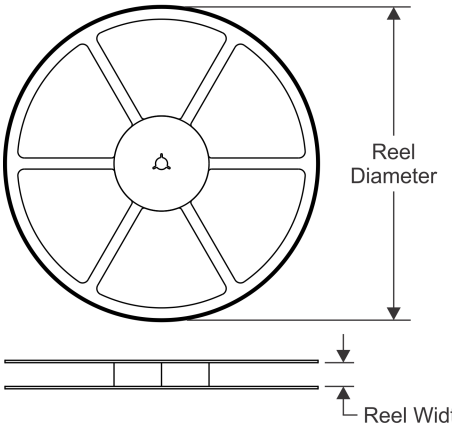
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

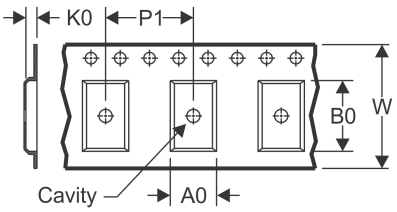
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

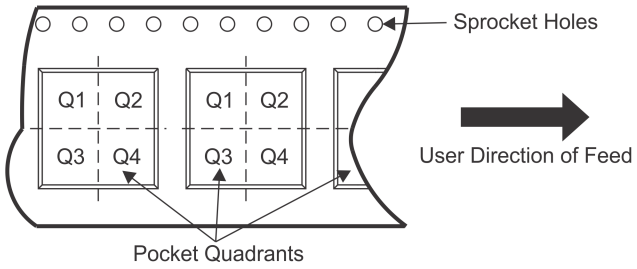


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

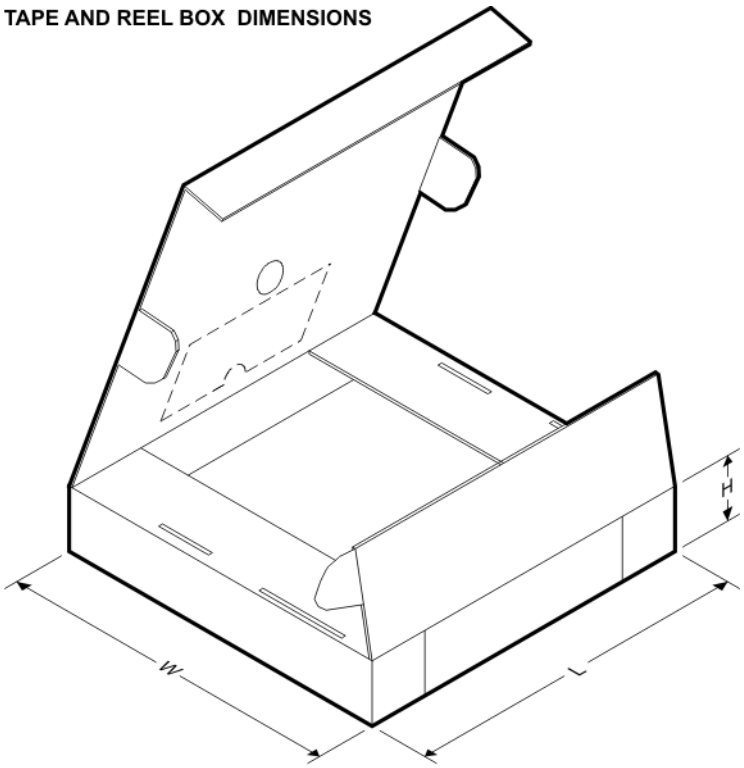
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8860PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

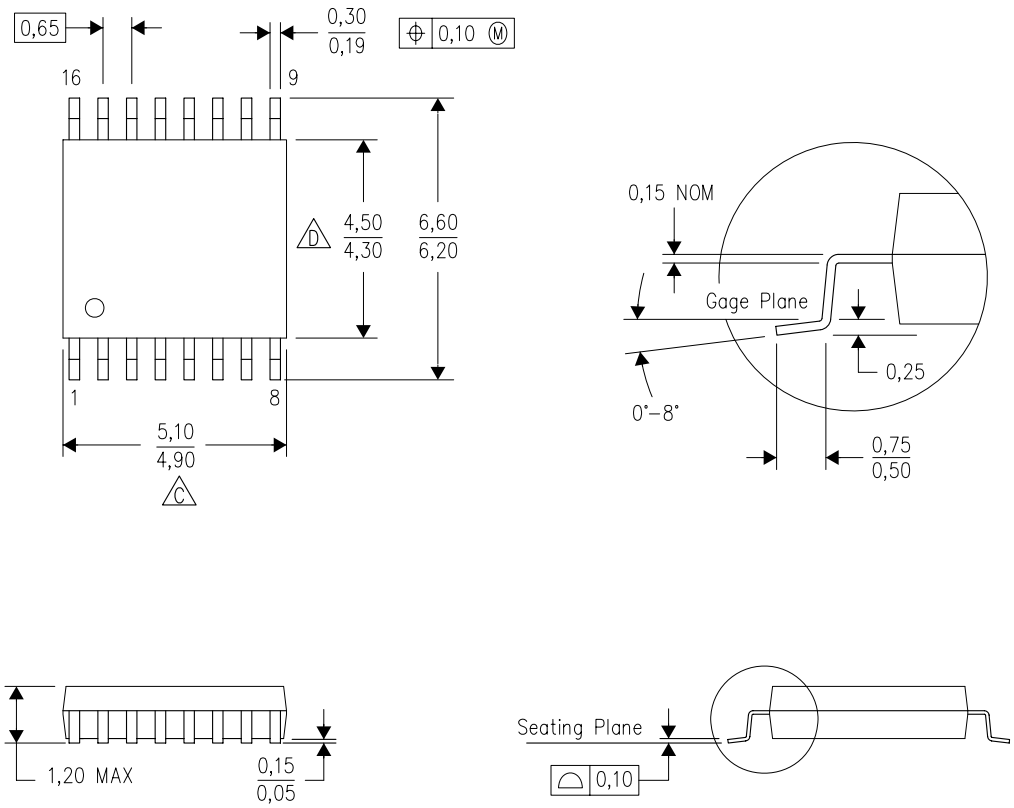
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8860PWR	TSSOP	PW	16	2000	367.0	367.0	35.0

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4040064–4/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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