Document Number: A2T21H410-24S
Rev. 0, 2/2016

RoHS

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 72 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 2110 to 2170 MHz.

2100 MHz

- Typical Doherty Single-Carrier W-CDMA Performance: V_{DD} = 28 Vdc, I_{DQA} = 600 mA, V_{GSB} = 0.4 Vdc, P_{out} = 72 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

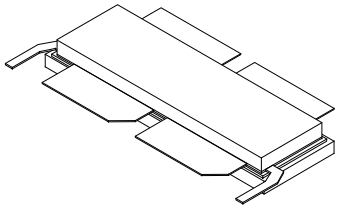
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
2110 MHz	15.7	49.1	7.9	–34.0
2140 MHz	15.7	49.0	7.8	–33.6
2170 MHz	15.6	48.9	7.6	–32.1

Features

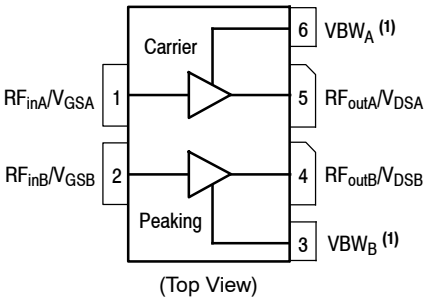
- Advanced High Performance In-Package Doherty
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems

A2T21H410-24SR6

2110–2170 MHz, 72 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR



NI-1230S-4L2L



(Top View)

Figure 1. Pin Connections

1. Device cannot operate with V_{DD} current supplied through pin 3 and pin 6.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C
CW Operation @ T_C = 25°C Derate above 25°C	CW	269 0.95	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 73°C, 72 W Avg., W-CDMA, 28 Vdc, I_{DQA} = 600 mA, V_{GSB} = 0.4 Vdc, 2140 MHz	$R_{\theta JC}$	0.24	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics (4)					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics - Side A, Carrier					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 160 μAdc)	$V_{GS(th)}$	1.2	1.2	2.4	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 600 mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	2.3	2.6	3.1	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.6 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc
On Characteristics - Side B, Peaking					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 270 μAdc)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.7 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com/RF/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.
4. Each side of device measured separately.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1,2) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 600 mA, V_{GSB} = 0.4 Vdc, P_{out} = 72 W Avg., f = 2170 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	14.8	15.6	17.8	dB
Drain Efficiency	η_D	44.0	48.9	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.8	7.6	—	dB
Adjacent Channel Power Ratio	ACPR	—	–32.1	–28.5	dBc
Load Mismatch (2) (In Freescale Doherty Test Fixture, 50 ohm system) I_{DQA} = 600 mA, V_{GSB} = 0.4 Vdc, f = 2140 MHz					
VSWR 10:1 at 32 Vdc, 331 W CW (3) Output Power (3 dB Input Overdrive from 316 W CW (3) Rated Power)	No Device Degradation				
Typical Performance (2) (In Freescale Doherty Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQA} = 600 mA, V_{GSB} = 0.4 Vdc, 2110–2170 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	316 (3)	—	W
P_{out} @ 3 dB Compression Point (4)	P3dB	—	447	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2110–2170 MHz bandwidth)	Φ	—	–5.9	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	90	—	MHz
Gain Flatness in 60 MHz Bandwidth @ P_{out} = 72 W Avg.	G_F	—	0.3	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.006	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C) (3)	ΔP1dB	—	0.008	—	dB/°C

Table 5. Ordering Information

Device	Tape and Reel Information	Package
A2T21H410-24SR6	R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel	NI-1230S-4L2L

1. Part internally matched both on input and output.
2. Measurements made with device in an asymmetrical Doherty configuration.
3. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.
4. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

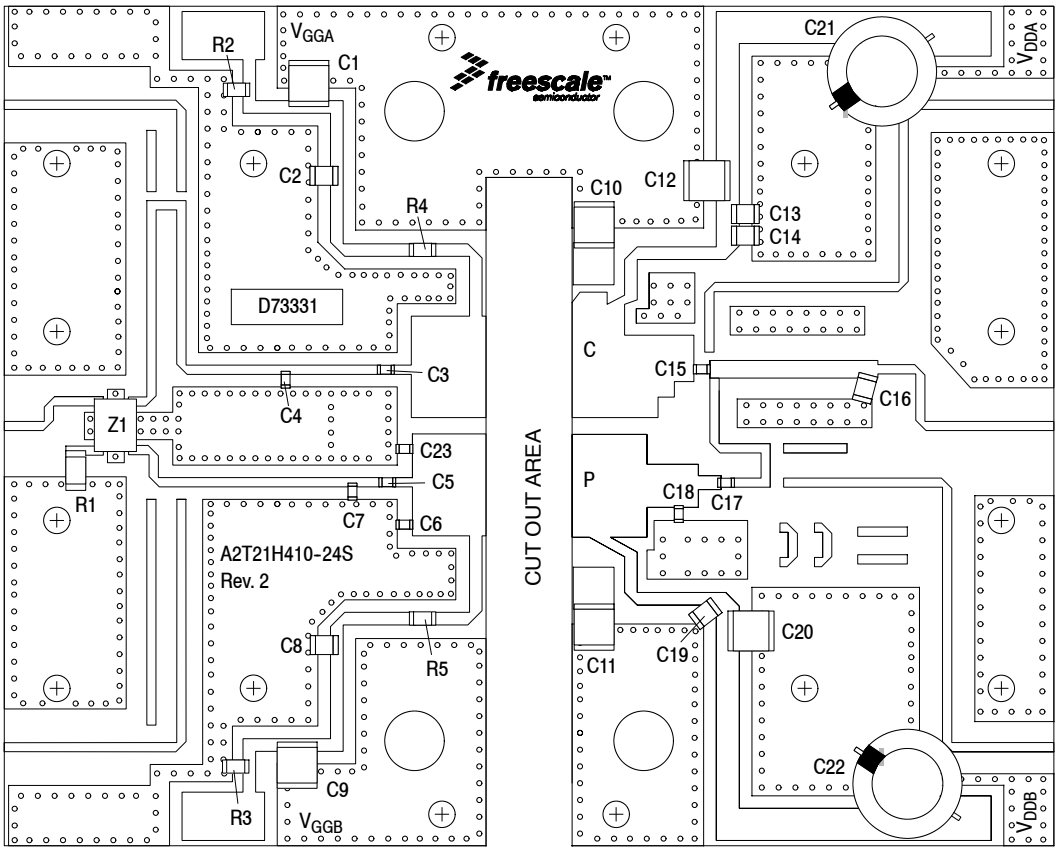


Figure 2. A2T21H410-24SR6 Test Circuit Component Layout

Table 6. A2T21H410-24SR6 Production Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C9, C10, C11, C12, C20	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C2, C8, C14, C19	9.1 pF Chip Capacitors	ATC100B9R1CT500XT	ATC
C3, C5, C17	9.1 pF Chip Capacitors	ATC600F9R1BT250XT	ATC
C4	1.1 pF Chip Capacitor	ATC600F1R1BT250XT	ATC
C6	0.5 pF Chip Capacitor	ATC600F0R5BT250XT	ATC
C7	0.7 pF Chip Capacitor	ATC600F0R7BT250XT	ATC
C13	0.8 pF Chip Capacitor	ATC100B0R8BT500XT	ATC
C15	4.7 pF Chip Capacitor	ATC600F4R7BT250XT	ATC
C16	0.3 pF Chip Capacitor	ATC100B0R3BT500XT	ATC
C18	0.7 pF Chip Capacitor	ATC600F0R7BT250XT	ATC
C21, C22	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
C23	0.6 pF Chip Capacitor	ATC600F0R6BT250XT	ATC
R1	50 Ω, 10 W Chip Resistor	C10A50Z4	Anaren
R2, R3	5.6 kΩ, 1/4 W Chip Resistors	CRCW12065K60FKEA	Vishay
R4, R5	6.2 Ω, 1/4 W Chip Resistors	CRCW12066R20FKEA	Vishay
Z1	2000–2300 MHz Band, 90°, 5 dB Directional Coupler	X3C21P1-05S	Anaren
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D73331	MTL

TYPICAL CHARACTERISTICS — 2110–2170 MHz

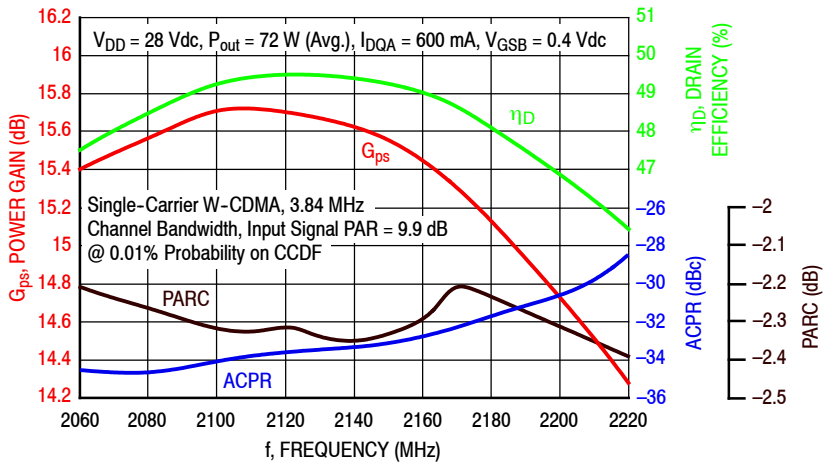


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 72 Watts Avg.

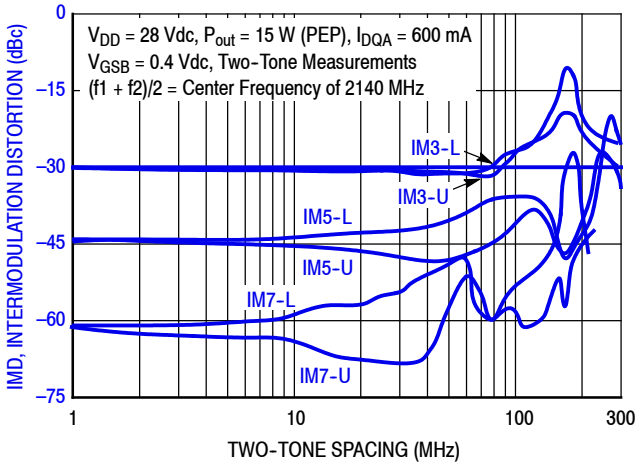


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

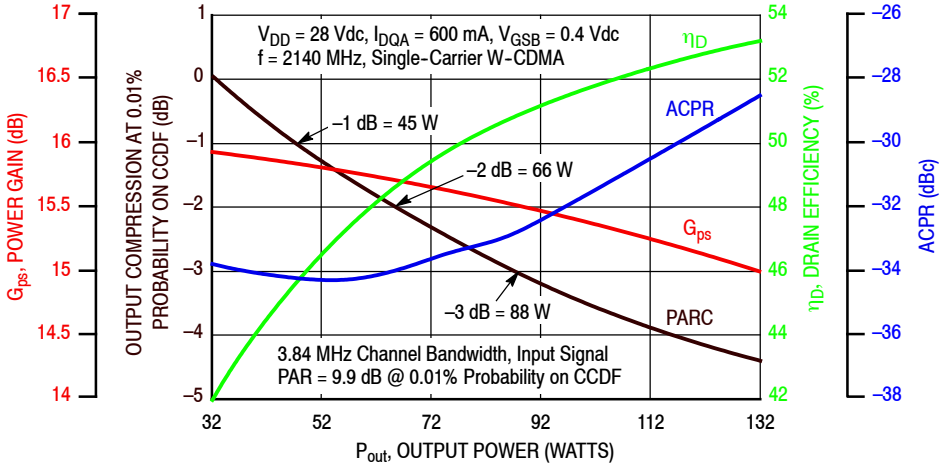


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 2110–2170 MHz

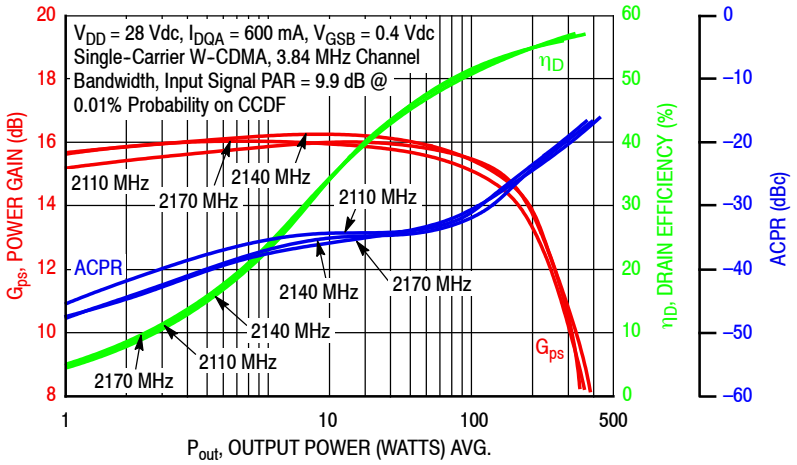


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

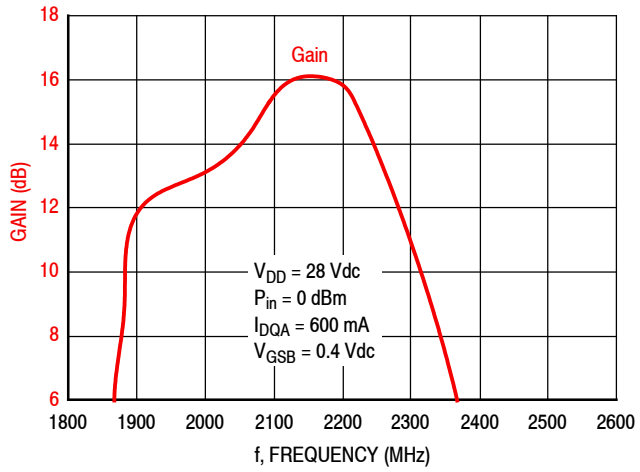


Figure 7. Broadband Frequency Response

Table 7. Carrier Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQA} = 793 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	3.30 – j6.14	3.02 + j4.76	1.35 – j4.14	18.6	52.7	186	56.7	–14
2140	4.34 – j6.54	3.93 + j4.80	1.37 – j4.16	18.6	52.4	175	54.5	–15
2170	5.86 – j6.79	5.32 + j4.64	1.38 – j3.97	19.0	52.5	176	55.9	–15

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	3.30 – j6.14	2.89 + j5.13	1.32 – j4.26	16.3	53.4	219	58.5	–16
2140	4.34 – j6.54	3.92 + j5.30	1.34 – j4.35	16.2	53.2	210	56.1	–17
2170	5.86 – j6.79	5.51 + j5.16	1.40 – j4.20	16.6	53.2	209	57.8	–18

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 8. Carrier Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ} = 793 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	3.30 – j6.14	3.88 + j5.00	2.93 – j3.33	21.6	50.8	121	67.6	–19
2140	4.34 – j6.54	4.86 + j4.65	2.71 – j3.46	21.1	50.9	124	64.7	–18
2170	5.86 – j6.79	6.35 + j3.90	2.65 – j3.16	21.4	50.7	118	64.9	–18

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	3.30 – j6.14	3.64 + j5.34	2.90 – j3.20	19.7	51.5	142	69.9	–25
2140	4.34 – j6.54	4.77 + j5.24	2.71 – j3.36	19.3	51.6	146	66.5	–23
2170	5.86 – j6.79	6.60 + j4.41	2.65 – j3.10	19.5	51.5	140	66.8	–24

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

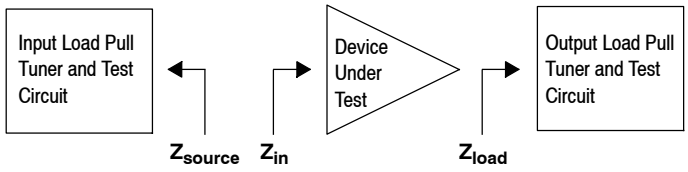


Table 9. Peaking Side Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, V_{GSB} = 0.4 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	2.03 – j5.13	1.94 + j5.32	1.29 – j4.13	15.1	55.2	328	55.2	–30
2140	2.71 – j5.57	2.54 + j5.76	1.32 – j4.16	15.1	55.0	319	53.8	–31
2170	3.89 – j5.89	3.46 + j6.28	1.33 – j4.13	15.1	55.0	318	54.1	–30

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	2.03 – j5.13	2.08 + j5.57	1.30 – j4.34	12.9	55.8	383	56.8	–36
2140	2.71 – j5.57	2.80 + j6.07	1.32 – j4.37	12.9	55.7	373	54.9	–37
2170	3.89 – j5.89	3.94 + j6.60	1.36 – j4.40	12.9	55.7	370	54.8	–36

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

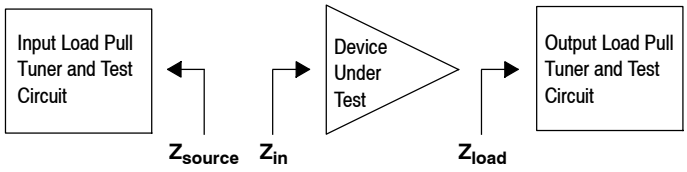
Table 10. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning

V_{DD} = 28 Vdc, V_{GSB} = 0.4 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	2.03 – j5.13	1.76 + j5.34	3.16 – j3.47	16.4	53.5	222	65.5	–37
2140	2.71 – j5.57	2.31 + j5.81	2.90 – j3.41	16.4	53.6	227	63.6	–37
2170	3.89 – j5.89	3.16 + j6.35	2.92 – j3.19	16.2	53.4	219	63.2	–37

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
2110	2.03 – j5.13	1.98 + j5.58	2.55 – j4.11	14.1	54.8	302	64.4	–42
2140	2.71 – j5.57	2.65 + j6.10	2.88 – j3.94	14.2	54.4	274	62.5	–43
2170	3.89 – j5.89	3.74 + j6.66	2.86 – j3.80	14.0	54.4	277	62.7	–43

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL CARRIER LOAD PULL CONTOURS — 2140 MHz

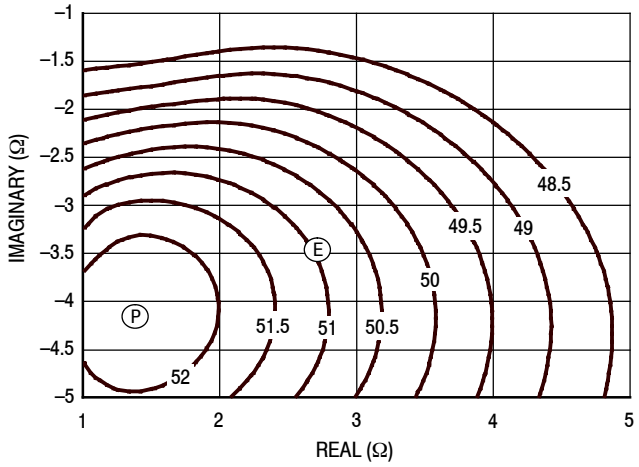


Figure 8. P1dB Load Pull Output Power Contours (dBm)

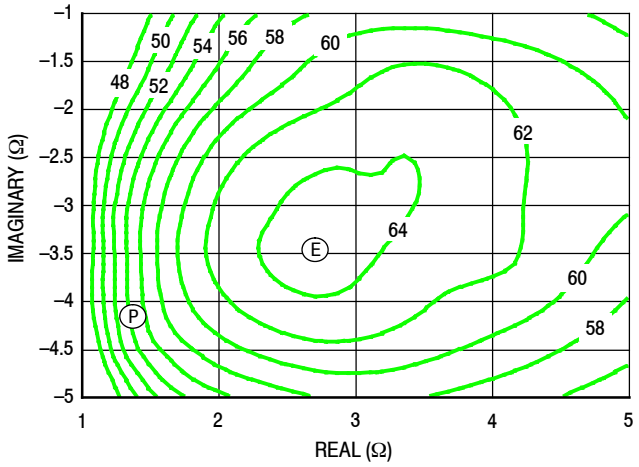


Figure 9. P1dB Load Pull Efficiency Contours (%)

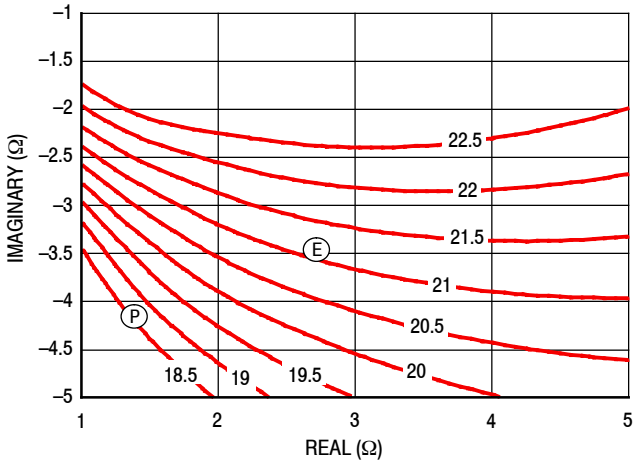


Figure 10. P1dB Load Pull Gain Contours (dB)

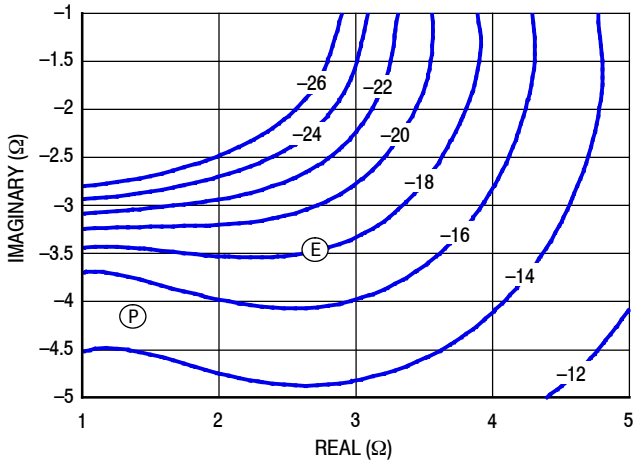


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL CARRIER LOAD PULL CONTOURS — 2140 MHz

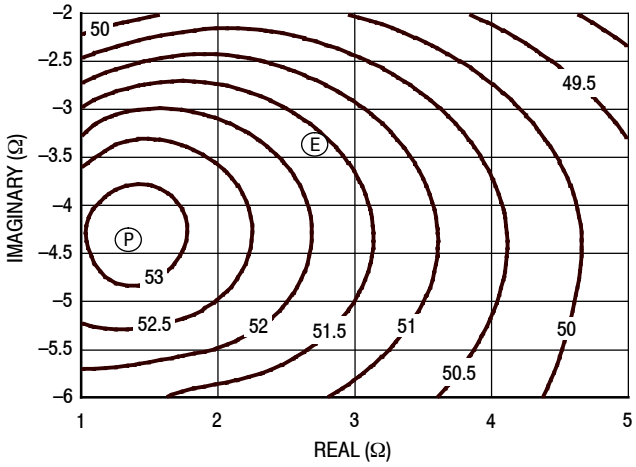


Figure 12. P3dB Load Pull Output Power Contours (dBm)

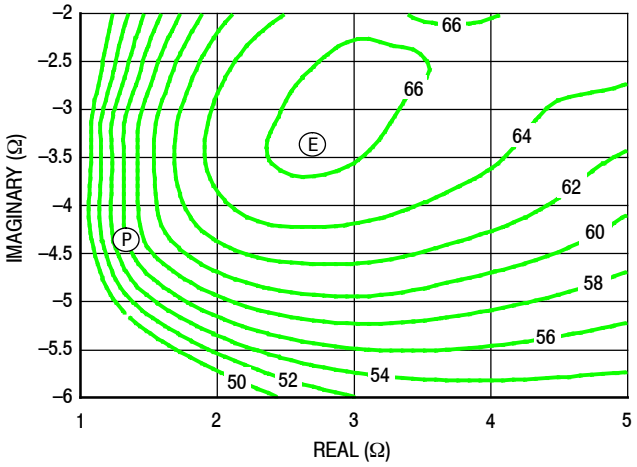


Figure 13. P3dB Load Pull Efficiency Contours (%)

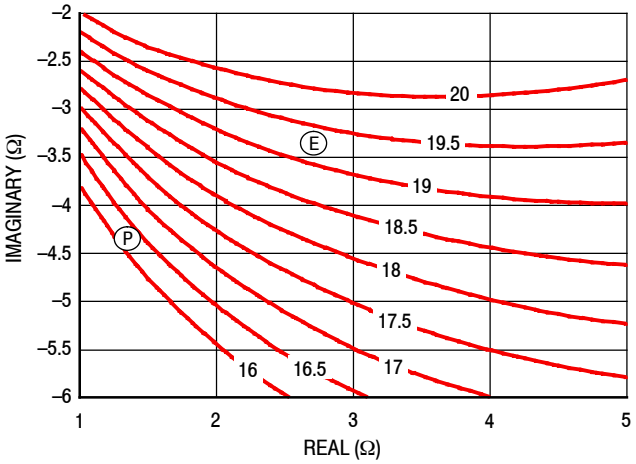


Figure 14. P3dB Load Pull Gain Contours (dB)

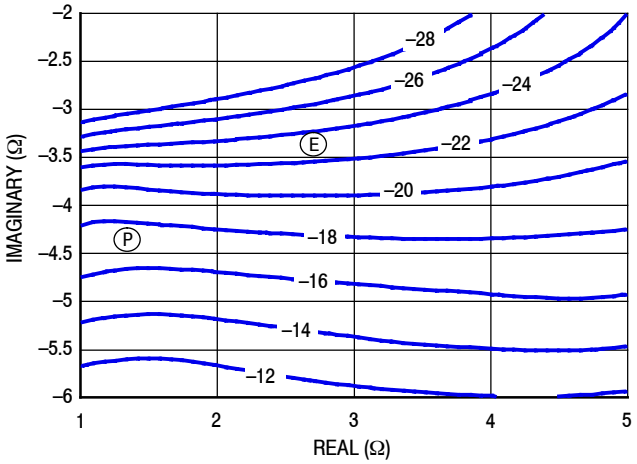


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P1dB – TYPICAL PEAKING LOAD PULL CONTOURS — 2140 MHz

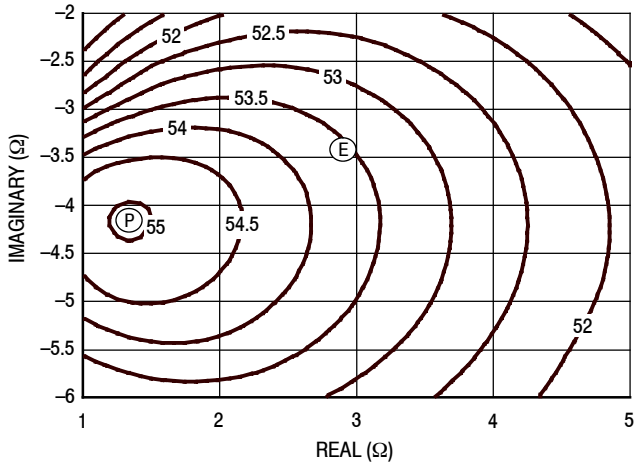


Figure 16. P1dB Load Pull Output Power Contours (dBm)

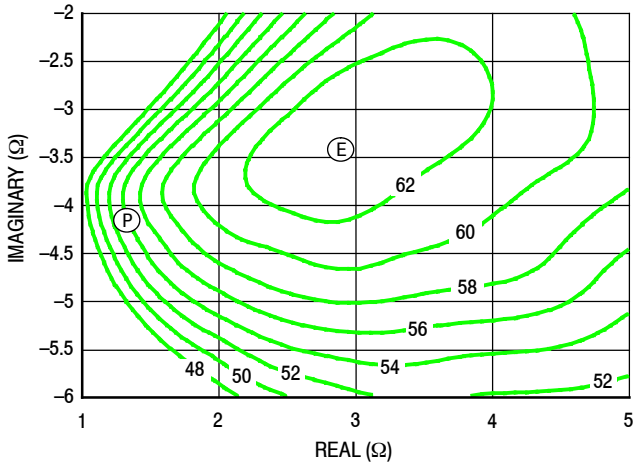


Figure 17. P1dB Load Pull Efficiency Contours (%)

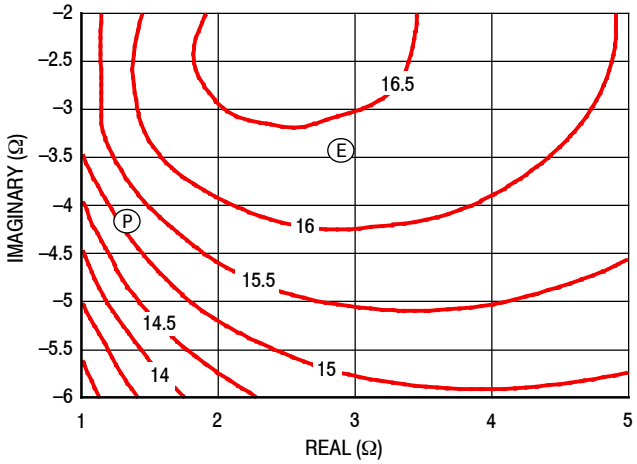


Figure 18. P1dB Load Pull Gain Contours (dB)

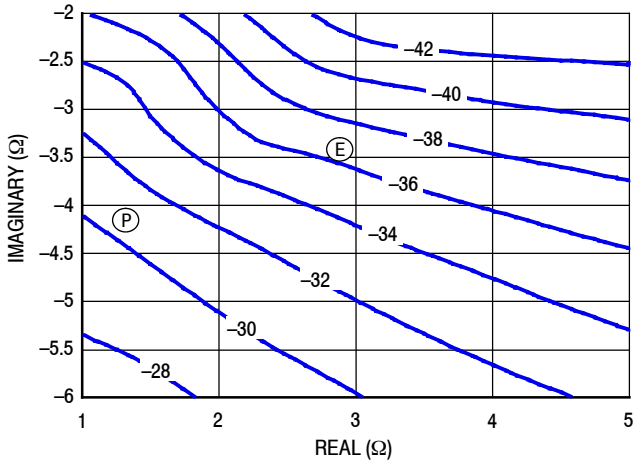


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL PEAKING LOAD PULL CONTOURS — 2140 MHz

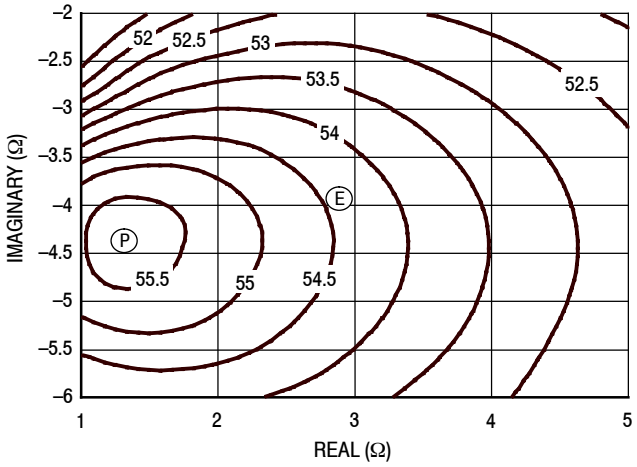


Figure 20. P3dB Load Pull Output Power Contours (dBm)

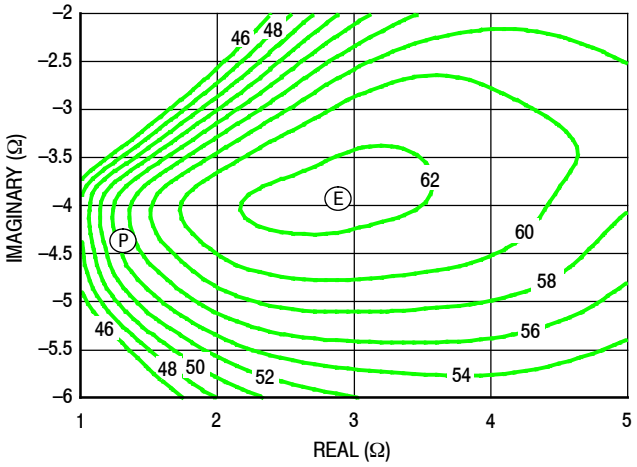


Figure 21. P3dB Load Pull Efficiency Contours (%)

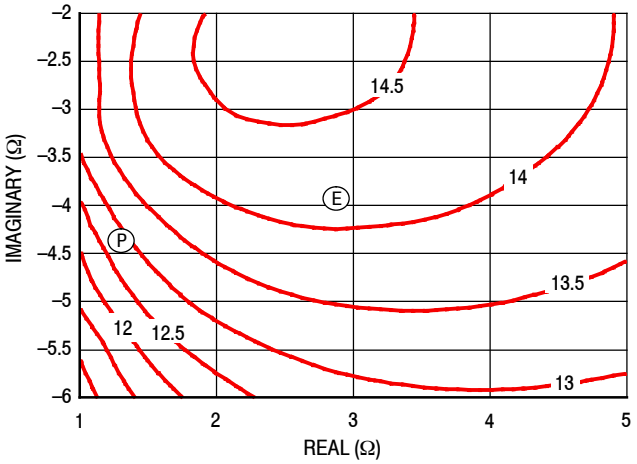


Figure 22. P3dB Load Pull Gain Contours (dB)

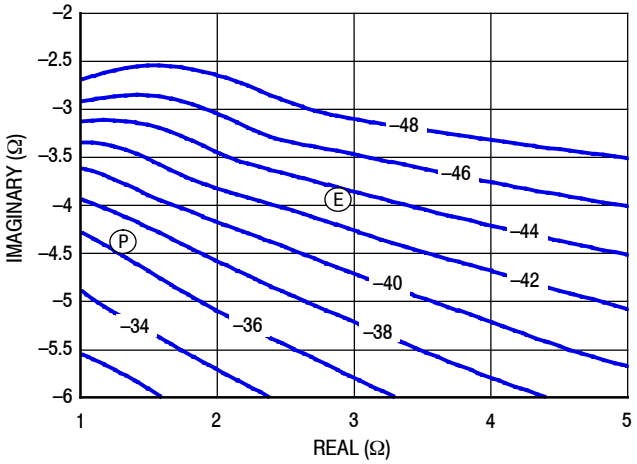
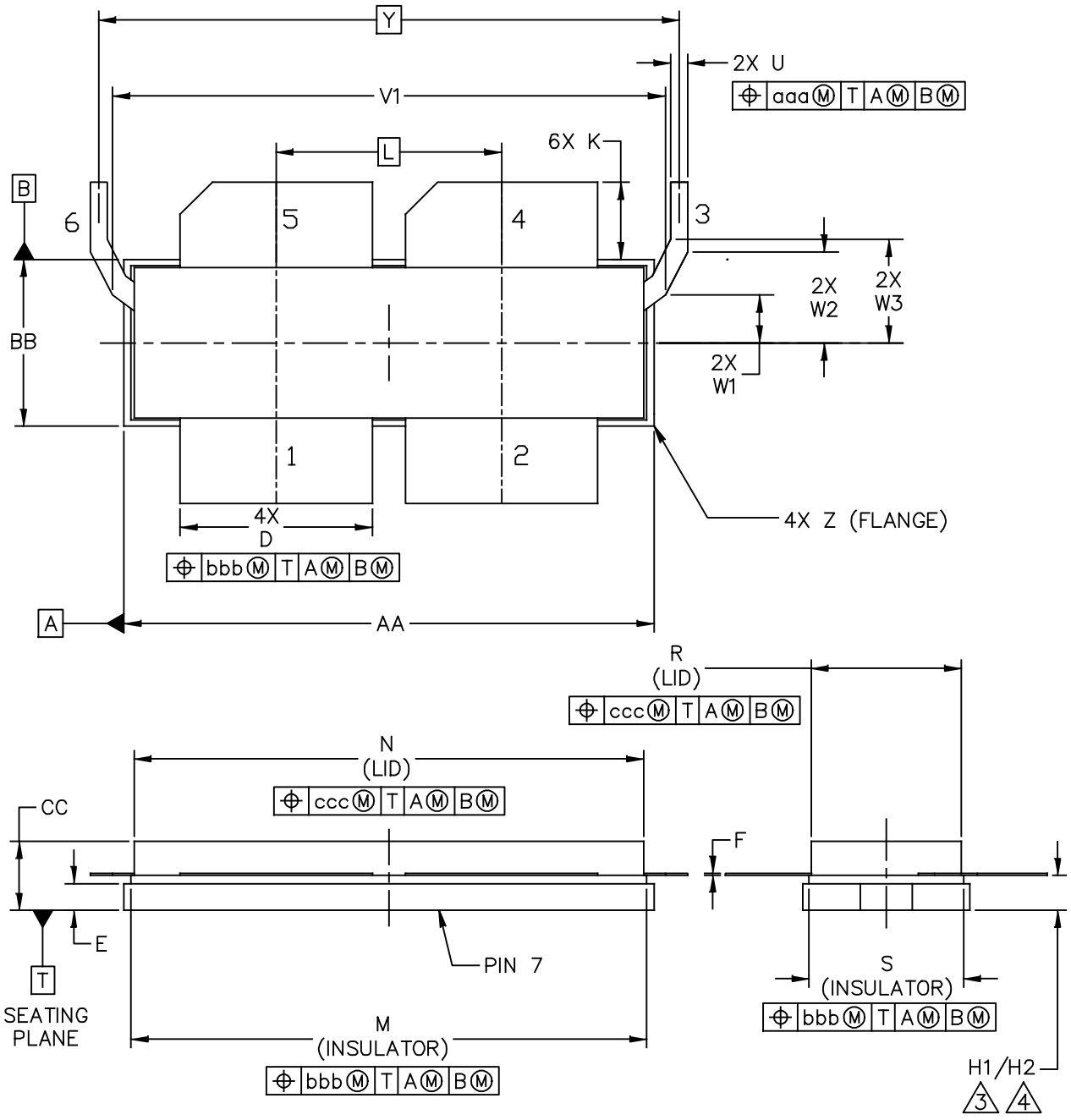


Figure 23. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

PACKAGE DIMENSIONS



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NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

2. CONTROLLING DIMENSION: INCH

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1, 2, 4 & 5. H2 APPLIES TO PINS 3 & 6.

4. TOLERANCE OF DIMENSION H2 IS TENTATIVE AND COULD CHANGE ONCE SUFFICIENT MANUFACTURING DATA IS AVAILABLE.

	INCH		MILLIMETER			INCH		MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	1.265	1.275	32.13	32.39	N	1.218	1.242	30.94	31.55
BB	.395	.405	10.03	10.29	R	.365	.375	9.27	9.53
CC	.170	.190	4.32	4.83	S	.365	.375	9.27	9.53
D	.455	.465	11.56	11.81	U	.035	.045	0.89	1.14
E	.062	.066	1.57	1.68	V1	1.320	1.330	33.53	33.78
F	.004	.007	0.10	0.18	W1	.110	.120	2.79	3.05
H1	.082	.090	2.08	2.29	W2	.213	.223	5.41	5.66
H2	.078	.094	1.98	2.39	W3	.243	.253	6.17	6.43
K	.175	.195	4.45	4.95	Y	1.390 BSC		35.31 BSC	
L	.540 BSC		13.72 BSC		Z	R.000	R.040	R0.00	R1.02
M	1.219	1.241	30.96	31.52	aaa	.015		0.38	
					bbb	.010		0.25	
					ccc	.020		0.51	

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Feb. 2016	• Initial Release of Data Sheet

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