2/1-Phase PWM Controller with SVID for VR12.5

General Description

The uP1651Q is a VR12.5 compliant PWM controller that surpports 2/1-phase operation. This device integrates 2 MOSFET gate drivers with embedded bootstrap diode to minimize external component count. To comply with VR12.5 specification, the uP1651Q accurately reports output current and VR temperature.

The uP1651Q provides programmable 2/1 phase operation. uP1651Q integrates 2 bootstrapped drivers that support 12V + 12V driving capability. 2/1 phase operation is enabled by a logic level ISENx output, achieving optimal balance between cost and flexibility.

The uP1651Q supports automatic phase adding/dropping that is activated by PSI command from SVID or H/W PSI setting. The uP1651Q operates in diode emulation mode at extreme light load condition, yielding maximum efficiency over entire load current range.

Other features include adjustable soft start, under/over voltage protection, over current protection and thermal shutdown. The uP1651Q is available in WQFN4x4-32L.

Ordering Information

Order Number	Package Type	Top Marking
uP1651QQKI	WQFN4x4-32L	uP1651Q

Note:
(1) Please check the sample/production availability with uPI representatives.
(2) uPI products are compatible with the current IPC/ JEDEC J-STD-020 requirement. They are halogen-free, RoHS compliant and 100% matte tin (Sn) plating that are suitable for use in SnPb or Pb-free soldering processes.

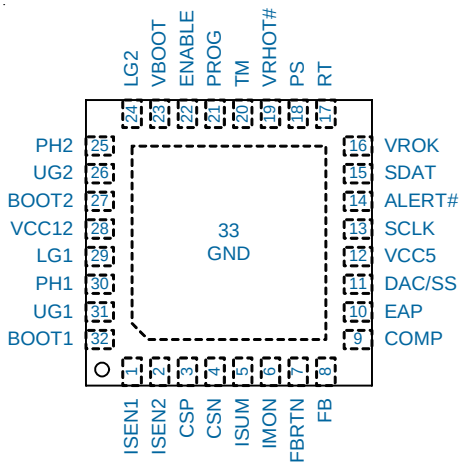
Applications

- **Desktop PC Core Power Supplies**

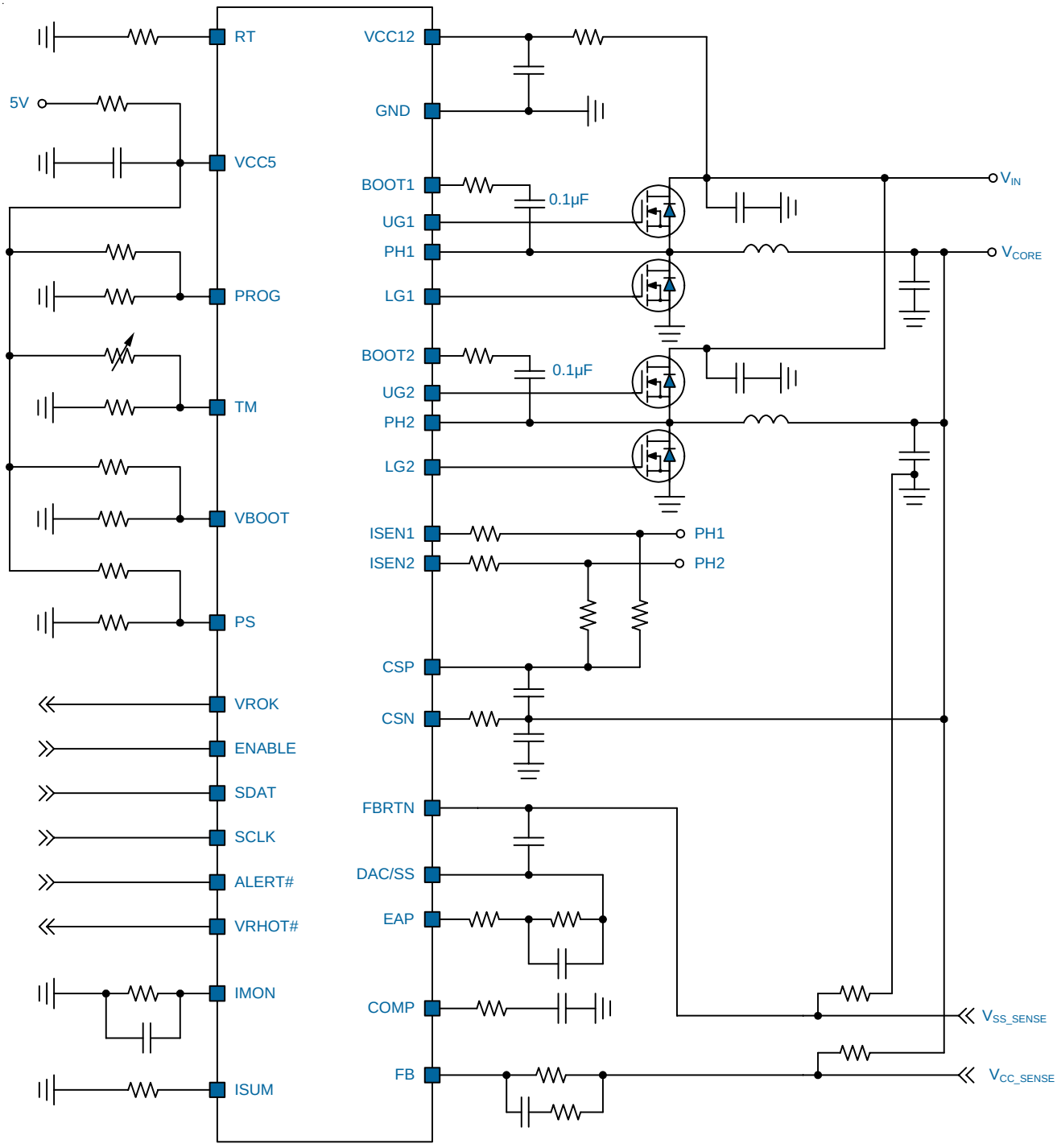
Features

- **Intel VR12.5 Compliant**
  - **Output Current and Thermal Reporting**
  - **Programmable ICCMAX,VBOOT**
- **RCOT™ Control Topology**
  - **Easy Setting**
  - **Smooth Mode Transition**
  - **Fast Transient Response**
- **Selectable 2/1-Phase Operation**
- **Differential Remote Voltage Sensing**
- **2 Embedded 12V MOSFET Gate Drivers with Integrated Bootstrap Diode**
- **Summed DCR Current Sensing for Load Line Setting**
- **Lower MOSFET $R_{DS(ON)}$ Current Sensing for Current Balance and Channel OCP**
- **Programmable Auto Phase Reduction per Load Current**
- **OCP/OVP/UVP/OTP**
- **Adjustable Soft-Start**
- **Support Pre-Biased Start Up**
- **RoHS Compliant and Halogen Free**

Pin Configuration



Typical Application Circuit



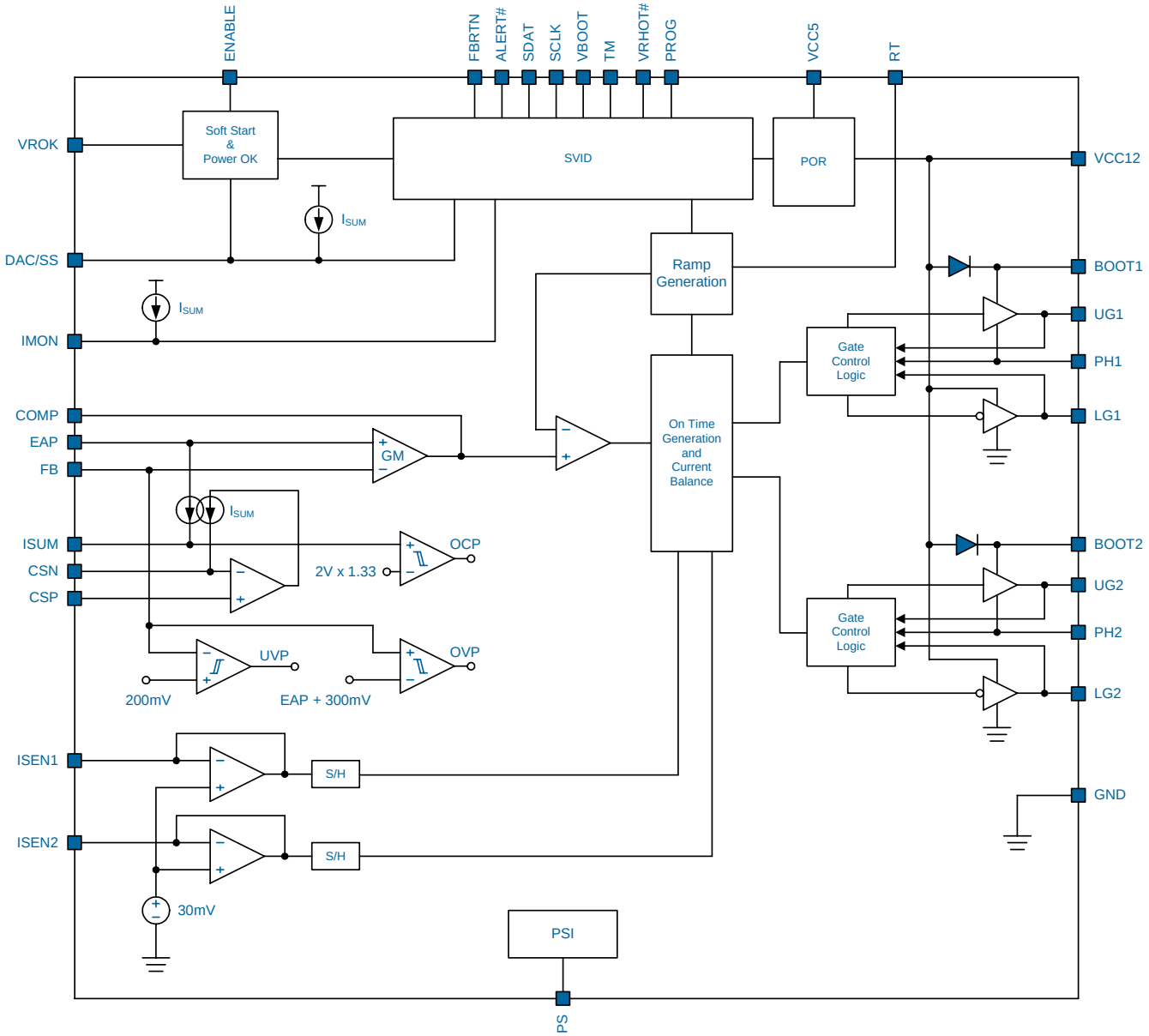
Functional Pin Description

No.	Name	Pin Function
1	ISEN1	**Current Sensing for Phase 1.** Connect a resistor from this pin to phase 1 switching node for current sensing.
2	ISEN2	**Current Sensing for Phase 2.** Connect a resistor from this pin to phase 2 switching node for current sensing.
3	CSP	**V_{CORE} Total Current Sense Positive Input.**
4	CSN	**V_{CORE} Total Current Sense Negative Input.**
5	ISUM	**V_{CORE} Output Current Indication.** Output current of ISUM pin is proportional to total load current. Connect a resistor between ISUM and GND then the voltage of ISUM is proportional to total load current. When ISUM is equal to 2V, it will trigger ICCMax Alert# of SVID. The ISUM voltage is also used for over current protection. Avoid add any capacitor to this pin.
6	IMON	**Output Current Monitor Pin.** The output current of IMON pin is proportional to the total load current. Connect a resistor from this pin to GND. The IMON voltage is decoded by ADC for current reporting. A capacitor may be added to this pin to adjust the response time of current reporting.
7	FBRTN	**V_{CORE} Feedback Return.** V_{CORE} VID DAC and error amplifier reference for remote sensing of the output voltage.
8	FB	**V_{CORE} Feedback Pin.** Error amplifier inverting input for remote sensing of the V_{CORE} output voltage.
9	COMP	**V_{CORE} Compensation Output.** Error amplifier output and compensation point.
10	EAP	**Non-Inverting Input of the Error Amplifier.** A resistor between EAP and the DAC/SS sets the load line.
11	DAC/SS	**V_{CORE} DAC Output.** Connect a capacitor from this pin to FBRTN to program the slew rate during soft start and dynamic VID transition.
12	VCC5	**Supply Input.** This pin supplies voltage for logic control circuit.
13	SCLK	**SVID Clock Pin.**
14	ALERT#	**SVID Alert# Pin.**
15	SDAT	**SVID Data Pin.**
16	VROK	**V_{CORE} Power Good Indication.** This pin is an open-drain output that indicates the soft start process is complete and no fault happens.
17	RT	**PWM On Time Setting.** Connect a resistor from this pin to GND to set the PWM on time.
18	PS	**Power Saving Mode Setting Input.** Connect a resistor voltage divider from VCC5 to GND to set the phase reduction threshold level.
19	VRHOT#	**VRHOT# Output.** This pin is an open-drain output. When the V_{TM} reaches the level that the decoded temperature reaches TEMPMAX (64h), it will trigger VRHOT#. Connect NTC network to this pin for sensing VR temperature. uP1651Q uses specific nonlinear A/D converter in thermal reporting. The recommended NTC thermistor is 10K, and the recommended lower dividing resistor is 6kΩ.
20	TM	**Thermal Monitoring.** Connect NTC network to this pin for V_{CORE} thermal monitoring.

Functional Pin Description

No.	Name	Pin Function
21	PROG	**Function Programming Pin.** This pin sets the platform maximum supported current ICCMAX. Connect a resistor voltage divider from VCC5 to GND to set the ICCMAX value.
22	ENABLE	**Chip Enable.** Voltage of this pin higher than 0.7V enables the controller. Lower than 0.3V disables the controller. It is recommended to use this pin to detect whether MOSFET driver power supply is ready.
23	VBOOT	**Function Programming Pin.** This pin sets two parameters: the initial start up voltage (Vboot) and the over current protection ratio. Connect a resistor voltage divider from VCC5 to GND to set the two parameters.
24	LG2	**Lower Gate Driver for Phase 2.** Connect this pin to the gate of phase 2 lower MOSFET.
25	PH2	**Phase Pin for Phase 2.** This pin is the return path of upper gate driver for phase 2. Connect a capacitor from this pin to BOOT2 to form a bootstrap circuit for upper gate driver of the phase 2.
26	UG2	**Upper Gate Driver for Phase 2.** Connect this pin to the gate of phase 2 upper MOSFET.
27	BOOT2	**BOOT for Phase 2.** Connect a capacitor from this pin to PH2 to form a bootstrap circuit for upper gate driver of the phase 2.
28	VCC12	**Supply Input.** This pin supplies current for gate drivers.
29	LG1	**Lower Gate Driver for Phase 1.** Connect this pin to the gate of phase 1 lower MOSFET.
30	PH1	**Phase Pin for Phase 1.** This pin is the return path of upper gate driver for phase 1. Connect a capacitor from this pin to BOOT1 to form a bootstrap circuit for upper gate driver of the phase 1.
31	UG1	**Upper Gate Driver for Phase 1.** Connect this pin to the gate of phase 1 upper MOSFET.
32	BOOT1	**BOOT for Phase 1.** Connect a capacitor from this pin to PH1 to form a bootstrap circuit for upper gate driver of the phase 1.
Exposed Pad		**Ground.** The exposed pad must be soldered to a large PCB and connected to GND.

Functional Block Diagram



Functional Description

The uP1651Q is a VR12.5 compliant PWM controller that supports 2/1-phase operation. This device integrates 2 MOSFET gate drivers with embedded bootstrap to minimize external component count.

Power Ready Detection

Figure 1 shows the power ready detection of the uP1651Q. The uP1651Q continuously monitors VCC5, ENABLE and VCC12 voltages to ensure all power voltages are ready for normal operation of logic control circuit and companion gate drivers. The VCC5 POR threshold level is VCC5 > 4.3V at the respective rising edge. When VCC5 POR = Low, the uP1651Q sets all gate drivers to turn off both high side and low side MOSFETs.

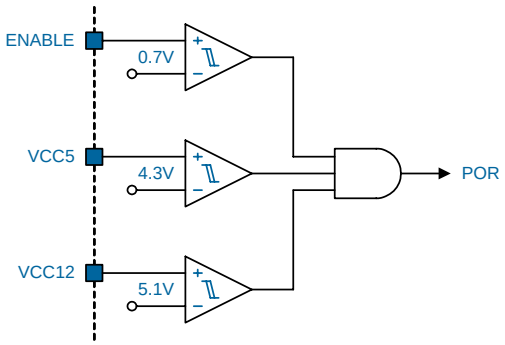


Figure1. Circuit for Power Ready Detection

Operation Phase Selection

The uP1651Q controller supports 2/1-phase operation. The phase number of operation is set and latched by the status of ISEN2 pin at POR rising edge. Normally, the controller operates as a 2-phase PWM controller. Pull ISEN2 to VCC5 for 1-phase operation.

Initial Parameters Setting

The PROG and VBOOT pins set the parameters required for VR12.5 as shown in Figure 2.

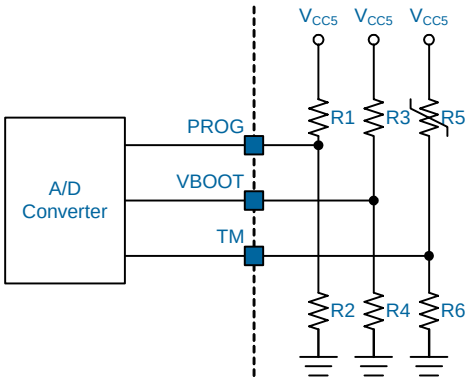


Figure 2. Initial Parameter Setting

The PROG pin is used for ICCMAX setting. The ICCMAX is the maximum supported output current of the VR, this value is stored in SVID register 0x21h.

The ADC scales one-fourth of VCC5 (0V to VCC5/4) into 256 levels for ICCMAX setting (SVID register 0x21h). The ratio of PROG pin voltage to VCC determines the SVID register 0x21h value, which means (VCC5/1024) equals 1A. If the PROG pin voltage is equal to or greater than (VCC5/4), the SVID register 0x21h value will be FFh. When VCC5 = 5V, the LSB = 1.25V / 256 = 4.9mV, which means 4.9mV applied to PROG pin equals to 1A setting. For example, if the maximum level of current is 50A, the PROG pin voltage should be 4.9mV x 50 = 0.245V.

Note that the ICCMAX setting is dependent on VCC5 voltage (it tracks VCC5 voltage). Therefore, make sure to use resistor voltage divider for ICCMAX setting as shown in Table 1.

Table 1. ICCMAX Setting

V_{PROG} = % of VCC	ICCMAX (A)
3.92%	40
4.90%	50
5.88%	60
6.86%	70
7.84%	80
8.82%	90
9.80%	100
10.78%	110

Functional Description

The VBOOT pin is used for initial start up voltage Vboot and OCP ratio setting. Connect a resistor voltage divider from VCC5 to GND to set the two parameters. The recommended resistance value is shown in Table 2.

Table 2. Boot Voltage and OCP Ratio Setting

R3 (kΩ)	R4 (kΩ)	Vboot (V)	OCP Ratio (%)
NC	0	0	133%
200	10	1.65	
120	10	1.7	
80	10	1.75	
64	10	1.75	150%
98	20	1.7	
78	20	1.65	
65	20	0	
55	20	0	171%
47	20	1.65	
40	20	1.7	
35	20	1.75	

Thermal Monitor and Reporting

The TM pin is designed for system thermal monitoring by connecting a NTC thermistor resistive voltage divider from VCC5 to GND. The NTC thermistor should be the upper resistor. The uP1651Q uses specific nonlinear A/D converter for thermal monitor function. The typical ratio of TM pin voltage to VCC5, the corresponding decoded temperature and thermal zone readout value are shown in Table 3.

Note that this A/D conversion is dependent on VCC5 voltage (it tracks VCC5 voltage). Therefore, make sure to use specific NTC thermistor in resistor voltage divider from VCC5 to GND. It is recommended to use Mitsubishi TH11-3H103H NTC as R5 and 6Kohm as R6 for TEMPMAX = 100°C thermal zone reporting.

PWM On Time Setting

The uP1651Q adopts uPI proprietary RCOT™ (Robust Constant On-Time) topology to have fast transient response and smooth mode transition.

The PWM on time is set by an external resistor connected between RT pin and GND. The PWM on time can be calculated as below.

$$T_{ON} = \frac{VID}{V_{IN}} \times R_{RT} \times 111$$

For example, if V_{IN} = 12V, VID = 1.7V, R_{RT} = 30kΩ, equation gives T_{ON} = 472ns.

V_{DAC} Generator

The uP1651Q builds in precise bandgap reference circuit as shown in Figure 3. The output voltage of bandgap reference is 3.04V with respective to FBRTN. The uP1651Q uses plural resistors to generate precise reference voltage ranging from 0.5V to 3.04V with 10mV increments. All the voltage connect to a multiplexer (MUX). The multiplexer outputs the selected voltage, V_{DAC}, according to the SVID inputs. Please note that all the voltage values in Figure 3 are referred to FBRTN.

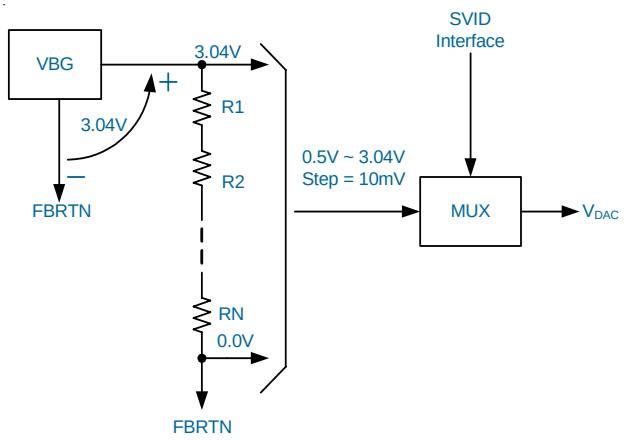


Figure 3. V_{DAC} Generator Circuit for V_{CORE}.

The V_{DAC} voltage is expressed as:

$$V_{DAC} = VID + Offset$$

where VID and Offset can be programmed by SVID.

Table 4 illustrates the VID voltages according to VID code.

Table 3. Thermal Monitor A/D Conversion

Temperature (°C)	Reg 0x12h (Temperature Zone) Readout	TM Voltage (% to VCC5)	TM Voltage(V) (VCC5=5V)	Note
75	01	75.61	3.780	
82	03	79.07	3.953	
85	07	80.42	4.021	
88	0F	81.67	4.083	
91	1F	82.84	4.142	
94	3F	83.94	4.197	
97	7F	84.96	4.248	Assert SVID thermal alert
100	FF	85.92	4.296	Assert VRHOT#

Table 4. Intel SVID Table

SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)	SVID HEX	V_{DAC} (V)
0x00	0.00	0x25	0.86	0x4A	1.23	0x6F	1.60	0x94	1.97	0xB8	2.33	0xDC	2.69
0x01	0.50	0x26	0.87	0x4B	1.24	0x70	1.61	0x95	1.98	0xB9	2.34	0xDD	2.70
0x02	0.51	0x27	0.88	0x4C	1.25	0x71	1.62	0x96	1.99	0xBA	2.35	0xDE	2.71
0x03	0.52	0x28	0.89	0x4D	1.26	0x72	1.63	0x97	2.00	0xBB	2.36	0xDF	2.72
0x04	0.53	0x29	0.90	0x4E	1.27	0x73	1.64	0x98	2.01	0xBC	2.37	0xE0	2.73
0x05	0.54	0x2A	0.91	0x4F	1.28	0x74	1.65	0x99	2.02	0xBD	2.38	0xE1	2.74
0x06	0.55	0x2B	0.92	0x50	1.29	0x75	1.66	0x9A	2.03	0xBE	2.39	0xE2	2.75
0x07	0.56	0x2C	0.93	0x51	1.30	0x76	1.67	0x9B	2.04	0xBF	2.40	0xE3	2.76
0x08	0.57	0x2D	0.94	0x52	1.31	0x77	1.68	0x9C	2.05	0xC0	2.41	0xE4	2.77
0x09	0.58	0x2E	0.95	0x53	1.32	0x78	1.69	0x9D	2.06	0xC1	2.42	0xE5	2.78
0x0A	0.59	0x2F	0.96	0x54	1.33	0x79	1.70	0x9E	2.07	0xC2	2.43	0xE6	2.79
0x0B	0.60	0x30	0.97	0x55	1.34	0x7A	1.71	0x9F	2.08	0xC3	2.44	0xE7	2.80
0x0C	0.61	0x31	0.98	0x56	1.35	0x7B	1.72	0xA0	2.09	0xC4	2.45	0xE8	2.81
0x0D	0.62	0x32	0.99	0x57	1.36	0x7C	1.73	0xA1	2.10	0xC5	2.46	0xE9	2.82
0x0E	0.63	0x33	1.00	0x58	1.37	0x7D	1.74	0xA2	2.11	0xC6	2.47	0xEA	2.83
0x0F	0.64	0x34	1.01	0x59	1.38	0x7E	1.75	0xA3	2.12	0xC7	2.48	0xEB	2.84
0x10	0.65	0x35	1.02	0x5A	1.39	0x7F	1.76	0xA4	2.13	0xC8	2.49	0xEC	2.85
0x11	0.66	0x36	1.03	0x5B	1.40	0x80	1.77	0xA5	2.14	0xC9	2.50	0xED	2.86
0x12	0.67	0x37	1.04	0x5C	1.41	0x81	1.78	0xA6	2.15	0xCA	2.51	0xEE	2.87
0x13	0.68	0x38	1.05	0x5D	1.42	0x82	1.79	0xA7	2.16	0xCB	2.52	0xEF	2.88
0x14	0.69	0x39	1.06	0x5E	1.43	0x83	1.80	0xA8	2.17	0xCC	2.53	0xF0	2.89
0x15	0.70	0x3A	1.07	0x5F	1.44	0x84	1.81	0xA9	2.18	0xCD	2.54	0xF1	2.90
0x16	0.71	0x3B	1.08	0x60	1.45	0x85	1.82	0xAA	2.19	0xCE	2.55	0xF2	2.91
0x17	0.72	0x3C	1.09	0x61	1.46	0x86	1.83	0xAB	2.20	0xCF	2.56	0xF3	2.92
0x18	0.73	0x3D	1.10	0x62	1.47	0x87	1.84	0xAC	2.21	0xD0	2.57	0xF4	2.93
0x19	0.74	0x3E	1.11	0x63	1.48	0x88	1.85	0xAD	2.22	0xD1	2.58	0xF5	2.94
0x1A	0.75	0x3F	1.12	0x64	1.49	0x89	1.86	0xAE	2.23	0xD2	2.59	0xF6	2.95
0x1B	0.76	0x40	1.13	0x65	1.50	0x8A	1.87	0xAF	2.24	0xD3	2.60	0xF7	2.96
0x1C	0.77	0x41	1.14	0x66	1.51	0x8B	1.88	0xB0	2.25	0xD4	2.61	0xF8	2.97
0x1D	0.78	0x42	1.15	0x67	1.52	0x8C	1.89	0xB1	2.26	0xD5	2.62	0xF9	2.98
0x1E	0.79	0x43	1.16	0x68	1.53	0x8D	1.90	0xB2	2.27	0xD6	2.63	0xFA	2.99
0x1F	0.80	0x44	1.17	0x69	1.54	0x8E	1.91	0xB3	2.28	0xD7	2.64	0xFB	3.00
0x20	0.81	0x45	1.18	0x6A	1.55	0x8F	1.92	0xB4	2.29	0xD8	2.65	0xFC	3.01
0x21	0.82	0x46	1.19	0x6B	1.56	0x90	1.93	0xB5	2.30	0xD9	2.66	0xFD	3.02
0x22	0.83	0x47	1.20	0x6C	1.57	0x91	1.94	0xB6	2.31	0xDA	2.67	0xFE	3.03
0x23	0.84	0x48	1.21	0x6D	1.58	0x92	1.95	0xB7	2.32	0xDB	2.68	0xFF	3.04
0x24	0.85	0x49	1.22	0x6E	1.59	0x93	1.96						

State Transition

Figure 4 illustrates the state diagram of the uP1651Q. The uP1651Q initiates it soft start cycle whenever POR transits from Low to High. VROK are set high when soft start cycle completes and no fault occurs. When any faults occurs, the uP1651Q will be shutdown and latched off. The latch state can only be reset by POR.

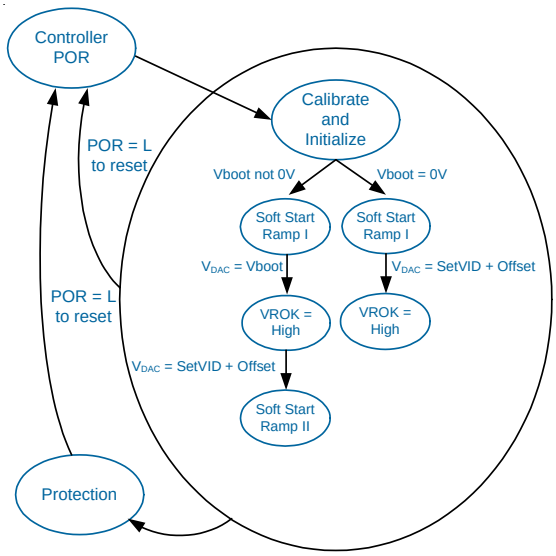


Figure 4. State Diagram.

Soft Start

The uP1651Q features programmable soft start functions for VR. The soft start function limits the output voltage slew rate during both soft start and VID on the fly (VID_OTF) periods as shown in Figure 5. The soft start buffer is a current limited buffer whose output current I_{SS} is used to charge/discharge the soft start capacitor C_{SS} when V_{DAC} transition during soft start and VID_OTF. This limits the slew rate of $V_{DAC/SS}$. Consequently EAP and FB pin voltages will follow the slew rate of $V_{DAC/SS}$.

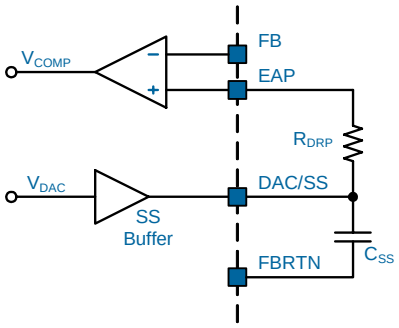


Figure 5. Circuit for Soft Start and Dynamic VID.

The DAC/SS level can be dynamically programmed by SVID interface.

Power Sequence

Figure 6 shows the typical start up power sequence of VR12.5 for non-zero Vboot. After VCC12 POR, Enable is set high to initialize the power sequence. Because platform pull-up bias rail VTT is still not available, all open drain outputs are floating. After a delay time T1 (< 5ms) upon ENABLE goes high, the PWM start switching and V_{OUT} ramps up to Vboot. The V_{OUT} ramping time T2 is determined by Vboot and SetVID_slow slew rate. After V_{OUT} ramps to Vboot, PWM controller asserts VROK and ALERT# immediately. The delay time T3 from ALERT# assertion to VROK assertion is less than 6us. Platform VTT then ramps up, and SVID bus is active and idle. PWM controller waits for SVID command. CPU then initializes SVID clock, and sends out initial SVID command sequence, reading varies SVID registers. After that, CPU sends out SetVID command to program VR output voltage. PWM controller acknowledges the SetVID command and ramps the output voltage to the targeted VID at commanded slew rate.

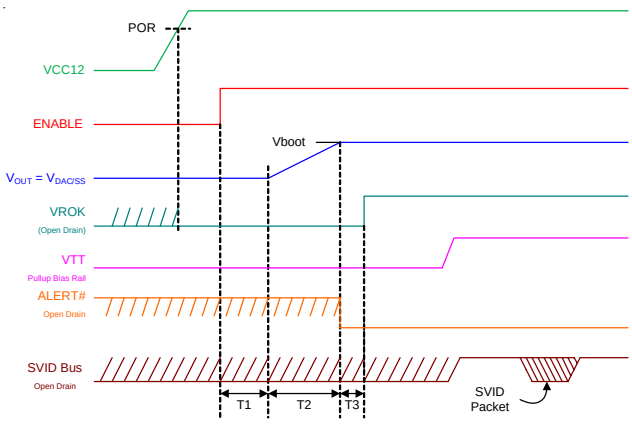


Figure 6. VR12.5 Typical Power Sequence

Dynamic VID

The uP1651Q can accept VID input changes during normal operation. This allows the output voltage V_{OUT} to change while the DC/DC converter is running and supplying current to the load. This is commonly referred to as VID on-the-fly (VID_OTF). A VID_OTF may occur under either light or heavy load conditions. This change can be positive or negative. During VID_OTF, V_{DAC} is a staircase waveform. In the uP1651Q, C_{SS} is also used to filter the $V_{DAC/SS}$. By properly selecting C_{SS}, VID_OTF performance can be improved.

Output Voltage Differential Sensing

The uP1651Q uses differential sensing by a high-gain low-offset error amplifier as shown in Figure 7. The CPU voltage is sensed between the FB and FBRTN pins. A

resistor R_{FB} connects FB pin and the positive remote sense pin of the CPU V_{CCP}. FBRTN pin connects to the negative remote sense pin of CPU V_{CCN} directly. The error amplifier compares The V_{FB} with V_{EAP} (= $V_{DAC/SS}$ - I_{SUM} x R_{DRP}) to regulate the output voltage.

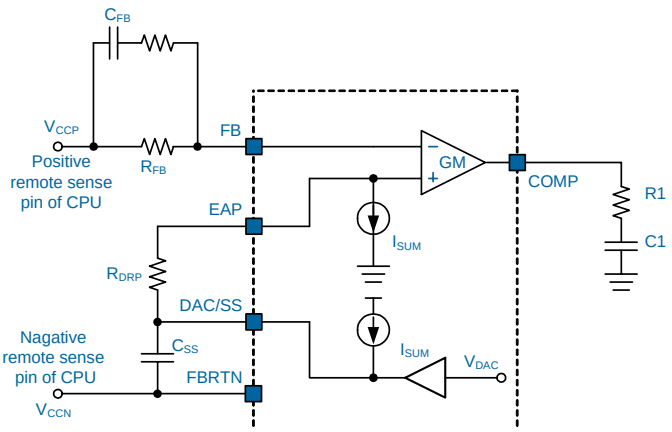


Figure 7. Circuit for V_{CORE} Differential Sensing.

Channel Current Sensing

The uP1651Q extracts phase currents for current balance and per channel over current protection by parasitic on-resistance of the lower MOSFETs when turn on as shown in Figure 8. The ISEN1/2 pins sense the corresponding phase current when the lower MOSFETs are turned on.

$$I_{SENX} = ((I_{PHX} \times R_{DS(ON)}) + V_{DC}) / R_{SENX}$$

where I_{SENX} is the sampled and held phase current signal, I_{PHX} is phase current, $R_{DS(ON)}$ is the on-resistance of the lower MOSFETs, and V_{DC} is an internal 30mV offset voltage for the current balance circuit. The current balance circuit increases the PWM on time width of the phase whose phase current is smaller than others and decrease the PWM on time width of the phase whose phase current is larger than others.

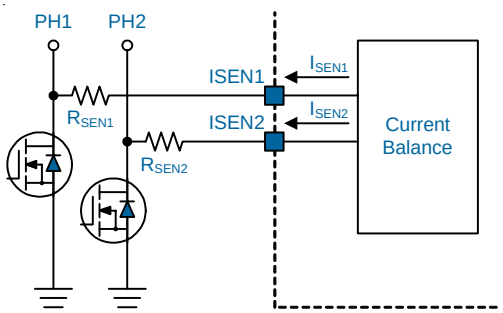


Figure 8. Phase Current Sensing and Current Balance.

Total Load Current Sensing

The uP1651Q provides low input offset current sense amplifier (CSA) to monitor the total load current flowing through inductor as shown in Figure 9.

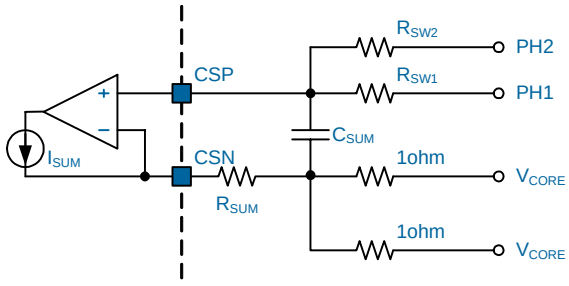


Figure 9. Total Load Current Sensing.

Output current of CSA (I_{SUM}) is used for active voltage positioning (AVP), load current monitoring and over current protection. R_{SW} and C_{SUM} must be selected according to the below equation:

$$k \times \frac{L}{R_{DC}} = \frac{R_{SW} \times C_{SUM}}{N}$$

where R_{DC} is the DCR of the output inductor, N is the phase number of operation. k is used for load transient response fine tune. Theoretically, k should be equal to 1 to sense the instantaneous total load curret. But in real application, k is usually set to between 1.2 and 1.8 to obtain better load transient response.

The relationship between sensed current I_{SUM} and total output current I_{OUT} is shown as follows.

$$I_{SUM} = \frac{I_{OUT} \times R_{DC}}{R_{SUM} \times N}$$

For a given VR maximum output current I_{MAX}, R_{SUM} can be determined using above equation.

Droop (Load Line) Setting

The I_{SUM} is mirrored to EAP pin as shown in Figure 7. The voltage drop across R_{DRP} and makes V_{EAP} as:

$$V_{EAP} = V_{DAC/SS} - I_{SUM} \times R_{DRP} = V_{DAC/SS} - \frac{I_{OUT} \times R_{DC} \times R_{DRP}}{R_{CSN} \times N}$$

In steady state, output voltage is equal to V_{EAP}. Thus, the output voltage decreasing linearly with obtained I_{OUT}. The loadline is defined as:

$$LoadLine = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{R_{DC} \times R_{DRP}}{R_{SUM} \times N}$$

Output Current Monitoring

The summed current I_{SUM} is mirrored to flow out of IMON pin for output current reporting. Connect a resistor R_{IMON} from the IMON pin to GND to obtain V_{IMON} voltage. The V_{IMON} voltage is proportional to the output current. The internal ADC converts V_{IMON} to a digital content for current reporting. The ADC outputs FFh when V_{IMON} is equal to or greater than 2V. A capacitor can be added to the IMON pin to adjust the response time of current reporting. The resistor R_{IMON} can be determined as follows.

$$\frac{2V}{R_{IMON}} = \frac{I_{MAX} \times R_{DC}}{R_{SUM} \times N}$$

Output Over Current Protection

The summed current I_{SUM} is separately mirrored to the ISUM pin for SVID ICCMAX alert and over current protection (OCP). Connect a resistor R_{ISUM} from the ISUM pin to GND to get V_{ISUM} voltage. The voltage V_{ISUM} is proportional to the output current. For 2-phase configuration, when V_{ISUM} reaches 2V, SVID ICCMAX alert is triggered. When V_{ISUM} is greater than 2V times the OCP ratio defined in Table 2, OCP is triggered. When OCP is triggered, VROK will go low immediately, and the controller will turn off all MOSFETs and set the PWM output to high impedance state. The OCP has a 20us time delay to prevent false-tripping. The ICCMAX alert and OCP threshold is dependent on the configuration and operating phase number as shown in Table 2. When the controller is in single-phase operation during SVID SetPS command or PSI setting, the ICCMAX alert and OCP threshold will be half of the original value of 2-phase operation.

The change in ICCMAX alert and OCP threshold is to reflect the actual operating condition so as to provide proper protection. The OCP is latch-off type and can be reset only by POR toggling.

Avoid adding capacitance to the ISUM pin. Any capacitance added to the ISUM pin will affect the SVID ICCMAX alert threshold and the OCP level.

Power Saving Mode and Automatic Phase Reduction

The PS pin is used for auto phase function setting by connecting a resistor voltage divider from VCC5 to GND. The auto phase has one level, V_{PS}, which can be calculated as below:

$$V_{PS} = VCC5 \times \frac{R2}{(R1+R2)}$$

According V_{ISUM} and V_{PS} information, the uP1651Q operation phase number is as shown in Table 5. When V_{PS} = 0.3V and V_{ISUM} = 0.25V, the uP1651Q turns off phase 2 and operates in 1-phase.

The automatic phase reduction reduces the switching and conduction losses at light load condition and enables high efficiency over a wide range of output current. There is no time delay in operation phase number increase. When operation phase number drops, there is a delay of 300us, and a hysteresis of 50mV.

Refer to Table 5, when uP1651Q operates in normal mode, the uP1651Q follows SVID SetPS command to determine the power state as shown in Table 6. When uP1651Q is configured to operate in forced 2-phase operation mode, it will ignore the SVID SetPS command and keep 2-phase operation. When uP1651Q is configured to operate in auto PSI mode, it will ignore the SVID SetPS command and changes the operating phase number by V_{PS} threshold setting.

Table 5. Operation Phase and Auto PSI Mode

Mode	PS level	Operation Phase Number
Normal Mode	V_{PS} = 0V	Follow SetPS Command, as shown in Table 6
Forced Full Phase Operation Mode (default is 2-phase, depends on configuration)	V_{PS} = 5V	Full Phase Operation (default is 2-phase, depends on configuration)
Auto PSI Mode	$V_{PS} < V_{ISUM}$	Full Phase Operation (default is 2-phase, depends on configuration)
	$V_{PS} > V_{ISUM}$	1 Phase Operation

Power State and Operation Mode Definition

The uP1651Q has different definition in power state and operation mode per ENABLE voltage level. ENABLE > 4V and ENABLE < 4V has individual definition. The power state and operation mode definition is as shown in Table 6.

Table 6. ENABLE and Power State Definition

ENABLE > 4V

Configuration		2-phase	1-phase
SVID SetPS Power State	PS0	2-ph CCM	1-ph CCM
	PS1	1-ph CCM	1-ph CCM
	PS2	1-ph DEM	1-ph DEM
	PS3	1-ph DEM	1-ph DEM

ENABLE < 4V

Configuration		2-phase	1-phase
SVID SetPS Power State	PS0	2-ph CCM	1-ph CCM
	PS1	1-ph DEM	1-ph DEM
	PS2	1-ph DEM	1-ph DEM
	PS3	1-ph DEM	1-ph DEM

Control Loop

The uP1651Q adopts the uPI proprietary RCOT™ control technology. The RCOT uses the constant on-time modulator. The output voltage is sensed to compare with the internal high accurate DAC. The DAC is commanded by CPU through the SVID interface. The amplified error signal, V_{COMP}, is compared to the internal ramp to initiate a PWM on time. The RCOT features easy design, fast transient response and smooth mode transition and is especially suitable for powering the microprocessor.

Over Voltage Protection (OVP)

The over voltage protection monitors the output voltage via the FB pin. Once V_{FB} exceeds V_{EAP} + 300mV, OVP is triggered and latched. The uP1651Q will try to turn on lower MOSFETs and turn off upper MOSFETs to protect CPU. A 20us delay is used in OVP detection circuit to prevent false trigger. Only re-start up can release OVP latch.

Under Voltage Protection (UVP)

The under voltage protection monitors the output voltage via the FB pin. After the uP1651Q starting up and V_{OUT} ramping up to V_{BOOT}, the uP1651Q initiates UVP function. Once V_{FB} is lower than 200mV, UVP is triggered and latched. The uP1651Q will try to turn off both upper and lower MOSFETs. A 5us time delay is used in UVP detection circuit to prevent false trigger. Only re-start up can release UVP latch.

SerialVID (SVID)

SerialVID is a three wire (SCLK,SDAT,Alert#) serial synchronous interface and used to transfer power management information between a micoprocessor and a VRM,The link is between one microprocessor and multiple VR Controller on the same bus. The supported data register is shown in Table 7.

Table 7. SVID Data and Configuration Registers

Index	Register Name	Access	Default	Description
00h	Vender_ID	RO	26h	Vender ID
01h	Product_ID	RO	18h	Product ID
02h	Product_Revision	RO	05h	Product Revision
05h	Protocol_Version	RO	04h	SVID Protocol Version
06h	VR_Capability	RO	81h	Bit mapped register, identifies the SVID VR capabilities and which of the optional telemetry are supported.
10h	Status_1	R-M, W-PWM	00h	Data register containing the status of VR.
11h	Status_2	R-M, W-PWM	00h	Data register containing the status of transmission.
12h	Temperature_Zone	R-M, W-PWM	00h	Data register showing temperature zone that have been entered.
15h	Output_Current	R-M, W-PWM	--	Data register showing the output current that have been entered.
1Ch	Status_2_LastRead	R-M, W-PWM	00h	This register contains a copy of the Status_2.
21h	ICC_Max	RO Platform	--	Data register containing the maximum output current the platform supports.
22h	Temp_Max	RO Platform	64h	Data register containing the maximum temperature the platform supports. Binary formate in ^{O}C, i.e. 64h = 100^{O}C.
24h	SR_Fast	RO	0Ah	Data register containing the capability of fast slew rate the platform can sustain. Binary format in mV/us, i.e. 0Ah = 10mV/us.
25h	SR_Slow	RO	02h	Data register containing the capability of slow slew rate the platform can sustain. Binary format in mV/us, i.e. 02h = 2.5mV/us.
26h	VBOOT	RO Platform	--	Data register containing V_{BOOT} voltage in VID steps.
30h	VOUT_Max	RW Master	FFh	This register is programmed by master and sets the maximum VID.
31h	VID_Setting	RW Master	00h	Data register containing currently programmed VID.
32h	Power_State	RW Master	00h	Data register containing the currently programmed power state.
33h	Offset	RW Master	00h	Set offset in VID steps.
34h	Multi_VR_Config	RW Master	00h	Bit mapped data register which configures multiple VRs behavior on the same bus.
35h	Pointer	RW Master	--	Scratch pad register for temporary storage of the SetRegADR pointer register.

Absolute Maximum Rating

(Note 1)

Supply Input Voltage, VCC5 ---------- -0.3V to +6V
Supply Input Voltage, VCC12 ---------- -0.3V to +15V
BOOTx to PHx ---------- -0.3V to +15V
PHx to GND
- DC ---------- -0.7V to 15V
- < 200ns ---------- -8V to 30V

BOOTx to GND
- DC ---------- -0.3V to VCC12 + 15V
- < 200ns ---------- -0.3V to 42V

UGx to PHx
- DC---------- -0.3V to (BOOTx - PHx +0.3V)
- <200ns ---------- -5V to (BOOTx - PHx + 0.3V)

LGx to GND
- DC ---------- -0.3V to + (VCC12 + 0.3V)
- <200ns ---------- -5V to VCC12 + 0.3V

Other Pins ---------- -0.3V to +6V
Storage Temperature Range ---------- -65°C to +150°C
Junction Temperature ---------- 150°C
Lead Temperature (Soldering, 10 sec) ---------- 260°C
ESD Rating (Note 2)
- HBM (Human Body Mode) ---------- 2kV
- MM (Machine Mode) ---------- 200V

Thermal Information

Package Thermal Resistance (Note 3)
- WQFN4x4 - 32L θ_{JA} ---------- 40°C/W
- WQFN4x4 - 32L θ_{JC} ---------- 4°C/W

Power Dissipation, P_D @ T_A = 25°C
- WQFN4x4 - 32L ---------- 2.5W

Recommended Operation Conditions

(Note 4)

Operating Junction Temperature Range ---------- -40°C to +125°C
Operating Ambient Temperature Range ---------- -40°C to +85°C
Supply Input Voltage, VCC5 ---------- 4.5V to 5.5V
Supply Input Voltage, VCC12 ---------- 10.8V to 13.2V

Note 1. Stresses listed as the above *Absolute Maximum Ratings* may cause permanent damage to the device. These are for stress ratings. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability.

Note 2. Devices are ESD sensitive. Handling precaution recommended.

Note 3. θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 4. The device is not guaranteed to function outside its operating conditions.

Electrical Characteristics

(VCC5 = 5V, VCC12 = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply Input						
VCC5 POR Threshold			4.1	4.3	4.5	V
VCC5 POR Hysteresis		VCC5 Falling.	--	0.3	--	V
VCC5 Supply Current	I_{VCC5}	EN = 0V	--	3	--	mA
VCC12 POR Threshold			4.9	5.1	5.3	V
VCC12 POR Hysteresis		VCC12 Falling.	--	1	--	V
VCC12 Supply Current	I_{VCC12}	EN = 0V	--	0.3	--	mA
Error Amplifier						
Offset Voltage	$V_{OS(EA)}$		-1	--	1	mV
Trans-conductance	GM		--	1500	--	uA/V
Gain Bandwidth Product	GBW_{EA}	Guaranteed by Design	--	10	--	MHz
Maximum Current (Source &Sink)	I_{COMP}		200	--	--	uA
DAC Voltage Accuracy						
DAC Output Accuracy	$V_{DAC/SS}$	1.5V to 3.04V	-0.5	--	0.5	%
		1V to 1.49V	-8	--	8	mV
		0.5V to 0.99V	-10	--	10	mV
Soft Start						
DAC/SS Charge/Discharge Current	I_{SS}	SetVID_Fast	180	200	240	uA
		SetVID_Slow	45	50	60	uA
ENABLE Input						
Input Low	V_{IL}		--	--	0.3	V
Input High	V_{IH}		0.7	--	--	V
Leakage Current of ENABLE	I_{ENABLE}	ENABLE = 0V	--	0	1	uA
		ENABLE = 1V	-1	0	--	uA
PWM On Time Setting						
On Time	T_{ON}	V_{IN} = 12V, VID = 1.7V, R_{RT} = 30kohm	--	472	--	ns
Minimum Off Time	T_{OFF_MIN}	Single phase operation	--	200	--	ns
Current Sense Amplifier for Droop						
Offset Voltage	$V_{OS(CSA)}$		-1	--	1	mV
Input Bias Current		Guaranteed by Design	-10	--	10	nA
Gain Bandwidth Product	$G_{BW(CSA)}$	Guaranteed by Design	--	10	--	MHz
Maximum Sourcing Current	I_{CSNMAX}		100	--	--	uA
Current Mirror Accuracy		I_{DROOP} to I_{CSN} ratio	94	100	106	%

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Current Sense Amplifier for Current Balance						
Offset Voltage	$VOS_{(VCCS)}$		22	30	40	mV
Offset Mismatch Between Channel			-2	0	+2	mV
Gain Bandwidth Product	$G_{BW(VCCS)}$	Guaranteed by Design	--	10	--	MHz
Zero Current Detection						
ZCD Threshold	V_{ZCD}	Measure PH1 voltage	-1	0	1	mV
SDAT, ALERT#, VRHOT#						
Pull Down Resistance	R_{on_SVID}		4	--	13	Ω
Leakage Current	I_{L_SVID}		-100	--	100	uA
Input Low Voltage	V_{IL_SVID}		--	--	0.45	V
Input High Voltage	V_{IH_SVID}		0.65	--	--	V
Open Drain Output (VROK)						
Output Low Voltage	V_{OL}	I_{SINK} = 4mA	--	--	0.2	V
Output High Leakage		V_{VROK} = 5V	--	--	1	uA
Current Monitoring (IMON, ISUM)						
Maximum Sourcing Current			100	--	--	uA
IMON, ISUM Current Mirror Accuracy		I_{IMON}, I_{ISUM} to I_{CSN} ratio	94	100	106	%
Digital Current Reporting Accuracy						
A/D Conversion Tolerance		V_{IMON} = 0V (00h) to 2V (FFh) Read Reg. 0x15h	-2	0	+2	DEC
Gate Drivers						
Upper Gate Source	R_{UG_SRC}	I_{UG} = -80mA	--	2	4	Ω
Upper Gate Sink	R_{UG_SNK}	I_{UG} = 80mA	--	2	4	Ω
Lower Gate Source	R_{LG_SRC}	I_{LG} = -80mA	--	2	4	Ω
Lower Gate Sink	R_{LG_SNK}	I_{LG} = 80mA	--	0.8	1.6	Ω
Dead Time	T_{DT}		--	30	--	ns
VR Maximum Current Setting (PROG)						
A/D Conversion Accuracy		V_{PROG} = 0V to 1/4 of VCC5	-2	0	+2	DEC

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Protection						
OVP Threshold	V_{OVP}	V_{FB} - V_{EAP}	--	300	--	mV
OVP Delay	T_{OVP}		--	20	--	us
UVP Threshold	V_{UVP}	Absolute UVP	--	200	--	mV
UVP Delay	T_{UVP}		--	5	--	us
ICCMAX Alert Threshold	V_{ISUM_ICCMAX}	2-phase operation, measure ISUM voltage	--	2	--	V
Total Current OCP Threshold	V_{ISUM_OCP}	Set OCP ratio to 133%, measure ISUM voltage	--	2.66	--	V
Total Current OCP Delay Time	T_{OCP1}		--	20	--	us
Channel Current OCP Threshold	I_{CSNx}		--	60	--	uA
Channel Current OCP Delay Time	T_{OCP2}		--	5	--	us
Thermal Shutdown Threshold	T_{OTP}		--	160	--	°C

Typical Operation Characteristics

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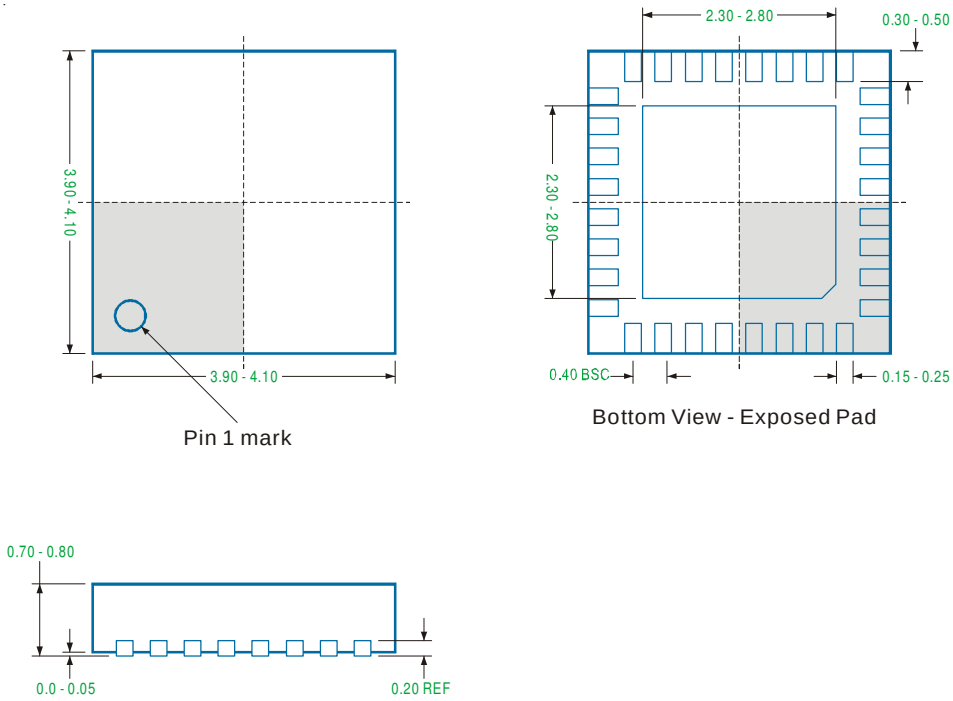
Package Information

WQFN4x4 - 32L



Note

1. Package Outline Unit Description:
   BSC: Basic. Represents theoretical exact dimension or dimension target
   MIN: Minimum dimension specified.
   MAX: Maximum dimension specified.
   REF: Reference. Represents dimension for reference use only. This value is not a device specification.
   TYP. Typical. Provided as a general value. This value is not a device specification.
2. Dimensions in Millimeters.
3. Drawing not to scale.
4. These dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm.

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