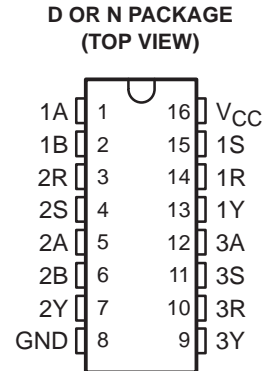


# SN75124 TRIPLE LINE RECEIVER

SLLS058B – SEPTEMBER 1973 – REVISED MAY 1995

- Meets or Exceeds the Requirements of IBM™ System 360 Input/Output Interface Specification
- Operates From Single 5-V Supply
- TTL Compatible
- Built-In Input Threshold Hysteresis
- High Speed . . . Typical Propagation Delay Time = 20 ns
- Independent Channel Strobes
- Input Gating Increases Application Flexibility
- Designed for Use With Dual Line Driver SN75123
- Designed to Be Interchangeable With Signetics N8T24



## description

The SN75124 triple line receiver is specifically designed to meet the input/output interface specifications for IBM System 360. It is also compatible with standard TTL logic and supply voltage levels.

The SN75124 has receiver inputs with built-in hysteresis to provide increased noise margin for single-ended systems. An open line affects the receiver input as does a low-level input voltage, and the receiver input can withstand a level of  $-0.15$  V with power on or off. The other inputs are in TTL configuration. The S input must be high to enable the receiver input. Two of the line receivers have A and B inputs that, if both are high, hold the output low. The third receiver has only an A input that, if high, holds the output low.

See the SN751730 for new IBM 360/370 interface designs.

The SN75124 is characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

FUNCTION TABLE

| INPUTS |    |   |   | OUTPUT<br>Y |
|--------|----|---|---|-------------|
| A      | B† | R | S |             |
| H      | H  | X | X | L           |
| X      | X  | L | H | L           |
| L      | X  | H | X | H           |
| L      | X  | X | L | H           |
| X      | L  | H | X | H           |
| X      | L  | X | L | H           |

† B input and last two lines of the function table are applicable to receivers 1 and 2 only.



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 **TEXAS  
INSTRUMENTS**

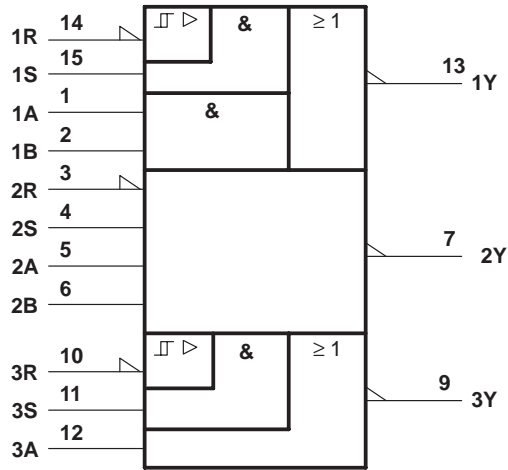
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# SN75124 TRIPLE LINE RECEIVER

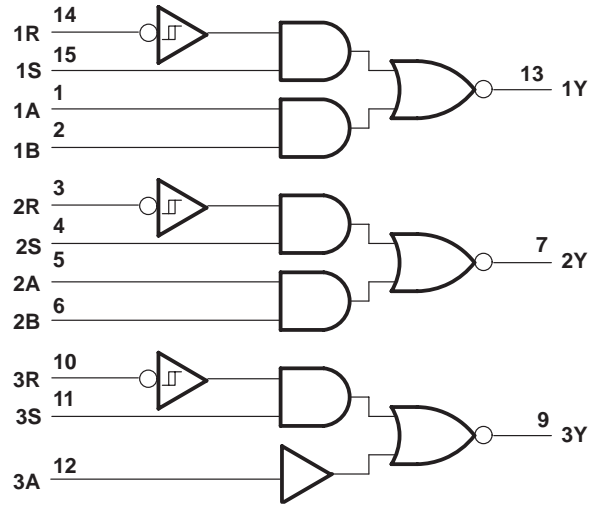
SLLS058B – SEPTEMBER 1973 – REVISED MAY 1995

## logic symbol†

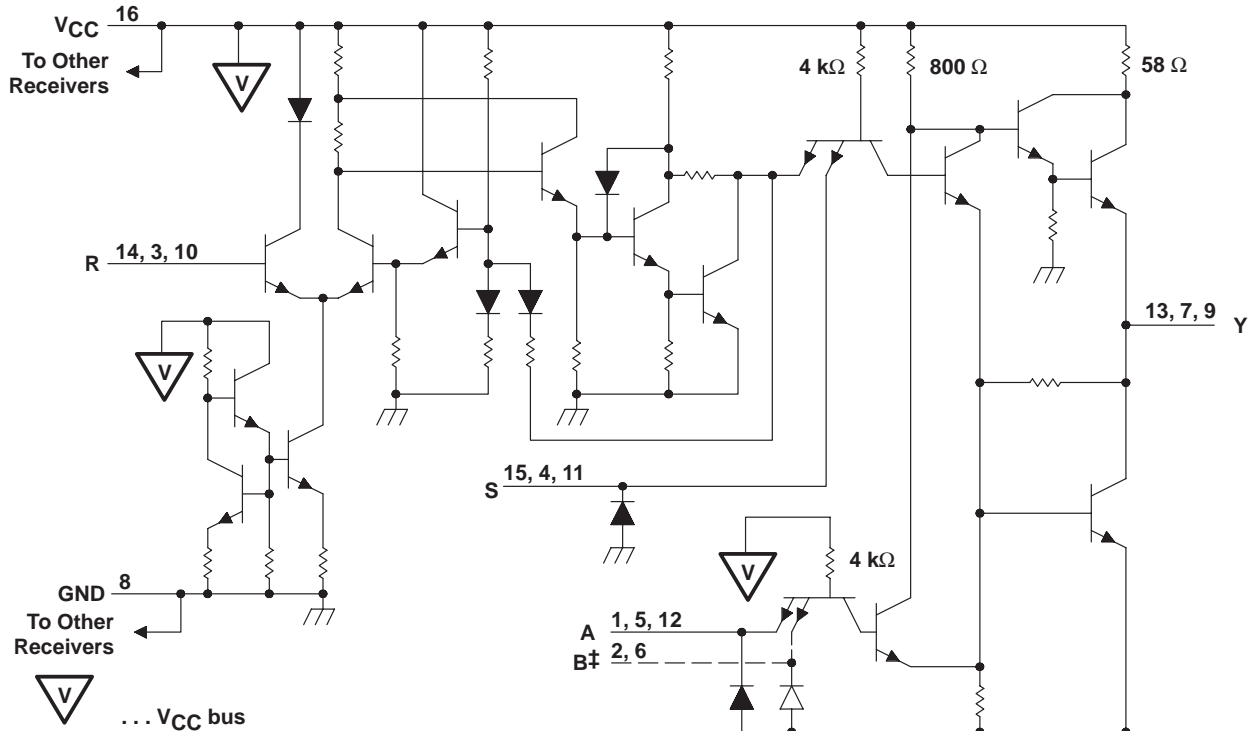


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## schematic (each receiver)



‡ B input is provided on receivers 1 and 2 only  
Resistor values shown are nominal.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

|  |  |
|--|--|
| Supply voltage, $V_{CC}$ (see Note 1) .....                        | 7 V  |
| Input voltage, $V_I$ : R input with $V_{CC}$ applied .....         | 7 V  |
| R input with $V_{CC}$ not applied .....                            | 6 V  |
| A, B, or S input .....   | 5.5 V                                      |
| Output voltage, $V_O$ .....  | 7 V  |
| Output current, $I_O$ .....  | $\pm 100$ mA                               |
| Continuous total dissipation .....                                 | See Dissipation Rating Table               |
| Operating free-air temperature range, $T_A$ .....                  | $0^\circ\text{C}$ to $70^\circ\text{C}$    |
| Storage temperature range, $T_{stg}$ .....                         | $-65^\circ\text{C}$ to $150^\circ\text{C}$ |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... | $260^\circ\text{C}$                        |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to network ground terminal

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \leq 25^\circ\text{C}$<br>POWER RATING | DERATING FACTOR<br>ABOVE $T_A = 25^\circ\text{C}$ | $T_A = 70^\circ\text{C}$<br>POWER RATING |
|---------|---|---|--|
| D       | 950 mW                                      | 7.6 mW/ $^\circ\text{C}$                          | 608 mW                                   |
| N       | 1150 mW                                     | 9.2 mW/ $^\circ\text{C}$                          | 736 mW                                   |

**recommended operating conditions**

|                                       |            | MIN  | NOM | MAX  | UNIT             |
|---------------------------------------|------------|------|-----|------|------------------|
| Supply voltage, $V_{CC}$              |            | 4.75 | 5   | 5.25 | V                |
| High-level input voltage, $V_{IH}$    | A, B, or S | 2    |     |      | V                |
|                                       | R          | 1.7  |     |      |                  |
| Low-level input voltage, $V_{IL}$     | A, B, or S | 0.8  |     |      | V                |
|                                       | R          | 0.7  |     |      |                  |
| High-level output current, $I_{OH}$   |            | -800 |     |      | $\mu\text{A}$    |
| Low-level output current, $I_{OL}$    |            | 16   |     |      | mA               |
| Operating free-air temperature, $T_A$ |            | 0    | 70  |      | $^\circ\text{C}$ |

# SN75124 TRIPLE LINE RECEIVER

SLLS058B – SEPTEMBER 1973 – REVISED MAY 1995

**electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)**

| PARAMETER   |  |            | TEST CONDITIONS  |                                      | MIN  | TYP | MAX  | UNIT          |
|-------------|--|------------|--|--------------------------------------|------|-----|------|---------------|
| $V_{hys}$   | Hysteresis voltage ( $V_{IT+} - V_{IT-}$ ) | R          | $V_{CC} = 5\text{ V}$ ,                                  | $T_A = 25^\circ\text{C}$             | 0.2  | 0.5 |      | V             |
| $V_{IK}$    | Input clamp voltage                        | A, B, or S | $V_{CC} = 5\text{ V}$ ,                                  | $I_I = 12\text{ mA}$                 |      |     | -1.5 | V             |
| $V_{I(BR)}$ | Input breakdown voltage                    | A, B, or S | $V_{CC} = 5\text{ V}$ ,                                  | $I_I = 10\text{ mA}$                 | 5.5  |     |      | V             |
| $V_{OH}$    | High-level output voltage                  |            | $V_{IH} = V_{IHmin}$ ,<br>$I_{OH} = -800\ \mu\text{A}$ , | $V_{IL} = V_{ILmax}$ ,<br>See Note 2 | 2.6  |     |      | V             |
| $V_{OL}$    | Low-level output voltage                   |            | $V_{IH} = V_{IHmin}$ ,<br>$I_{OL} = 16\text{ mA}$ ,      | $V_{IL} = V_{ILmax}$ ,<br>See Note 2 |      |     | 0.4  | V             |
| $I_I$       | Input current at maximum input voltage     | R          | $V_I = 7\text{ V}$                                       |                                      |      |     | 5    | mA            |
|             |  |            | $V_I = 6\text{ V}$ ,                                     | $V_{CC} = 0$                         |      |     | 5    |               |
| $I_{IH}$    | High-level input current                   | A, B, or S | $V_I = 4.5\text{ V}$                                     |                                      |      |     | 40   | $\mu\text{A}$ |
|             |  | R          | $V_I = 3.11\text{ V}$                                    |                                      |      |     | 170  |               |
| $I_{IL}$    | Low-level input current                    | A, B, or S | $V_I = 0.4\text{ V}$ ,                                   | $V_{IR} = 0.8\text{ V}$              | -0.1 |     | -1.6 | mA            |
| $I_{OS}$    | Short-circuit output current†              |            |  |                                      | -50  |     | -100 | mA            |
| $I_{CC}$    | Supply current                             |            | All inputs = 0.8 V                                       |                                      |      |     | 72   | mA            |
|             |  |            | All inputs = 2 V   |                                      |      |     | 100  |               |

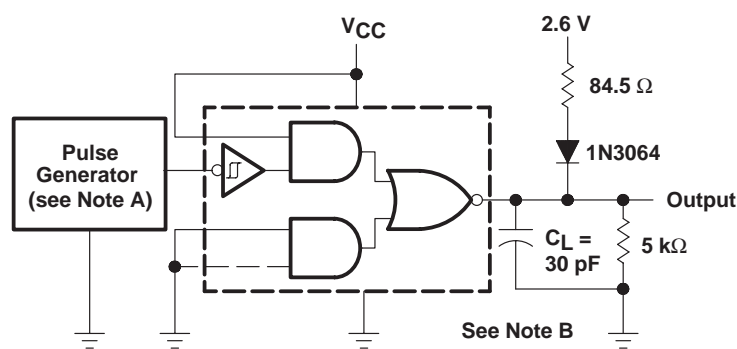
† Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

NOTE 2: The output voltage and current limits are characterized for any appropriate combination of high and low inputs specified by the function table for the desired output.

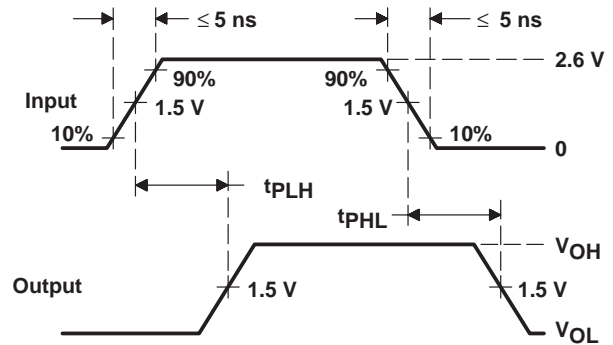
## switching characteristics, $V_{CC} = 5\text{ V}$ , $T_A = 25^\circ\text{C}$

| PARAMETER |   | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|-----------------|-----|-----|-----|------|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output from R input | See Figure 1    |     | 20  | 30  | ns   |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output from R input |                 |     | 20  | 30  |      |

### PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

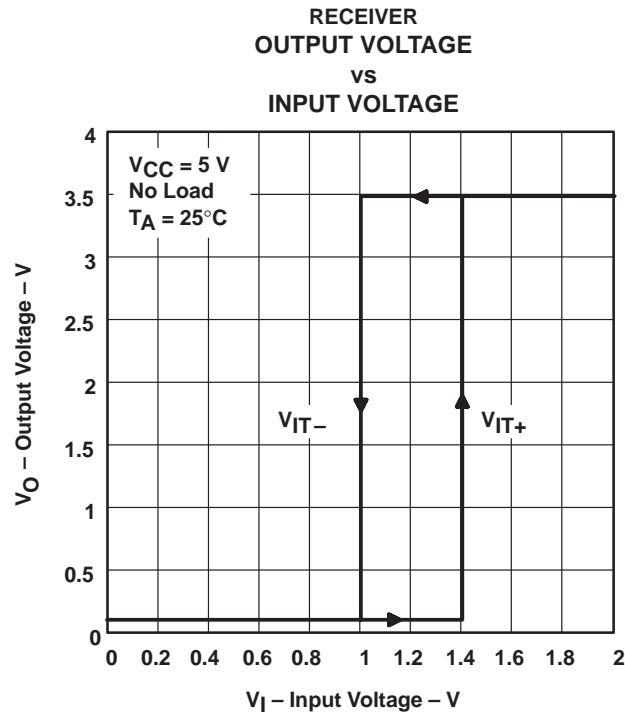


VOLTAGE WAVEFORMS

- NOTES: A. The pulse generator has the following characteristics:  $Z_O \approx 50\ \Omega$ ,  $PRR \leq 5\text{ MHz}$ , duty cycle = 50%.  
B.  $C_L$  includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS



APPLICATION INFORMATION

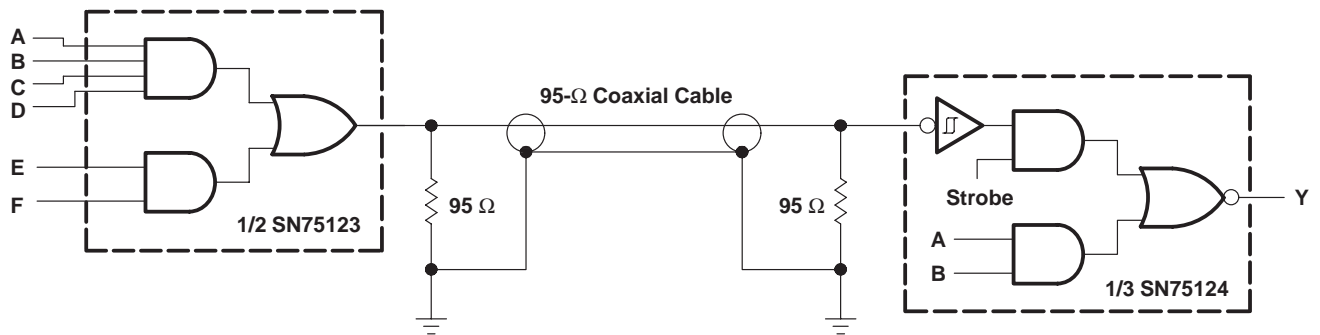


Figure 3. Unbalanced Line Communication Using SN75123 and SN75124

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples        |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|----------------|
| SN75124D         | OBSOLETE      | SOIC         | D               | 16   |             | TBD                     | Call TI                 | Call TI              | 0 to 70      |                         |                |
| SN75124N         | ACTIVE        | PDIP         | N               | 16   | 25          | Pb-Free (RoHS)          | CU NIPDAU               | N / A for Pkg Type   | 0 to 70      | SN75124N                | <b>Samples</b> |
| SN75124NSR       | ACTIVE        | SO           | NS              | 16   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | 0 to 70      | SN75124                 | <b>Samples</b> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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