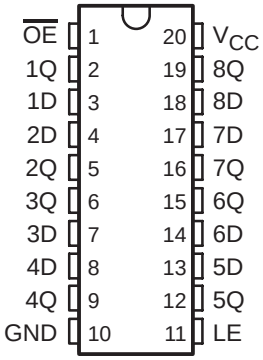
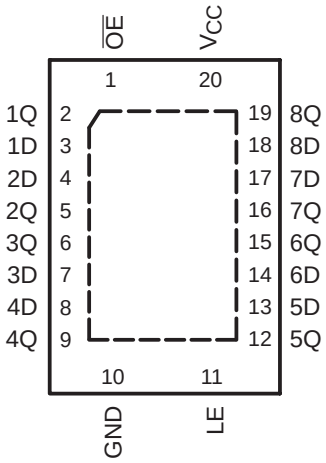
- 2-V to 5.5-V V_{CC} Operation
- Max t_{pd} of 8.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output V_{OH} Undershoot) >2.3 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

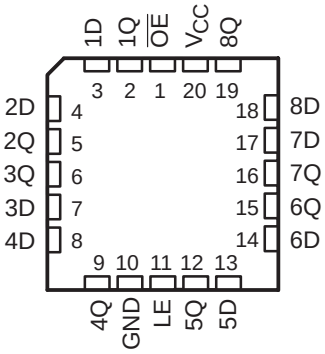
SN54LV373A . . . J OR W PACKAGE
SN74LV373A . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)



SN74LV373A . . . RGY PACKAGE
(TOP VIEW)



SN54LV373A . . . FK PACKAGE
(TOP VIEW)



description/ordering information

The ’LV373A devices are octal transparent D-type latches designed for 2-V to 5.5-V V_{CC} operation.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	QFN − RGY	Reel of 1000	SN74LV373ARGYR	LV373A
	SOIC − DW	Tube of 25	SN74LV373ADW	LV373A
		Reel of 2500	SN74LV373ADWR	
	SOP − NS	Reel of 2000	SN74LV373ANSR	74LV373A
	SSOP − DB	Reel of 2000	SN74LV373ADBR	LV373A
	TSSOP − PW	Tube of 70	SN74LV373APW	LV373A
		Reel of 2000	SN74LV373APWR	
		Reel of 250	SN74LV373APWT	
	TVSOP − DGV	Reel of 2000	SN74LV373ADGVR	LV373A
	VFBGA − GQN	Reel of 1000	SN74LV373AGQNR	LV373A
−55°C to 125°C	CDIP − J	Tube of 20	SNJ54LV373AJ	SNJ54LV373AJ
	CFP − W	Tube of 85	SNJ54LV373AW	SNJ54LV373AW
	LCCC − FK	Tube of 55	SNJ54LV373AFK	SNJ54LV373AFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

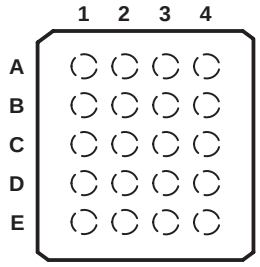
A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

GQN PACKAGE
(TOP VIEW)



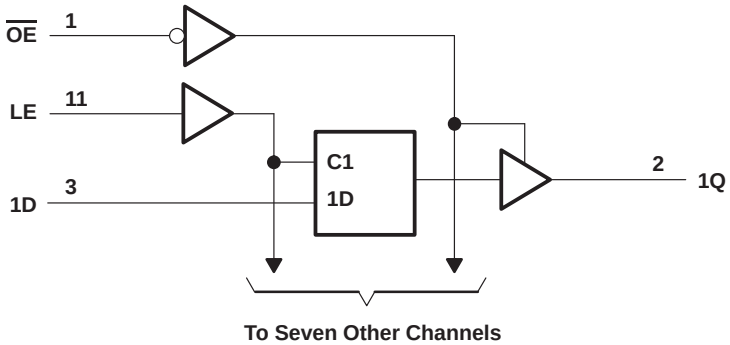
terminal assignments

	1	2	3	4
A	1Q	$\overline{OE}$	V_{CC}	8Q
B	2D	7D	1D	8D
C	3Q	2Q	6Q	7Q
D	4D	5D	3D	6D
E	GND	4Q	LE	5Q

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



Pin numbers shown are for the DB, DGV, DW, FK, J, NS, PW, RGY, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	−0.5 V to 7 V
Output voltage range, V_O (see Notes 1 and 2)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0)	−20 mA
Output clamp current, I_{OK} (V_O < 0)	−50 mA
Continuous output current, I_O (V_O = 0 to V_{CC})	±35 mA
Continuous current through V_{CC} or GND	±70 mA
Package thermal impedance, θ_{JA} (see Note 3): DB package	70°C/W
(see Note 3): DGV package	92°C/W
(see Note 3): DW package	58°C/W
(see Note 3): GQN package	78°C/W
(see Note 3): NS package	60°C/W
(see Note 3): PW package	83°C/W
(see Note 4): RGY package	37°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 5)

			SN54LV373A		SN74LV373A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 2.3 V to 2.7 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 3 V to 3.6 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
		V_{CC} = 4.5 V to 5.5 V	$V_{CC} \times 0.7$		$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 2.3 V to 2.7 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 3 V to 3.6 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
		V_{CC} = 4.5 V to 5.5 V		$V_{CC} \times 0.3$		$V_{CC} \times 0.3$	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	0	V_{CC}	V
		3-state	0	5.5	0	5.5	
I_{OH}	High-level output current	V_{CC} = 2 V		−50		−50	µA
		V_{CC} = 2.3 V to 2.7 V		−2		−2	mA
		V_{CC} = 3 V to 3.6 V		−8		−8	
		V_{CC} = 4.5 V to 5.5 V		−16		−16	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	µA
		V_{CC} = 2.3 V to 2.7 V		2		2	mA
		V_{CC} = 3 V to 3.6 V		8		8	
		V_{CC} = 4.5 V to 5.5 V		16		16	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 2.3 V to 2.7 V		200		200	ns/V
		V_{CC} = 3 V to 3.6 V		100		100	
		V_{CC} = 4.5 V to 5.5 V		20		20	
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 5: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	SN54LV373A			SN74LV373A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}		I_{OH} = −50 µA	2 V to 5.5 V	V_{CC}−0.1			V_{CC}−0.1			V
		I_{OH} = −2 mA	2.3 V	2			2			
		I_{OH} = −8 mA	3 V	2.48			2.48			
		I_{OH} = −16 mA	4.5 V	3.8			3.8			
V_{OL}		I_{OL} = 50 µA	2 V to 5.5 V			0.1			0.1	V
		I_{OL} = 2 mA	2.3 V			0.4			0.4	
		I_{OL} = 8 mA	3 V			0.44			0.44	
		I_{OL} = 16 mA	4.5 V			0.55			0.55	
	I_I	V_I = 5.5 V or GND	0 to 5.5 V			±1			±1	µA
	I_{OZ}	V_O = V_{CC} or GND	5.5 V			±5			±5	µA
	I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20			20	µA
	I_{off}	V_I or V_O = 0 to 5.5 V	0			5			5	µA
	C_i	V_I = V_{CC} or GND	3.3 V		2.9			2.9		pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV373A		SN74LV373A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		6		6.5		6.5		ns
t_{su}	Setup time, data before LE↓	High or low	4.5		5		5		ns
t_h	Hold time, data after LE↓	High or low	1.5		1.5		1.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV373A		SN74LV373A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		5		5		5		ns
t_{su}	Setup time, data before LE↓	High or low	4		4		4		ns
t_h	Hold time, data after LE↓	High or low	1		1		1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		SN54LV373A		SN74LV373A		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high		5		5		5		ns
t_{su}	Setup time, data before LE↓	High or low	4		4		4		ns
t_h	Hold time, data after LE↓	High or low	1		1		1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV373A		SN74LV373A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	C_L = 15 pF		8.3*	15.2*	1*	17*	1	17	ns
	LE	Q			9.1*	15.7*	1*	19*	1	19	
t_{en}	$\overline{OE}$	Q			8.9*	15.8*	1*	19*	1	19	
t_{dis}	$\overline{OE}$	Q			6.2*	12.6*	1*	15*	1	15	
t_{pd}	D	Q	C_L = 50 pF		10.4	18	1	21	1	21	ns
	LE	Q			11.1	18.6	1	22	1	22	
t_{en}	$\overline{OE}$	Q			10.9	18.8	1	22	1	22	
t_{dis}	$\overline{OE}$	Q			8.3	17.4	1	19	1	19	
$t_{sk(o)}$						2				2	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV373A		SN74LV373A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	C_L = 15 pF		5.8*	11.4*	1*	13.5*	1	13.5	ns
	LE	Q			6.4*	11*	1*	13*	1	13	
t_{en}	$\overline{OE}$	Q			6.3*	11.4*	1*	13.5*	1	13.5	
t_{dis}	$\overline{OE}$	Q			4.7*	10*	1*	12*	1	12	
t_{pd}	D	Q	C_L = 50 pF		7.3	14.9	1	17	1	17	ns
	LE	Q			7.8	14.5	1	16.5	1	16.5	
t_{en}	$\overline{OE}$	Q			7.7	14.9	1	17	1	17	
t_{dis}	$\overline{OE}$	Q			6	13.2	1	15	1	15	
$t_{sk(o)}$						1.5				1.5	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54LV373A		SN74LV373A		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	D	Q	C_L = 15 pF		4.1*	7.2*	1*	8.5*	1	8.5	ns
	LE	Q			4.5*	7.2*	1*	8.5*	1	8.5	
t_{en}	$\overline{OE}$	Q			4.5*	8.1*	1*	9.5*	1	9.5	
t_{dis}	$\overline{OE}$	Q			3.3*	7.2*	1*	8.5*	1	8.5	
t_{pd}	D	Q	C_L = 50 pF		5.1	9.2	1	10.5	1	10.5	ns
	LE	Q			5.5	9.2	1	10.5	1	10.5	
t_{en}	$\overline{OE}$	Q			5.5	10.1	1	11.5	1	11.5	
t_{dis}	$\overline{OE}$	Q			4	9.2	1	10.5	1	10.5	
$t_{sk(o)}$						1				1	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C (see Note 6)

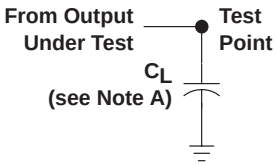
PARAMETER		SN74LV373A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		−0.6	−0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		2.9		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

NOTE 6: Characteristics are for surface-mount packages only.

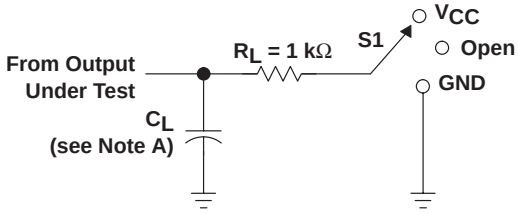
operating characteristics, T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	Outputs enabled	C_L = 50 pF, f = 10 MHz	3.3 V	17.4	pF
				5 V	19.5	

PARAMETER MEASUREMENT INFORMATION

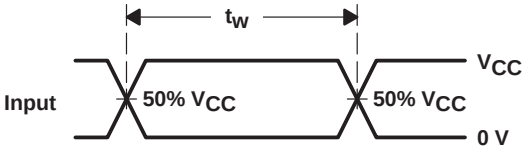


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

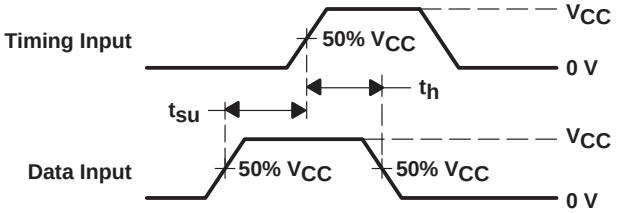


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

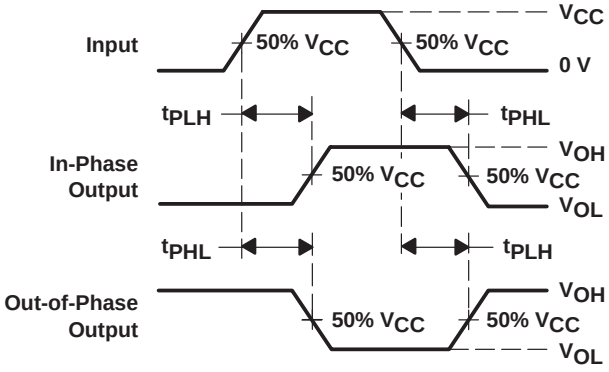
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



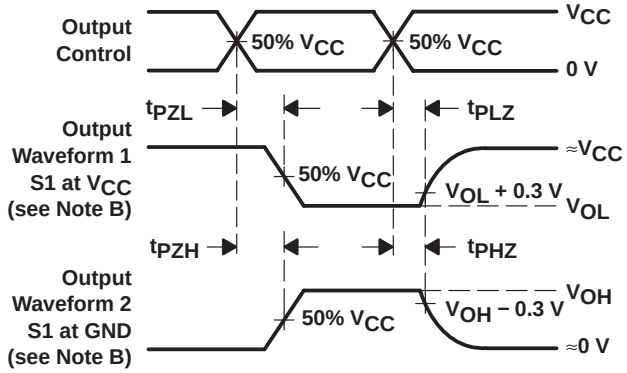
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

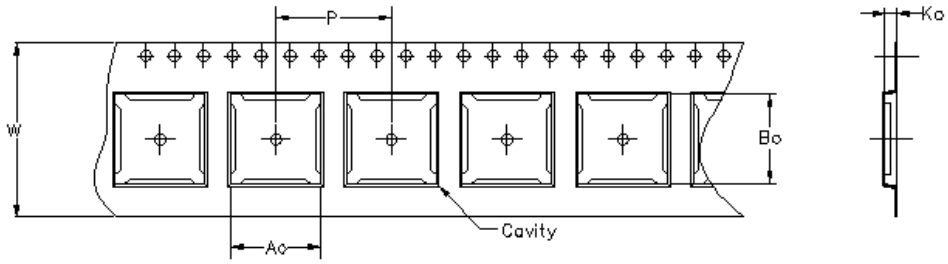
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74LV373ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373ADBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373ADBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373ADGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373ADGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373ADGVRG4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373ADWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373ADWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373ADWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373ADWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373AGQNR	NRND	BGA MICROSTAR JUNIOR	GQN	20	1000	TBD	SNPB	Level-1-240C-UNLIM
SN74LV373ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373ANSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373ANSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373APWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373APWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373APWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373APWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373APWT	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373APWTE4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74LV373APWTG4	ACTIVE	TSSOP	PW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LV373ARGYR	ACTIVE	QFN	RGY	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74LV373ARGYRG4	ACTIVE	QFN	RGY	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN74LV373AZQNR	ACTIVE	BGA MICROSTAR JUNIOR	ZQN	20	1000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

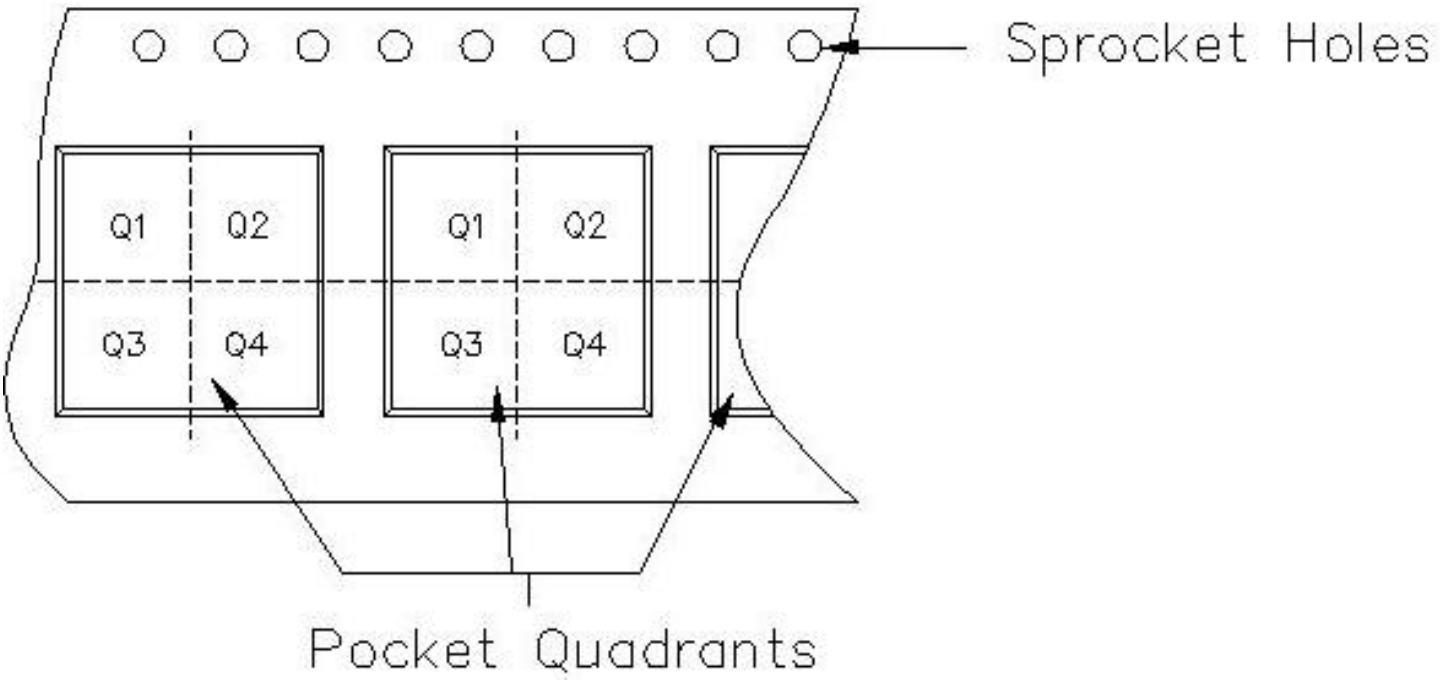
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



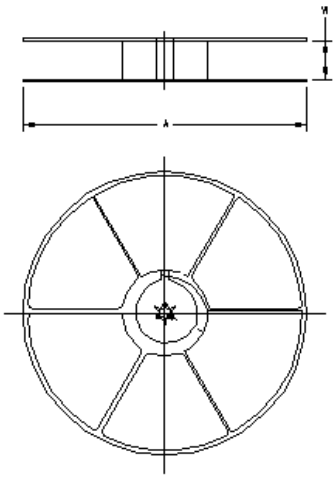
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



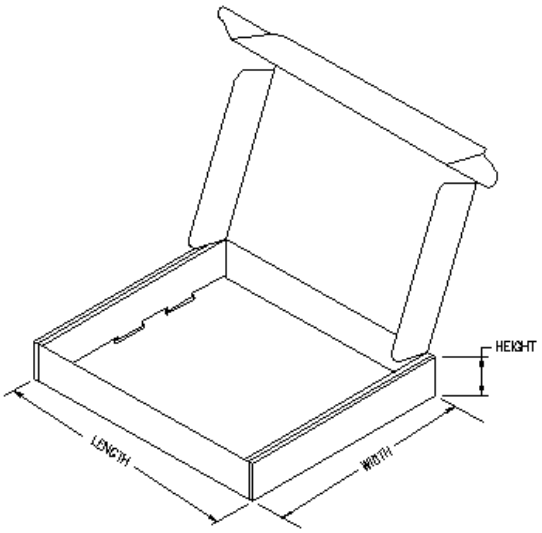
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV373ADBR	DB	20	MLA	330	16	8.2	7.5	2.5	12	16	Q1
SN74LV373ADGVR	DGV	20	MLA	330	12	7.0	5.6	1.6	8	12	Q1
SN74LV373ADWR	DW	20	MLA	330	24	10.8	13.0	2.7	12	24	Q1
SN74LV373AGQNR	GQN	20	HIJ	330	12	3.3	4.3	1.5	8	12	Q1
SN74LV373AGQNR	GQN	20	TAI	330	12	3.3	4.3	1.6	8	12	Q1
SN74LV373ANSR	NS	20	MLA	330	24	8.2	13.0	2.5	12	24	Q1
SN74LV373APWR	PW	20	MLA	330	16	6.95	7.1	1.6	8	16	Q1
SN74LV373ARGYR	RGY	20	MLA	180	12	3.8	4.8	1.6	8	12	Q1
SN74LV373AZQNR	ZQN	20	HIJ	330	12	3.3	4.3	1.5	8	12	Q1
SN74LV373AZQNR	ZQN	20	TAI	330	12	3.3	4.3	1.6	8	12	Q1

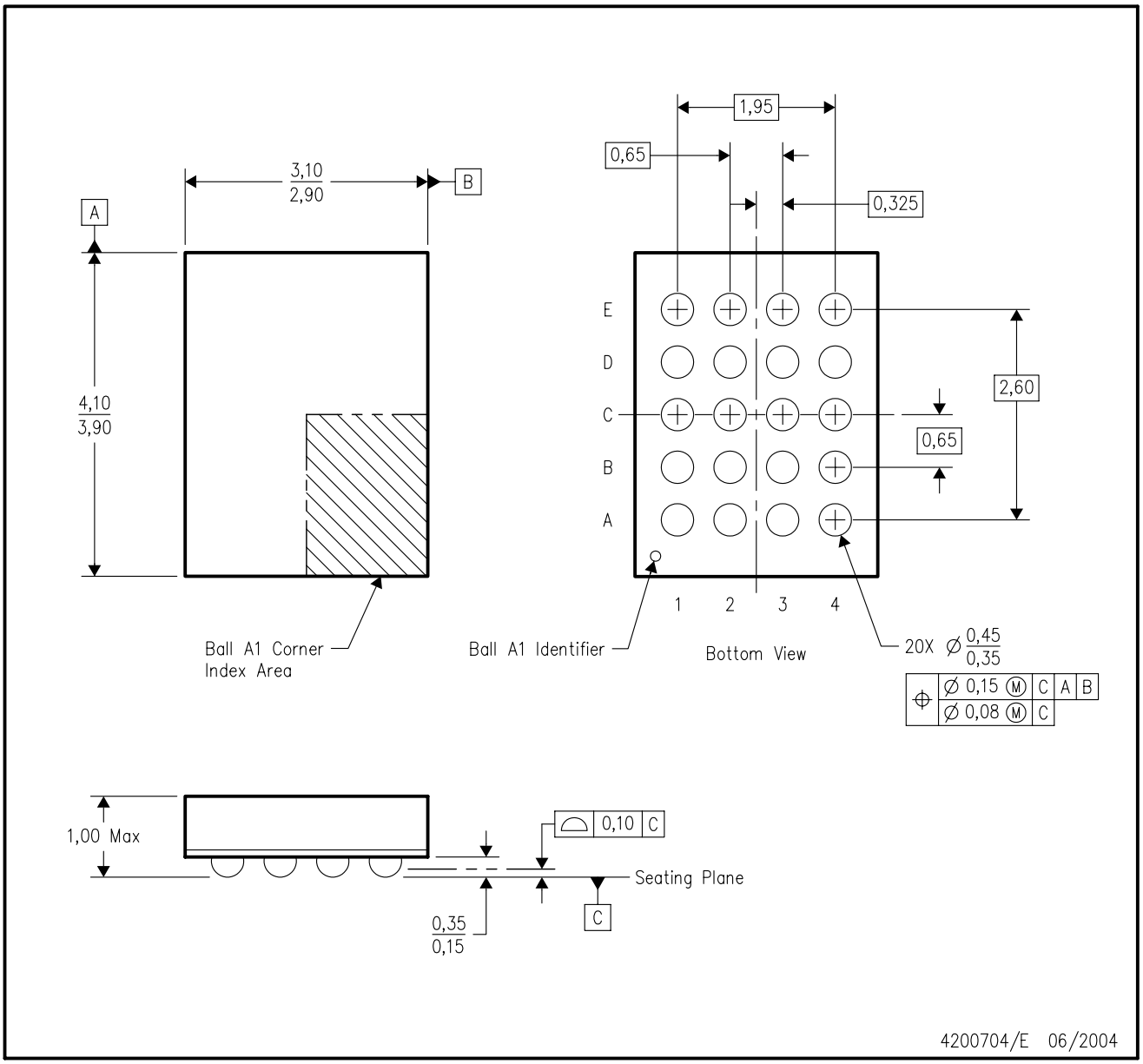


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74LV373ADBR	DB	20	MLA	342.9	336.6	28.58
SN74LV373ADGVR	DGV	20	MLA	338.1	340.5	20.64
SN74LV373ADWR	DW	20	MLA	333.2	333.2	31.75
SN74LV373AGQNR	GQN	20	HIJ	346.0	346.0	29.0
SN74LV373AGQNR	GQN	20	TAI	338.1	340.5	20.64
SN74LV373ANSR	NS	20	MLA	333.2	333.2	31.75
SN74LV373APWR	PW	20	MLA	342.9	336.6	28.58
SN74LV373ARGYR	RGY	20	MLA	190.0	212.7	31.75
SN74LV373AZQNR	ZQN	20	HIJ	346.0	346.0	29.0
SN74LV373AZQNR	ZQN	20	TAI	338.1	340.5	20.64

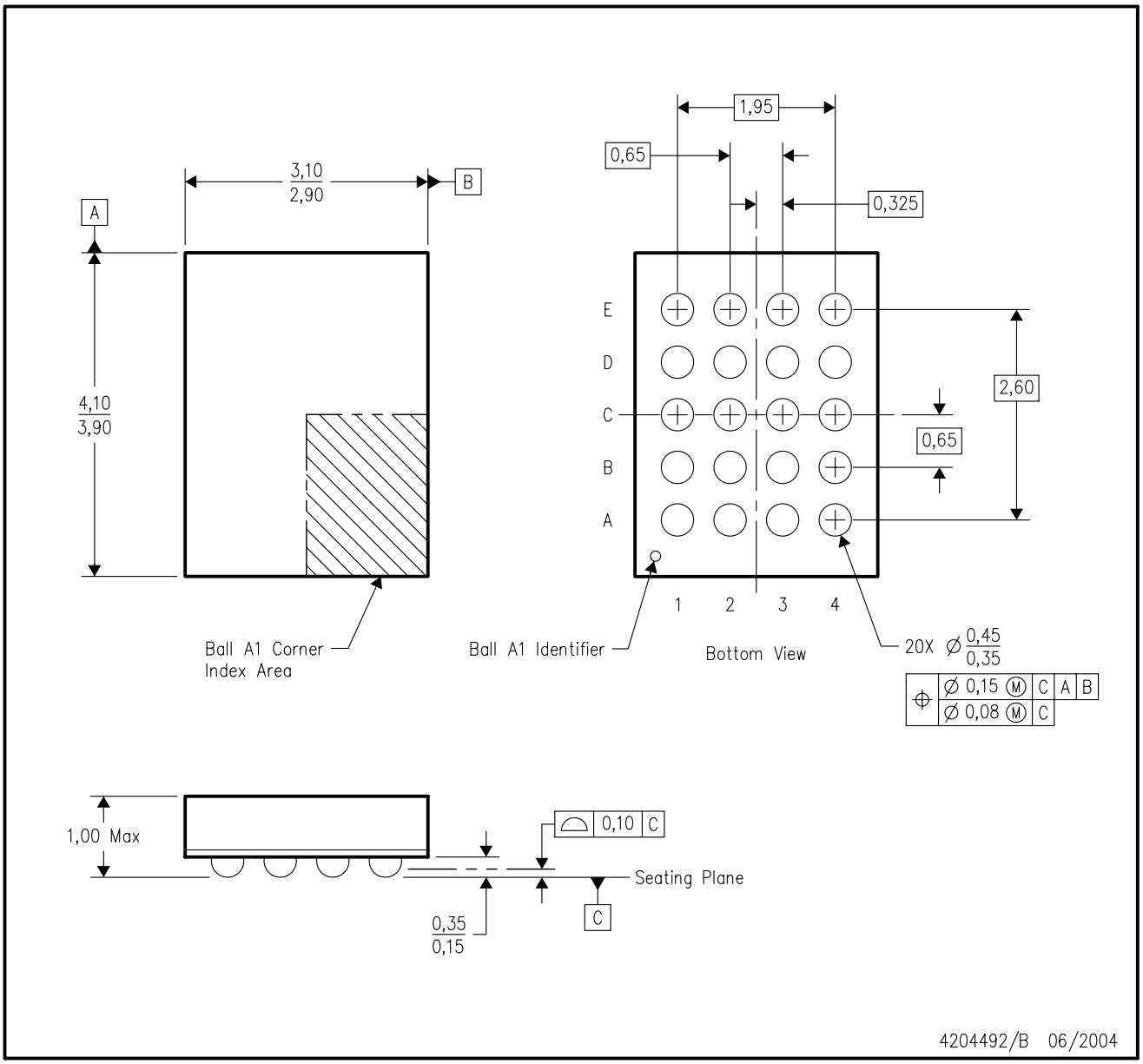

HEIGHT
LENGTH
WIDTH

GQN (R–PBGA–N20) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225 variation BC.
D. This package is tin–lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead–free.

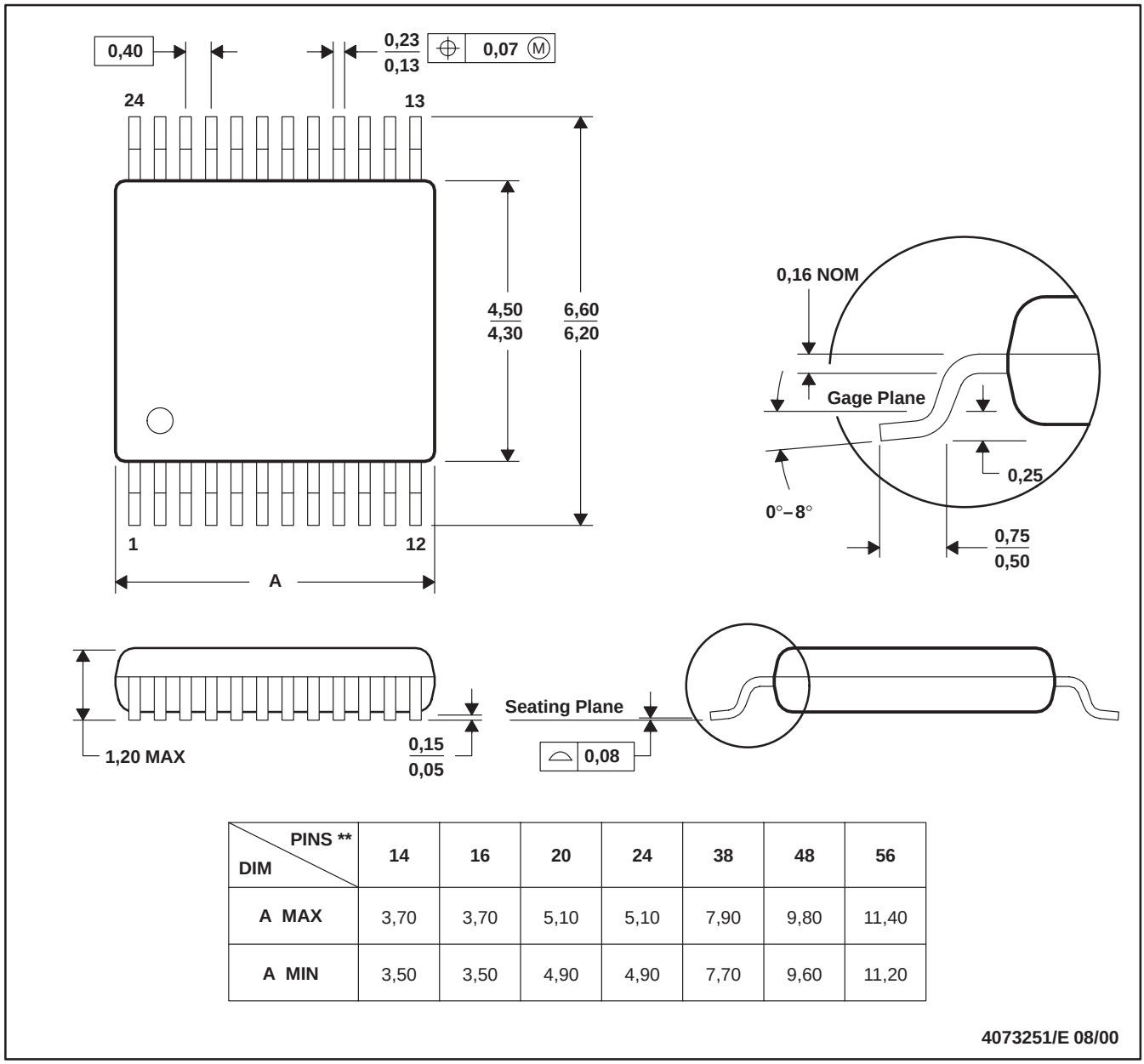
ZQN (R–PBGA–N20) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225 variation BC.
D. This package is lead–free. Refer to the 20 GQN package (drawing 4200704) for tin–lead (SnPb).

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

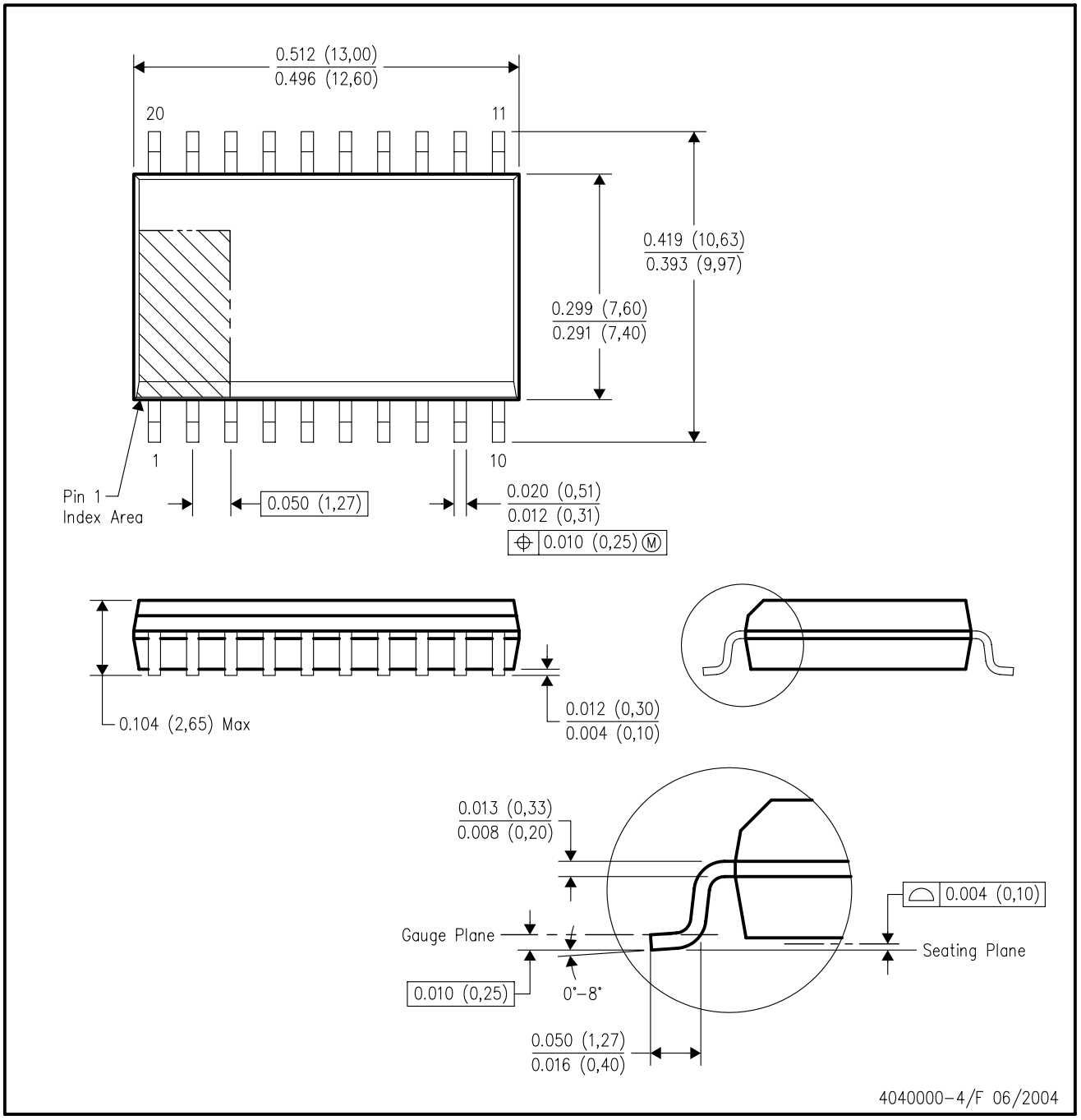


DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

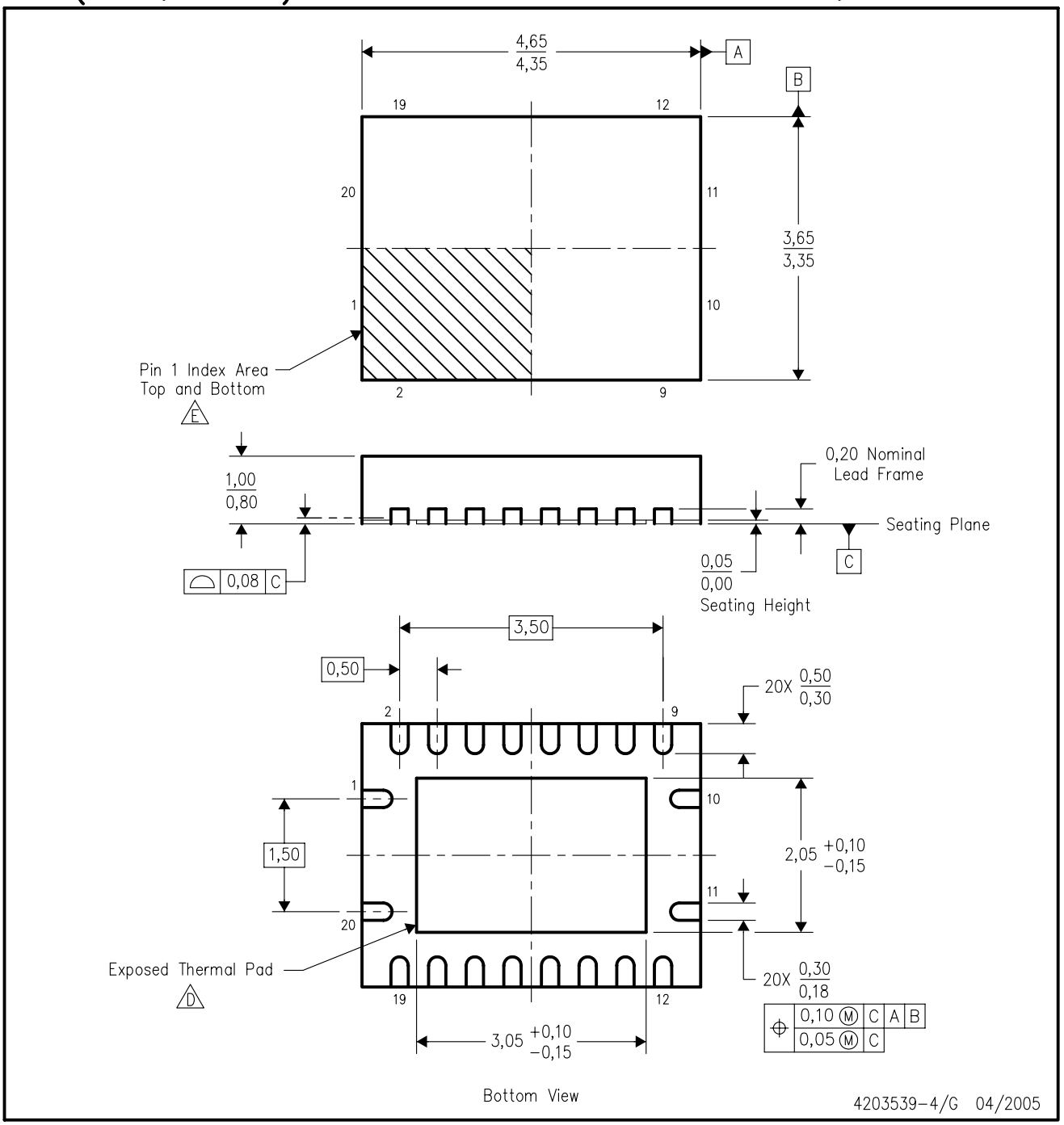
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

DW (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AC.

RGY (R–PQFP–N20) PLASTIC QUAD FLATPACK

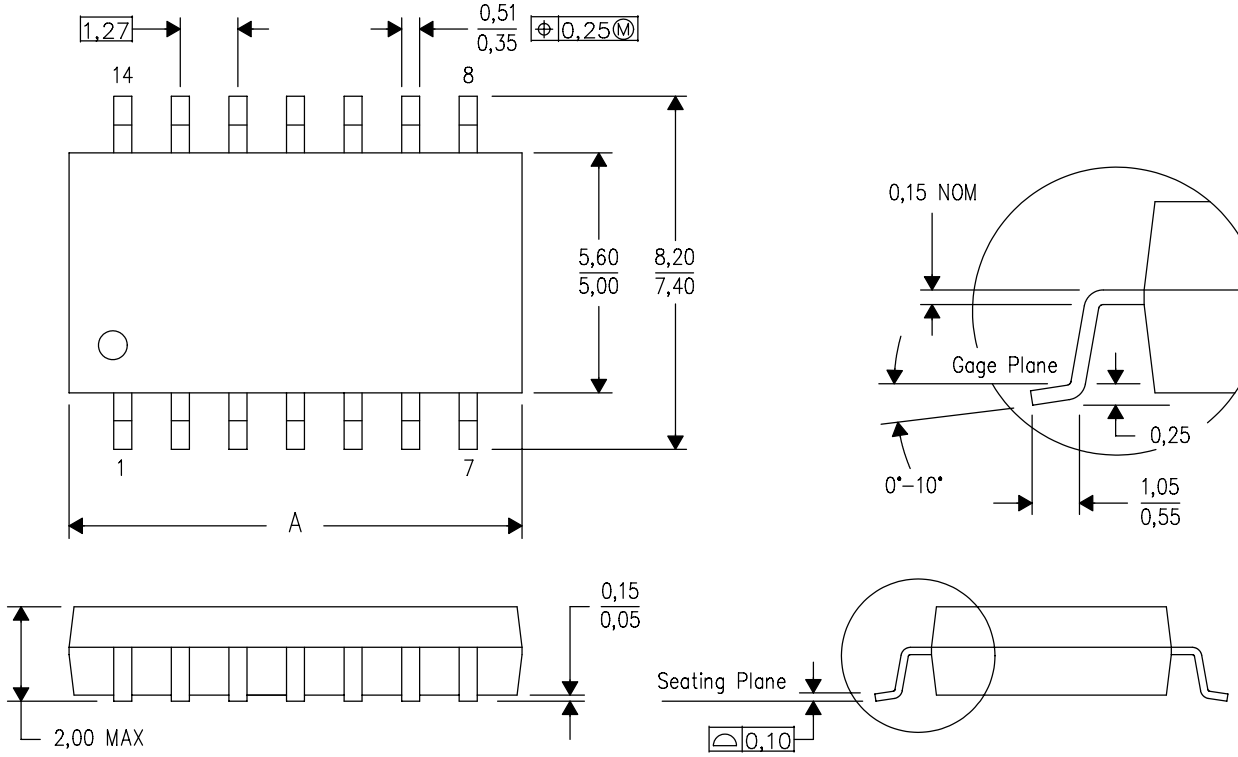


NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
F. Package complies to JEDEC MO–241 variation BC.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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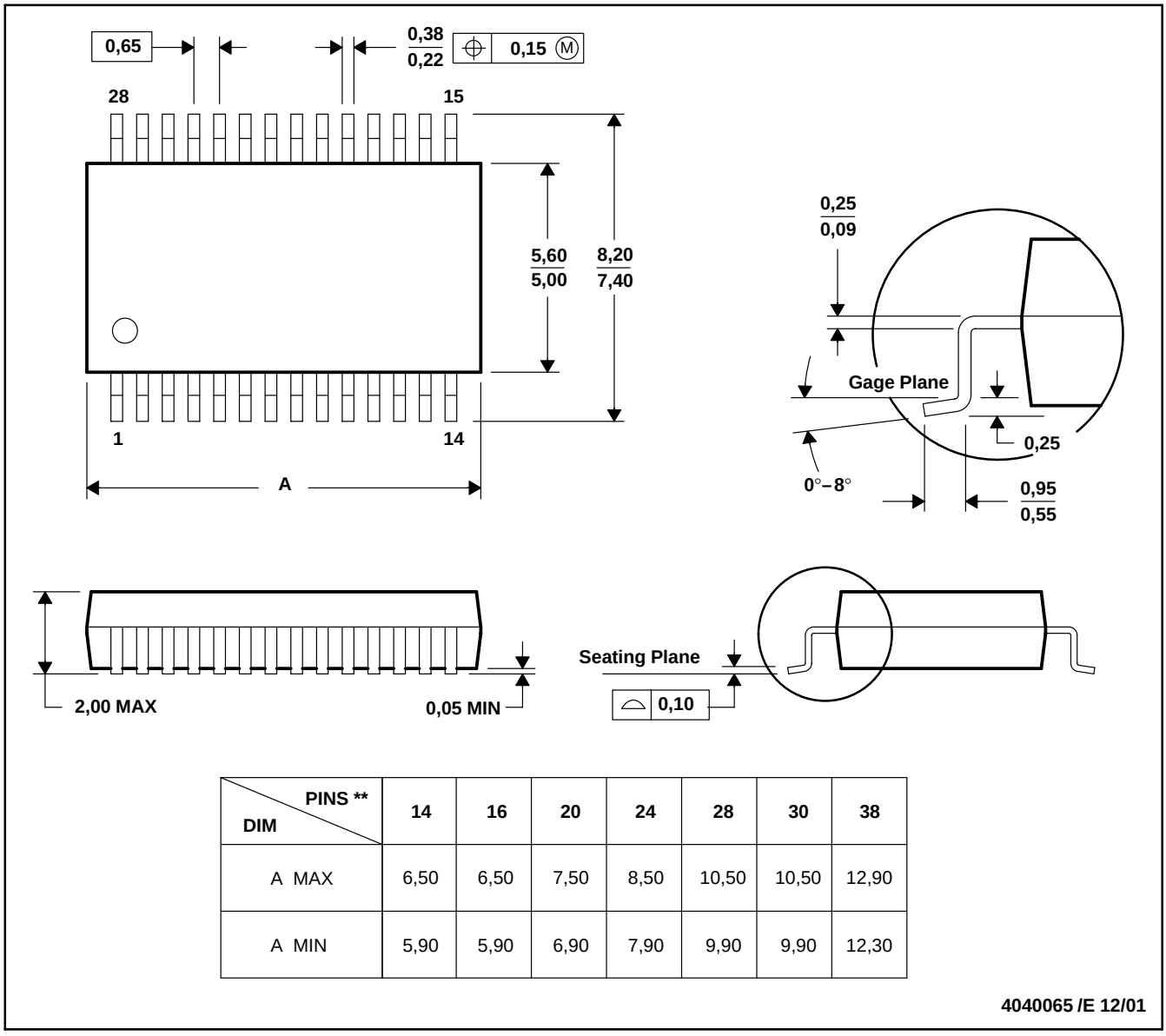
DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



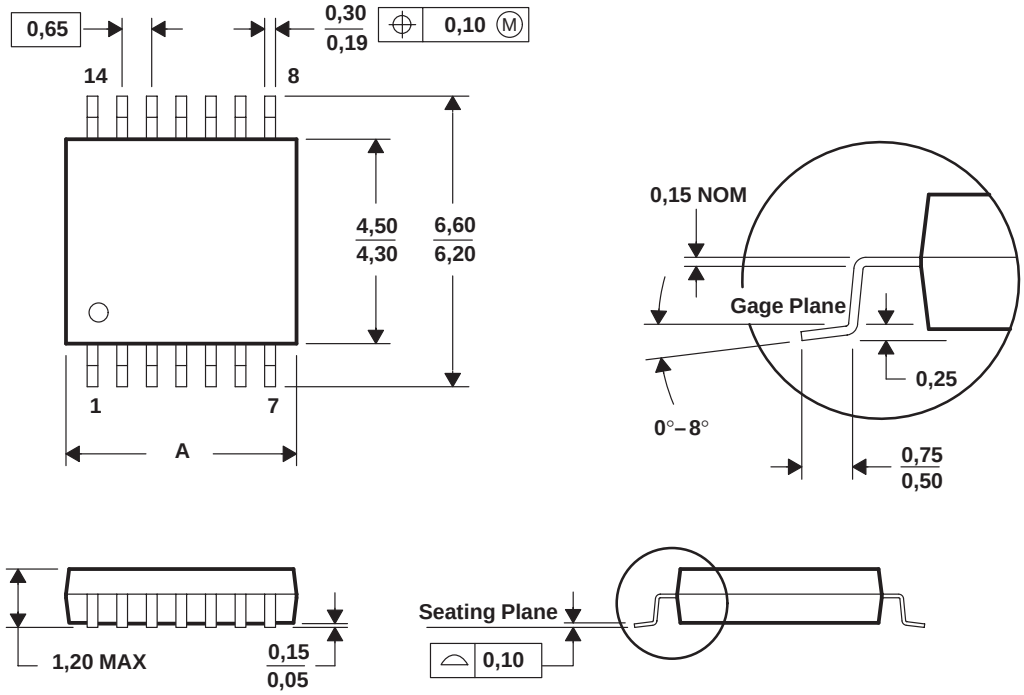
DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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