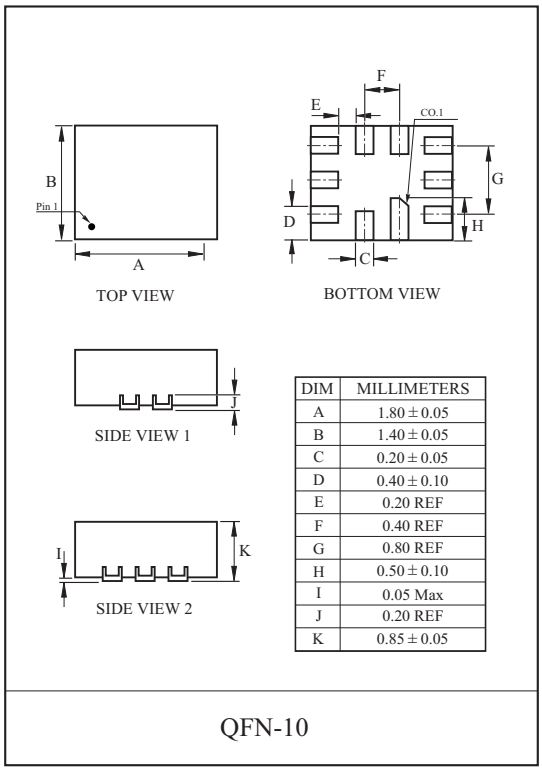
HIGH-SPEED(480Mbps) USB2.0 DPDT SWITCH

DESCRIPTION

The KUSB50QN is a High-Speed(480Mbps) USB2.0 signal switch. Configured as a double-pole double-throw (DPDT) switch, it is optimized for switching between 2 Hi-Speed sources or a Hi-Speed(480Mbps) and Full-Speed(12Mbps) source. Its wide Bandwidth (720MHz) is wide enough to pass High-Speed USB2.0 differential signals. Industry-leading advantages include a propagation delay of less than 250ps, resulting from its low channel resistance and low on capacitance. It is bidirectional and offers little or no attenuation of the High-Speed signal at the outputs.

Its high channel-to-channel crosstalk rejection results in minimal noise interference. The switch is designed to minimize current consumption even when the control voltage applied to the S pin, is lower than the V_{CC}. The KUSB50QN also offers over-voltage protection per the USB2.0 Specification. With the chip powered ON or OFF, all data I/O pins can withstand a short to Vbus(5.25V).



DIM	MILLIMETERS
A	1.80 ± 0.05
B	1.40 ± 0.05
C	0.20 ± 0.05
D	0.40 ± 0.10
E	0.20 REF
F	0.40 REF
G	0.80 REF
H	0.50 ± 0.10
I	0.05 Max
J	0.20 REF
K	0.85 ± 0.05

QFN-10

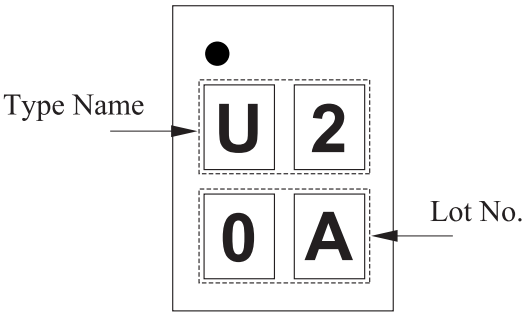
FEATURES

- USB2.0 compliant (High-speed and Full-speed).
- Low On Resistance, 5.5Ω(Typ) @ V_{CC}=3V .
- Channel On Capacitance, 6.5pF(Typ) @ f=1㎒.
- Low Power Consumption (Max :1㎂)
  : 10㎂Maximum I_{CCT} over an Expanded Voltage Range (V_{IN}=1.8V, V_{CC}=4.3V).
- Wide-3dB bandwidth, >720MHz.
- High ESD Protection.
  :Data Pin ESD Rating : 8.0kV(HBM)
  Control Pin ESD Rating : 8.0kV(HBM)
  Power/GND ESD Rating : > 20kV(HBM)
  All pins ESD Rating : 300V(MM).
- Power Off protection
  : When V_{CC} =0V, D+/D -can tolerate up to 5.25V

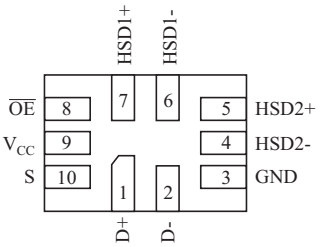
APPLICATIONS

- Routes signals for USB2.0
- Differential Signal Data Routing
- Hand-held devices

Marking

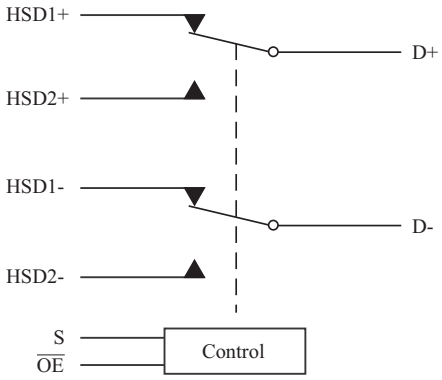


Pin Configuration



Top View

Block Diagram



Truth Table

S	OE	Diretion
X	HIGH	Disconnect
HIGH	LOW	D+, D- = HSD1x
LOW	LOW	D+, D- = HSD2x

Pin Descriptions

PIN	NAME		Function
1	D+	Dx	Data Port
2	D-		Data Port
3	GND		Ground
4	HSD2-	HSDnx	Data Port
5	HSD2+		Data Port
6	HSD1-		Data Port
7	HSD1+		Data Port
8	$\overline{OE}$ (OE-)		Bus Switch Enable Control
9	V_{CC}		Supply Voltage
10	S		Select Input Control

Absolute Maximum Ratings

CHARACTERISTIC	SYMBOL	RATING		UNIT
Supply Voltage	V_{CC}	-0.5 ~ 4.6		V
Control Port Input Voltage (S, OE-)	V_{IN}	-0.5 ~ 4.6		V
Switch Input Voltage (HSDnx, Dx)	V_{SW}	HSDnx	-0.5 ~ V_{CC}+0.5	V
		Dx @V_{CC}>0	-0.5 ~ V_{CC}+0.5	
		Dx @V_{CC}=0	5.25	
Data Port Output Current	I_{OD}	120		mA
Power Dissipation	P_D	0.5		W
Operating Ambient Temperature	T_a	-40 ~ +85		℃
Storage Temperature Range	T_{stg}	-65 ~ +150		℃

DC Electrical Characteristics(1) (V_{CC}=3.0~4.3V, Ta = -40~85℃)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input HIGH Voltage	V_{IH}	V_{CC}=4.3V	1.7	-	-	V
		V_{CC}=3.0V	1.3	-	-	V
Input LOW Voltage	V_{IL}	V_{CC}=4.3V	-	-	0.7	V
		V_{CC}=3.0V	-	-	0.5	V
Clamp Diode Voltage	V_{IK}	V_{CC}=Max, I_{IN}=-18mA	-	-0.7	-1.2	V
Control Input Leakage	I_{IN}	V_{CC}=Max, 0≤V_{IN}≤V_{CC}	-1.0	-	1.0	μA
OFF State Leakage	I_{OZ}	V_{CC}=V_{OE-}=Max, 0≤V_{SW}≤V_{CC}	-2.0	-	2.0	μA
Power OFF Leakage Current (D+, D-)	I_{OFF}	V_{CC}=0V, 0≤V_{SW}≤4.3V	-2.0	-	2.0	μA
Quiescent Supply Current	I_{CC}	V_{CC}=Max, V_{IN}=0V or V_{CC}	-	-	1.0	μA
Increase in I_{CC} per Control Voltage	I_{CCT}	V_{CC}=Max, V_{IN}=1.8V	-	-	10.0	μA
Switch ON Resistance	R_{ON}	V_{CC}=Min, 0V≤V_{SW}≤1.0V, I_{ON}=-40mA	-	5.5	6.5	Ω
ON Resistance Flatness	$R_{FLAT(ON)}$	V_{CC}=Min, 0V≤V_{SW}≤1.0V, I_{ON}=-40mA	-	1.5	-	Ω
ON Resistance Match from Center Port to any other port	ΔR_{ON}	V_{CC}=Min, V_{SW}=1.0V, I_{ON}=-40mA	-	0.2	0.35	Ω

Note(1) : All typical values are at V_{CC}=3.3V(unless otherwise noted), Ta=25℃

Capacitance Characteristics(1) (Ta =-40~85℃, f=1㎒)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	FIGURE NO.
HSDnx, Dnx, Switch ON Capacitance	C_{ON}	V_{CC}=3.3V, V_{OE-}=0V	-	6.5	-	pF	6
HSDnx, Switch OFF Capacitance	C_{OFF}	V_{CC}=3.3V, V_{OE-}=3.3V	-	3.0	-	pF	7
Control Pin Input Capacitance	C_{IN}	V_{CC}=0V	-	3.6	-	pF	7

AC Electrical Characteristics(1) (Ta = -40~85°C)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS	FIGURE NO.
Propagation Delay(2)	t_{PD}	V_{CC}=3.3V, R_L=50Ω, C_L=5pF		-	0.25	-	ns	9
Turn-On Time	t_{ON}	3.0≤V_{CC}≤3.6V, V_{SW}=0.8V, R_L=50Ω, C_L=5pF		-	13.0	30.0	ns	10
Turn-Off Time	t_{OFF}	3.0≤V_{CC}≤3.6V, V_{SW}=0.8V, R_L=50Ω, C_L=5pF		-	12.0	25.0	ns	
Break-Before-Make	t_{BBM}	3.0≤V_{CC}≤3.6V, V_{SW}=0.8V, R_L=50Ω, C_L=5pF		2.0	-	6.5	ns	11
-3dB Bandwidth	BW	3.0≤V_{CC}≤3.6V, R_T=50Ω	C_L=0pF	-	720	-	MHz	13
			C_L=5pF	-	550	-		
Off Isolation (Non-Adjacent)	O_{IRR}	3.0≤V_{CC}≤3.6V, R_T=50Ω, f=240MHz		-	-30.0	-	dB	14
Channel Crosstalk (Non-Adjacent)	X_{TALK}	3.0≤V_{CC}≤3.6V, R_T=50Ω, f=240MHz		-	-45.0	-	dB	15

Note(2) : Guaranteed by characterization.

AC Electrical Characteristics For USB2.0 High-Speed Switching (1) (Ta = -40~85°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	FIGURE NO.
Skew of Opposite Transitions of the Same Output(2)	$t_{SK(P)}$	3.0≤V_{CC}≤3.6V, R_L=50Ω, C_L=5pF	-	20	-	ps	12
Channel-to-Channel Skew(2)	$t_{SK(O)}$	3.0≤V_{CC}≤3.6V, R_L=50Ω, C_L=5pF	-	50	-	ps	
Total Jitter(2)	t_J(2)	3.0≤V_{CC}≤3.6V, R_L=50Ω, C_L=5pF t_R=t_F=500ps at 480Mbps	-	200	-	ps	-

Application Information

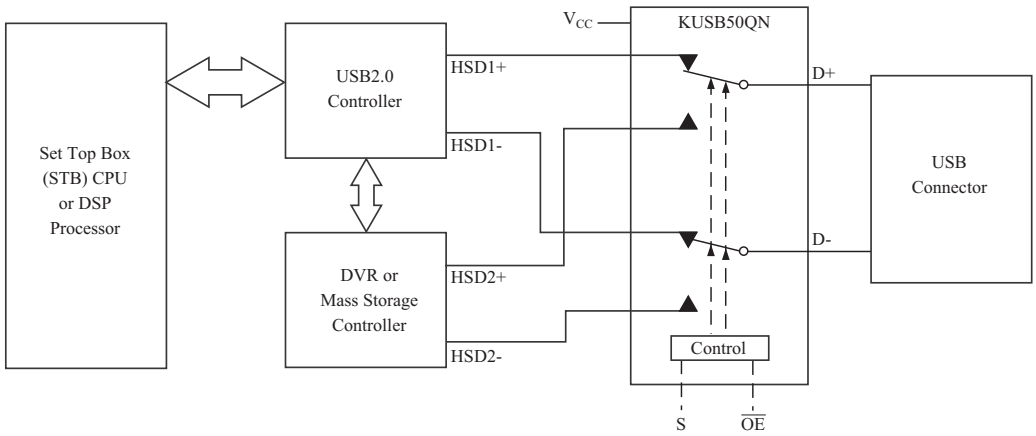
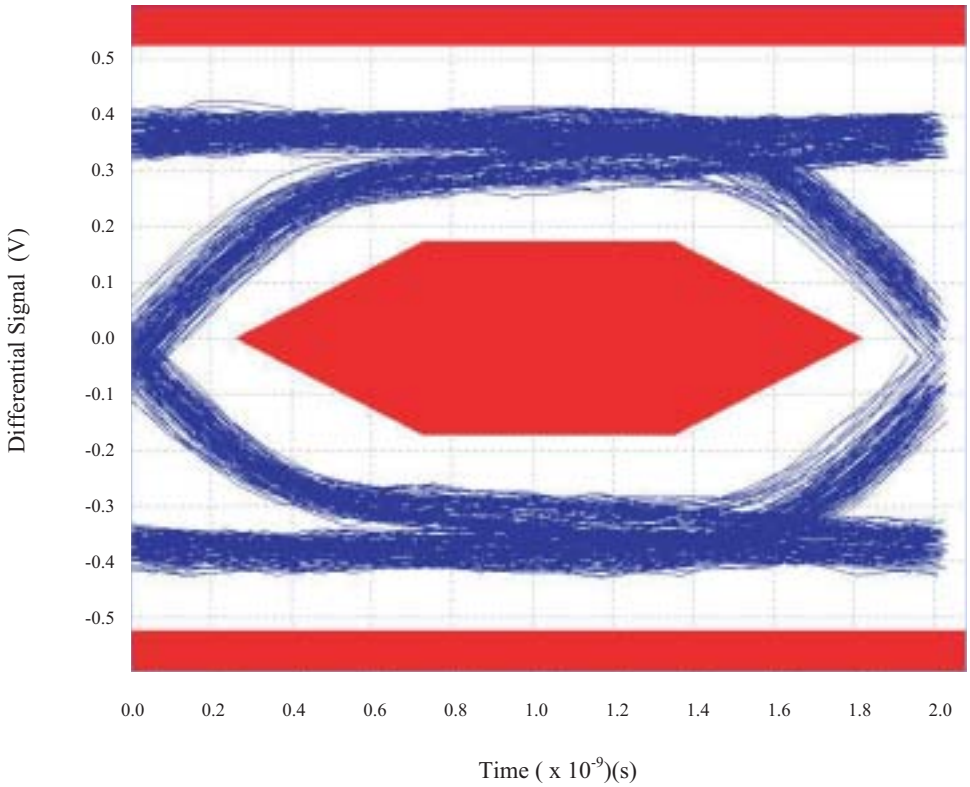
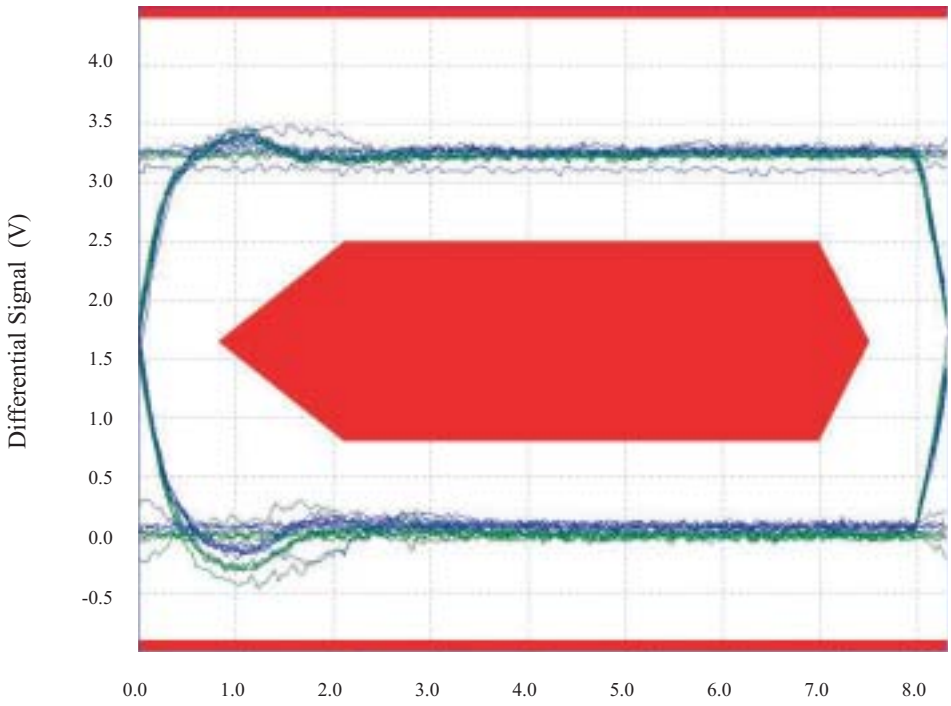


Fig. 1 Application Diagram



Measurement Name	Minimum	Maximum	Mean	RMS	STATUS
Eye Diagram Test	-	-	-	-	PASS
Signal Rate (Mbps)	442.4563	527.4987	480.0518	481.5582	PASS
EOP Width (Bits)		-	16.56572	-	PASS
Rise Time (ns)	788.3502	2.399811	1.222390	1.304253	PASS
Fall Time (ns)	798.1337	2.396142	1.214730	1.287723	PASS
Consecutive Jitter Range	-157.9ps to 139.6ps RMS Jitter 59.29ps				PASS
KJ Paired Jitter Range	-135.6ps to 138.3ps RMS Jitter 53.00ps				PASS
JK Paired Jitter Range	-110.1ps to 155.5ps RMS Jitter 49.48ps				PASS

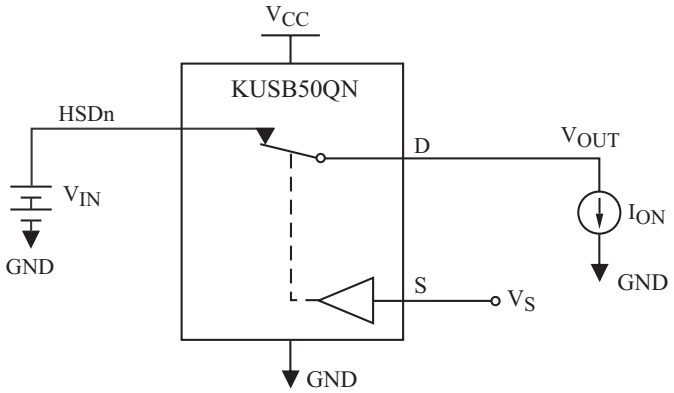
Fig. 2 High-Speed Eye Diagram



Measurement Name	Minimum	Maximum	Mean	RMS	STATUS
Eye Diagram Test	-	-	-	-	PASS
Signal Rate (Mbps)	11.98705	12.02102	12.00205	12.00283	PASS
Crossover Voltage	1.622501	1.735276	1.678898	-	PASS
EOP Width (Bits)		-	167.017	-	PASS
Rise Time (ns)	7.2297	7.5460	7.3464	7.3472	PASS
Fall Time (ns)	7.1852	7.6988	7.4212	7.4230	PASS
Consecutive Jitter Range	-188.3988ps to 140.1242ps RMS Jitter 91.71091ps				PASS
KJ Paired Jitter Range	-178.1923ps to 110.7530ps RMS Jitter 137.6440ps				PASS
JK Paired Jitter Range	-116.2675ps to 86.31155ps RMS Jitter 78.24693ps				PASS

Fig. 3 Full-Speed Eye Diagram

Test Diagram (Continued)

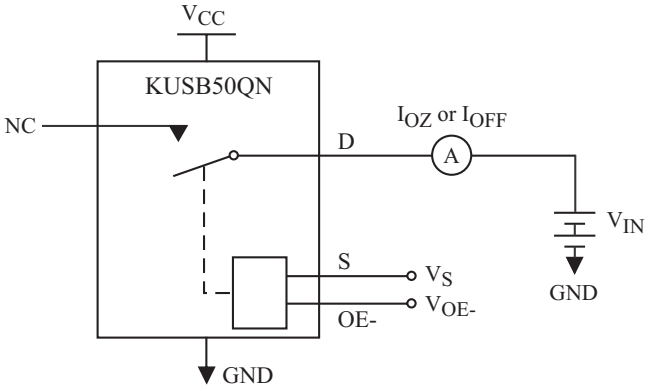


$R_{ON} = V_{ON} / I_{ON}$

$V_{ON} = V_{IN} - V_{OUT}$

$V_S = V_{IL}$ or V_{IH}

Fig. 4 Switch On Resistance



$I_{OFF} = (V_{CC} = 0V)$

I_{OZ} ($V_{OE-} = V_{CC}$)

$V_S = V_{IL}$ or V_{IH}

Each Data Ports is tested separately

Fig. 5 OFF Leakage

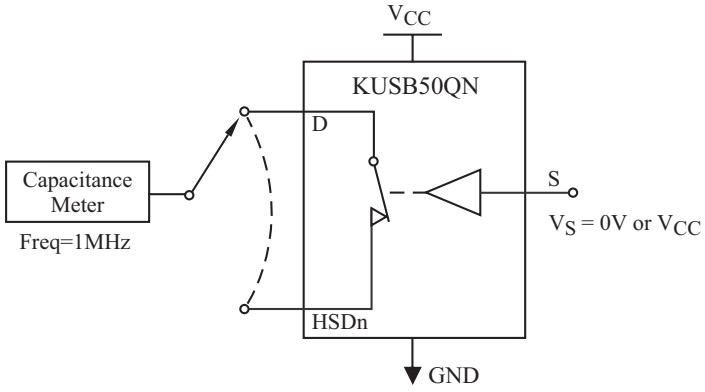


Fig. 6 Channel On Capacitance

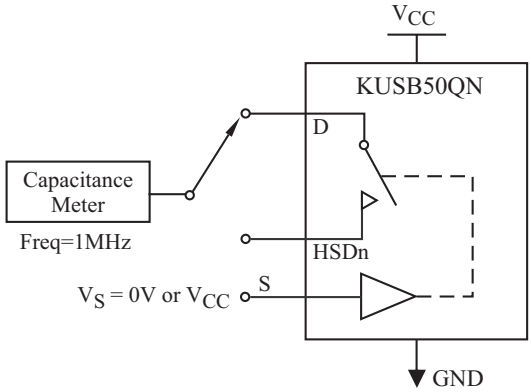
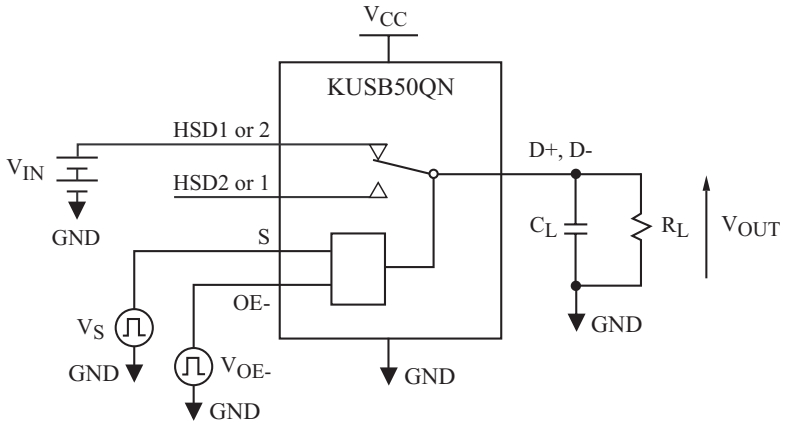


Fig. 7 Channel OFF Capacitance



1. R_L and C_L are functions of application environment.
2. C_L includes test jig and probe capacitance.

Fig. 8 AC Test Circuit

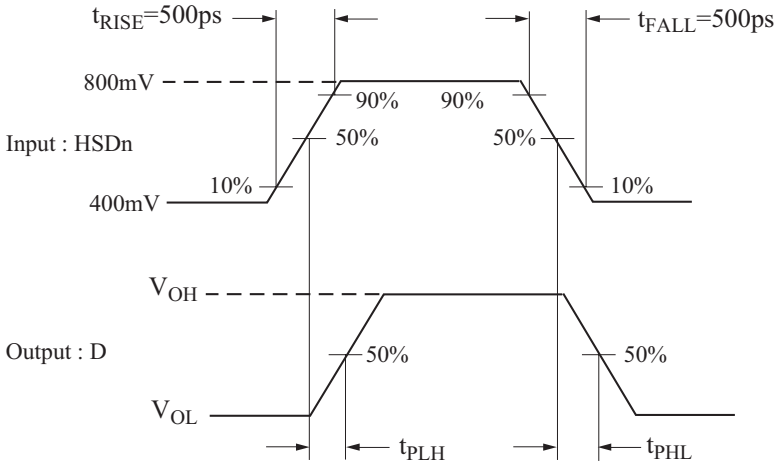


Fig. 9 Propagation Delay Time

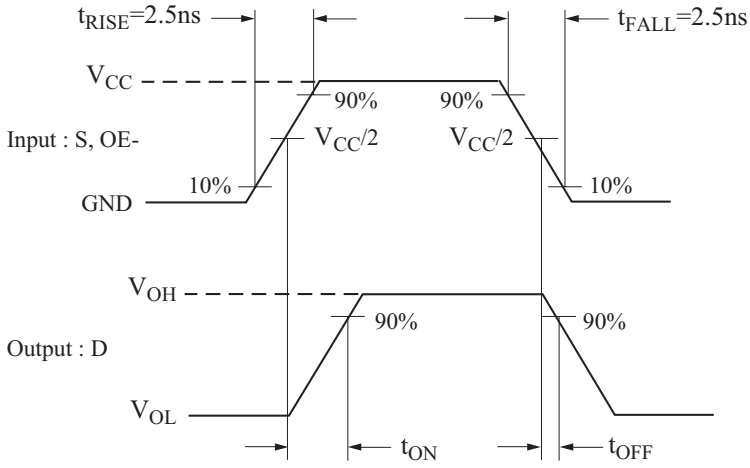
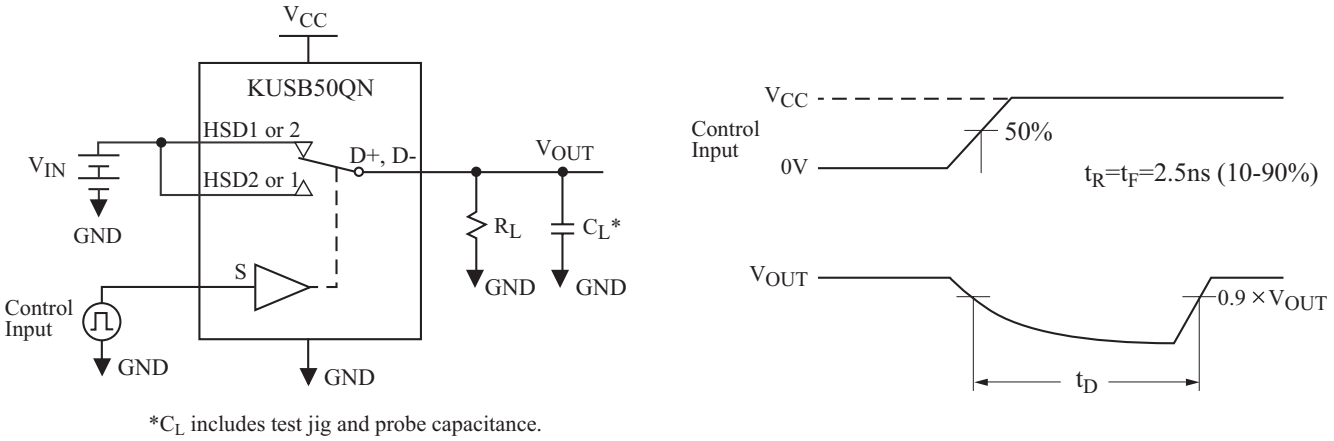
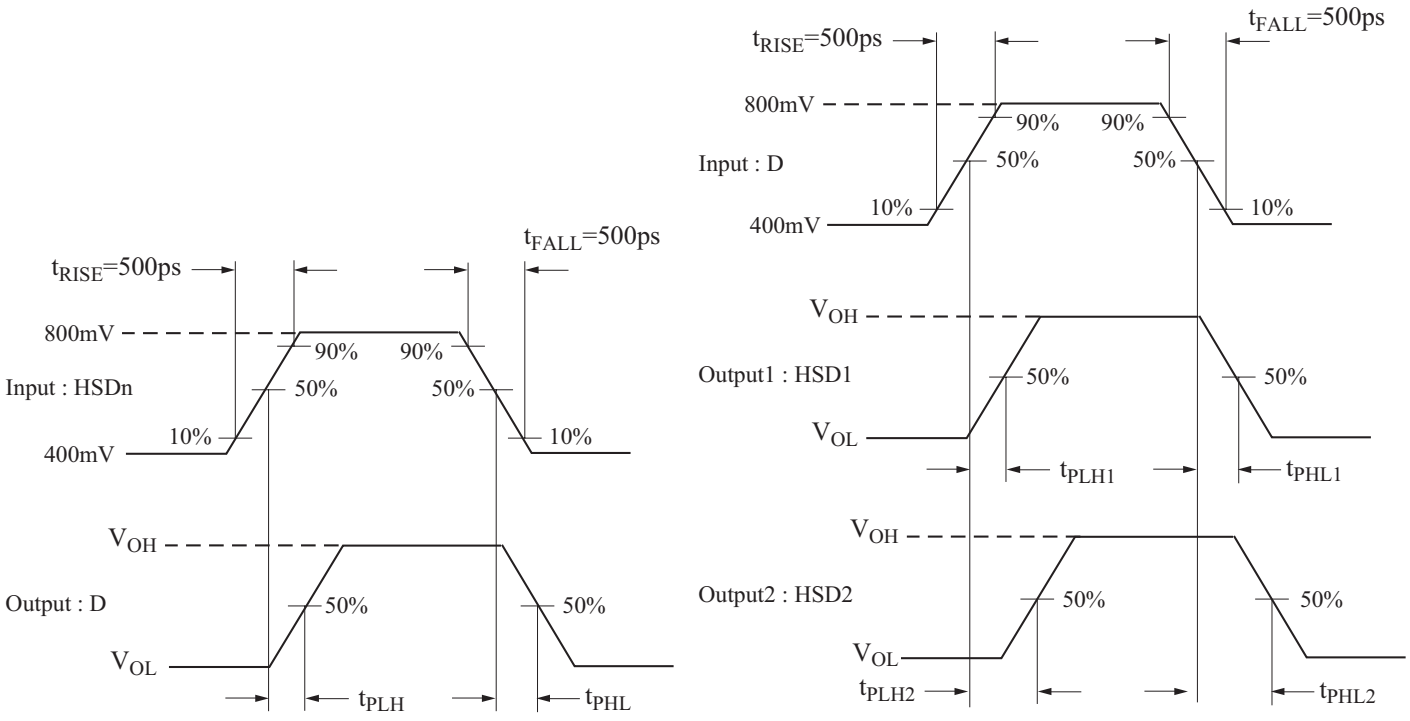


Fig. 10 Turn-On / Turn-Off Time



*C_L includes test jig and probe capacitance.

Fig. 11 Break-Before-Make



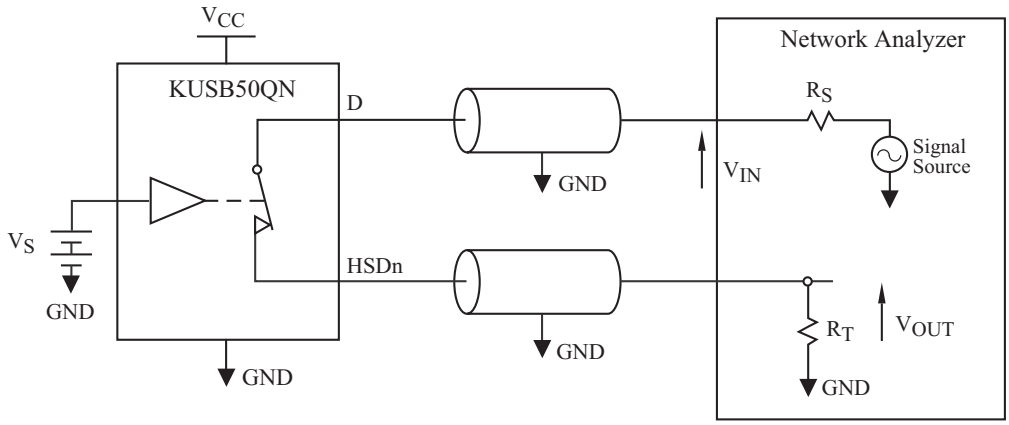
$T_{SK(P)} = |t_{PHL} - t_{PLH}|$

Pulse Skew, $T_{SK(P)}$

$T_{SK(O)} = |t_{PHL1} - t_{PLH2}|$ or $|t_{PHL1} - t_{PLH2}|$

Output Skew, $T_{SK(OUT)}$

Fig. 12 Skew Tests

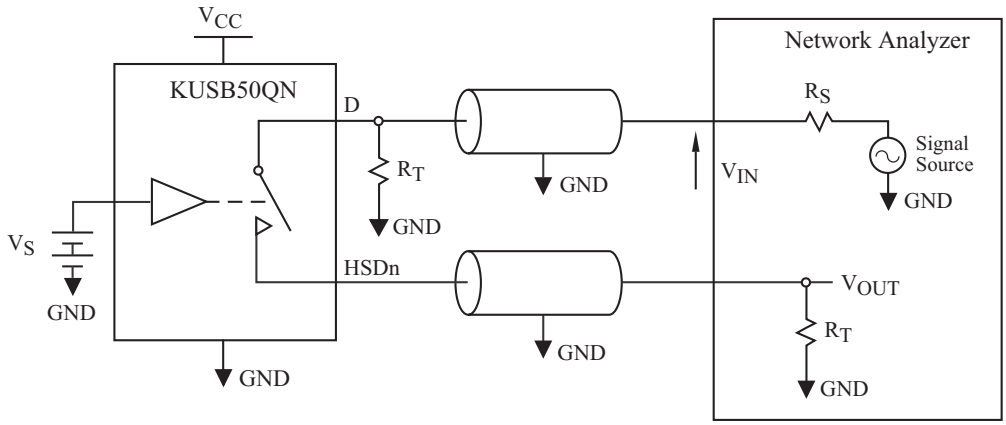


$BW = 20Log(V_{OUT}/V_{IN})$

R_S and R_T are functions of the application environment

Signal Source Direction can be reversed

Fig. 13 Bandwidth

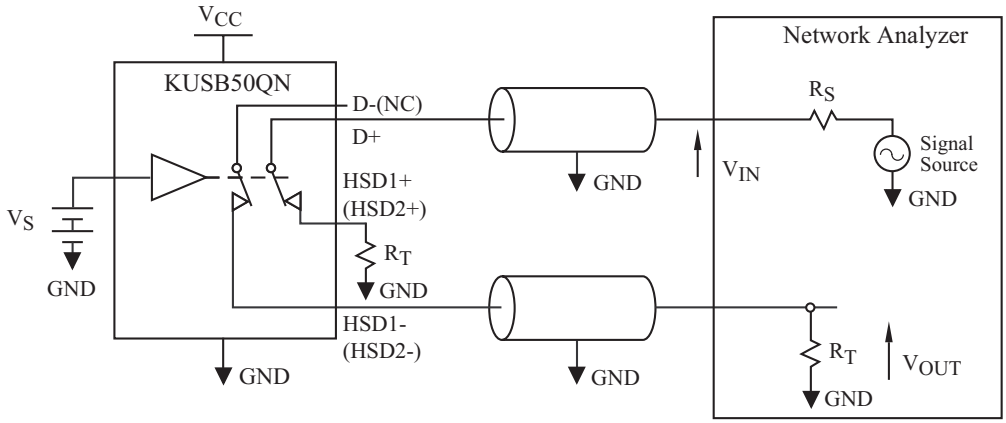


$O_{IRR} = 20Log(V_{OUT}/V_{IN})$

R_S and R_T are functions of the application environment

Signal Source Direction can be reversed

Fig. 14 Channel OFF Isolation



$X_{TALK} = 20Log(V_{OUT}/V_{IN})$

R_S and R_T are functions of the application environment

Signal Source Direction can be reversed

Fig. 15 Non-adjacent Channel-to-Channel Crosstalk