

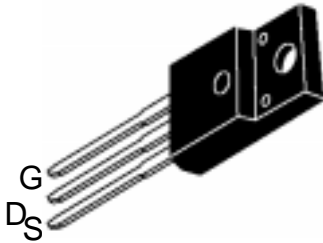


IRF640FP 18A 200V N CHANNEL POWER MOSFET

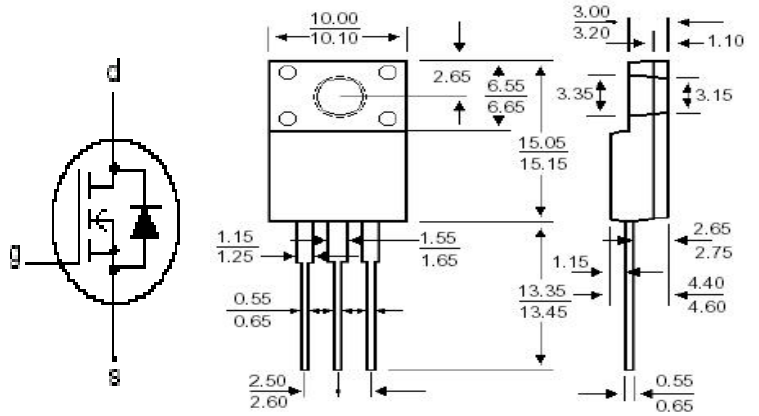
Description

Mechanical Dimensions

IRF640FP



ITO-220AB



DIMENSION IN MM

GENERAL DESCRIPTION

This Power MOSFET is designed for low voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

FEATURES

- ◆ Silicon Gate for Fast Switching Speeds
- ◆ Low $R_{DS(on)}$ to Minimize On-Losses. Specified at Elevated Temperature
- ◆ Rugged – SOA is Power Dissipation Limited
- ◆ Source-to-Drain Characterized for Use With Inductive Loads

ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|----------------|------------|------|
| Drain to Current – Continuous | I_D | 18 | A |
| – Pulsed | I_{DM} | 72 | |
| Gate-to-Source Voltage – Continue | V_{GS} | ± 20 | V |
| – Non-repetitive | V_{GSM} | ± 40 | V |
| Total Power Dissipation | P_D | 125 | W |
| Derate above 25°C | | 1.00 | W/°C |
| Operating and Storage Temperature Range | T_J, T_{STG} | -55 to 150 | °C |
| Single Pulse Drain-to-Source Avalanche Energy – $T_J = 25^\circ\text{C}$ ($V_{DD} = 100\text{V}, V_{GS} = 10\text{V}, I_L = 18\text{A}, L = 1.38\text{mH}, R_G = 25\Omega$) | E_{AS} | 224 | mJ |
| Thermal Resistance – Junction to Case | θ_{JC} | 1.00 | °C/W |
| – Junction to Ambient | θ_{JA} | 62.5 | |
| Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds | T_L | 260 | °C |

(1) Pulse Width and frequency is limited by $T_J(\text{max})$ and thermal response



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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, $T_J = 25^\circ\text{C}$.

| Characteristic | Symbol | IRF640 | | | Units |
|---|--|--------------|-----|--------------|----------|
| | | Min | Typ | Max | |
| Drain-Source Breakdown Voltage ($V_{GS} = 0\text{ V}$, $I_D = 250\ \mu\text{A}$) | $V_{(BR)DSS}$ | 200 | | | V |
| Drain-Source Leakage Current ($V_{DS} = \text{Rated } V_{DSS}$, $V_{GS} = 0\text{ V}$) ($V_{DS} = 0.8\text{Rated } V_{DSS}$, $V_{GS} = 0\text{ V}$, $T_J = 125^\circ\text{C}$) | I_{DSS} | | | 0.025 1.0 | mA |
| Gate-Source Leakage Current-Forward ($V_{gsf} = 20\text{ V}$, $V_{DS} = 0\text{ V}$) | I_{GSSF} | | | 100 | nA |
| Gate-Source Leakage Current-Reverse ($V_{gsr} = 20\text{ V}$, $V_{DS} = 0\text{ V}$) | I_{GSSR} | | | 100 | nA |
| Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$) | $V_{GS(th)}$ | 2.0 | | 4.0 | V |
| Static Drain-Source On-Resistance ($V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$) * | $R_{DS(on)}$ | | | 0.18 | Ω |
| Drain-Source On-Voltage ($V_{GS} = 10\text{ V}$) ($I_D = 5.0\text{ A}$) | $V_{DS(on)}$ | | | 6.0 | V |
| Forward Transconductance ($V_{DS} = 50\text{ V}$, $I_D = 10\text{ A}$) * | g_{FS} | 6.8 | | | mhos |
| Input Capacitance | $(V_{DS} = 25\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$) | C_{iss} | | 1600 | pF |
| Output Capacitance | | C_{oss} | | 750 | pF |
| Reverse Transfer Capacitance | | C_{rss} | | 300 | pF |
| Turn-On Delay Time | $(V_{DD} = 30\text{ V}$, $I_D = 10\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 4.7\Omega$) * | $t_{d(on)}$ | | 30 | ns |
| Rise Time | | t_r | | 60 | ns |
| Turn-Off Delay Time | | $t_{d(off)}$ | | 80 | ns |
| Fall Time | | t_f | | 60 | ns |
| Total Gate Charge | $(V_{DS} = 0.8\text{Rated } V_{DSS}$, $I_D = \text{Rated } I_D$, $V_{GS} = 10\text{ V}$) * | Q_g | 36 | 63 | nC |
| Gate-Source Charge | | Q_{gs} | 16 | | nC |
| Gate-Drain Charge | | Q_{gd} | 26 | | nC |
| Internal Drain Inductance (Measured from the drain lead 0.25" from package to center of die) | L_D | | 4.5 | | nH |
| Internal Drain Inductance (Measured from the source lead 0.25" from package to source bond pad) | L_S | | 7.5 | | nH |
| SOURCE-DRAIN DIODE CHARACTERISTICS | | | | | |
| Forward On-Voltage(1) | $(I_S = \text{Rated } I_D$, $dI_S/dt = 100\text{A}/\mu\text{s}$) | V_{SD} | | 1.5 | V |
| Forward Turn-On Time | | t_{on} | ** | | ns |
| Reverse Recovery Time | | t_{rr} | | 450 | |

* Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$

** Negligible, Dominated by circuit inductance



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TYPICAL ELECTRICAL CHARACTERISTICS

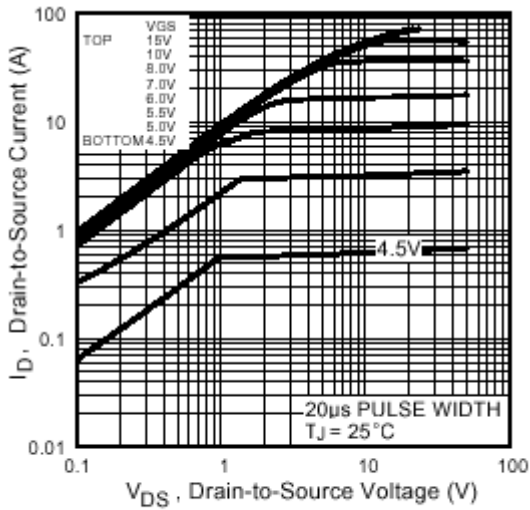


Fig 1. Typical Output Characteristics

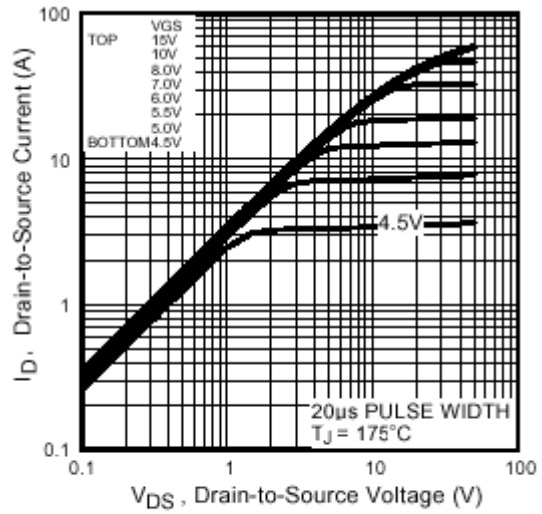


Fig 2. Typical Output Characteristics

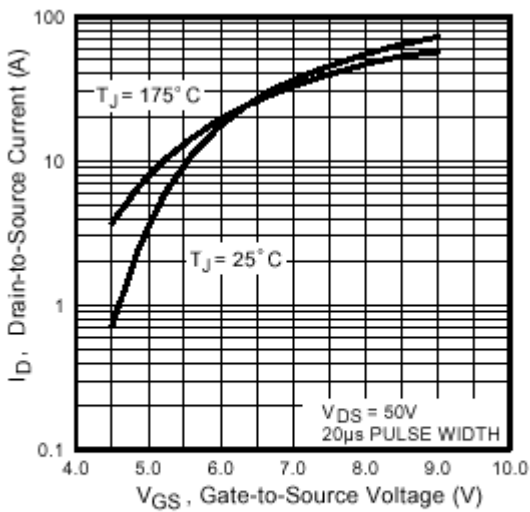


Fig 3. Typical Transfer Characteristics

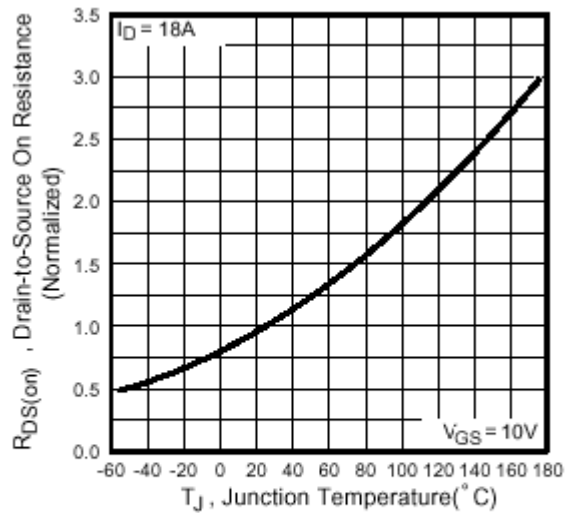


Fig 4. Normalized On-Resistance Vs. Temperature



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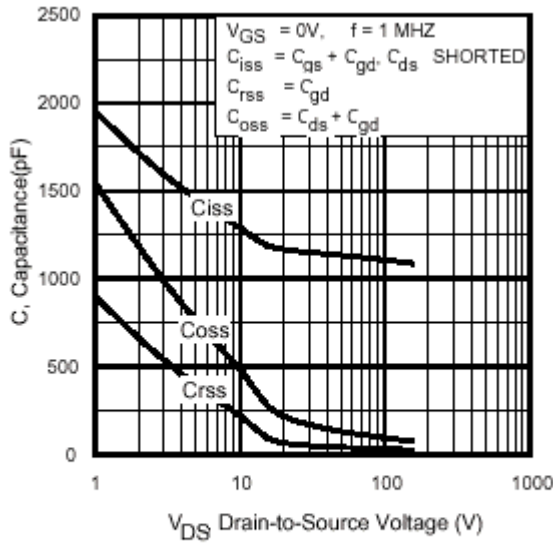


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

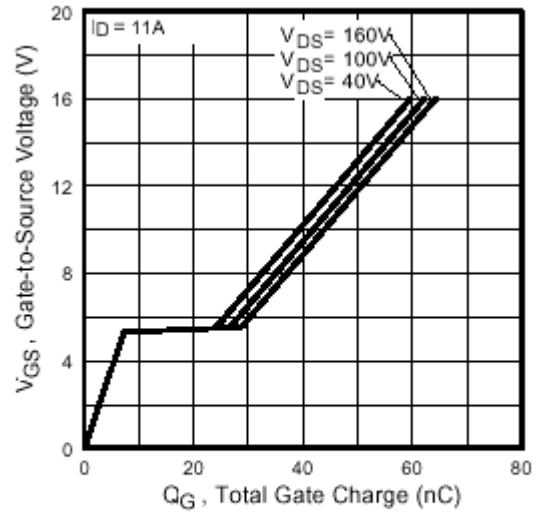


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

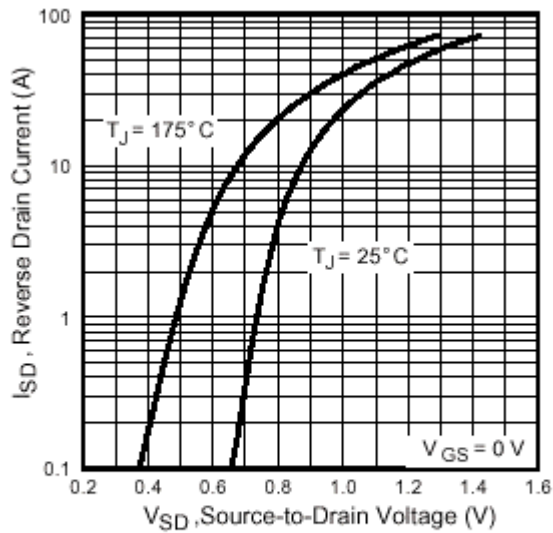


Fig 7. Typical Source-Drain Diode Forward Voltage

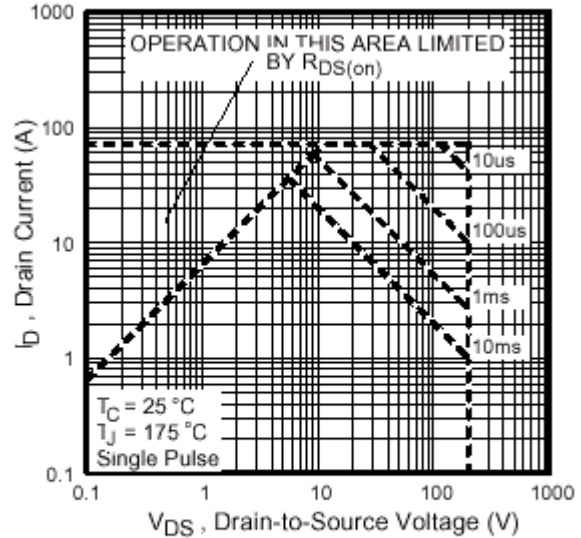


Fig 8. Maximum Safe Operating Area



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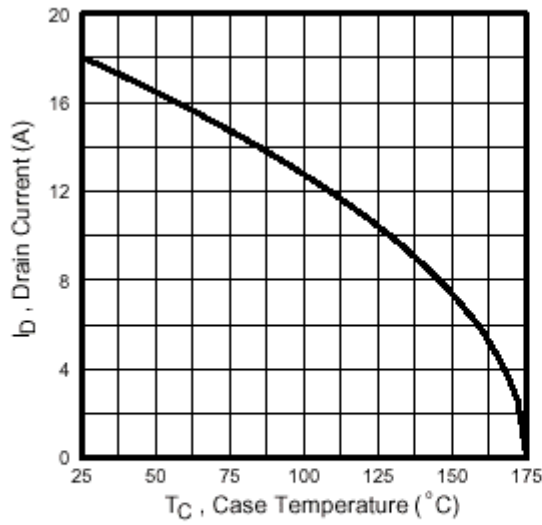


Fig 9. Maximum Drain Current Vs. Case Temperature

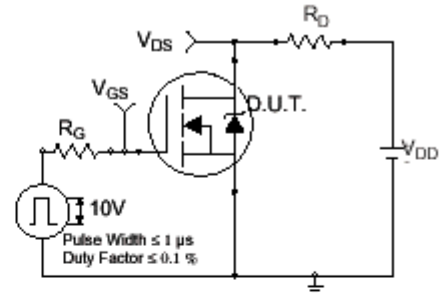


Fig 10a. Switching Time Test Circuit

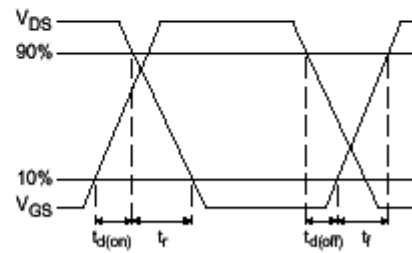


Fig 10b. Switching Time Waveforms

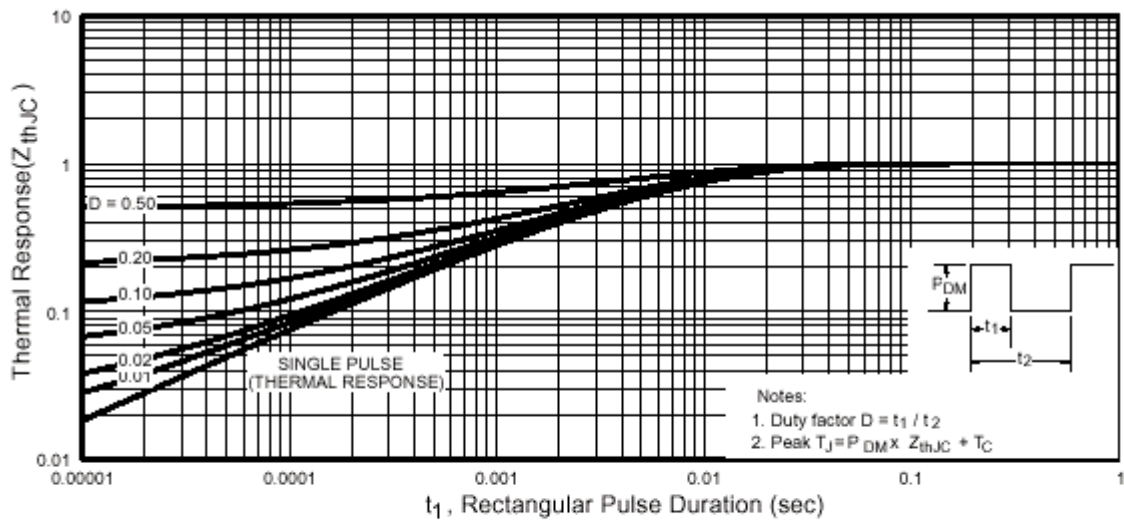


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case