

September 2015

### GENERAL DESCRIPTION

The HI-3718 is a low-power CMOS transceiver designed to meet the requirements of the ARINC 717 and ARINC 429 specifications. The device acts as an interface between ARINC 717 or ARINC 429 digital protocols and the Harvard Bi-Phase (HBP) and/or Bi-Polar Return-to-Zero (BPRZ) encoded physical layers.

The part includes a Harvard Bi-Phase (HBP) or Bi-Polar Return-to-Zero (BPRZ) line receiver which produces correct HBP or BPRZ digital signals for input to a decoder. The device also has HBP and BPRZ line drivers capable of accepting HBP and BPRZ encoded digital signals.

The device operates from a single +3.3V supply using only four external capacitors, making it the ideal interface device between an FPGA and ARINC 717 physical layer.

The HI-3718 is available in very small 32-pin 7mm x 7mm chip-scale (QFN) and 32-pin Quad Flat Pack (PQFP) plastic packages.

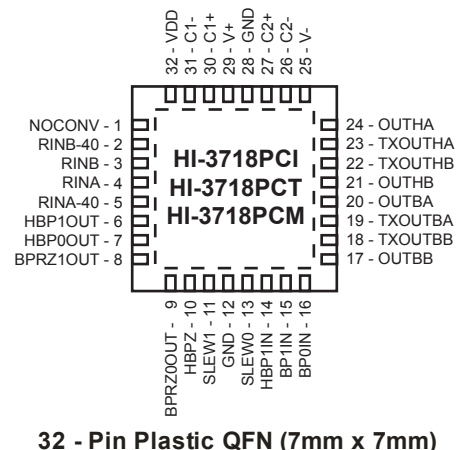
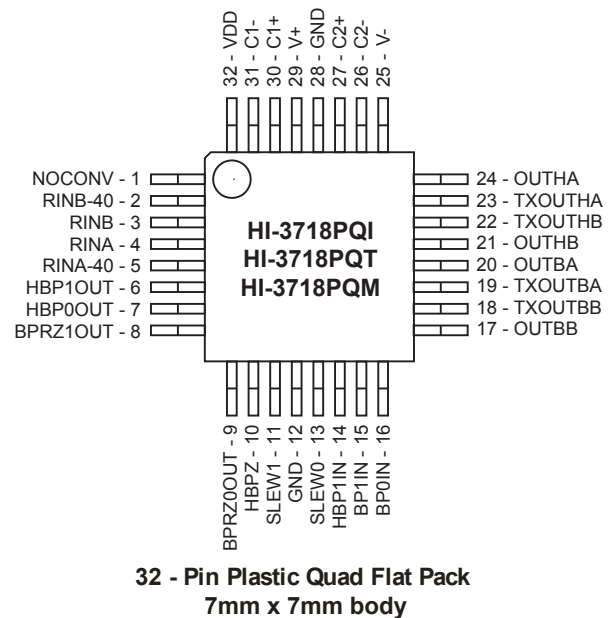
### FEATURES

- Compliant with ARINC 717-15 (June 6, 2011) and ARINC 573 standards
- BPRZ line driver and line receiver are ARINC 429 compliant
- Operates from a single +3.3V supply with on-chip DC/DC converter
- Independent Harvard Bi-Phase and Bipolar Return-to-Zero line drivers with digital slew rate control: set rise/fall times to 1.5µs, 3.75 µs, 7.5µs or 10µs
- Line drivers have independent tri-state control
- HBP and BPRZ line receivers have common inputs
- DC/DC converter may be disabled if external V+ and V- supplies are desired.
- “-40” inputs allow for DO-160G level 3 lightning protection using only two external resistors.
- Industrial and Extended temperature ranges

### APPLICATIONS

- ARINC 717 physical layer interface
- Digital Flight Data Acquisition Units (DFDAU)
- Digital Flight Data Recorders (DFDR)
- Quick Access Recorders (cassette type)
- Expandable Flight Data Acquisition and Recording Systems

### PIN CONFIGURATIONS (TOP VIEW)



## BLOCK DIAGRAM

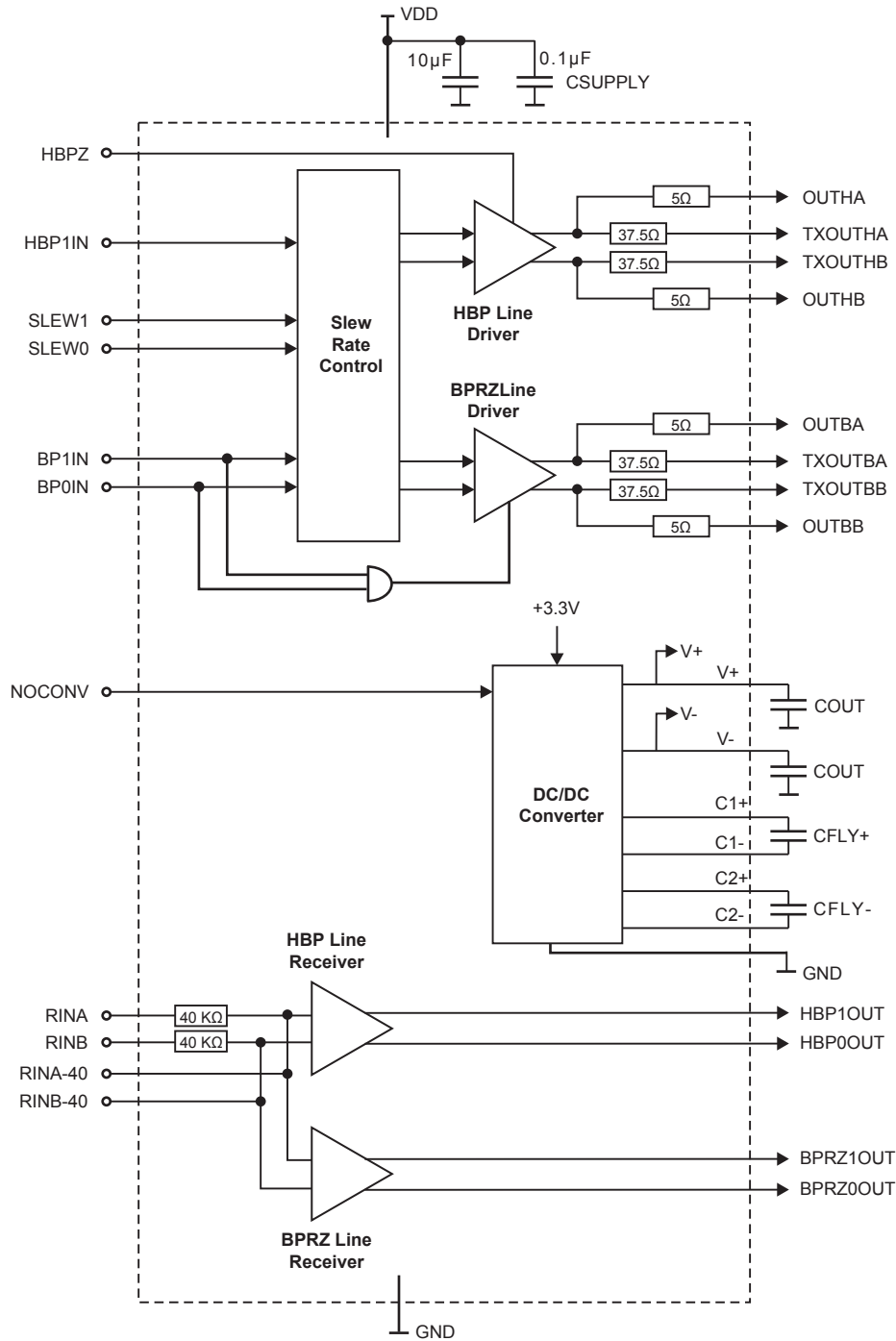


Figure 1. HI-3718 Block Diagram

## PIN DESCRIPTIONS

Table 1. Pin Descriptions

Pin Name	Function	Description	Internal Pull-Up / Pull-Down
NOCONV	INPUT	Disables on-chip DC-DC voltage converter	50 kΩ Pull-Down
RINB-40	INPUT	Alternate receiver negative input. Requires external 40 kΩ resistor	
RINB	INPUT	Receiver negative input. Direct connection to ARINC 717 bus (Bi-Polar Return-to-Zero or Harvard Bi-Phase)	
RINA	INPUT	Receiver positive input. Direct connection to ARINC 717 bus (Bi-Polar Return-to-Zero or Harvard Bi-Phase)	
RINA-40	INPUT	Alternate receiver positive input. Requires external 40 kΩ resistor	
HBP1OUT	OUTPUT	Harvard Bi-Phase (HBP) line receiver high output	
HBP0OUT	OUTPUT	Harvard Bi-Phase (HBP) line receiver low output	
BPRZ1OUT	OUTPUT	Bi-Polar Return-to-Zero (BPRZ) line receiver high output	
BPRZ0OUT	OUTPUT	Bi-Polar Return-to-Zero (BPRZ) line receiver low output	
HBPZ	INPUT	Setting this pin to a '1' tri-states the HBP line driver.	50 kΩ Pull-Up
SLEW1	INPUT	Slew rate control pin. Used with SLEW0 to set one of three programmable slew rates, 1.5 μs, 3.75 μs, 7.5 μs or 10 μs	
GND	POWER	Chip 0V Supply (All GND pins on package must be connected)	
SLEW0	INPUT	Slew rate control pin. Used with SLEW1 to set one of three programmable slew rates, 1.5 μs, 3.75 μs, 7.5 μs or 10 μs	
HPB1IN	INPUT	Encoded HBP line driver input (High or Low)	
BP1IN	INPUT	Encoded BPRZ line driver high input	50 kΩ Pull-Up
BP0IN	INPUT	Encoded BPRZ line driver low input	50 kΩ Pull-Up
OUTBB	OUTPUT	Alternate BPRZ line driver low output. Requires external 32.5 Ω resistor	
TXOUTBB	OUTPUT	BPRZ line driver low output. Direct connect to ARINC 717 bus	
TXOUTBA	OUTPUT	BPRZ line driver high output. Direct connect to ARINC 717 bus	
OUTBA	OUTPUT	Alternate BPRZ line driver high output. Requires external 32.5 Ω resistor	

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Pin Name	Function	Description	Internal Pull-Up / Pull-Down
OUTHB	OUTPUT	Alternate HBP line driver low output. Requires external 32.5Ω resistor	
TXOUTHB	OUTPUT	HBP line driver low output. Direct connect to ARINC 717 bus	
TXOUTH A	OUTPUT	HBP line driver high output. Direct connect to ARINC 717 bus	
OUTH A	OUTPUT	Alternate HBP line driver high output. Requires external 32.5Ω resistor	
V-	CONVERTER	DC/DC converter negative voltage	
C2-	CONVERTER	DC/DC converter flyback capacitor for V-	
C2+	CONVERTER	DC/DC converter flyback capacitor for V-	
GND	CONVERTER	DC/DC converter 0V Supply (All GND pins on package must be connected)	
V+	CONVERTER	DC/DC converter positive voltage	
C1+	CONVERTER	DC/DC converter flyback capacitor for V+	
C1-	CONVERTER	DC/DC converter flyback capacitor for V+	
V <sub>DD</sub>	POWER	Chip +3.3V Supply. Decoupled with 0.1μF, and 10μF (10VDC).	

## FUNCTIONAL DESCRIPTION

### Overview

ARINC 717 is a continuous transmission of 12-bit words in 4 second frames divided into four 1 second subframes. The data rate determines the number of words per subframe. ARINC 717 requires a basic data rate of 64 words per second (wps) with support for 128, 256, 512 and 1024 wps. Many ARINC 717 controllers, including Holt's HI-3717, offer an expanded range of 32 to 8192 wps for testing purposes and future expansion. The first 12-bit word of each subframe is reserved for a unique sync mark, an octal Barker Code which delineates the boundaries of the data frames.

ARINC 717 uses two encoding methods, Harvard Bi-Phase (HBP) and Bi-polar Return-to-Zero (BPRZ), which is similar to ARINC 429. The HI-3718 transceiver allows direct connection to any ARINC 717 compliant bus, allowing reception and transmission of either type of data. Furthermore, the BPRZ channel may be used as an ARINC 429 transceiver.

### ARINC 717 Line Receivers

The input data stream for ARINC 717 can be one of two formats. The main ARINC 717 bus to a Digital Flight Data Recorder (DFDR) uses Harvard Bi-phase (HBP) encoding and the auxiliary output bus to an Aircraft Integrated Data System (AIDS) uses Bi-Polar Return to Zero (BPRZ) encoding, as shown in Figure 2.

The HI-3718 line receivers are capable of connection to either HBP or BPRZ encoded busses via the RINA/B or RINA/B-40 pins. The BPRZ line receiver will also work with a standard ARINC 429 bus. The Line A and Line B digitally encoded signals (HBP and BPRZ) will appear on the HBP[1:0]OUT and BPRZ[1:0]OUT pins respectively.

**Note:** If RINA/B or RINA/B-40 are connected to a HBP bus, the BPRZ[1:0]OUT pins may be left floating. Similarly, if RINA/B or RINA/B-40 are connected to a BPRZ bus, the HBP[1:0]OUT pins may be left floating.

The ARINC 717 specification requires the following detection levels for the HBP inputs:

State	Differential Voltage
HI	+2 Volts to +8 Volts
LO	-2 Volts to -8 Volts

The BPRZ input detection levels are the same as standard ARINC 429 levels:

State	Differential Voltage
HI	+6.5 Volts to +13 Volts
NULL	+2.5 Volts to -2.5 Volts
LO	-6.5 Volts to -13 Volts

The HI-3718 guarantees recognition of these levels with a common mode voltage with respect to GND less than  $\pm 25V$  for the worst case conditions (3.15V supply, 8V HBP signal level and 13V BPRZ signal level).

Design tolerances guarantee detection of the above levels, so the actual acceptance ranges are slightly larger. If the signal (including nulls) is outside the differential voltage ranges, the HI-3718 receiver rejects the data.

### Line Receiver Input Pins

The HI-3718 has an alternate set of Line Receiver input pins, RINA/B-40, that are shared with the HBP and BPRZ line receivers. Only one pair of pins, RINA/B or RINA/B-40, may be used to connect to the ARINC 717 bus. The unused pair must be left floating.

The RINA/B-40 pins require an external 40 k $\Omega$  resistor in series with each ARINC 717 input. The resistors do not affect the ARINC 717 receiver level detection thresholds. When using the RINA/B-40 pins, each side of the ARINC 717 bus must be connected through a 40 k $\Omega$  series resistor in order for the chip to detect the correct ARINC 717 levels.

By keeping excessive voltage outside the device, the RINA/B-40 input option is helpful in applications where lightning protection is required. Please refer to the Holt AN-300 and AN-301 Application Notes for additional information and recommendations on lightning protection of Holt line drivers and line receivers.

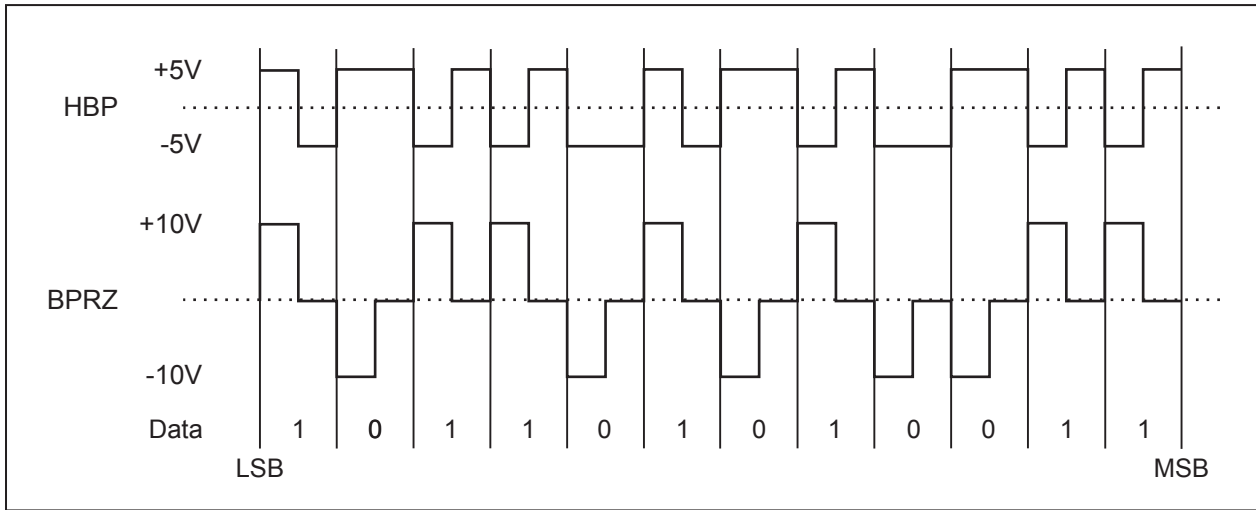


Figure 2. ARINC 717 HBP & BPRZ Differential Bus Signals

## DC/DC Converter

The HI-3718 requires only a single +3.3V power supply. The recommended decoupling capacitors for 3.3V VDD are ceramic 0.1μF, and 10μF, 10VDC minimum. An integrated inverting / non-inverting voltage doubler generates the rail voltages (±5.7V) which then power the line drivers to produce the required +5V ARINC 717 HBP and ±5V ARINC 717 BPRZ signal levels.

The internal dual-polarity charge pump requires four external capacitors, two for each polarity generated by the charge pump. Pins C1+ and C1- connect the external “fly” capacitor, CFLY+, to the positive portion of the charge pump, resulting in 5.7V at the V+ pin that is generated by an on-board voltage converter. An output bulk storage capacitor, COUT, is connected between V+ and GND. The inverting negative portion of the converter works in a similar fashion, with CFLY- and COUT connected between C2+ / C2- and V- / GND respectively. Note that **low ESR** capacitors must be used. Recommended values and ESR are given on page 10.

The NOCONV pin is set to “1” to disable the internal DC/DC converter. In this case, an external power supply should be used to supply +5V & -5V to the V+ & V- pins respectively. The “fly” capacitor pins may be left floating in this case.

## ARINC 717 Line Drivers

The line drivers in the HI-3718 directly drive the ARINC 717 HBP or BPRZ busses. The two ARINC 717 HBP outputs (TXOUTH A and TXOUTH B) provide a differential voltage of ±5V in accordance with the Harvard Bi-Phase format. The two ARINC 717 BPRZ outputs (TXOUTBA and TXOUTBB) provide a differential voltage to produce a +10V One, a -10V Zero, and a 0V Null. The BPRZ line driver outputs are also ARINC 429 compliant.

The slew rate of the HBP and BPRZ outputs is controllable with pins SLEW[1:0] as shown in Table 2. A 3.75μs slew rate conforms to all the required ARINC 717 data rates. A 1.5μs data rate is provided for the higher data rates beyond the standard. In addition, slower slew rates of 7.5μs and 10μs are available to further optimize an application.

Table 2. Line Driver Output Slew Rate Control

SLEW1	SLEW0	Slew Rate
0	0	7.5μs
1	0	10μs (same as ARINC 429 low speed)
0	1	3.75μs (ARINC 717 data rates)
1	1	1.5μs (higher data rates beyond ARINC 717)

No additional hardware is required to control the slope.

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Slope rate is set by on-chip resistors and capacitors.

## Line Driver Input Pins

The HBP line driver is driven by a single input pin, HBP1IN. This pin should be connected to a Harvard Bi-Phase digitally encoded signal. The HI-3718 will automatically generate the complement and output both the Line A and Line B HBP signal to drive the ARINC 717 bus.

The BPRZ line driver is driven by the BP1IN and BP0IN input pins. These pins should be connected to digitally encoded complimentary Bipolar Return to Zero signals. The HI-3718 will output both the Line A and Line B BPRZ signals to drive the ARINC 717 bus. Forcing both the BP1IN and BP0IN input pins to a logic high will force the BPRZ line driver into a high impedance state.

## Line Driver Output Pins

The Harvard Bi-phase (HBP) TXOUTH A and TXOUTH B pins as well as the Bipolar Return to Zero (BPRZ) TXOUTBA and TXOUTBB pins have  $37.5\ \Omega$  in series with each line driver output, and may be directly connected to an ARINC 717 bus. The OUTHA, OUTHB, OUTBA and OUTBB pins have  $5\ \Omega$  of internal series resistance and require an external  $32.5\ \Omega$  resistor in series with each pin. OUTHA, OUTHB, OUTBA and OUTBB pins are for applications where external series resistance is applied, typically for lightning protection devices. Please refer to the Holt AN-300 and AN-301 Application Notes for additional information and recommendations on lightning protection of Holt line drivers and line receivers.

## Line Driver Tri-State Capability

Each line driver has an independent tri-state function. Forcing the HBPZ pin high will force the HBP line driver into a high impedance state, independent of the BPRZ line driver. Similarly, forcing both BP[1:0]IN pins simultaneously high will force the BPRZ line driver into a high impedance state, independent of the HBP line driver. This independent functionality enables both line drivers to share a common bus if required in a given application. **NOTE: If the BPRZ and HBP line driver outputs are multiplexed into a single bus, care should be taken not to drive both inputs simultaneously.** The user should adopt a break-before-make strategy, by forcing an active line driver into a high impedance state before the other is driven (see Figure 7).

## ABSOLUTE MAXIMUM RATINGS

Supply Voltages		
$V_{DD}$ .....	-0.3 V to +5.0 V	
V+ .....	+7.0 V	
V- .....	-7.0 V	
Voltage at Input pins RINxx .....		-120 V to +120 V
Voltage at Output pins TXOUTxx, OUTxx .....		V- to V+
Voltage at all other pins .....		-0.3 V to $V_{DD} + 0.3$ V
DC current drain per digital input pin .....		$\pm 10$ mA
Solder Temperature (reflow) .....		260 °C
Junction Temperature .....		175 °C
Storage Temperature .....		-65 °C to +150 °C

**NOTE:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

Supply Voltages	
$V_{DD}$ .....	+3.0 V to +3.6 V
V+ .....	+5.5 V
V- .....	-5.5 V
Operating Temperature	
Industrial Screening .....	-40 °C to +85 °C
Hi-Temp Screening .....	-55 °C to +125 °C

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## DC ELECTRICAL CHARACTERISTICS

$V_{DD} = +3.3V$ ,  $T_A =$  Operating Temperature Range (unless otherwise stated)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit		
<b>Line Receiver Inputs - Pins RINA, RINB, RINA-40 (with external 40 k<math>\Omega</math>), RINB-40 (with external 40 k<math>\Omega</math>)</b>								
HBP Differential Input Voltage (RINA - RINB)	HI	$V_{IHH}$	Common mode voltages less than $\pm 25V$ with respect to GND		2.0	5.0	8.0	V
	LO	$V_{ILH}$			-8.0	-5.0	-2.0	V
HBP Single-Ended Input Voltage (Ref. to GND)	RINA	HI	$V_{IHHA}$	Common mode voltages less than $\pm 25V$ with respect to GND	3.5	5.0	6.5	V
		LO	$V_{ILHA}$		-1.5	0	+1.5	V
	RINB	HI	$V_{IHBB}$		-1.5	0	+1.5	V
		LO	$V_{ILBB}$		3.5	5.0	6.5	V
BPRZ Differential Input Voltage (RINA - RINB)	ONE	$V_{IHB}$	Common mode voltages less than $\pm 25V$ with respect to GND		6.5	10.0	13.0	V
	ZERO	$V_{ILB}$			-13.0	-10.0	-6.5	V
	NULL	$V_{INUL}$			-2.5	0	+2.5	V
BPRZ Single-Ended Input Voltage (Ref. to GND)	RINA	ONE	$V_{IHHA}$	Common mode voltages less than $\pm 25V$ with respect to GND	3.25	5.0	6.5	V
		ZERO	$V_{ILHA}$		-6.5	-5.0	-3.25	V
	RINB	ONE	$V_{IHBB}$		-6.5	-5.0	-3.25	V
		ZERO	$V_{ILBB}$		3.25	5.0	6.5	V
Input Resistance	Differential	$R_I$		140		k $\Omega$		
	To GND	$R_G$		140		k $\Omega$		
	To $V_{DD}$	$R_H$		100		k $\Omega$		
Input Current	Input Sink	$I_{IH}$			200	$\mu A$		
	Input Source	$I_{IL}$	-450			$\mu A$		
Input Capacitance (Guaranteed but not tested)	Differential	$C_I$	RINA - RINB			20	pF	
	To GND	$C_G$				20	pF	
	To $V_{DD}$	$C_H$				20	pF	
<b>Logic Inputs - Pins HBPZ, SLEW1, SLEW0, NOCONV, HBP1IN, BP1IN, BP0IN</b>								
Input Voltage	Input Voltage HI	$V_{IH}$		80% $V_{DD}$		V		
	Input Voltage LO	$V_{IL}$			20% $V_{DD}$	V		
Input Current	Input Sink	$I_{IH}$			1.5	$\mu A$		
	Input Source	$I_{IL}$	-1.5			$\mu A$		
<b>Harvard Bi-Phase (HBP) Outputs - Pins TXOUTH A, TXOUTH B, (or OUTH A, OUTH B with external 32.5 <math>\Omega</math>)</b>								
HBP Differential Output Voltage (TXOUTH A - TXOUTH B or OUTH A - OUTH B)	HI	$V_{OHH}$	No load		4.0	5.0	6.0	V
	LO	$V_{OLH}$			-6.0	-5.0	-4.0	V



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Parameter			Symbol	Conditions	Min	Typ	Max	Unit
HBP Single-Ended Output Voltage (Ref. to GND)	TXOUTH or OUTHA	HI	$V_{OHHA}$	No load	4.5	5.0	5.5	V
		LO	$V_{OLHA}$		-0.5	0	+0.5	V
	TXOUTH or OUTHB	HI	$V_{OHHB}$		-0.5	0	+0.5	V
		LO	$V_{OLHB}$		4.5	5.0	5.5	V
HBP Output Tri-State Current			$I_{OZH}$	HBPZ = $V_{DD}$ $-5.75V < V_{OUT} < +5.75V$	-1.0	0	+1.0	$\mu A$
<b>Bi-Polar Return to Zero (BPRZ) Outputs - Pins TXOUTBA, TXOUTBB, (or OUTBA, OUTBB with external 32.5 <math>\Omega</math>)</b>								
BPRZ Differential Output Voltage (TXOUTBA - TXOUTBB or OUTBA - OUTBB)		ONE	$V_{OHB}$	No load	9.0	10.0	11.0	V
		ZERO	$V_{OLB}$		-11.0	-10.0	-9.0	V
		NULL	$V_{ONUL}$		-0.5	0	+0.5	V
BPRZ Single-Ended Output Voltage (Ref. to GND)	TXOUTBA or OUTBA	ONE	$V_{OHBA}$	No load	4.5	5.0	5.5	V
		ZERO	$V_{OLBA}$		-5.5	-5.0	-4.5	V
	TXOUTBB or OUTBB	ONE	$V_{OHBB}$		-5.5	-5.0	-4.5	V
		ZERO	$V_{OLBB}$		4.5	5.0	5.5	V
BPRZ Output Tri-State Current			$I_{OZB}$	BP1IN = BP0IN = $V_{DD}$ $-5.75V < V_{OUT} < +5.75V$	-1.0	0	+1.0	$\mu A$
<b>Logic Outputs - Pins HBP1OUT, HBP0OUT, BPRZ1OUT, BPRZ0OUT</b>								
Output Voltage	Logic "1"		$V_{OH}$	$I_{OH} = -100 \mu A$	90% $V_{DD}$			V
	Logic "0"		$V_{OL}$	$I_{OL} = 1 \text{ mA}$			10% $V_{DD}$	V
Output Current	Output Sink		$I_{OL}$	$V_{OUT} = 0.4 \text{ V}$	1.6			mA
	Output Source		$I_{OH}$	$V_{OUT} = V_{DD} - 0.4 \text{ V}$			-1.0	mA
Output Capacitance			$C_O$			15		pF
Operating Voltage Range			$V_{DD}$		3.15		3.45	V
<b>Operating Supply Current</b>								
No Load			$I_{DD}$				35	mA
HBP Max Load			$I_{DDLH}$	600 $\Omega$ Differential Output Load			120	mA
BPRZ Max. Load			$I_{DDLb}$	400 $\Omega$ Differential Output Load			120	mA
Line Driver Outputs Shorted			$I_{DDSH}$	See Note 1		165		mA
<b>Output Impedance</b>								
TXOUT Pins						37.5		$\Omega$
OUT Pins						5		$\Omega$

**Note 1:** TXOUTH and/or TXOUTH shorted to each other or ground. OUTHA and/or OUTHB shorted to each other or ground (assumes external resistors are connected to OUTHA and OUTHA to comply with 37.5 Ohm output resistance requirement).

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**Note 2:** TXOUTBA and/or TXOUTBB shorted to each other or ground. OUTBA and/or OUTBB shorted to each other or ground (assumes external resistors are connected to OUTBA and OUTBA to comply with 37.5 Ohm output resistance requirement).

## CONVERTER CHARACTERISTICS

$V_{DD} = +3.3V$ ,  $T_A =$  Operating Temperature Range (unless otherwise stated)

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Start-up transient (V+, V-)	$t_{START}$		-	-	10	ms
Operating Switching Frequency	$f_{sw}$		-	500	-	kHz
Worst case maximum converter output	$V_{+(max)}$	$V_{DD} = 3.6V$ . $T = -55^{\circ}C$ . Open load.	-	-	6.0	V
	$V_{-(max)}$		-	-	-6.0	
<b>Capacitor Requirements (see “HI-3718 Block Diagram” on page 2 for capacitor placement)</b>						
V+ Flyback capacitor, non-polarized x7R MLCC, 10V minimum	$C_{FLY+}$	500 kHz	0.47	-	-	$\mu F$
	$ESR_{(CFLY+)}$		-	-	500	m $\Omega$
V- Flyback capacitor, non-polarized x7R MLCC, 10V minimum	$C_{FLY-}$	500 kHz	2.2	-	-	$\mu F$
	$ESR_{(CFLY-)}$		-	-	500	m $\Omega$
Two bulk storage capacitors, non-polarized X7R MLCC or tantalum, 10V minimum	$C_{OUT}$	500 kHz	10	-	47	$\mu F$
	$ESR_{(COUT)}$		-	-	300	m $\Omega$
Supply de-coupling capacitors, non-polarized x7R MLCC, 10V min.	$C_{SUPPLY}$	Two parallel capacitors	-	0.1	-	$\mu F$
			10	-	47	$\mu F$

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## AC ELECTRICAL CHARACTERISTICS

$V_{DD} = +3.3V$ ,  $T_A =$  Operating Temperature Range (unless otherwise stated)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>Line Driver Propagation Delay</b>						
Output high to low	$t_{phlx}$	Defined in Figure 3 and Figure 5, no load		500		ns
Output low to high	$t_{plhx}$			500		ns
<b>Line Driver Output Transition Times</b>						
Output high to low	$t_{fx}$	Pins SLEW[1:0] = 00 See Figure 3 and Figure 5	5.0	7.5	10.0	$\mu s$
Output low to high	$t_{rx}$		5.0	7.5	10.0	$\mu s$
Output high to low	$t_{fx}$	Pins SLEW[1:0] = 01 See Figure 3 and Figure 5	2.5	3.75	5.0	$\mu s$
Output low to high	$t_{rx}$		2.5	3.75	5.0	$\mu s$
Output high to low	$t_{fx}$	Pins SLEW[1:0] = 10 See Figure 3 and Figure 5	5.0	10.0	15.0	$\mu s$
Output low to high	$t_{rx}$		5.0	10.0	15.0	$\mu s$
Output high to low	$t_{fx}$	Pins SLEW[1:0] = 11 See Figure 3 and Figure 5	1.0	1.5	2.0	$\mu s$
Output low to high	$t_{rx}$		1.0	1.5	2.0	$\mu s$
<b>Line Receiver Propagation Delay</b>						
Output high to low	$t_{phlr}$	Defined in Figure 4 and Figure 6, no load		500		ns
Output low to high	$t_{plhr}$			500		ns
<b>Line Receiver Output Transition Times</b>						
Output high to low	$t_{fr}$	50 pF load		6.0	12.0	ns
Output low to high	$t_{rr}$			6.0	12.0	ns
<b>High Impedance Break-Before-Make on Muxed Line Driver Outputs</b>	$t_{DZ}$		1.0			$\mu s$
Input Capacitance (Logic) <sup>1</sup>	$C_{IN}$				10	pF
Output Capacitance (Tri-state) <sup>1</sup>	$C_{OUT}$	BP1IN = BP0IN = $V_{DD}$ HBPZ = $V_{DD}$			10	pF

**Note 1:** Guaranteed but not tested

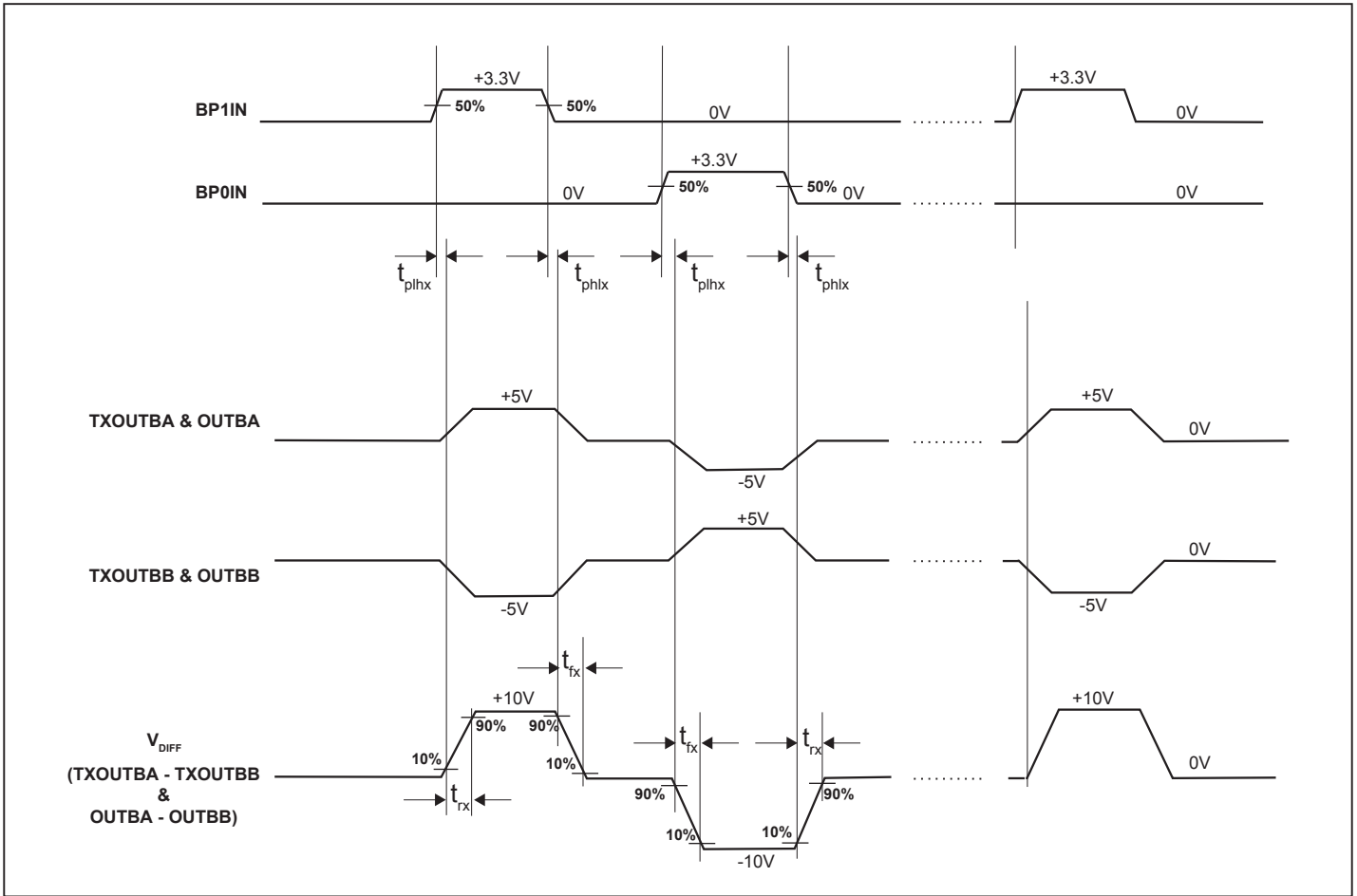


Figure 3. BPRZ Line Driver Waveforms

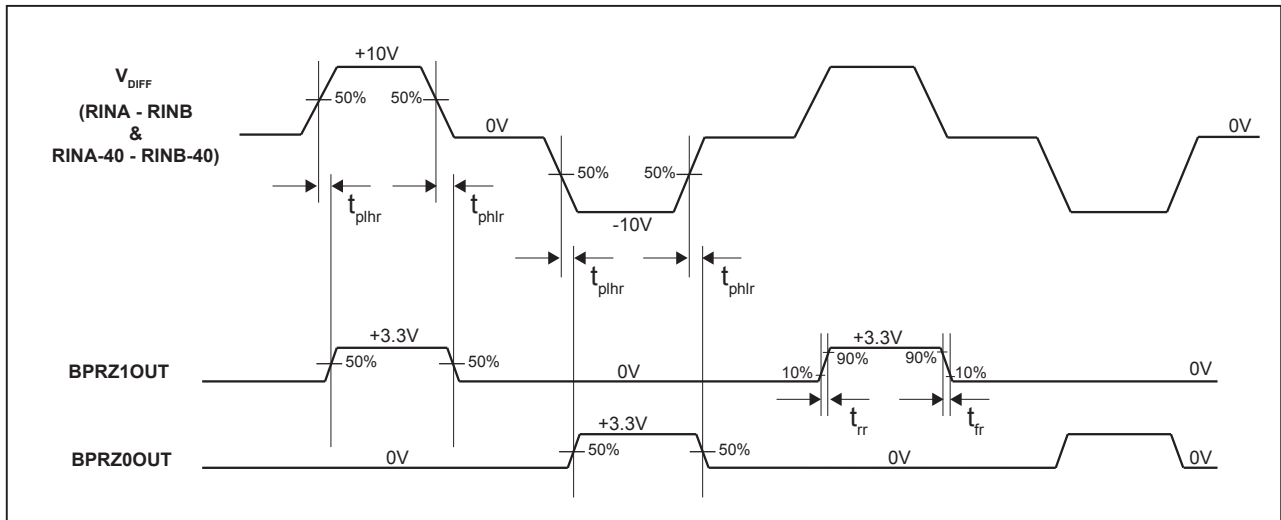


Figure 4. BPRZ Line Receiver Waveforms

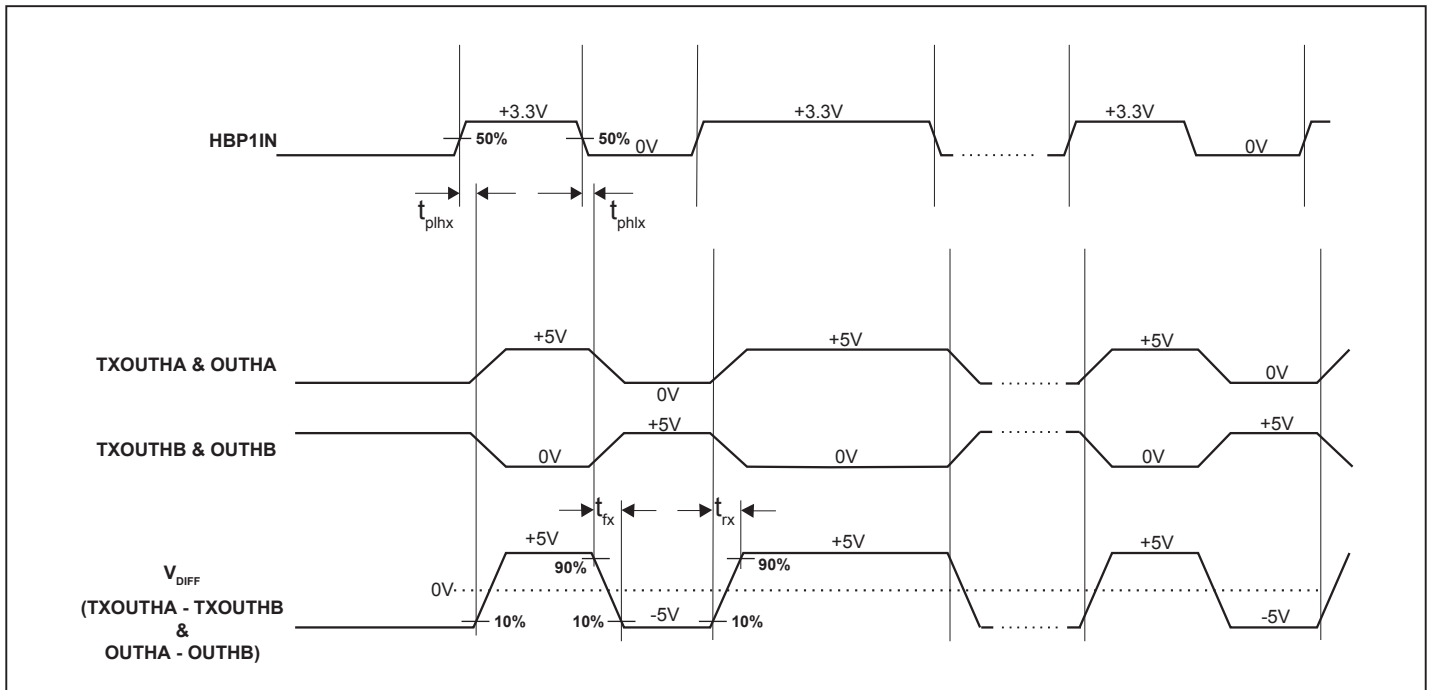


Figure 5. HBP Line Driver Waveforms

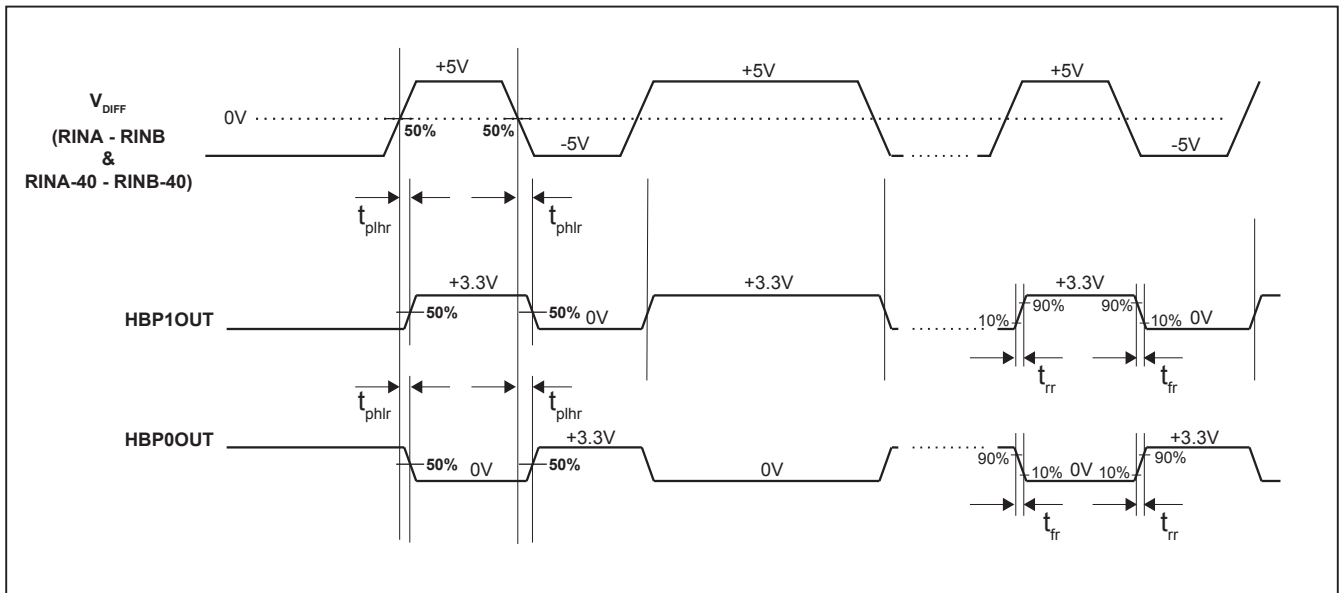


Figure 6. HBP Line Receiver Waveforms

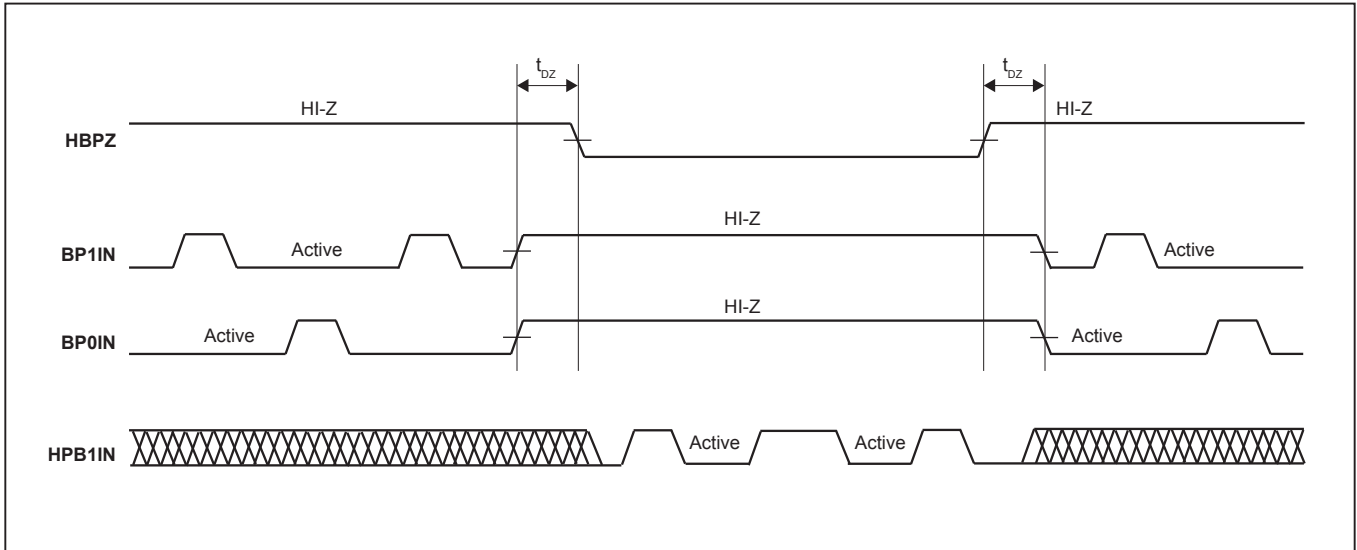


Figure 7. Single-Bus Line Driver Outputs (Multiplexed).

# HI-3718

## ORDERING INFORMATION

HI - 3718Px x x

PART NUMBER	LEAD FINISH
F	Pb-free, RoHS compliant

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C to +85°C	I	No
T	-55°C to +125°C	T	No
M	-55°C to +125°C	M	Yes

PART NUMBER	PACKAGE DESCRIPTION
3718PC	32 PIN PLASTIC 7mm x 7mm QFN - (32PCS7). Lead finish - NiPdAu.
3718PQ	32 PIN PLASTIC QUAD FLAT PACK - (32PQS). Lead finish - Matte Tin.

## REVISION HISTORY

Revision	Date	Description of Change
DS3718, Rev. New	06/03/14	Initial Release
Rev. A	06/09/14	Change transmit test conditions from 600 $\Omega$ to No load.
Rev. B	08/04/14	Update 32PCS7 package drawing (incorrect number of pins shown in drawing).
Rev. C	09/24/14	Addition of 3.75 $\mu$ s slew rate into Features, Pin Descriptions Table 1, ARINC 717 Line Drivers description, and Table 2 Line Driver Output Slew Rate Control.
Rev. D	10/03/14	Add 3.75 $\mu$ s slew rate information to Line Driver Output Transition Times table.
Rev. E	09/03/15	Remove Max. Power Dissipation from Absolute Maximum Ratings table

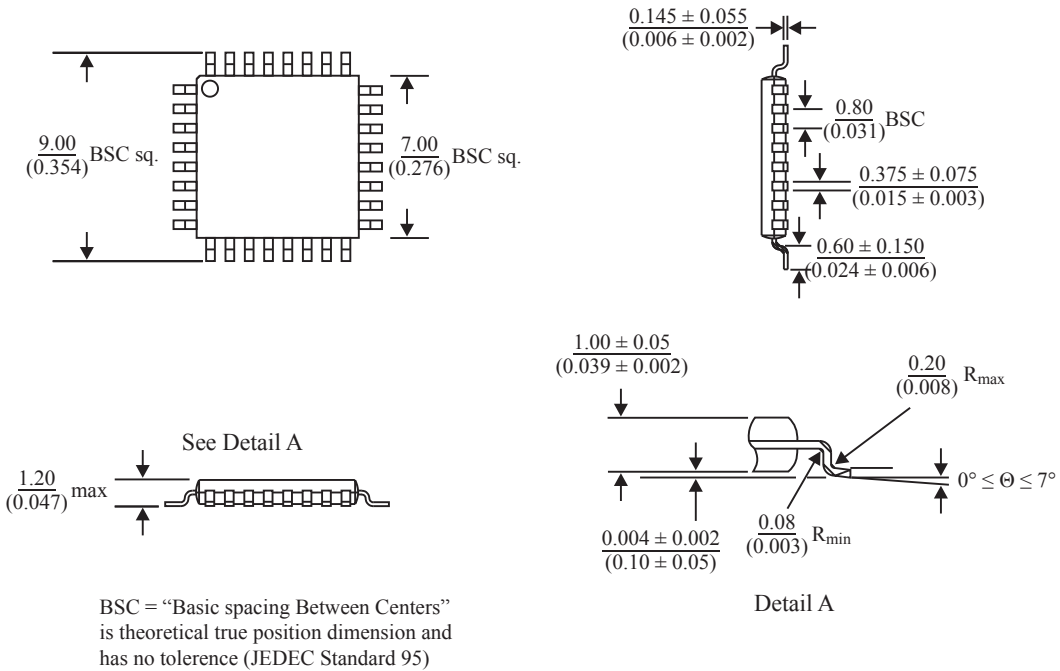


**PACKAGE DIMENSIONS**

**32-PIN PLASTIC QUAD FLAT PACK (PQFP)**

millimeters (inches)

Package Type: 32PQS



**32-PIN PLASTIC CHIP-SCALE PACKAGE (QFN)**

millimeters (inches)

Package Type: 32PCS7

