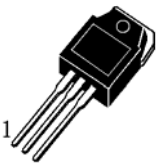
N-Channel Enhancement Mode Field Effect Transistor

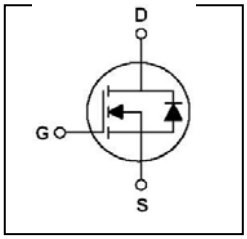
General Description

These are N-Channel enhancement mode silicon gate power field effect transistors. They are advanced power MOSFETs designed, this advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode . These devices are well suited for high efficiency switch mode power supply, power factor correction, electronic lamp ballast based on half bridge.

TO-3P



1- G 2-D 3-S



Features

- **7A, 600V(See Note), R_{DS}(on) <1.2Ω@V_{GS} = 10 V**
- **Fast switching**
- **100% avalanche tested**
- **Improved dv/dt capability**
- **RoHS compliant**

Maximum Ratings (Ta=25℃ unless otherwise specified)

T_{stg}——Storage Temperature ---------- -55~150℃

T_j ——Operating Junction Temperature ---------- 150℃

V_{DSS} —— Drain-Source Voltage ----------600V

V_{GSS} —— Gate-Source Voltage ---------- ±30V

I_D —— Drain Current (Continuous)(T_c=25℃) ---------- 7A

I_{DM} —— Pulsed Drain Current (Note 1)---------- 28A

P_D —— Maximum Power Dissipation (T_c=25℃) ---------- 198W

Derate Above 25℃ ---------- 1.75W/℃

E_{AS}—— Pulsed Avalanche Energy (Note 2) ---------- 580mJ

I_{AR}—— Avalanche Current (Note 1) ---------- 7A

E_{AR} —— Repetitive Avalanche Energy (Note 1) ---------- 30mJ

dv/dt —— Peak Diode Recovery dv/dt (Note 3) ----------4.0V/ns

Thermal Characteristics

Symbol	Items	TO-3P	Unit
Rthj-case	Thermal Resistance Junction-case	Max 0.63	℃/W
Rthj-amb	Thermal Resistance Junction-ambient	Max 40	℃/W

Electrical Characteristics (Ta=25℃ unless otherwise specified)

Symbol	Items	Min.	Typ.	Max.	Unit	Conditions
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	600			V	I_D=250μA ,V_{GS}=0V
I_{DSS}	Zero Gate Voltage Drain Current			10	μA	V_{DS} =600V, V_{GS}=0V
				100	μA	V_{DS} =480V, V_{GS}=0V,Tj=125℃
I_{GSS}	Gate – Body Leakage			±100	nA	V_{GS}= ±30V , V_{DS} =0V
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	2.0		4.0	V	V_{DS} = V_{GS} , I_D=250μA
$R_{DS(on)}$	Static Drain-Source On-Resistance		0.91	1.2	Ω	V_{GS}=10V, I_D=3.5A
Dynamic Characteristics and Switching Characteristics						
Ciss	Input Capacitance		1290		pF	V_{DS} = 25 V, V_{GS} = 0V, f = 1.0 MHz
Coss	Output Capacitance		120		pF	
Crss	Reverse Transfer Capacitance		10		pF	
$t_{d(on)}$	Turn - On Delay Time		20	40	nS	V_{DS} = 300V, I_D=7A, R_G= 25 Ω (Note 4,5)
tr	Rise Time		55	110	nS	
$t_{d(off)}$	Turn - Off Delay Time		90	180	nS	
t_f	Fall Time		60	120	nS	
Qg	Total Gate Charge		30	40	nC	V_{DS}=480V, ID=7A, V_{GS} = 10 V (Note 4,5)
Qgs	Gate–Source Charge		6		nC	
Qgd	Gate–Drain Charge		13		nC	
Drain-Source Diode Characteristics and Maximun Ratings						
I_S	Continuous Source–Drain Diode Forward Current			7	A	
I_{SM}	Pulsed Drain-Source Diode Forward Current			28	A	
V_{SD}	Source–Drain Diode Forward On–Voltage			1.4	V	I_S=7A,V_{GS}=0

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L=22.2mH,I_{AS}=7.0A, V_{DD}=50V, R_G=25 Ω ,Starting T_J=25℃
3. I_{SD}≤8.4A, di/dt≤200A/μS,V_{DD}≤BVDSS, Starting T_J=25℃
4. Pulse Test: Pulse width≤300μS, Duty Cycle≤2%
5. Essentially independent of operating temperature

Typical Characteristics

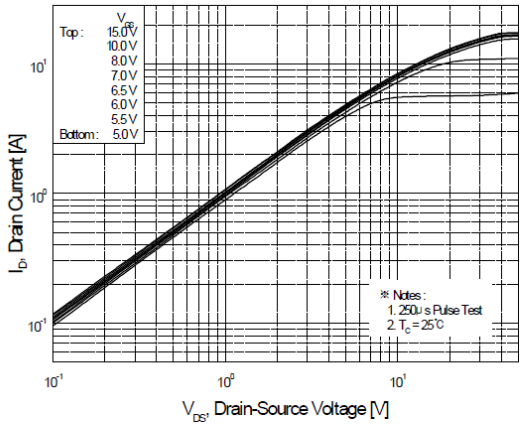


Figure 1. On-Region Characteristics

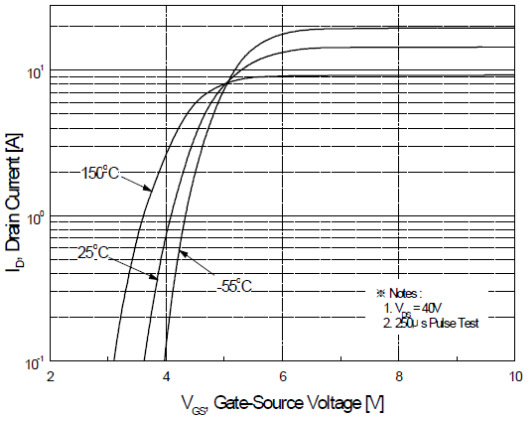


Figure 2. Transfer Characteristics

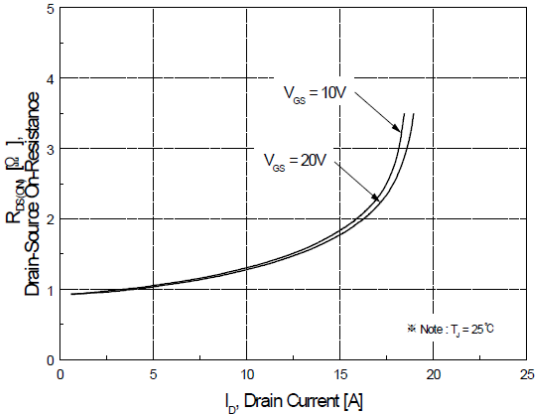


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

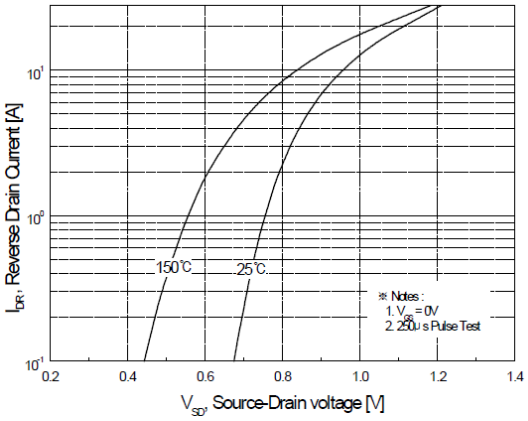


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

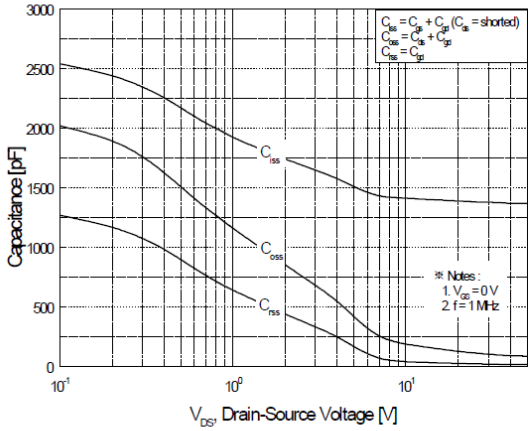


Figure 5. Capacitance Characteristics

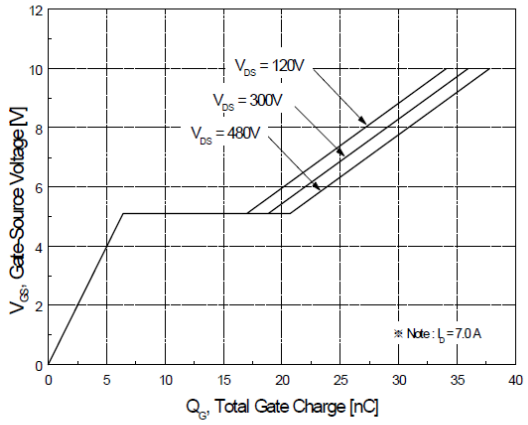


Figure 6. Gate Charge Characteristics

Typical Characteristics

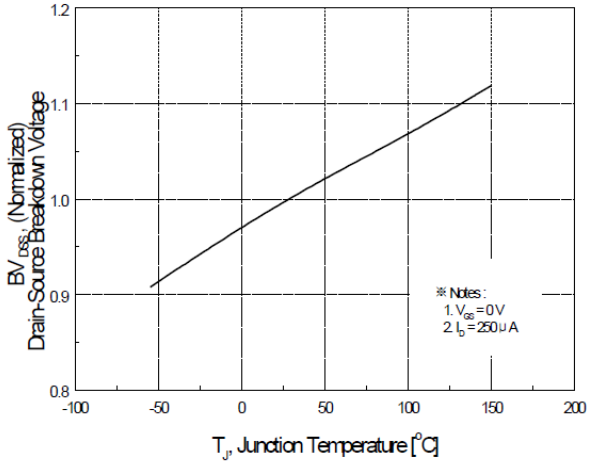


Figure 7. Breakdown Voltage Variation vs Temperature

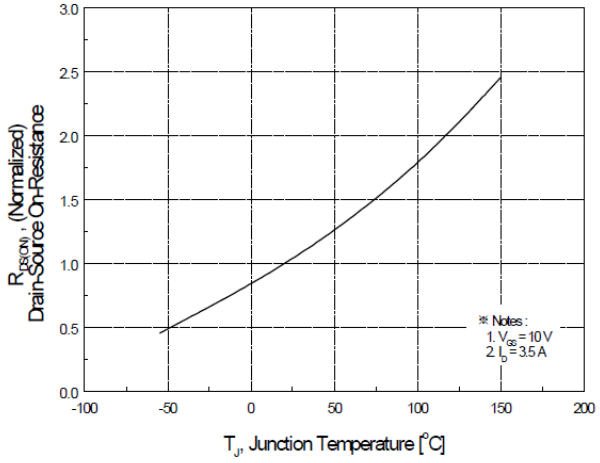


Figure 8. On-Resistance Variation

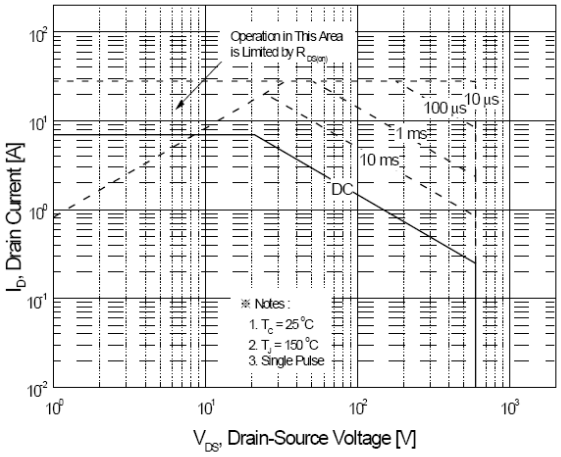


Figure 9. Maximum Safe Operating Area

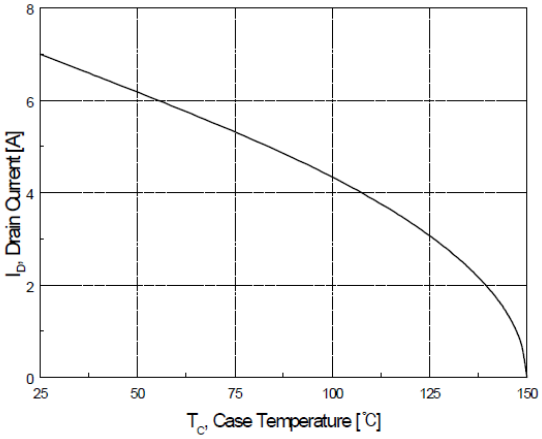


Figure 10. Maximum Drain Current vs Case Temperature

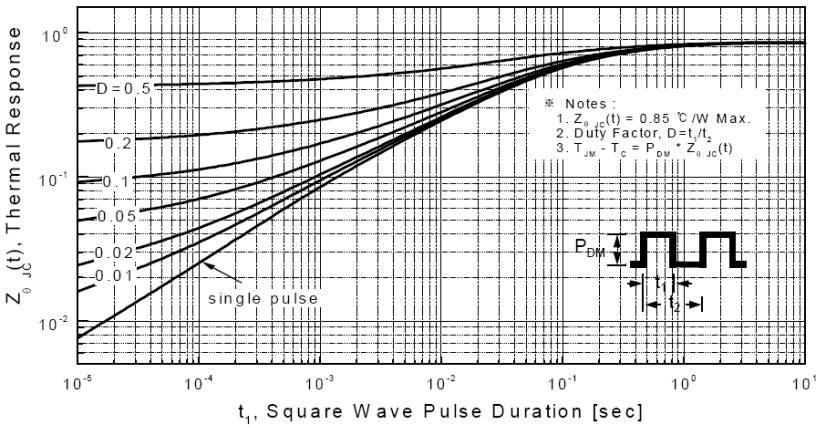


Figure 11. Transient Thermal Response Curve

Typical Characteristics

Fig 12. Gate Charge Test Circuit & Waveform

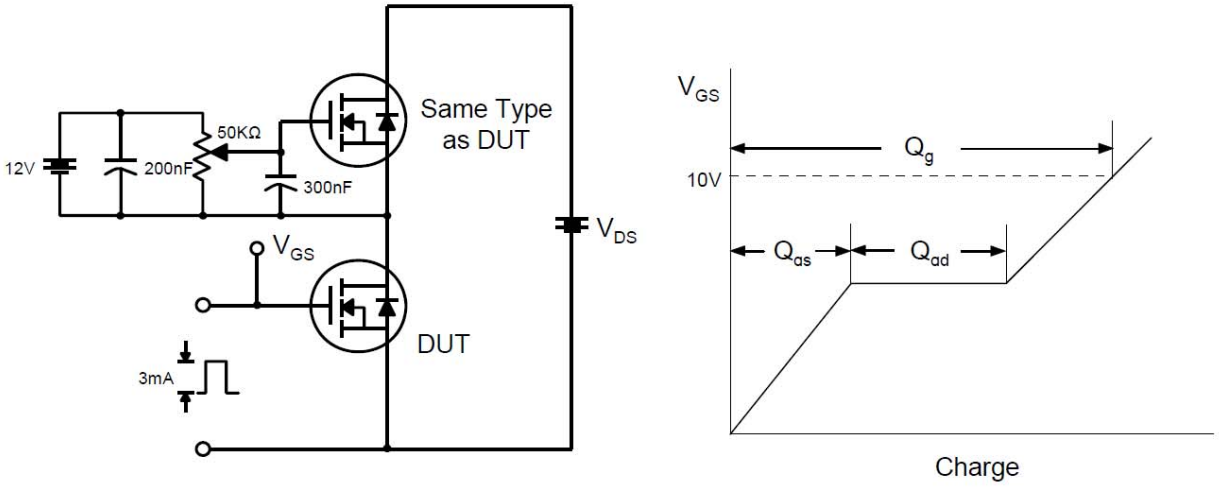


Fig 13. Resistive Switching Test Circuit & Waveforms

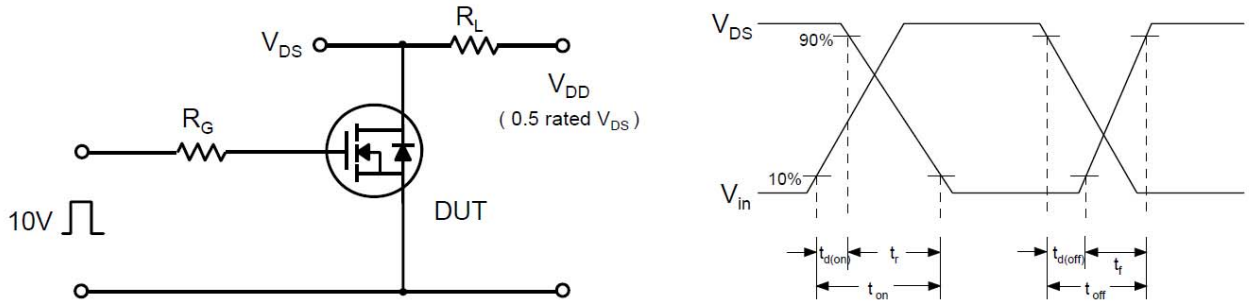
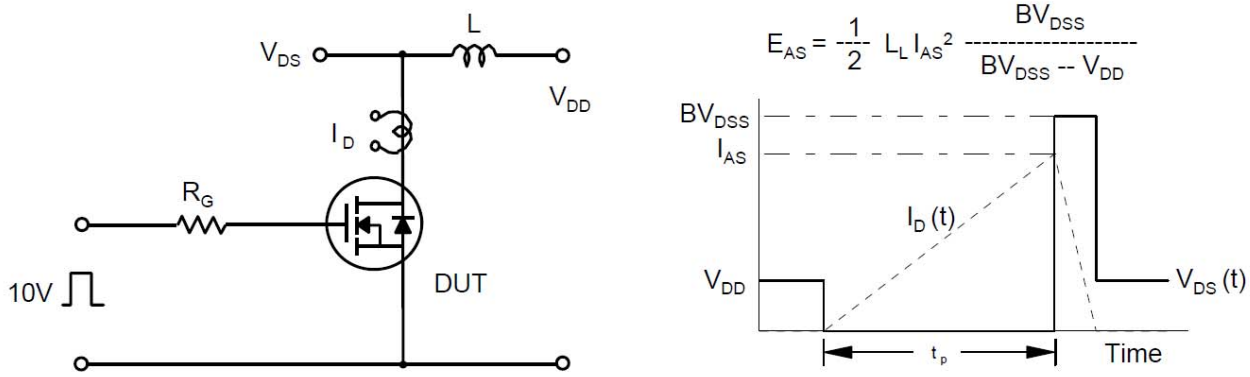


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms



Typical Characteristics

Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms