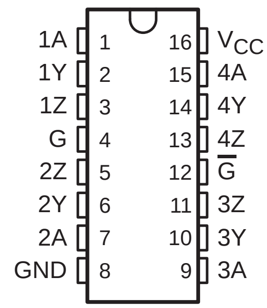
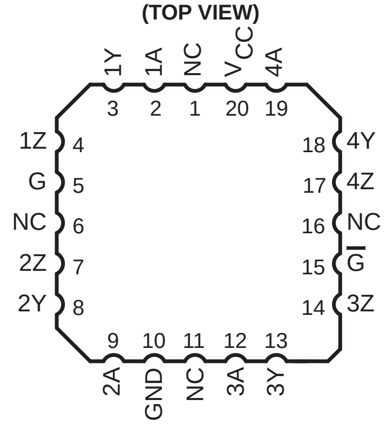
- Meets or Exceeds the Requirements of ANSI TIA/EIA-644 Standard
- Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100-Ω Load
- Typical Output Voltage Rise and Fall Times of 500 ps (400 Mbps)
- Typical Propagation Delay Times of 1.7 ns
- Operates From a Single 3.3-V Supply
- Power Dissipation 25 mW Typical per Driver at 200 MHz
- Driver at High Impedance When Disabled or With V_{CC} = 0
- Bus-Terminal ESD Protection Exceeds 8 kV
- Low-Voltage TTL (LVTTL) Logic Input Levels
- Pin-Compatible With the AM26LS31, MC3487, and μA9638

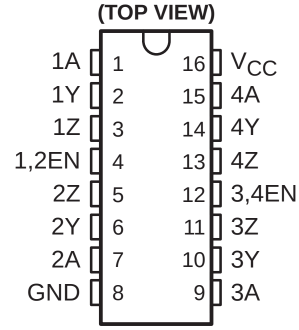
SN55LVDS31 . . . J OR W
SN65LVDS31D
(Marked as **LVDS31** or **65LVDS31**)
(TOP VIEW)



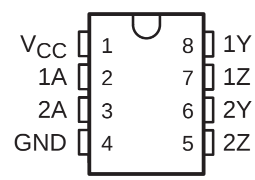
SN55LVDS31FK
(TOP VIEW)



SN65LVDS3487D
(Marked as **LVDS3487** or **65LVDS3487**)
(TOP VIEW)



SN65LVDS9638D (Marked as **DK638** or **LVDS38**)
SN65LVDS9638DGN (Marked as **L38**)
(TOP VIEW)



description

The SN55LVDS31, SN65LVDS31, SN65LVDS3487, and SN65LVDS9638 are differential line drivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5 V differential standard levels (such as TIA/EIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the four current-mode drivers will deliver a minimum differential output voltage magnitude of 247 mV into a 100-Ω load when enabled.

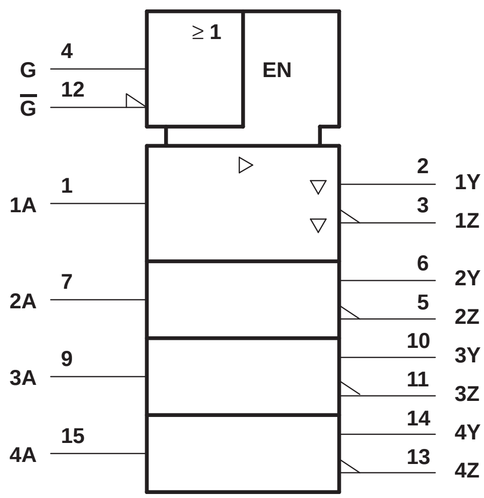
The intended application of these devices and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDS31, SN65LVDS3487, and SN65LVDS9638 are characterized for operation from –40°C to 85°C. The SN55LVDS31 is characterized for operation from –55°C to 125°C.

AVAILABLE OPTIONS

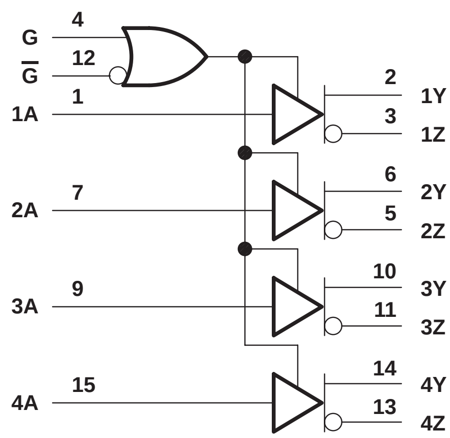
T_A	PACKAGE				
	SMALL OUTLINE (D)	MSOP (DGN)	CHIP CARRIER (FK)	CERAMIC DIP (J)	FLAT PACK (W)
–40°C to 85°C	SN65LVDS31D	—	—	—	—
	SN65LVDS3487D	—	—	—	—
	SN65LVDS9638D	SN65LVDS9638DGN	—	—	—
–55°C to 125°C	—	—	SN55LVDS31FK	SN55LVDS31J	SN55LVDS31W

logic symbol†

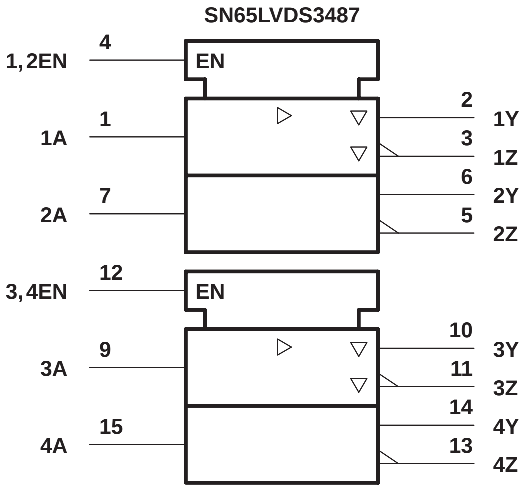


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

’LVDS31 logic diagram (positive logic)

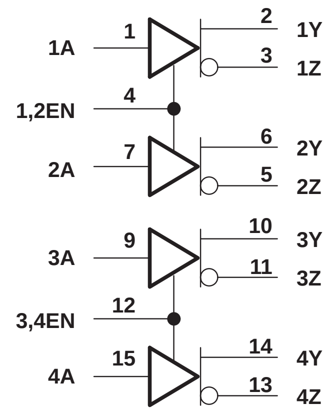


logic symbol†

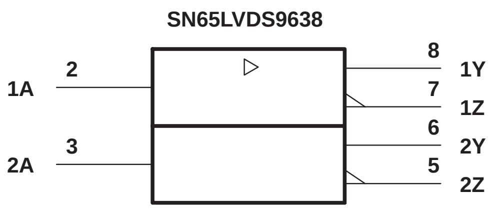


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

’LVDS3487 logic diagram (positive logic)

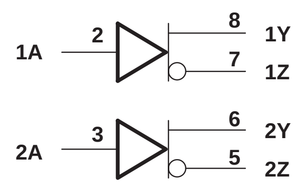


logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

’LVDS9638 logic diagram (positive logic)



Function Tables

SN55LVDS31, SN65LVDS31

INPUT A	ENABLES		OUTPUTS	
	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z
Open	H	X	L	H
Open	X	L	L	H

H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

SN65LVDS3487

INPUT A	ENABLE	OUTPUTS	
	EN	Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z
OPEN	H	L	H

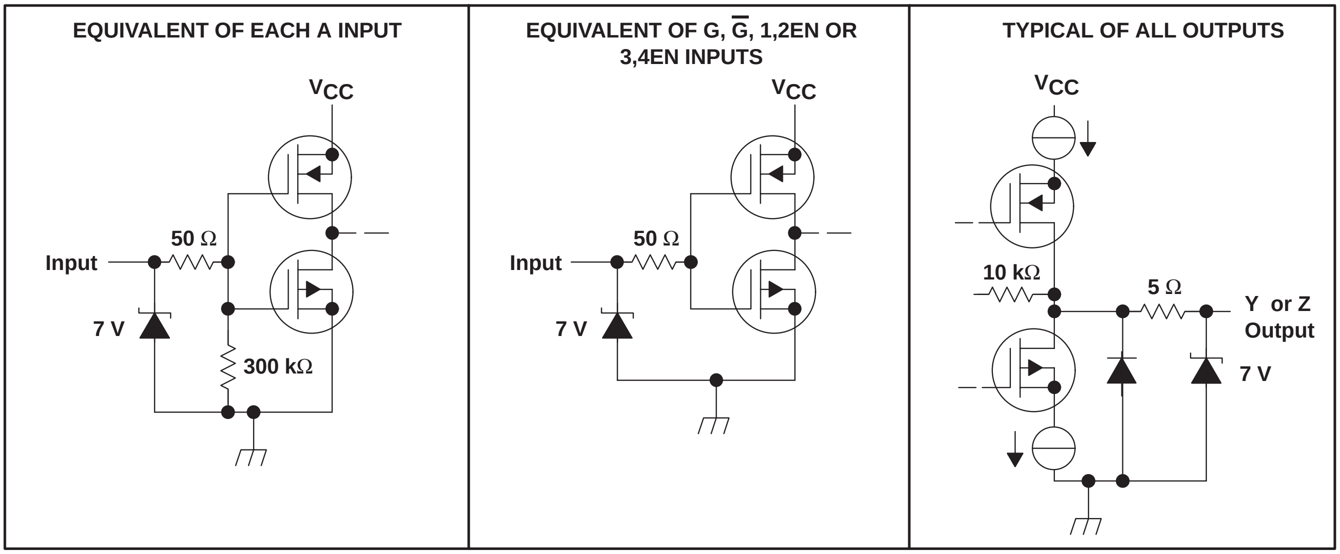
H = high level, L = low level, X = irrelevant,
Z = high impedance (off)

SN65LVDS9638

INPUT A	OUTPUTS	
	Y	Z
H	H	L
L	L	H
OPEN	L	H

H = high level, L = low level

equivalent input and output schematic diagrams



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . –0.5 V to 4 V
Input voltage range, V_I . . . . –0.5 V to V_{CC} + 0.5 V
Continuous total power dissipation . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages, except differential I/O bus voltages, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D (8)	725 mW	5.8 mW/°C	464 mW	377 mW	—
D (16)	950 mW	7.6 mW/°C	608 mW	494 mW	—
DGN	2.14 W	17.1 mW/°C	1.37 W	1.11 W	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
W	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Operating free-air temperature, T_A	SN65 prefix	–40		85	°C
	SN55 prefix	–55		125	°C

SN65LVDSxxxx electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		SN65LVDS31, ’3487, ’ 9638 MIN	TYP†	MAX	UNIT
V_{OD}	Differential output voltage magnitude		R_L = 100 Ω,	See Figure 2	247	340	454	mV
ΔV_{OD}	Change in differential output voltage magnitude between logic states		R_L = 100 Ω,	See Figure 2	–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage		See Figure 3		1.125	1.2	1.375	mV
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		See Figure 3		–50		50	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage		See Figure 3			50	150	mV
I_{CC}	Supply current	SN65LVDS31, ’3487	V_I = 0.8 V or 2 V, No load	Enabled,		9	20	mA
			V_I = 0.8 or 2 V, Enabled	R_L = 100 Ω,		25	35	mA
			V_I = 0 or V_{CC},	Disabled		0.25	1	mA
		SN65LVDS9638	V_I = 0.8 V or 2 V	No load		4.7	8	mA
			V_I = 0.8 V or 2 V	R_L = 100 Ω		9	13	mA
I_{IH}	High-level input current		V_{IH} = 2			4	20	μA
I_{IL}	Low-level input current		V_{IL} = 0.8 V			0.1	10	μA
I_{OS}	Short-circuit output current		$V_{O(Y)}$ or $V_{O(Z)}$ = 0			–4	–24	mA
			V_{OD} = 0				±12	mA
I_{OZ}	High-impedance output current		V_O = 0 or 2.4 V				±1	μA
$I_{O(OFF)}$	Power-off output current		V_{CC} = 0,	V_O = 2.4 V			±1	μA
C_I	Input capacitance					3		pF

† All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.

SN65LVDSxxxx switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN65LVDS31, ’3487, ’ 9638 MIN	TYP†	MAX	UNIT
t_{pLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 2	0.5	1.4	2	ns
t_{pHL}	Propagation delay time, high-to-low-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 2	1	1.7	2.5	ns
t_r	Differential output signal rise time (20% to 80%)	R_L = 100 Ω, C_L = 10 pF, See Figure 2	0.4	0.5	0.6	ns
t_f	Differential output signal fall time (80% to 20%)	R_L = 100 Ω, C_L = 10 pF, See Figure 2	0.4	0.5	0.6	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH}\rvert$)	R_L = 100 Ω, C_L = 10 pF, See Figure 2		0.3	0.6	ns
$t_{sk(o)}$	Channel-to-channel output skew‡	R_L = 100 Ω, C_L = 10 pF, See Figure 2		0	0.3	ns
$t_{sk(pp)}$	Part-to-part skew§				800	ps
t_{pZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 4		5.4	15	ns
t_{pZL}	Propagation delay time, high-impedance-to-low-level output	See Figure 4		2.5	15	ns
t_{pHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 4		8.1	15	ns
t_{pLZ}	Propagation delay time, low-level-to-high-impedance output	See Figure 4		7.3	15	ns

† All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.
‡ $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.
§ $t_{sk(pp)}$ is the magnitude of the different in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, same temperature, and have identical packages and test circuits.

SN55LVDS31 electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN55LVDS31 MIN	TYP†	MAX	UNIT
V_{OD}	Differential output voltage magnitude	$R_L = 100\ \Omega$,	See Figure 2	247	340	454	mV
ΔV_{OD}	Change in differential output voltage magnitude between logic states			–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3		1.125	1.2	1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states			–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				50	150	mV
I_{CC}	Supply current	V_I = 0.8 V or 2 V, No load	Enabled,		9	20	mA
		V_I = 0.8 or 2 V, Enabled	$R_L = 100\ \Omega$,		25	35	mA
		V_I = 0 or V_{CC},	Disabled		0.25	1	mA
I_{IH}	High-level input current	V_{IH} = 2			4	20	μA
I_{IL}	Low-level input current	V_{IL} = 0.8 V			0.1	10	μA
I_{OS}	Short-circuit output current	$V_{O(Y)}$ or $V_{O(Z)}$ = 0			–4	–24	mA
		V_{OD} = 0				±12	mA
I_{OZ}	High-impedance output current	V_O = 0 or 2.4 V				±1	μA
$I_{O(OFF)}$	Power-off output current	V_{CC} = 0,	V_O = 2.4 V			±4	μA
C_I	Input capacitance				3		pF

† All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.

SN55LVDS31 switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN55LVDS31 MIN	TYP†	MAX	UNIT
t_{pLH}	Propagation delay time, low-to-high-level output	$R_L = 100\ \Omega$, See Figure 2	C_L = 10 pF,	0.5	1.4	4	ns
t_{pHL}	Propagation delay time, high-to-low-level output			1	1.7	4.5	ns
t_r	Differential output signal rise time (20% to 80%)			0.4	0.5	1	ns
t_f	Differential output signal fall time (80% to 20%)			0.4	0.5	1	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)				0.3	0.6	ns
$t_{sk(o)}$	Channel-to-channel output skew‡				0.3	0.6	ns
t_{pZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 4			5.4	15	ns
t_{pZL}	Propagation delay time, high-impedance-to-low-level output				2.5	15	ns
t_{pHZ}	Propagation delay time, high-level-to-high-impedance output				8.1	17	ns
t_{pLZ}	Propagation delay time, low-level-to-high-impedance output				7.3	15	ns

† All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.
‡ $t_{sk(o)}$ is the maximum delay time difference between drivers on the same device.

PARAMETER MEASUREMENT INFORMATION

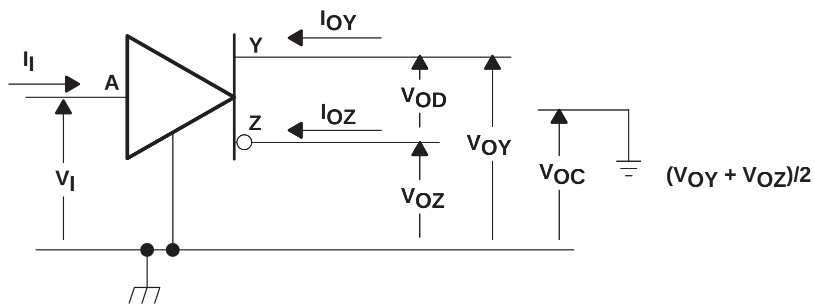
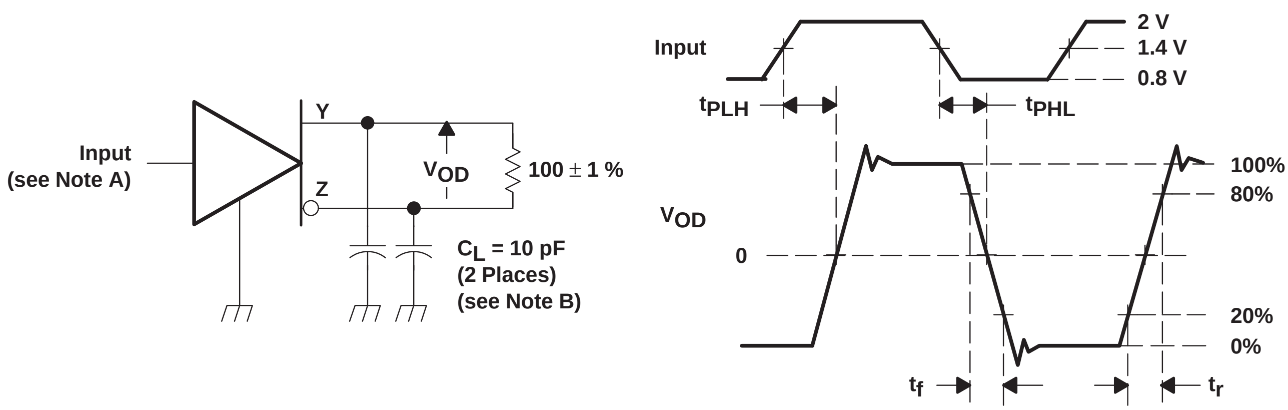
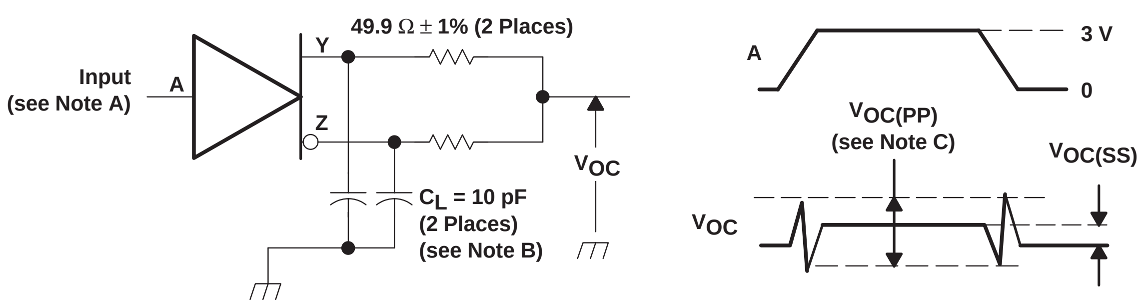


Figure 1. Voltage and Current Definitions



NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.
B. CL includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

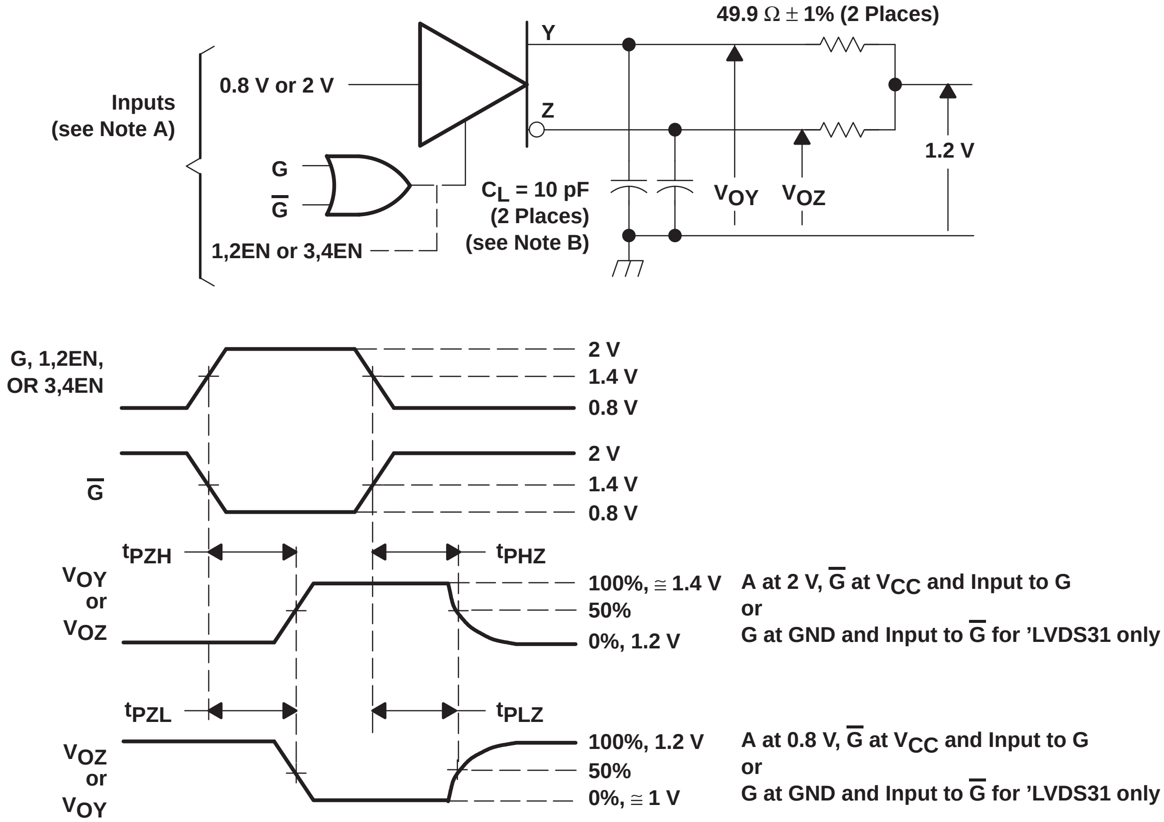
Figure 2. Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.
B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.
C. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION



NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f < 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns.

B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

Figure 4. Enable and Disable Time Circuit and Definitions

TYPICAL CHARACTERISTICS

SN55LVDS31, SN65LVDS31
SUPPLY CURRENT
vs
FREQUENCY

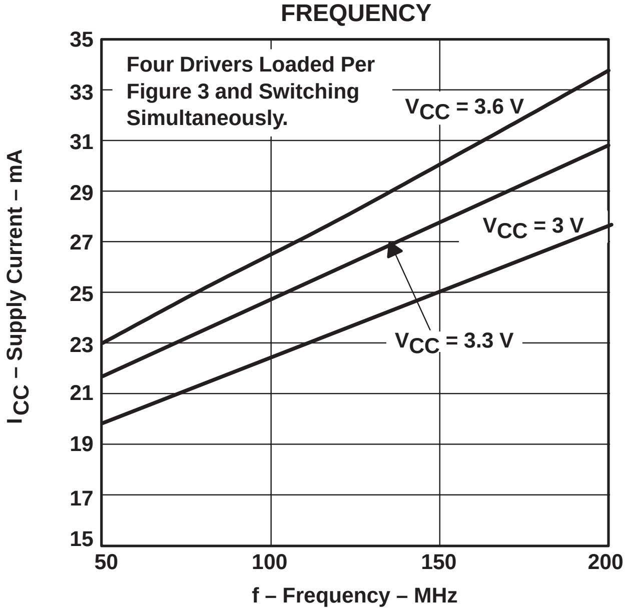


Figure 5

LOW-TO-HIGH PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

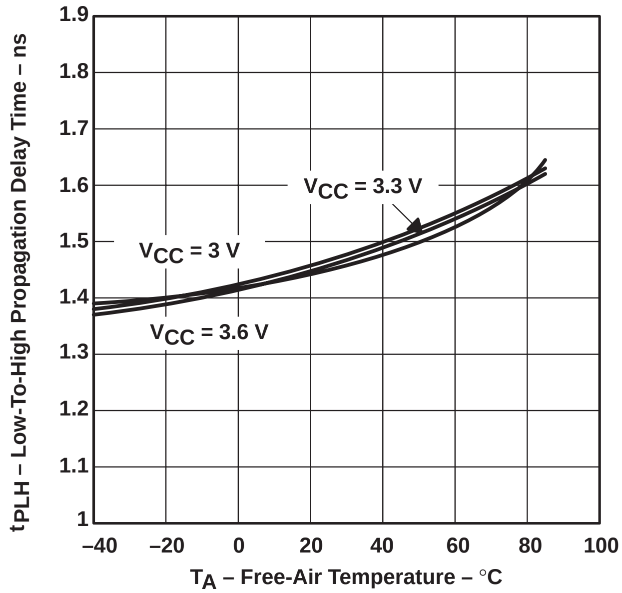


Figure 6

HIGH-TO-LOW PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

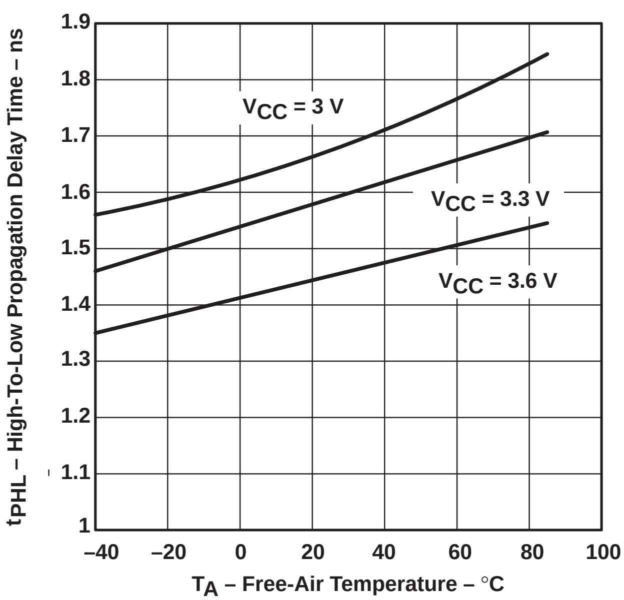
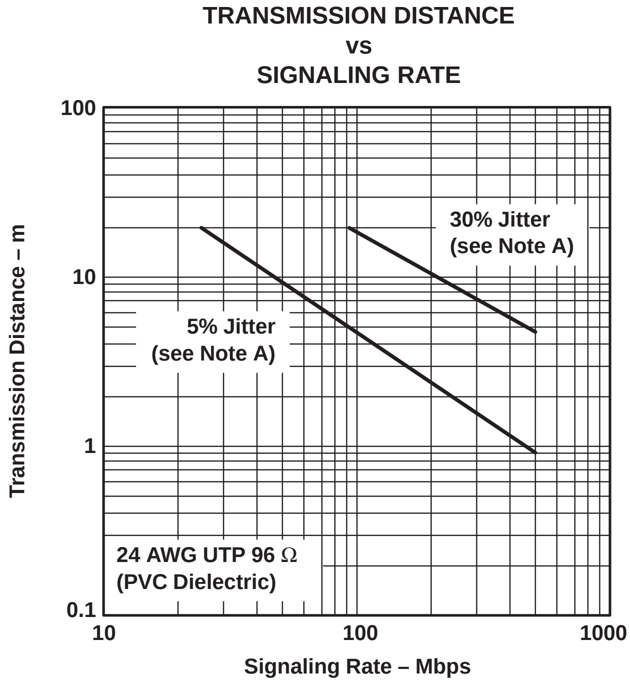


Figure 7

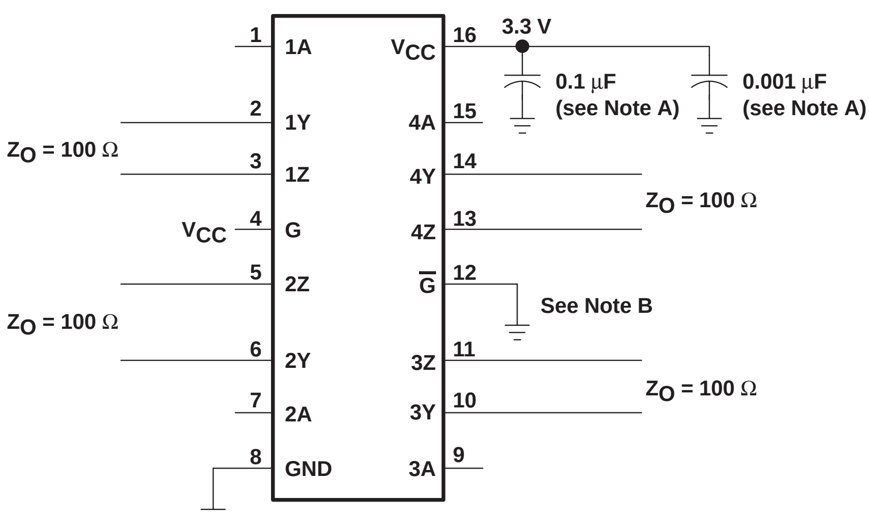
APPLICATIONS INFORMATION

The devices are generally used as building blocks for high-speed point-to-point data transmission where ground differences are less than 1 V. Devices can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/receivers approach ECL speeds without the power and dual supply requirements.



NOTE A: This parameter is the percentage of distortion of the unit interval (UI) with a pseudo-random data pattern.

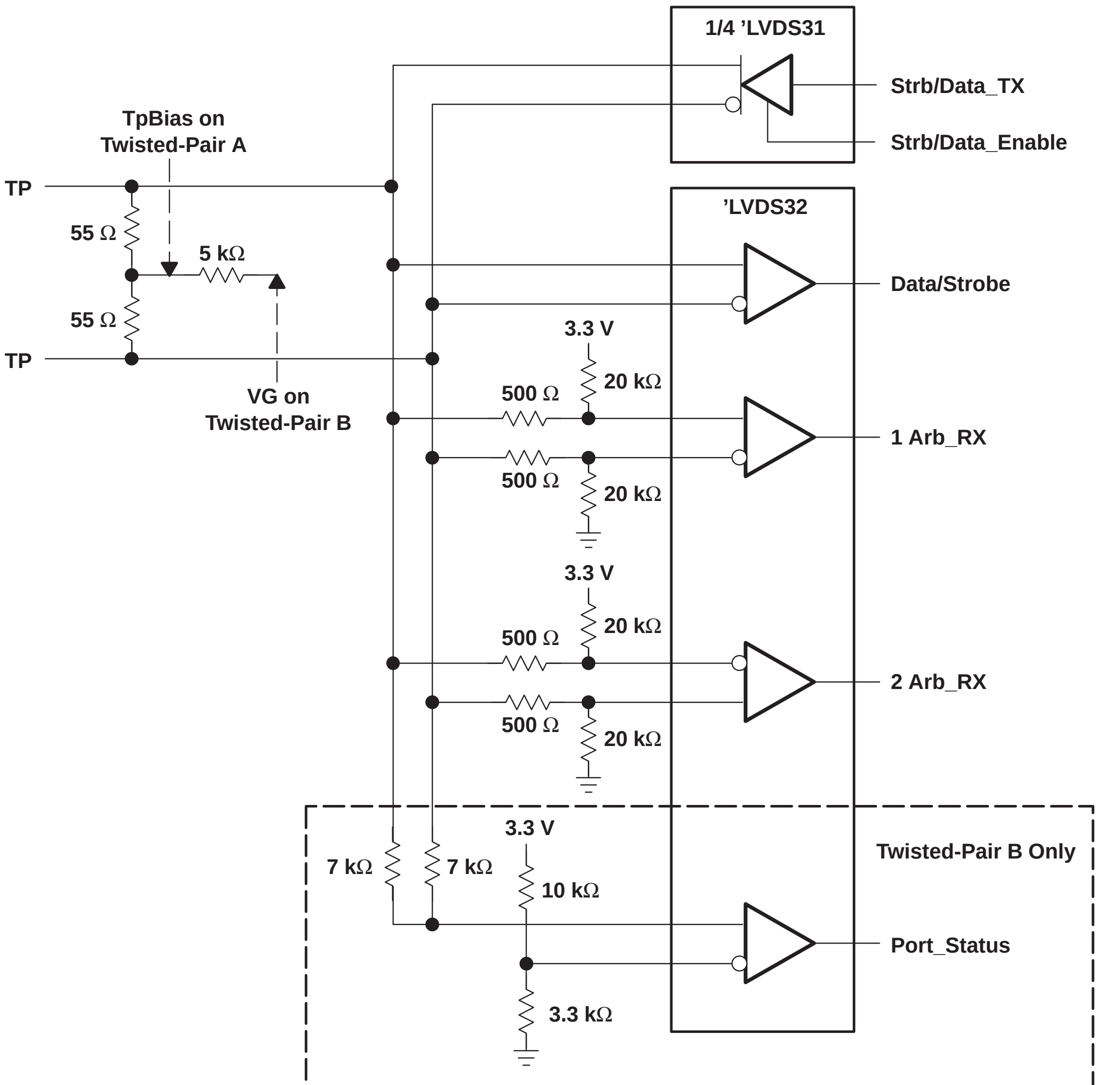
Figure 8. Typical Transmission Distance Versus Signaling Rate



NOTES: A. Place a 0.1 µF and a 0.001 µF Z5U ceramic, mica or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitors should be located as close as possible to the device terminals.
B. Unused enable inputs should be tied to V_{CC} or GND as appropriate.

Figure 9. Typical Application Circuit Schematic

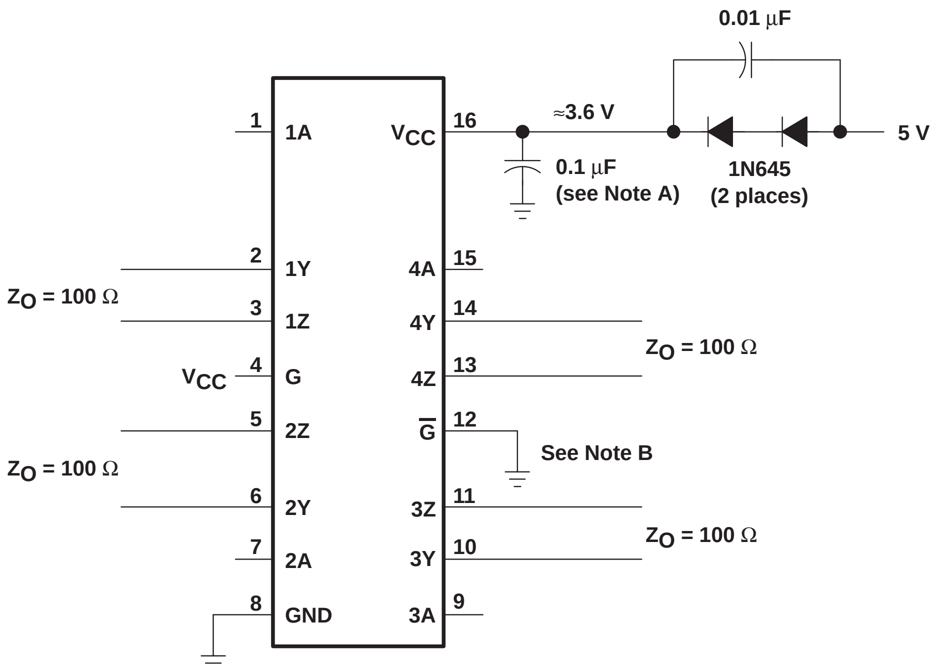
APPLICATIONS INFORMATION



NOTES: A. Resistors are leadless thick-film (0603) 5% tolerance.
B. Decoupling capacitance is not shown but recommended.
C. V_{CC} is 3 V to 3.6 V.
D. The differential output voltage of the ’LVDS31 can exceed that specified by IEEE1394.

Figure 10. 100 Mbps IEEE1394 Transceiver

APPLICATIONS INFORMATION



NOTE A: Place a 0.1 µF Z5U ceramic, mica or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitor should be located as close as possible to the device terminals.

Figure 11. Operation with a 5-V Supply

related information

IBIS modeling is available for this device. Please contact the local TI sales office or the TI Web site at *www.ti.com* for more information.

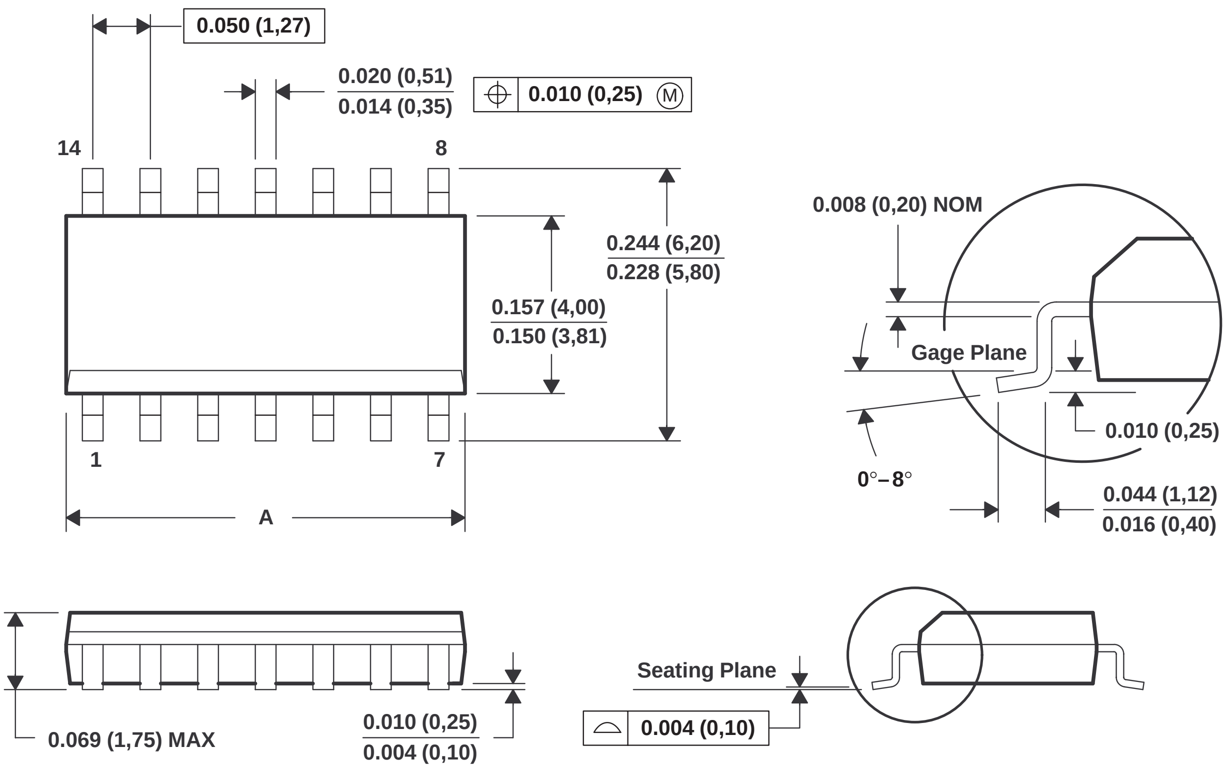
For more application guidelines, please see the following documents:

- *Low-Voltage Differential Signalling Design Notes* (TI literature number SLLA014)
- *Interface Circuits for TIA/EIA-644* (LVDS) (SLLA038)
- *Reducing EMI with LVDS* (SLLA030)
- *Slew Rate Control of LVDS Circuits* (SLLA034)
- *Using an LVDS Receiver with RS-422 Data* (SLLA031)
- *Evaluating the LVDS EVM* (SLLA033)

MECHANICAL INFORMATION

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



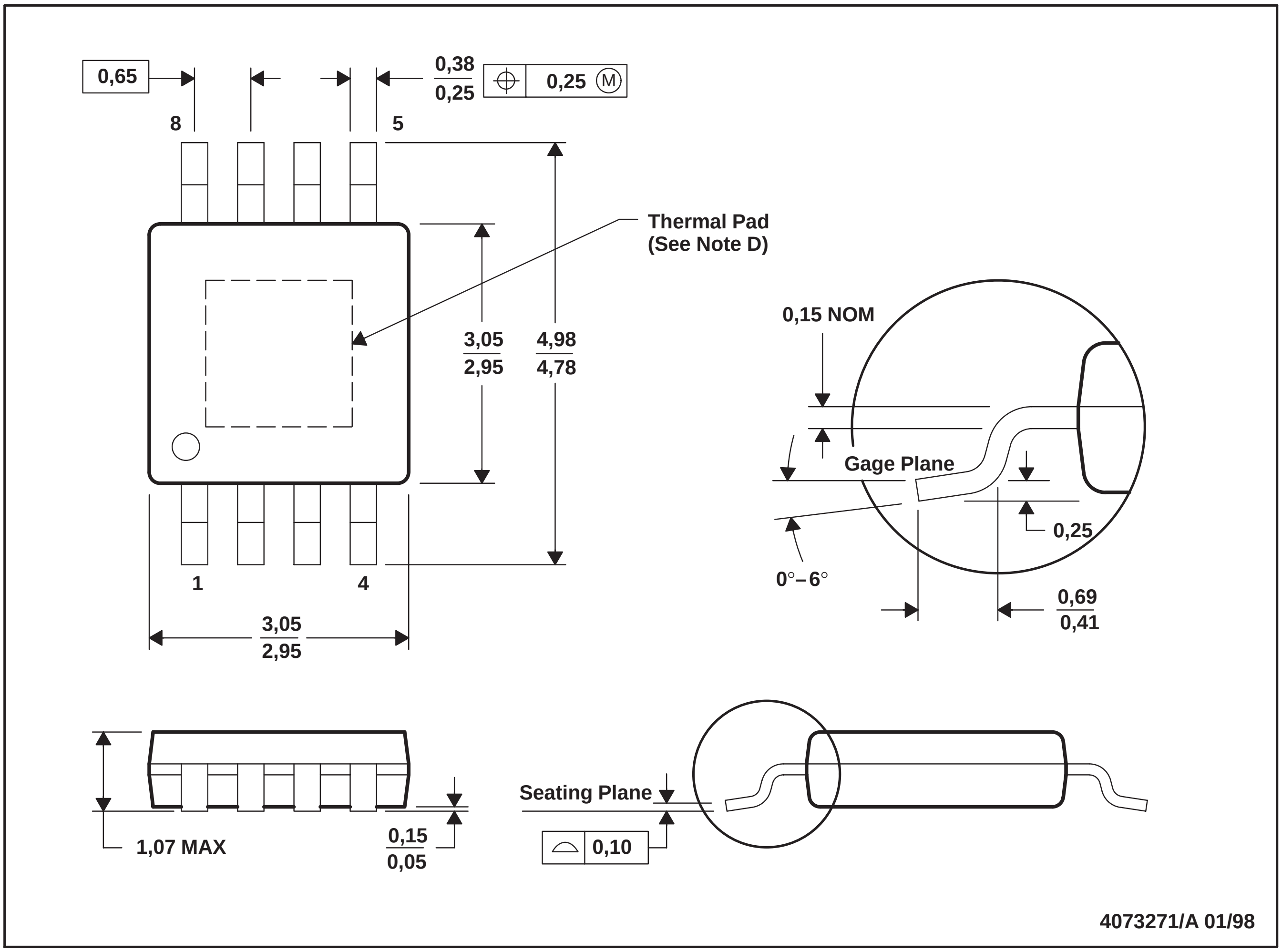
PINS ** / DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

MECHANICAL INFORMATION

DGN (S-PDSO-G8) **PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**



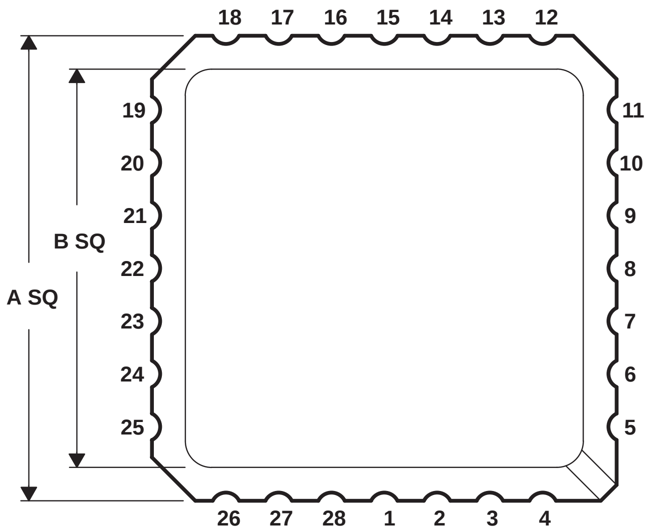
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions include mold flash or protrusions.
D. The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MO-187

PowerPAD is a trademark of Texas Instruments Incorporated.

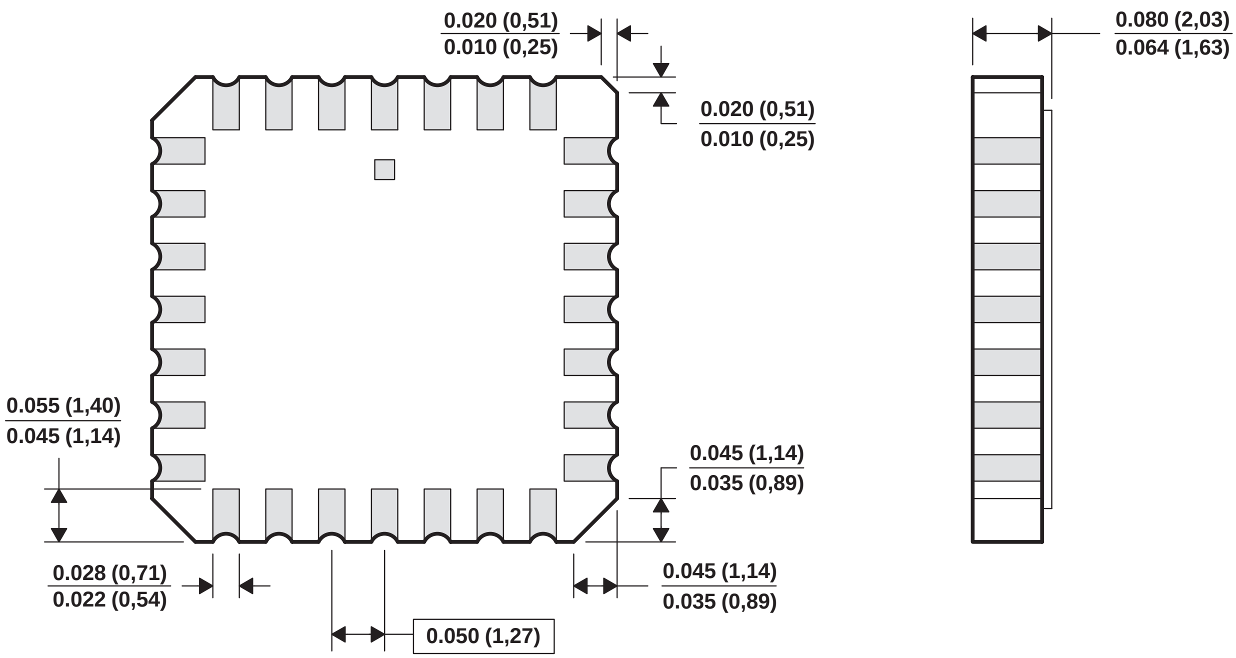
MECHANICAL INFORMATION

FK (S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 10/96

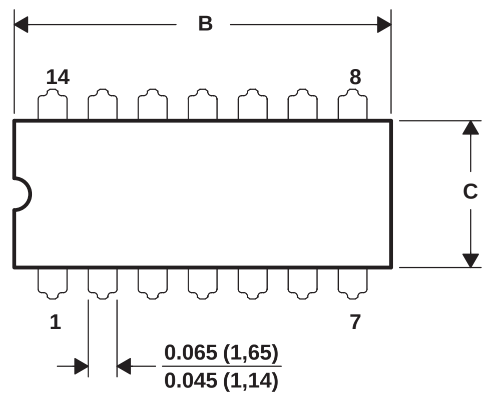
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MS-004

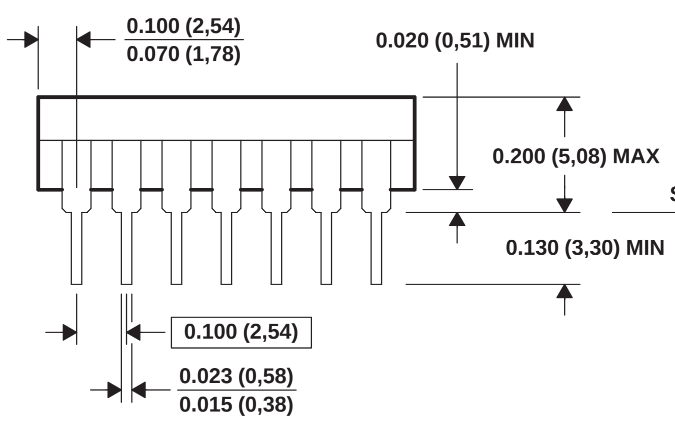
MECHANICAL INFORMATION

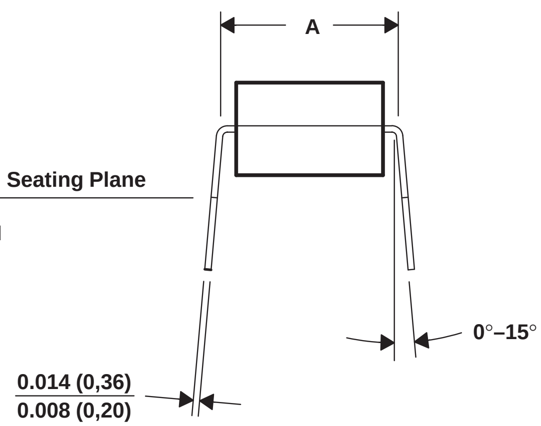
J (R-GDIP-T)** **CERAMIC DUAL-IN-LINE PACKAGE**

14 PIN SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)
B MAX	0.785 (19,94)	0.785 (19,94)	0.910 (23,10)	0.975 (24,77)
B MIN	0.755 (19,18)	0.755 (19,18)	—	0.930 (23,62)
C MAX	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)





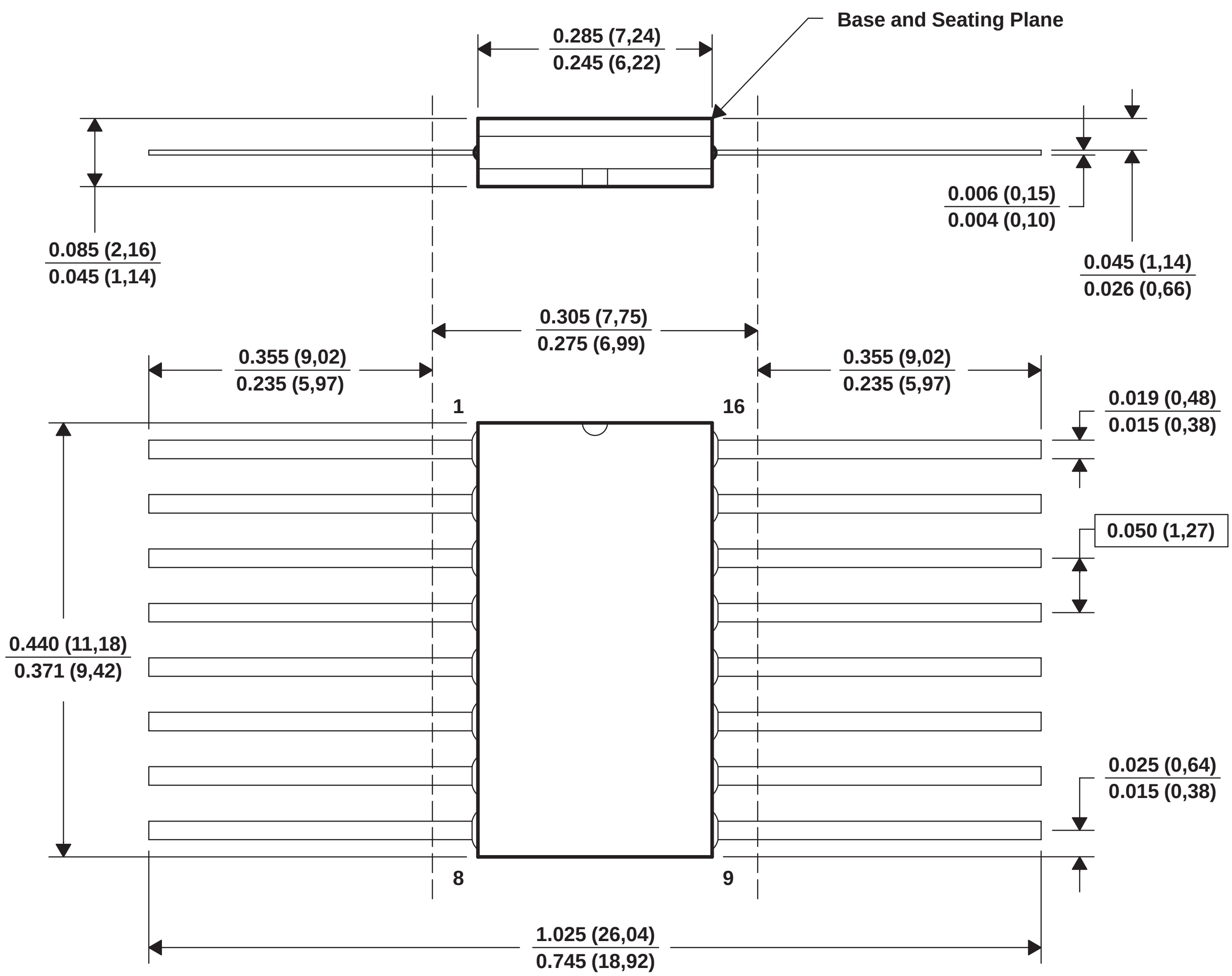


4040083/D 08/98

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, GDIP1-T20, and GDIP1-T22.

MECHANICAL INFORMATION

W (R-GDFP-F16) **CERAMIC DUAL FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL-STD-1835 GDFP1-F16 and JEDEC MO-092AC

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