Synchronous SEPIC/ Inverting/Boost Controller with Output Current Control

FEATURES

- **Wide Input Range: 4.5V to 80V**
- **Rail-to-Rail Output Current Monitor and Control**
- **Input Voltage Regulation for High Impedance Inputs**
- **C/10 or Power Good Indication Pin**
- **MODE Pin for Forced CCM or Pulse-Skipping Operation**
- Switching Frequency Up to 750kHz
- Easily Configurable as a Boost, SEPIC, Inverting or Flyback Converter with Single Feedback Pin
- Can Be Synchronized to External Clock
- High Gain EN/FBIN Pin Accepts Slowly Varying Input Signals
- 20-Lead TSSOP Package

APPLICATIONS

- High Power Local Power Supply
- Wide Input Voltage Range SEPIC/Inverting
- Lead Acid Battery Charger
- Automotive Engine Control Unit (ECU) Power
- Solar Panel Power Converter

DESCRIPTION

The LT®8710 is a synchronous PWM DC/DC controller with a rail-to-rail output current monitor and control. The LT8710 is ideal for many types of power supply topologies and can be easily configured for boost, SEPIC, inverting, or flyback configurations.

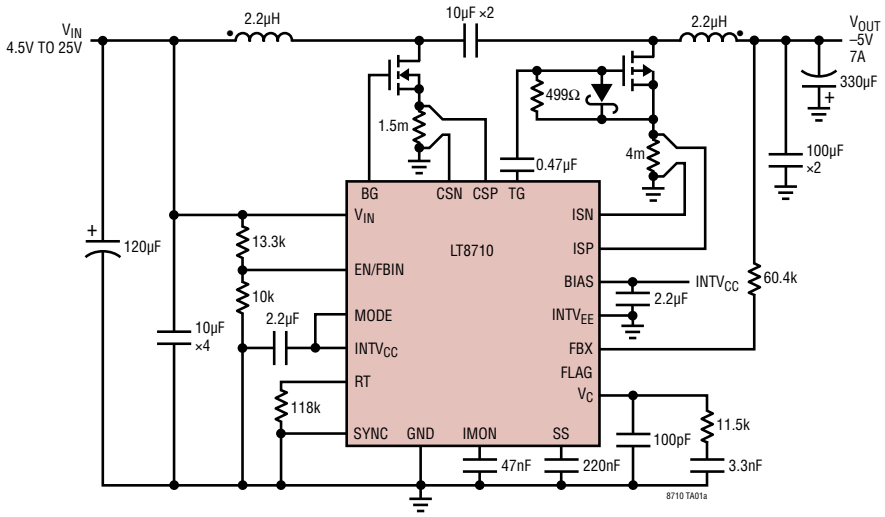
The LT8710's rail-to-rail output current monitor and control allows the part to be configured in current limited applications such as battery charging. The FLAG pin can be used as a power good indication or C/10 indication allowing for accurate bulk and float battery voltages.

The LT8710's switching frequency range can be set between 100kHz and 750kHz using an external resistor or synchronized to an external clock.

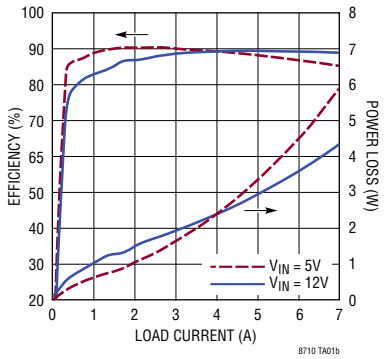
The LT8710 also features innovative EN/FBIN pin circuitry that allows for slowly varying input signals and an adjustable undervoltage lockout function. The pin is also used for input voltage regulation to avoid collapsing a high impedance input supply. Additional features such as frequency foldback and soft-start are integrated. The LT8710 is available in a 20-lead TSSOP package.

TYPICAL APPLICATION

300kHz Inverter Generates –5V from a 4.5V to 25V Input



Efficiency and Power Loss

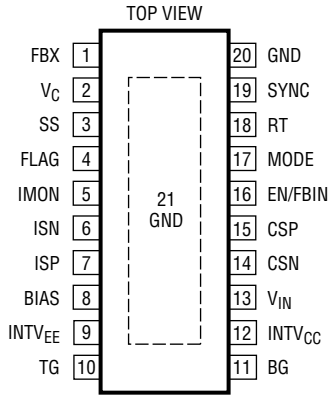


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Voltage ..... –0.3V to 80V
BIAS Voltage ..... –0.3V to 80V
EN/FBIN Voltage..... –0.3V to 80V
BG Voltage .....Note 5
TG Voltage .....Note 5
RT Voltage ..... –0.3V to 5V
SS Voltage ..... –0.3V to 3V
FBX Voltage.....5V
FBX Current.....–1mA
V_C Voltage..... –0.3V to 2V
SYNC Voltage..... –0.3V to 5.5V
FLAG Voltage ..... –0.3V to 7V
FLAG Current ..... ±1mA
MODE Voltage..... –0.3V to 40V
$INTV_{CC}$ Voltage ..... –0.3V to 7V
$INTV_{EE}$ Voltage.....Note 5
CSP Voltage ..... –0.3V to 2V
CSN Voltage..... –0.3V to 2V
ISP Voltage ..... ISN – 0.4V to ISN + 2V
ISN Voltage..... –0.3V to 80V
IMON Voltage..... –0.3V to 2.5V
Operating Junction Temperature Range
LT8710E..... –40°C to 125°C
LT8710I..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PIN CONFIGURATION



FE PACKAGE
20-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 38°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8710EFE#PBF	LT8710EFE#TRPBF	LT8710FE	20-Lead Plastic TSSOP	–40°C to 125°C
LT8710IFE#PBF	LT8710IFE#TRPBF	LT8710FE	20-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications for each channel are at T_A = 25°C. V_{IN} = 12V, $V_{EN/FBIN}$ = 12V, V_{BIAS} = 12V, unless otherwise noted (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Operating Input Voltage	V_{IN} OR V_{BIAS} V_{IN} if $V_{BIAS} \geq$ 4.5V	● 	 0	4.25	4.5	V V
Quiescent Current, I_{VIN}	V_{BIAS} = V_{ISN} = 7.5V, Not Switching V_{BIAS} = 6.3V, V_{INTVEE} = V_{ISN} = 0V, Not Switching			4 5.5	5.5 7.5	mA mA
Quiescent Current in Shutdown	$V_{EN/FBIN}$ = 0V			0	1	µA
EN/FBIN Active Mode	EN/FBIN Rising	●	1.64	1.7	1.76	V
EN/FBIN Chip Enable	EN/FBIN Rising EN/FBIN Falling	● ●	1.22 1.18	1.3 1.26	1.38 1.34	V V
EN/FBIN Chip Enable Hysteresis				44		mV
EN/FBIN Input Voltage Low	Shutdown Mode	●			0.3	V
EN/FBIN Pin Bias Current	$V_{EN/FBIN}$ = 3V $V_{EN/FBIN}$ = 1.7V $V_{EN/FBIN}$ = 1.6V $V_{EN/FBIN}$ = 0V		 14 13	44 19.5 17.5 0	60 25 22.5 0.1	µA µA µA µA
SS Charge Current	V_{SS} = 0V, Current Flows Out of SS Pin	●	7	10.1	13.8	µA
SS Low Detection Voltage	Part Exiting Undervoltage Lockout	●	18	50	82	mV
SS Hi Detection Voltage	SS Rising SS Falling		1.5 1.3	1.8 1.7	2.1 2.05	V V
SS Hi Detection Hysteresis				100		mV
Low Dropout Regulators, $INTV_{CC}$ and $INTV_{EE}$						
$INTV_{CC}$ Voltage	I_{INTVCC} = 10mA	●	6.2	6.3	6.4	V
$INTV_{CC}$ Undervoltage Lockout	$INTV_{CC}$ Rising $INTV_{CC}$ Falling	● ●	3.88 3.5	4 3.73	4.12 3.95	V V
$INTV_{CC}$ Undervoltage Lockout Hysteresis				270		mV
$INTV_{CC}$ Dropout Voltage	V_{IN} – $INTV_{CC}$, V_{IN} = 6V, V_{BIAS} = 0V, I_{INTVCC} = 10mA V_{BIAS} – V_{INTVCC}, V_{IN} = 0V, V_{BIAS} = 6V, I_{INTVCC} = 10mA			255 280		mV mV
$INTV_{CC}$ Load Regulation	V_{IN} = 12V, V_{BIAS} = 0V, I_{INTVCC} = 0mA to 80mA V_{IN} = 0V, V_{BIAS} = 12V, I_{INTVCC} = 0mA to 40mA			–0.44 –0.34	–2 –2	% %
$INTV_{CC}$ Line Regulation	10V ≤ V_{IN} ≤ 80V, V_{BIAS} = 0V, I_{INTVCC} = 10mA 10V ≤ V_{BIAS} ≤ 80V, V_{IN} = 0V, I_{INTVCC} = 10mA			–0.003 –0.006	–0.03 –0.03	%/V %/V
$INTV_{CC}$ Maximum External Load Current					5	mA
$INTV_{EE}$ Voltage, V_{BIAS} – V_{INTVEE}	I_{INTVEE} = 10mA	●	6.03	6.18	6.33	V
$INTV_{EE}$ Undervoltage Lockout, V_{BIAS} – V_{INTVEE}	V_{BIAS} – V_{INTVEE} Rising V_{BIAS} – V_{INTVEE} Falling	● ●	3.24 2.94	3.42 3.22	3.6 3.48	V V
$INTV_{EE}$ Undervoltage Lockout Hysteresis, V_{BIAS} – V_{INTVEE}				200		mV
$INTV_{EE}$ Dropout Voltage, V_{INTVEE}	V_{BIAS} = 6V, I_{INTVEE} = 10mA			0.75		V
Control Loops (Refer to Block Diagram to Locate Amplifiers)						
Current Limit Voltage, V_{CSP} – V_{CSN}	V_{FBX} = 1.1V, Minimum Duty Cycle V_{FBX} = 1.1V, Maximum Duty Cycle	● ●	46 23	50 31	54 38	mV mV
	V_{FBX} = 1.4V, MODE = 0V, Minimum Duty Cycle V_{FBX} = 1.4V, MODE = 0V, Maximum Duty Cycle	● ●	–23 –38	–32 –51	–41 –65	mV mV
FBX Positive Output Regulation Voltage, EA1		●	1.191	1.213	1.237	V
FBX Negative Output Regulation Voltage, EA2		●	–2	9.6	21	mV

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Positive FBX Pin Bias Current	V_{FBX} = Positive FBX Reg Voltage, Current into Pin	●	81.9	83.7	85.6	µA
Negative FBX Pin Bias Current	V_{FBX} = Negative FBX Reg Voltage, Current Out of Pin	●	81.1	83.1	85.2	µA
FBX Amp Transconductance, EA1 or EA2	ΔI = 2µA			200		µmhos
FBX Amp Voltage Gain, EA1 or EA2				70		V/V
FBX Line Regulation	4.5V ≤ V_{IN} ≤ 80V, V_{BIAS} = 0V		–0.02	–0.001	0.02	%/V
Output Current Sense Regulation Voltage, $V_{ISP} – V_{ISN}$	V_{ISN} = 80V, V_{FBX} = 1V V_{ISN} = 12V, V_{FBX} = 1V V_{ISN} = 0V, V_{FBX} = 1V V_{ISN} = 12V, V_{FBX} = 1V, $INTV_{EE}$ in UVLO and V_{SS} > 1.8V	● ● ● ●	43 43 40 17	50 50 50 25	57 57 60 34	mV mV mV mV
IMON Regulation Voltage, EA3	V_{FBX} = 1V V_{FBX} = 1V, $INTV_{EE}$ in UVLO and V_{SS} > 1.8V	● ●	1.184 0.885	1.213 0.916	1.24 0.947	V V
Output Current Sense Amp Transconductance, A6	ΔI = 10µA			1000		µmhos
Output Current Sense Amp Voltage Gain, A6				11.9		V/V
Output Current Sense Amp Input Dynamic Range, A6	Negative Input Range, $V_{ISP} – V_{ISN}$ Positive Input Range, $V_{ISP} – V_{ISN}$		500	–51.8		mV mV
IMON Amp Transconductance, EA3	ΔI = 2µA, V_{FBX} = 1V			165		µmhos
IMON Amp Voltage Gain, EA3	V_{FBX} = 1V			65		V/V
EN/FBIN Input Regulation Voltage, EA4	V_{FBX} = 1V	●	1.55	1.607	1.662	V
EN/FBIN Amp Transconductance, EA4	ΔI = 2µA, V_{FBX} = 1V			140		µmhos
EN/FBIN Amp Voltage Gain, EA4	V_{FBX} = 1V			55		V/V
MODE Forced CCM Threshold	To Exit Forced CCM Mode, MODE Rising To Enter Forced CCM Mode, MODE Falling	● ●	1.19 1.125	1.224 1.175	1.258 1.23	V V
MODE Forced CCM Threshold Hysteresis				49		mV
DCM Comparator Threshold in Pulse-Skipping Mode, MODE = 2V	V_{ISN} = 80V, To Enter DCM Mode, $V_{ISP} – V_{ISN}$ Falling V_{ISN} = 12V, To Enter DCM Mode, $V_{ISP} – V_{ISN}$ Falling V_{ISN} = 0V, To Enter DCM Mode, $V_{ISP} – V_{ISN}$ Falling	● ● ●	–4.5 –4.5 –7.5	2.8 2.8 2.8	10 10 13	mV mV mV
DCM Comparator Threshold in Forced CCM, MODE =0V	V_{ISN} = 80V, To Enter DCM Mode, $V_{ISP} – V_{ISN}$ Falling V_{ISN} = 12V, To Enter DCM Mode, $V_{ISP} – V_{ISN}$ Falling V_{ISN} = 0V, To Enter DCM Mode, $V_{ISP} – V_{ISN}$ Falling	● ● ●	–220 –220 –220	–300 –300 –300	–380 –380 –380	mV mV mV
Oscillator						
Switching Frequency, f_{OSC}	R_T = 46.4k R_T = 357k	● ●	640 85	750 100	860 115	kHz kHz
Switching Frequency in Foldback	Compared to Normal f_{OSC}			1/5		ratio
Switching Frequency Range	Free-Running or Synchronizing	●	100		750	kHz
SYNC High Level for Sync		●	1.5			V
SYNC Low Level for Sync		●			0.4	V
SYNC Clock Pulse Duty Cycle	V_{SYNC} = 0V to 3V		20		80	%
Recommended Min SYNC Ratio f_{SYNC}/f_{OSC}				3/4		

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications for each channel are at T_A = 25°C. V_{IN} = 12V, $V_{EN/FBIN}$ = 12V, V_{BIAS} = 12V, unless otherwise noted (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Drivers, BG and TG						
BG Rise Time	C_{BG} = 3300pF (Note 3)			24		ns
BG Fall Time	C_{BG} = 3300pF (Note 3)			21		ns
TG Rise Time	C_{TG} = 3300pF (Note 3)			15		ns
TG Fall Time	C_{TG} = 3300pF (Note 3)			16		ns
BG and TG Non-Overlap Time	TG Rising to BG Rising, C_{BG} = C_{TG} = 3300pF (Note 3) BG Falling to TG Falling, C_{BG} = C_{TG} = 3300pF (Note 3)		80 45	140 90	220 150	ns ns
BG Minimum On-Time	C_{BG} = C_{TG} = 3300pF		150		420	ns
BG Minimum Off-Time	C_{BG} = C_{TG} = 3300pF		100		480	ns
TG Minimum On-Time	C_{BG} = C_{TG} = 3300pF		0		150	ns
TG Minimum Off-Time	C_{BG} = C_{TG} = 3300pF		290		770	ns
C/10 and Power Good Indicators, FLAG						
FLAG C/10 Indicator Threshold	V_{ISP} – V_{ISN} Falling, V_{FBX} = 1.215V V_{ISP} – V_{ISN} Rising, V_{FBX} = 1.215V	● ●	1 4	5 10	16 23	mV mV
FLAG C/10 Indicator Hysteresis				5		mV
FLAG Power Good Threshold for Positive FBX Voltage	V_{FBX} Rising, V_{ISP} – V_{ISN} = 0V V_{FBX} Falling, V_{ISP} – V_{ISN} = 0V	● ●	1.127 1.062	1.153 1.095	1.184 1.126	V V
FLAG Power Good Threshold for Negative FBX Voltage	V_{FBX} Falling, V_{ISP} – V_{ISN} = 0V V_{FBX} Rising, V_{ISP} – V_{ISN} = 0V	● ●	46 103	68.5 126	90 152	mV mV
FLAG Power Good Hysteresis for Positive or Negative FBX Voltage				58		mV
FLAG Anti-Glitch	Delay from C/10 or Power Good Threshold Trip to FLAG Toggle			100		µs
FLAG Output Voltage Low	100µA into FLAG Pin	●		9	50	mV
FLAG Leakage Current	V_{FLAG} = 7V, FLAG Off			0.01	1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8710E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LT8710I is guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 3: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

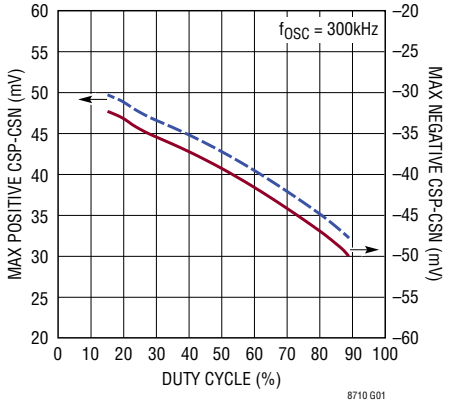
Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation over the specified maximum operating junction temperature may impair device reliability.

Note 5: Do not apply a positive or negative voltage or current source to the BG, TG, and $INTV_{EE}$ pins, otherwise permanent damage may occur.

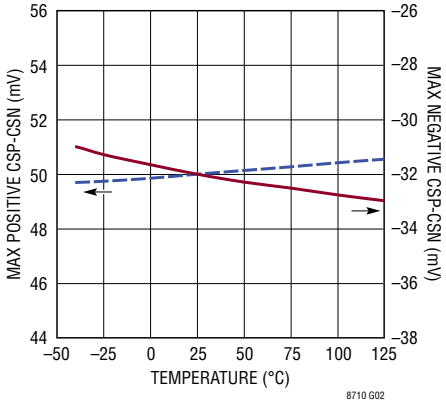
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

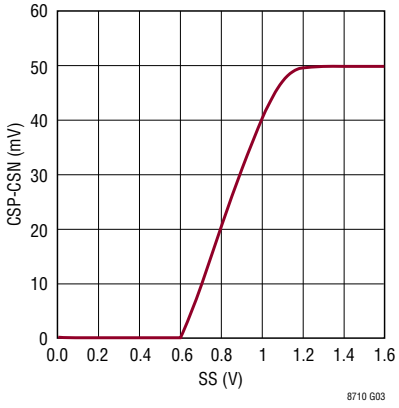
Max Current Limit vs Duty Cycle (CSP - CSN)



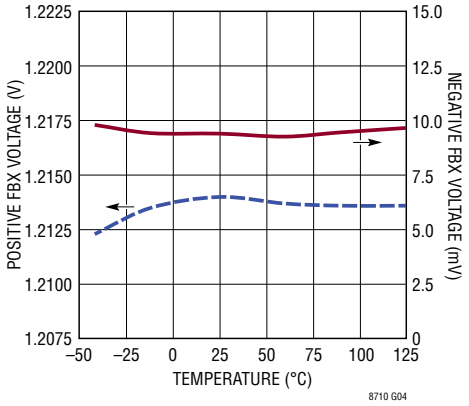
Max Current Limit vs Temperature at Min DC (CSP - CSN)



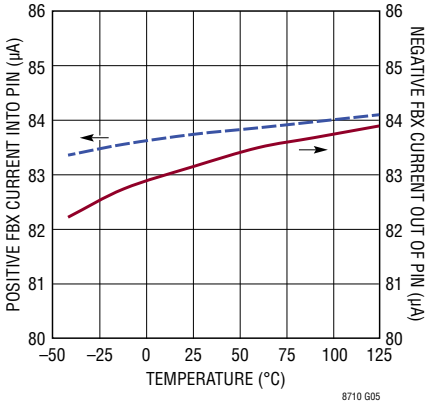
Max Current Limit vs SS (CSP - CSN)



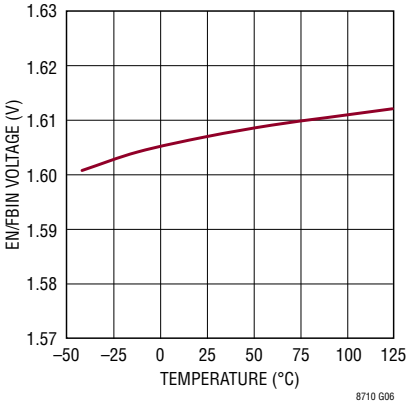
Positive and Negative Output Voltage Regulation (FBX)



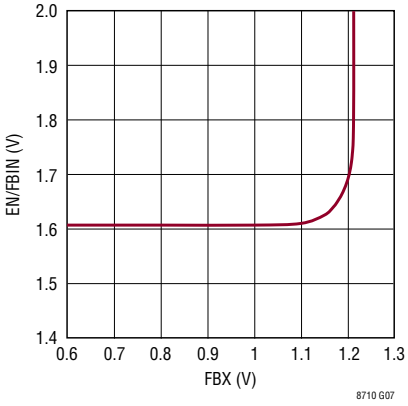
Positive and Negative FBX Current at Output Voltage Regulation



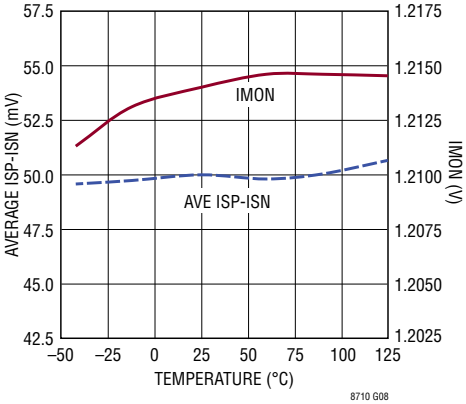
Input Voltage Regulation (EN/FBIN)



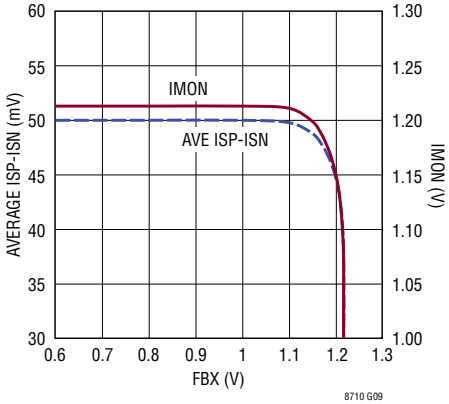
Input Voltage Regulation vs FBX (EN/FBIN)



Output Current Sense Regulation Voltage (ISP-ISN and IMON)

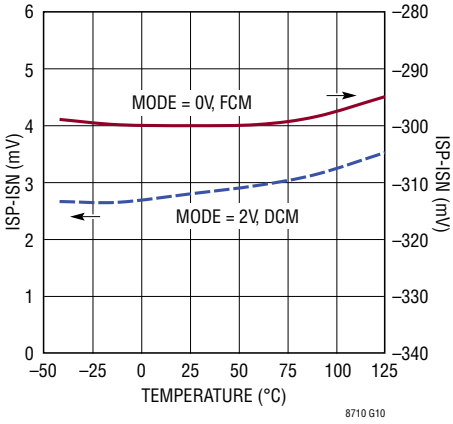


Output Current Sense Regulation Voltage vs FBX (ISP-ISN and IMON)

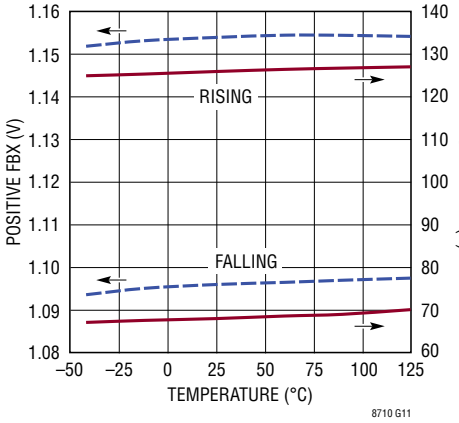


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

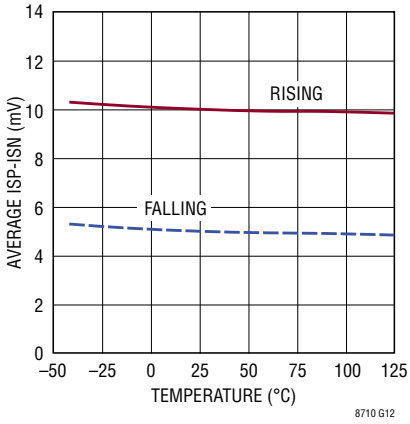
DCM Thresholds (ISP-ISN)



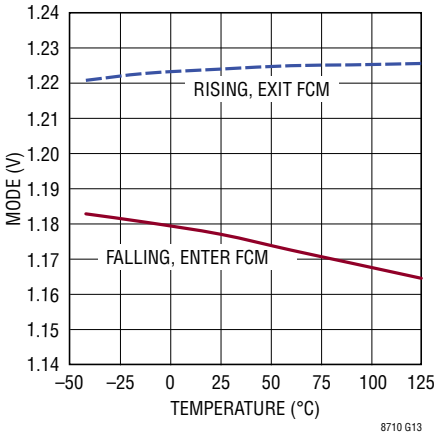
Power Good Thresholds (FBX)



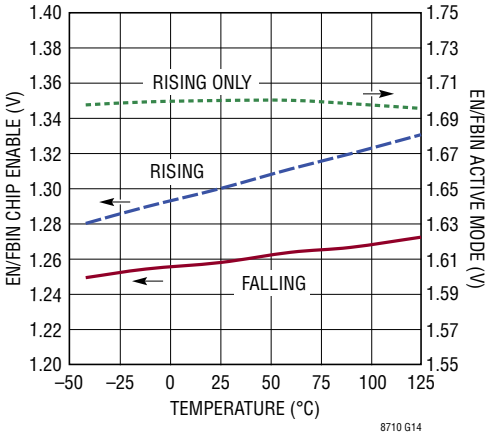
C/10 Thresholds (ISP-ISN)



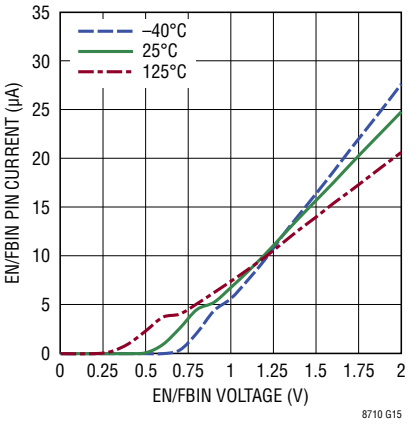
MODE Forced CCM Thresholds



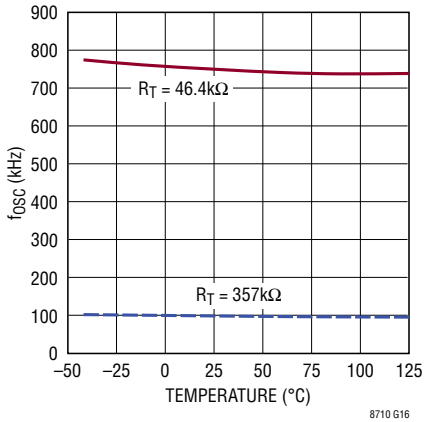
EN/FBIN Chip Enable and Active Mode Thresholds



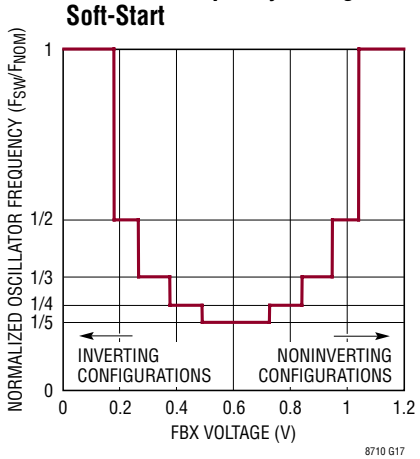
EN/FBIN Pin Current



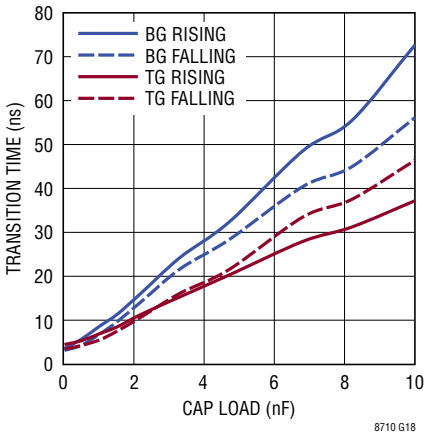
Oscillator Frequency vs Temperature



Oscillator Frequency During Soft-Start



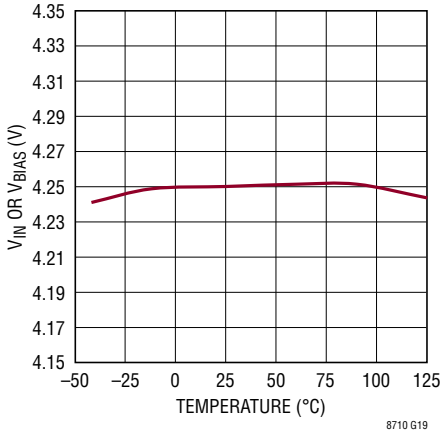
BG and TG Transition Time



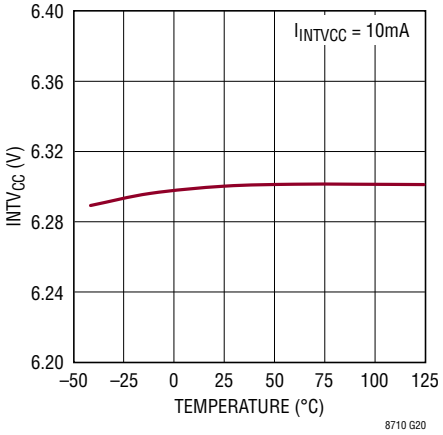
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

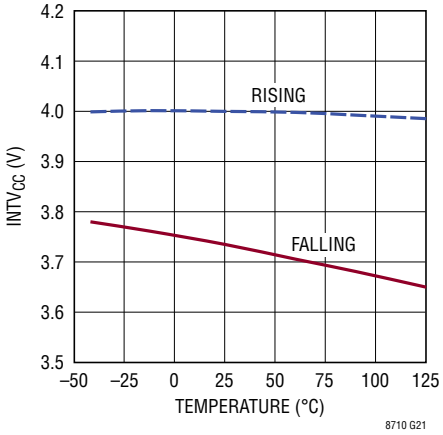
Minimum Operating Input Voltage



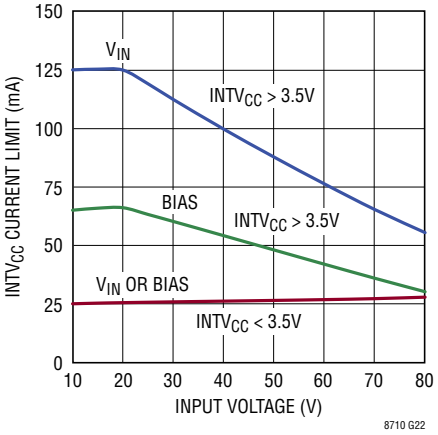
$INTV_{CC}$ vs Temperature



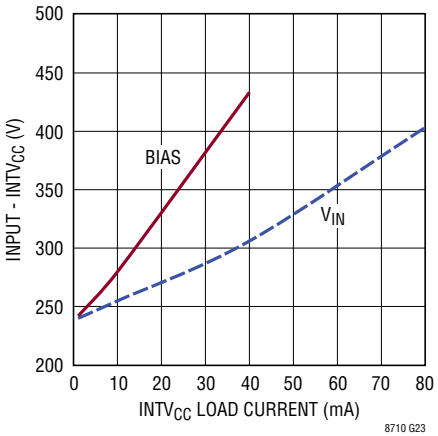
$INTV_{CC}$ UVLO vs Temperature



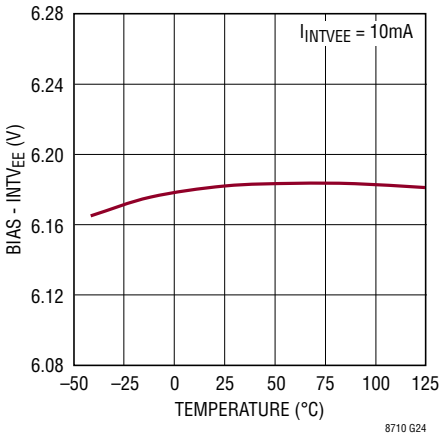
$INTV_{CC}$ Current Limit vs V_{IN} or BIAS



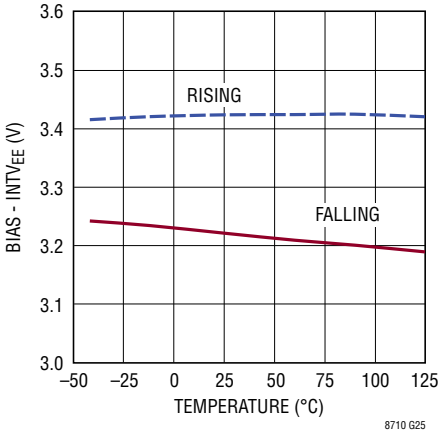
$INTV_{CC}$ Dropout from V_{IN} or BIAS



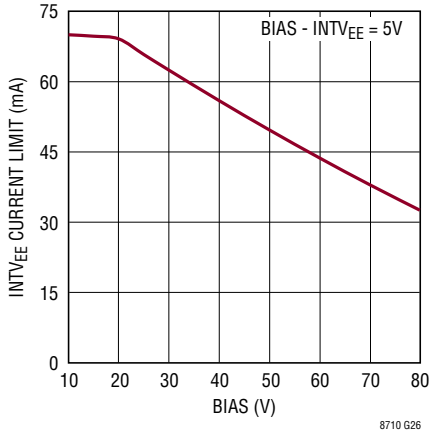
$INTV_{EE}$ vs Temperature



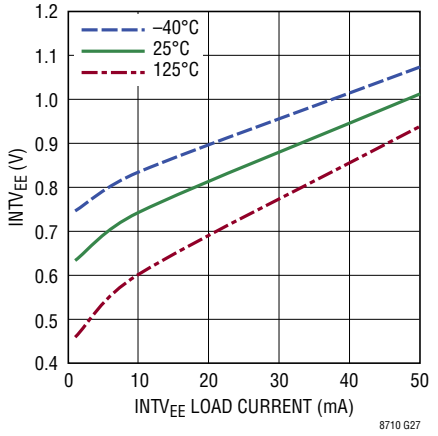
$INTV_{EE}$ UVLO vs Temperature



$INTV_{EE}$ Current Limit vs BIAS



$INTV_{EE}$ Dropout (BIAS = 6V)



PIN FUNCTIONS

FBX (Pin 1): Positive and Negative Feedback Pin. For a boost, SEPIC, or inverting converter, tie a resistor from the FBX pin to V_{OUT} according to the following equations:

$$R_{FBX} = \left(\frac{V_{OUT} - 1.213V}{83.7\mu A}\right) \text{ ; Boost or SEPIC Converter}$$

$$R_{FBX} = \left(\frac{|V_{OUT}| + 9.6mV}{83.1\mu A}\right) \text{ ; Inverting Converter}$$

V_C (Pin 2): Error Amplifier Output Pin. Tie external compensation network to this pin.

SS (Pin 3): Soft-Start Pin. Place a soft-start capacitor here that is greater than 5x the IMON capacitor. Upon start-up, the SS pin will be charged by a (nominally) 260k resistor to ~2.7V. During a current overload as seen by ISP - ISN, overtemperature, or UVLO condition, the SS pin will be quickly discharged to reset the part. Once those conditions are clear, the part will attempt to restart.

FLAG (Pin 4): Power Good or C/10 Indication Pin. The FLAG pin functions as an active high power good pin if C/10 is true. Alternatively, the FLAG pin functions as an active high C/10 indication pin if power is good. Power is good when FBX < 68.5mV or FBX > 1.153V and has 58mV of hysteresis. When FBX = 1.153V, it's 5% below regulation which corresponds to ~10% below regulation on V_{OUT} (for V_{OUT} > 8V). Active high C/10 indication is when the charge current seen by the ISP and ISN pins is less than 10% of full current ($V_{ISP} - V_{ISN}$ < 5mV) as the charge current decreases. For increasing charge currents, the C/10 threshold has to reach 20% of full current ($V_{ISP} - V_{ISN}$ > 10mV). The C/10 indication can be used to set the bulk and float voltage when charging a battery. For either C/10 or power good indicators, there is a 100µs anti-glitch delay. A pull-up resistor or some other form of pull-up network needs to exist on this pin to use these features. See the Block Diagram and Applications section for more information.

IMON (Pin 5): Output Current Sense Monitor Output Pin. Outputs a voltage that is proportional to the voltage seen across the ISP and ISN pins.

$$V_{IMON} = 11.9 \bullet (V_{ISP-ISN} + 51.8mV)$$

Since the voltage across the ISP and ISN pins is AC, a filtering capacitor is needed on the IMON pin to average out the ISP and ISN voltage. Recommended capacitor value is 10nF to 100nF. A 51.8mV offset is added to the amplifier, so when the average ISP – ISN voltage is 0V, the IMON voltage is 616mV. When the average voltage across the ISP and ISN pins is 50mV, the IMON pin will output 1.213V. Do not resistively load down this pin.

ISN, ISP (Pins 6, 7): Output Current Sense Negative and Positive Input Pins Respectively. Kelvin connect ISN and ISP pins to a sense resistor to limit the output current. The commanded NFET current will limit the voltage difference across the sense resistor to 50mV.

BIAS (Pin 8): Alternate Input Supply and PFET Bias Pin. Must be locally bypassed. The BIAS pin sets the top rail for the TG gate driver. Must connect to the converter's V_{OUT} for a positive output voltage or $INTV_{CC}$ for a converter's negative output voltage.

$INTV_{EE}$ (Pin 9): 6.18V-Below-BIAS Regulator Pin. Must be locally bypassed with a minimum capacitance of 2.2µF to BIAS. This pin sets the bottom rail for the TG gate driver. The TG gate driver can begin switching when BIAS – $INTV_{EE}$ exceeds 3.42V (typical). Connect pin to ground for an inverting converter.

TG (Pin 10): PFET Gate Drive Pin. Low and high levels are BIAS – $INTV_{EE}$ and BIAS respectively.

BG (Pin 11): NFET Gate Drive Pin. Low and high levels are GND and $INTV_{CC}$ respectively.

$INTV_{CC}$ (Pin 12): 6.3V Dual Input LDO Regulator Pin. Must be locally bypassed with a minimum capacitance of 2.2µF to GND. Logic will choose to run $INTV_{CC}$ from the V_{IN} or BIAS pins. A maximum 5mA external load can connect to the $INTV_{CC}$ pin. The undervoltage lockout on $INTV_{CC}$ is 4V (typical). The BG gate driver can begin switching when $INTV_{CC}$ exceeds 4V (typical).

V_{IN} (Pin 13): Input Supply Pin. Must be locally bypassed. Can run down to 0V as long as BIAS > 4.5V.

CSN, CSP (Pins 14, 15): NFET Current Sense Negative and Positive Input Pins Respectively. Kelvin connect these pins to a sense resistor to limit the NFET switch current. The maximum sense voltage at low duty cycle is 50mV.

EN/FBIN (Pin 16): Enable and Input Voltage Regulation Pin. In conjunction with the UVLO (undervoltage lockout) circuit, this pin is used to enable/disable the chip and restart the soft-start sequence. The EN/FBIN pin is also

PIN FUNCTIONS

used to limit the NFET current to avoid collapsing the input supply. Drive below 0.3V to disable the chip with very low quiescent current. Drive above 1.7V (typical) to activate the chip and restart the soft-start sequence. The commanded NFET current will adjust when the EN/FBIN pin voltage drops between 1.55V and 1.662V. See the Block Diagram and Applications section for more information. Do not float this pin.

MODE (Pin 17): Forced CCM Mode Pin. Drive below 1.175V (typical) to operate in forced CCM. Drive above 1.224V (typical) to operate in DCM and/or pulse-skipping mode at light loads. If SS < 1.8V (typical) or $INTV_{EE}$ is in UVLO, the part will operate in DCM at light load.

RT (Pin 18): Timing Resistor Pin. Adjusts the LT8710's switching frequency. Place a resistor from this pin to ground to set the frequency to a fixed free-running level. Do not float this pin.

SYNC (Pin 19): To synchronize the switching frequency to an outside clock, simply drive this pin with a clock. The high voltage level of the clock must exceed 1.5V, and the low level must be less than 0.4V. Drive this pin to less than 0.4V to revert to the internal free running clock. See the Applications Information section for more information.

GND (Pin 20, Exposed Pad Pin 21): Ground. Must be soldered directly to local ground plane.

BLOCK DIAGRAM

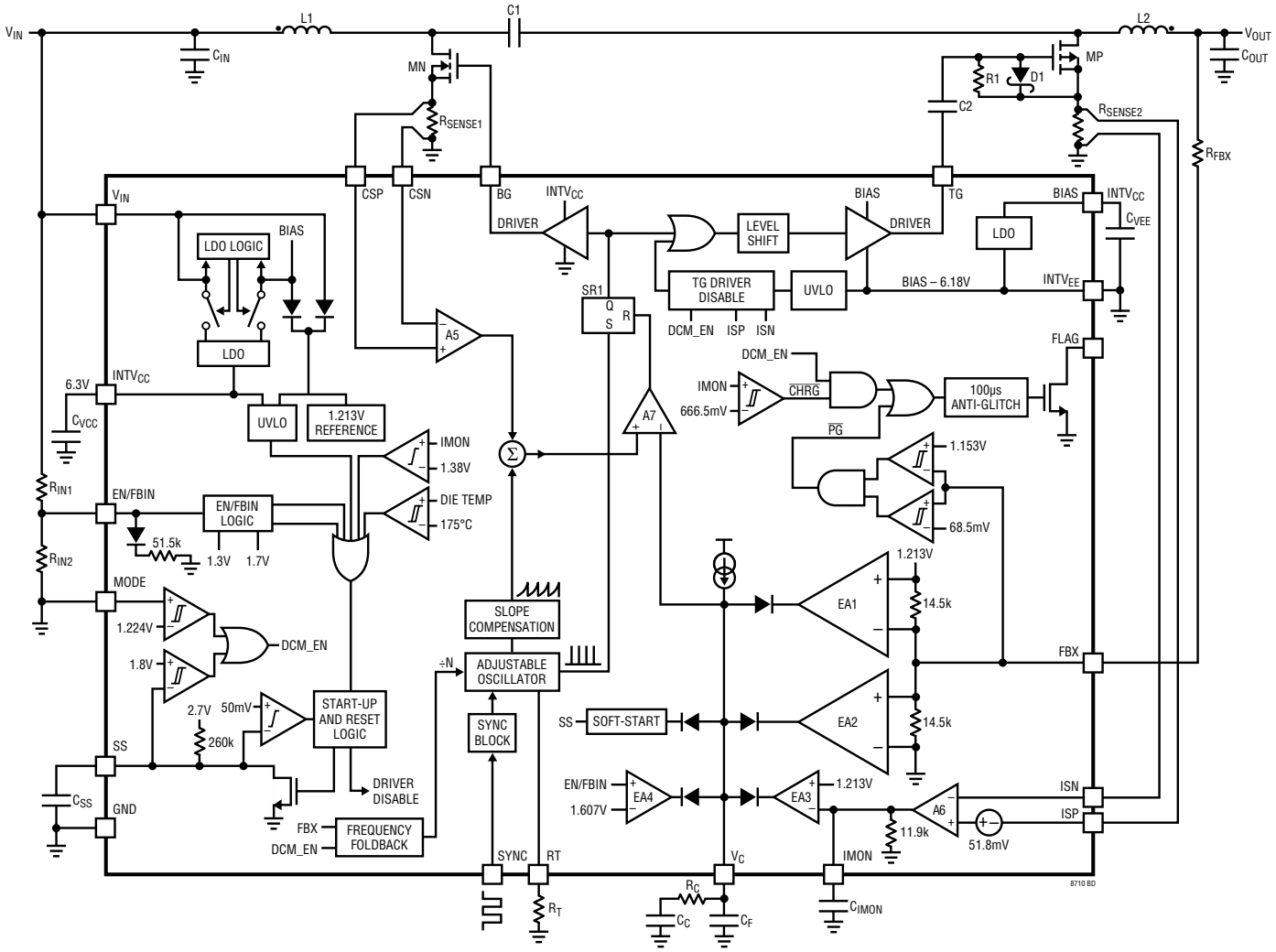


Figure 1. Block Diagram

STATE DIAGRAM

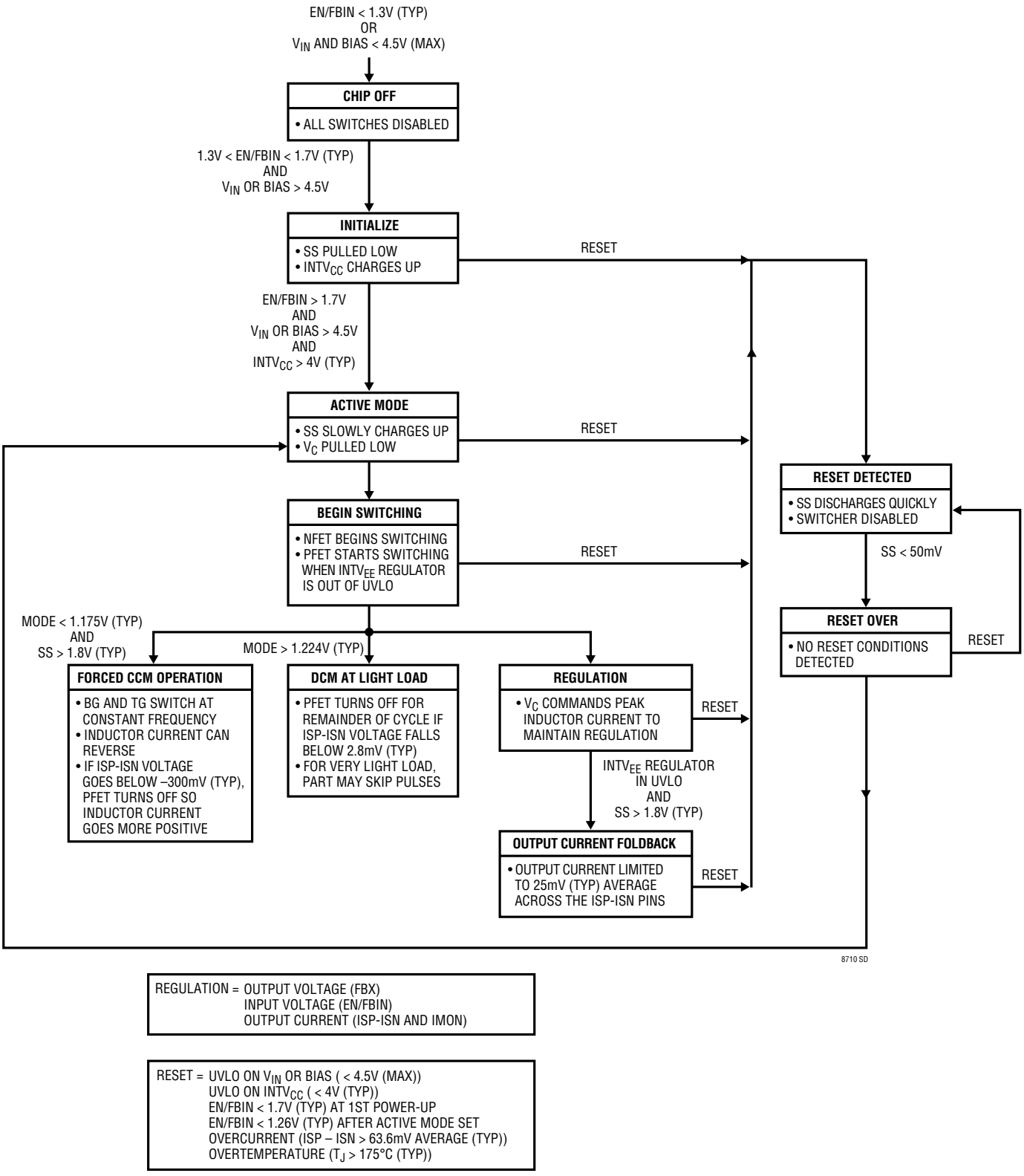


Figure 2. State Diagram

OPERATION

OPERATION – OVERVIEW

The LT8710 uses a constant frequency, current mode control scheme to provide excellent line and load regulation. The part's undervoltage lockout (UVLO) function, together with soft-start and frequency foldback, offers a controlled means of starting up. Output voltage, output current, and input voltage have control over the commanded peak current which allows a wide range of applications to be built using the LT8710. Synchronous switching makes high efficiency and high output current applications possible. When operating at light currents with the MODE pin > 1.224V (typical), the LT8710 will disable synchronous operation for part of the cycle to prevent negative switch currents. Refer to the Block Diagram (Figure 1) and the State Diagram (Figure 2) for the following description of the part's operation.

OPERATION – START-UP

Several functions are provided to enable a very clean start-up of the LT8710.

Precise Turn-On Voltages

The EN/FBIN pin has two voltage levels for activating the part; one that enables the part and allows internal rails to operate and a 2nd voltage threshold which activates a soft-start cycle and switching can begin. To enable the part, take the EN/FBIN pin above 1.3V (typical). This comparator has 44mV of hysteresis to protect against glitches and slow ramping. To activate a soft-start cycle and allow switching, take EN/FBIN above 1.7V (typical). When EN/FBIN exceeds 1.7V (typical), the logic state is latched so that if EN/FBIN drops between 1.3V to 1.7V (typical), the SS pin is not pulled low by the EN/FBIN pin. The EN/FBIN pin is also used for input voltage regulation which is at 1.607V (typical). Input voltage regulation is explained in more detail in the Operation – Regulation section. Taking the EN/FBIN pin below 0.3V shuts down the chip, resulting in extremely low quiescent current. See Figure 3 that illustrates the different EN/FBIN voltage thresholds.

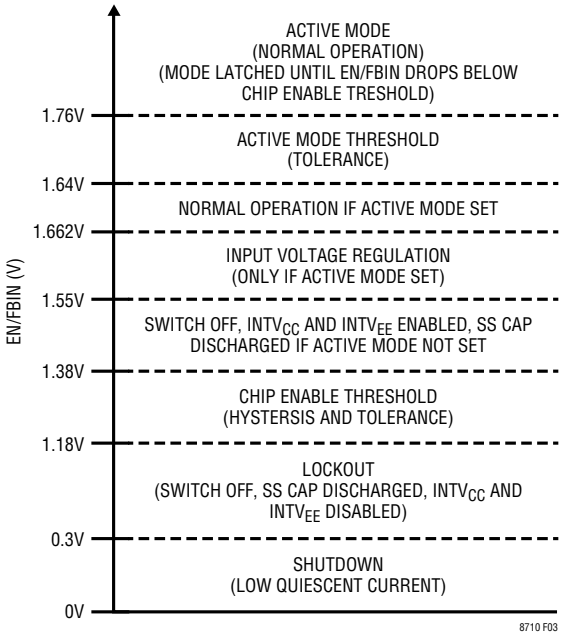


Figure 3. EN/FBIN Modes of Operation

Undervoltage Lockout (UVLO)

The LT8710 has internal UVLO circuitry that disables the chip when the greater of V_{IN} or BIAS < 4.5V (maximum) or $INTV_{CC}$ < 4V (typical). The EN/FBIN pin can also be used to create a configurable UVLO. See the Applications section for more information.

Soft-Start of Switch Current

The soft-start circuitry provides for a gradual ramp-up of the switch current (refer to *Max Current Limit vs SS* in Typical Performance Characteristics). When the part is brought out of shutdown, the external SS capacitor is first discharged which resets the states of the logic circuits in the chip. Once $INTV_{CC}$ comes out of UVLO (> 4V typical) and the chip is in active mode, an integrated 260k resistor pulls the SS pin to ~2.7V at a ramp rate set by the external capacitor connected to the pin. Typical values for the soft-start capacitor range from 100nF to 1µF. The soft-start capacitor should also be at least 5x greater than the external capacitor connected to the IMON pin to avoid start-up issues.

OPERATION

Frequency Foldback

The frequency foldback circuitry reduces the switching frequency when 175mV < FBX < 1.01V (typical). This feature lowers the minimum duty cycle that the part can achieve, thus allowing better control of the inductor current at start-up. When the FBX voltage is pulled outside of this range, the switching frequency returns to normal. If the part is configured to be in forced continuous conduction mode (MODE pin is driven below 1.175V), then the frequency foldback circuitry is disabled as long as $INTV_{EE}$ is not in UVLO and the SS pin is higher than the SS Hi threshold.

Note that the peak inductor current at start-up is a function of many variables including load profile, output capacitance, target V_{OUT}, V_{IN}, switching frequency, etc.

OPERATION – REGULATION

Use the Block Diagram when stepping through the following description of the LT8710 operating in regulation. Also, assume the converter's load current is high enough such that the part is operating in synchronous switching. The LT8710 has three modes of regulation:

1. Output Voltage (via FBX pin)
2. Input Voltage (via EN/FBIN pin)
3. Output Current (via ISP, ISN, and IMON pins)

All three of these regulation loops control the peak commanded current through the external NFET, MN. This operation is the same regardless of the regulation mode, so that will be described first.

At the start of each oscillator cycle, the SR latch (SR1) is set, which first turns off the external PFET, MP, and then turns on the external NFET, MN. The NFET's source current flows through an external current sense resistor (R_{SENSE1}) generating a voltage proportional to the NFET switch current. This voltage is then amplified by A5 and added to a stabilizing ramp. The resulting sum is fed into the positive terminal of the PWM comparator A7. When the voltage on the positive input of A7 exceeds the voltage on the negative input (V_C pin), the SR latch is reset, turning off the NFET and then turning on the PFET. The voltage on the V_C pin is controlled by one of the regulation loops, or a combination of regulation loops. For simplicity, each mode of regulation will be described independently so that only one of the modes of regulation is in command of the LT8710.

Output Voltage Regulation

A single external resistor is used to set the target output voltage. See the Pin Functions section for selecting the feedback resistor for a desired output voltage. The V_C pin voltage (negative input of A7) is set by EA1 (or EA2), which is simply an amplified difference between the FBX pin voltage and the reference voltage (1.213V if the LT8710 is configured as a noninverting converter or 9.6mV if configured as an inverting converter). In this manner, the FBX error amplifier sets the correct peak current level to maintain output voltage regulation.

Input Voltage Regulation

A single resistor or resistor divider from the EN/FBIN pin to the converter's input voltage sets the input voltage regulation. It is recommended to use a resistor divider for improved accuracy as described in the Setting the Input Voltage Regulation or Undervoltage Lockout section. The EN/FBIN pin voltage connects to the positive input of amplifier EA4. The V_C pin voltage is set by EA4, which is simply an amplified difference between the EN/FBIN pin voltage and a 1.607V reference voltage. In this manner, the EN/FBIN error amplifier sets the correct peak current level to maintain input voltage regulation.

Output Current Regulation

An external sense resistor connected between the ISP and ISN pins (R_{SENSE2}) sets the maximum output current of the converter when placed in the source of the PFET, MP. A built-in 51.8mV offset is added to the voltage seen across R_{SENSE2}. That voltage is then amplified and outputs to the IMON pin. An external capacitor must be placed from IMON to ground to filter the amplified chopped voltage that's sensed across R_{SENSE2}. The voltage at the IMON pin is fed to the negative input of the IMON error amplifier, EA3. The V_C pin voltage is set by EA3, which is simply an amplified difference between the IMON pin voltage and the 1.213V reference voltage. In this manner, the IMON error amplifier sets the correct peak current level to maintain output current regulation.

OPERATION

Note that if the $INTV_{EE}$ LDO is in UVLO and SS > 1.8V (typical), then the voltage reference at the positive input of EA3 is 916mV (typical), resulting in limiting the output current to about half of its set limit.

OPERATION – RESET CONDITIONS

The LT8710 has three reset cases. When the part is in reset, the SS pin is pulled low and both power switches, MN and MP, are forced off. Once all of the reset conditions are gone, the part is allowed to begin a soft-start sequence and switching can commence. Each of the following events can cause the LT8710 to be in reset:

1. UVLO
   a. The greater of V_{IN} and BIAS is < 4.5V (maximum)
   b. $INTV_{CC}$ < 4V (typical)
   c. EN/FBIN < 1.7V (typical) at first power-up
2. Overcurrent sensed by IMON > 1.38V (typical)
3. Die Temperature > 175°C

OPERATION – POWER SWITCH CONTROL

The main power switch is the external NFET (MN in Block Diagram) and the synchronous power switch is the external PFET (MP in Block Diagram). The two switches are never on at the same time, and there is a non-overlap time of ~140ns and ~90ns on the rising and falling edges respectively (see Electrical Characteristics) to prevent cross conduction. Figure 4 below shows the BG and TG (BIAS–TG) signals:

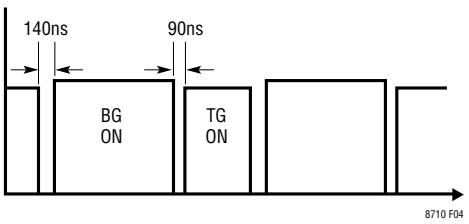


Figure 4. Synchronous Switching

Light Load Current (MODE Pin)

The MODE pin can be used to tell the LT8710 to operate in forced CCM regardless of load current, or operate in DCM at light loads.

- MODE < 1.175V (typical) = Forced CCM or FCM
- MODE > 1.224V (typical) = DCM or Pulse-Skipping

The forced continuous mode (FCM) allows the inductor current to reverse directions without any switches being forced off. At very light load currents, the inductor current will swing positive and negative as the appropriate average current is delivered to the output. There are some exceptions that negate the MODE pin and force the part to operate in DCM at light loads:

1. The $INTV_{EE}$ LDO is in UVLO (BIAS – $INTV_{EE}$ < 3.42V typical).
2. SS < 1.8V (typical).
3. The part is in a reset condition.

When the LT8710 is in discontinuous mode (DCM), synchronous switch MP is held off whenever MP's current falls near 0 current (less than 2.8mV (typical) across R_{SENSE2}). This is to prevent current draw from the output and/or feeding current to the input supply. Under very light loads, the current comparator A7, may also remain tripped for several cycles (i.e. skipping pulses). Since MP is held off during the skipped pulses, the inductor current will not reverse.

OPERATION – C/10 AND POWER GOOD (FLAG PIN)

The FLAG pin is an open-drain pin that functions as an active high C/10 and power good pin. The FLAG pin changes states 100µs (typical) after the internal comparators tell the FLAG pin to change states to reject glitches or transient events.

OPERATION

C/10 Indication

If power is good, then the FLAG pin will function as an active high C/10 indication pin. C/10 is when the charging current (output current) has dropped to 1/10 its maximum and is useful in battery charging applications. The C/10 comparator monitors the voltage at the IMON pin, and when the average ISP-ISN voltage drops below 5mV (typical), the FLAG pin pull-down device is turned off, and the FLAG pin voltage is allowed to pull high. The FLAG pin will pull low again if the average ISP-ISN voltage rises above 10mV (typical). The IMON voltage corresponding to 5mV and 10mV on ISP – ISN is 666.5mV and 727.5mV respectively.

Note that if the LT8710 is set to operate in FCM (MODE pin low), then the C/10 comparator is disabled and the FLAG pin operates only as a power good pin. See the Applications section for more information.

Power Good Indication

If C/10 is detected (average ISP-ISN < 5mV typical), then the FLAG pin functions as an active high power good (PG) pin. Power is good when the FBX voltage is greater than 95% of its regulation target, which corresponds to ~90% of the V_{OUT} regulation target (for V_{OUT} > ~8V). This corresponds to FBX > 1.153V (typical) for noninverting converters and FBX < 68.5mV (typical) for inverting converters. The PG comparators have 58mV of hysteresis to reject glitches.

OPERATION – LDO REGULATORS ($INTV_{CC}$ AND $INTV_{EE}$)

The $INTV_{CC}$ LDO regulates at 6.3V (typical) and is used as the top rail for the BG gate driver. The $INTV_{CC}$ LDO can run from V_{IN} or BIAS and will intelligently select to run from the best for minimizing power loss in the chip, but at the same time, select the proper input for maintaining $INTV_{CC}$ as close to 6.3V as possible. The $INTV_{CC}$ regulator also has safety features to limit the power dissipation in the internal pass device and also to prevent it from damage if the pin is shorted to ground. The UVLO threshold on $INTV_{CC}$ is 4V (typical), and the LT8710 will be in reset until the LDO comes out of UVLO.

The $INTV_{EE}$ regulator regulates to 6.18V (typical) below the BIAS pin voltage. The BIAS and $INTV_{EE}$ voltages are used for the top and bottom rails of the TG gate driver respectively. Just like the $INTV_{CC}$ regulator, the $INTV_{EE}$ regulator has a safety feature to limit the power dissipation in the internal pass device. The TG pin can begin switching after the $INTV_{EE}$ regulator comes out of UVLO (3.42V typical across the BIAS and $INTV_{EE}$ pins) and the part is not in a reset condition.

APPLICATIONS INFORMATION

BOOST CONVERTER COMPONENT SELECTION

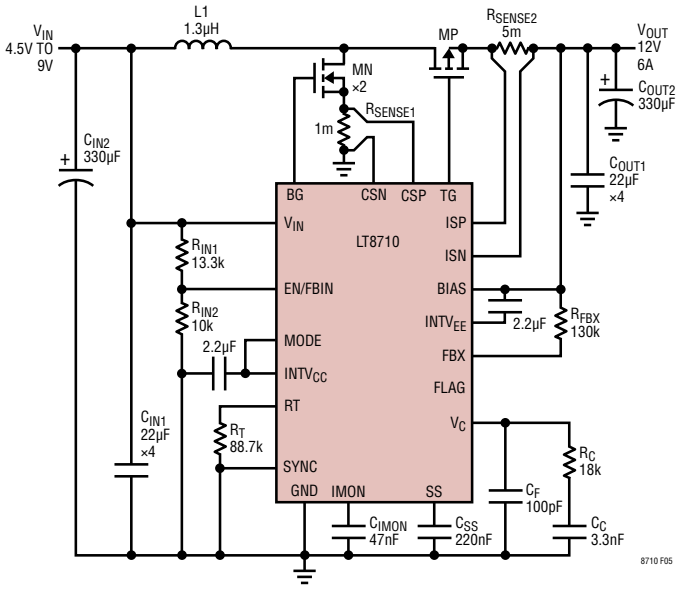


Figure 5. Boost Converter – The Component Values Given are Typical Values for a 400kHz, 4.5V to 9V to 12V/6A Boost.

The LT8710 can be configured as a boost converter as in Figure 5. This topology generates a positive output voltage where the input voltage is lower than the output voltage. A single feedback resistor sets the output voltage.

For a desired output current and output voltage over a given input voltage range, Table 1 is a step-by-step set of equations to calculate component values for the LT8710 when operating as a boost converter. Refer to more detail in this section and the Appendix for further information on the design equations presented in Table 1.

Variable Definitions:

$V_{IN(MIN)}$ = Minimum Input Voltage
$V_{IN(MAX)}$ = Maximum Input Voltage
V_{OUT} = Output Voltage
I_{OUT} = Output Current of Converter
f = Switching Frequency
DC_{MAX} = Power Switch Duty Cycle at $V_{IN(MIN)}$
V_{CSPN} = Current Limit Voltage at DC_{MAX}

Table 1. Boost Design Equations

	Parameters/Equations
Step 1: Inputs	Pick V_{IN}, V_{OUT}, I_{OUT}, and f to calculate equations below.
Step 2: DC_{MAX}	$DC_{MAX} \cong 1-\frac{V_{IN(MIN)}}{V_{OUT}}$
Step 3: V_{CSPN}	See Max Current Limit vs Duty Cycle plot in Typical Performance Characteristics to find V_{CSPN} at DC_{MAX}.
Step 4: R_{SENSE1}	$R_{SENSE1} \le 0.58 \bullet \frac{V_{CSPN}}{I_{OUT}} \bullet (1-DC_{MAX})$
Step 5: R_{SENSE2}	$R_{SENSE2} \le \frac{0.05}{1.6 \bullet I_{OUT}}$
Step 6: L	$L_{TYP} = \frac{R_{SENSE1} \bullet V_{IN(MIN)}}{12.5m \bullet f} \bullet \left(1-\frac{V_{IN(MIN)}}{V_{OUT}}\right)$ (1) $L_{MIN} = \frac{R_{SENSE1} \bullet V_{OUT}}{40m \bullet f} \bullet \left(1-\frac{V_{IN(MIN)}}{V_{OUT}-V_{IN(MIN)}}\right)$ (2) $L_{MAX1} = \frac{R_{SENSE1} \bullet V_{IN(MIN)}}{5m \bullet f} \bullet \left(1-\frac{V_{IN(MIN)}}{V_{OUT}}\right)$ (3) $L_{MAX2} = \frac{R_{SENSE1} \bullet V_{IN(MAX)}}{5m \bullet f} \bullet \left(1-\frac{V_{IN(MAX)}}{V_{OUT}}\right)$ (4) • Solve equations 1 to 4 for a range of L values. • The minimum value of the L range is the higher of L_{TYP} and L_{MIN}. The maximum of the L value range is the lower of L_{MAX1} and L_{MAX2}.
Step 7: C_{OUT}	$C_{OUT} \ge \frac{I_{OUT} \bullet DC_{MAX}}{f \bullet 0.005 \bullet V_{OUT}}$
Step 8: C_{IN}	$C_{IN} \ge \frac{DC_{MAX}}{8 \bullet L \bullet f^2 \bullet 0.005}$
Step 9: C_{IMON}	$C_{IMON} \ge \frac{100\mu \bullet DC_{MAX}}{0.005 \bullet f}$
Step 10: R_{FBX}	$R_{FBX} = \frac{V_{OUT}-1.213V}{83.7\mu A}$
Step 11: R_T	$R_T = \frac{35{,}880}{f}-1$; f in kHz and R_T in kΩ

NOTE: The final values for C_{OUT} and C_{IN} may deviate from the above equations in order to obtain desired load transient performance for a particular application. The C_{OUT} and C_{IN} equations assume zero ESR, so increase the capacitance accordingly based on the combined ESR.

APPLICATIONS INFORMATION

SEPIC CONVERTER COMPONENT SELECTION – COUPLED OR UNCOUPLED INDUCTORS

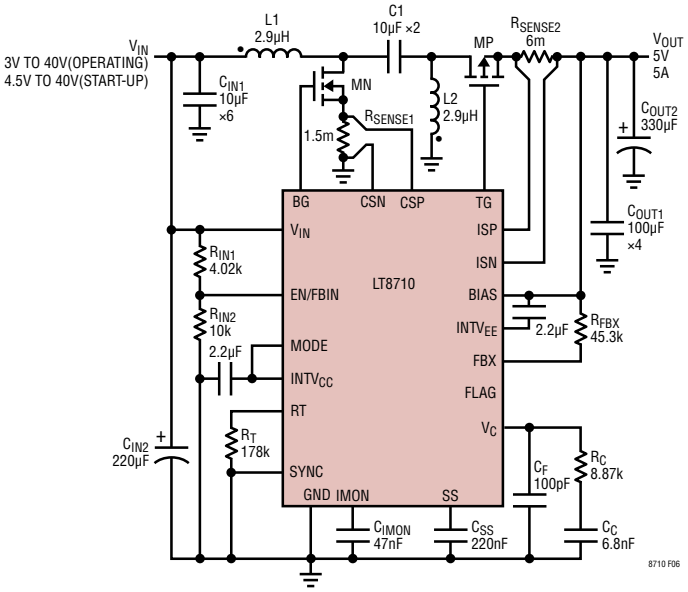


Figure 6. SEPIC Converter – The Component Values Given Are Typical Values for a 200kHz, 3V to 40V to 5V/5A SEPIC Topology Using Coupled Inductors.

The LT8710 can also be configured as a SEPIC as in Figure 6. This topology generates a positive output voltage where the input voltage can be lower, equal, or higher than the output voltage. Output disconnect is inherently built into the SEPIC topology, meaning no DC path exists between the input and output due to capacitor C1.

For a desired output current and output voltage over a given input voltage range, Table 2 is a step-by-step set of equations to calculate component values for the LT8710 when operating as a SEPIC converter. Refer to more detail in this section and the Appendix for further information on the design equations presented in Table 2.

Variable Definitions:

$V_{IN(MIN)}$ = Minimum Input Voltage
V_{OUT} = Output Voltage
I_{OUT} = Output Current of Converter
f = Switching Frequency
DC_{MAX} = Power Switch Duty Cycle at $V_{IN(MIN)}$
V_{CSPN} = Current Limit Voltage at DC_{MAX}

Table 2. SEPIC Design Equations

	Parameters/Equations
Step 1: Inputs	Pick V_{IN}, V_{OUT}, I_{OUT}, and f to calculate equations below.
Step 2: DC_{MAX}	$DC_{MAX} \cong \frac{V_{OUT}}{V_{IN(MIN)} + V_{OUT}}$
Step 3: V_{CSPN}	See Max Current Limit vs Duty Cycle plot in Typical Performance Characteristics to find V_{CSPN} at DC_{MAX}.
Step 4: R_{SENSE1}	$R_{SENSE1} \le 0.58 \bullet \frac{V_{CSPN}}{I_{OUT}} \bullet (1 - DC_{MAX})$
Step 5: R_{SENSE2}	$R_{SENSE2} \le \frac{0.05}{1.6 \bullet I_{OUT}}$
Step 6: L	$L_{TYP} = \frac{R_{SENSE1} \bullet V_{OUT}}{12.5m \bullet f} \bullet \left(\frac{V_{IN(MIN)}}{V_{IN(MIN)} + V_{OUT}}\right)$ (1) $L_{MIN} = \frac{R_{SENSE1} \bullet V_{OUT}}{40m \bullet f} \bullet \left(1 - \left(\frac{V_{IN(MIN)}}{V_{OUT}}\right)^2\right)$ (2) $L_{MAX} = \frac{R_{SENSE1} \bullet V_{OUT}}{5m \bullet f} \bullet \left(\frac{V_{IN(MIN)}}{V_{IN(MIN)} + V_{OUT}}\right)$ (3) • Solve equations 1, 2, and 3 for a range of L values. • The minimum value of the L range is the higher of L_{TYP} and L_{MIN}. The maximum of the L value range is L_{MAX}. • $L = L_1 = L_2$ for coupled inductors. • $L = L_1 \parallel L_2$ for uncoupled inductors.
Step 7: C1	$C1 \ge 10\mu F$ (TYPICAL); $V_{RATING} > V_{IN}$
Step 8: C_{OUT}	$C_{OUT} \ge \frac{I_{OUT} \bullet DC_{MAX}}{f \bullet 0.005 \bullet V_{OUT}}$
Step 9: C_{IN}	$C_{IN} \ge \frac{DC_{MAX}}{8 \bullet L \bullet f^2 \bullet 0.005}$
Step 10: C_{IMON}	$C_{IMON} \ge \frac{100\mu \bullet DC_{MAX}}{0.005 \bullet f}$
Step 11: R_{FBX}	$R_{FBX} = \frac{V_{OUT} - 1.213V}{83.7\mu A}$
Step 12: R_T	$R_T = \frac{35,880}{f} - 1$; f in kHz and R_T in kΩ

NOTE: The final values for C_{OUT} and C_{IN} may deviate from the above equations in order to obtain desired load transient performance for a particular application. The C_{OUT} and C_{IN} equations assume zero ESR, so increase the capacitance accordingly based on the combined ESR.

APPLICATIONS INFORMATION

DUAL INDUCTOR INVERTING COMPONENT SELECTION – COUPLED OR UNCOUPLED INDUCTORS

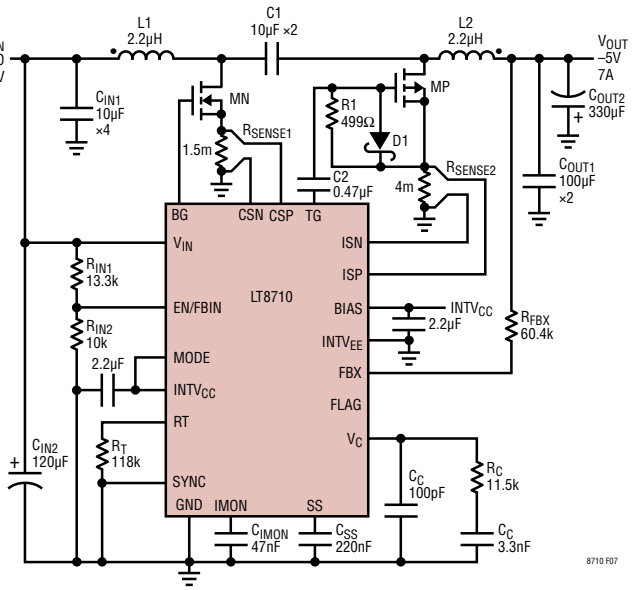


Figure 7. Dual Inductor Inverting Converter – The Component Values Given Are Typical Values for a 300kHz, 4.5V to 25V to –5V/7A Inverting Topology Using Coupled Inductors.

Due to its unique FBX pin, the LT8710 can work in a dual inductor inverting configuration as in Figure 7. Changing the connections of L2 and the PFET in the SEPIC topology, results in generating negative output voltages. This solution results in very low output voltage ripple due to inductor L2 in series with the output. Output disconnect is inherently built into this topology due to the capacitor C1.

For a desired output current and output voltage over a given input voltage range, Table 3 is a step-by-step set of equations to calculate component values for the LT8710 when operating as a dual inductor inverting converter. Refer to more detail in this section and the Appendix for further information on the design equations presented in Table 3.

Variable Definitions:

$V_{IN(MIN)}$ = Minimum Input Voltage
$V_{IN(MAX)}$ = Maximum Input Voltage
V_{OUT} = Output Voltage
I_{OUT} = Output Current of Converter
f = Switching Frequency
DC_{MAX} = Power Switch Duty Cycle at $V_{IN(MIN)}$
V_{CSPN} = Current Limit Voltage at DC_{MAX}

Table 3. Dual Inductor Inverting Design Equations

	Parameters/Equations
Step 1: Inputs	Pick V_{IN}, V_{OUT}, I_{OUT}, and f to calculate equations below.
Step 2: DC_{MAX}	$DC_{MAX} \cong \frac{\lvert V_{OUT}\rvert}{V_{IN(MIN)}+\lvert V_{OUT}\rvert}$
Step 3: V_{CSPN}	See Max Current Limit vs Duty Cycle plot in Typical Performance Characteristics to find V_{CSPN} at DC_{MAX}.
Step 4: R_{SENSE1}	$R_{SENSE1} \le 0.58 \bullet \frac{V_{CSPN}}{I_{OUT}} \bullet (1-DC_{MAX}$
Step 5: R_{SENSE2}	$R_{SENSE2} \le \frac{0.05}{1.6 \bullet I_{OUT}}$
Step 6: L	$L_{TYP} = \frac{R_{SENSE1} \bullet \lvert V_{OUT}\rvert}{12.5m \bullet f} \bullet \left(\frac{V_{IN(MIN)}}{V_{IN(MIN)}+\lvert V_{OUT}\rvert}\right)$ (1) $L_{MIN} = \frac{R_{SENSE1} \bullet \lvert V_{OUT}\rvert}{40m \bullet f} \bullet \left(1-\left(\frac{V_{IN(MIN)}}{V_{OUT}}\right)^2\right)$ (2) $L_{MAX} = \frac{R_{SENSE1} \bullet \lvert V_{OUT}\rvert}{5m \bullet f} \bullet \left(\frac{V_{IN(MIN)}}{V_{IN(MIN)}+\lvert V_{OUT}\rvert}\right)$ (3) • Solve equations 1, 2, and 3 for a range of L values. • The minimum value of the L range is the higher of L_{TYP} and L_{MIN}. The maximum of the L value range is L_{MAX}. • $L = L_1 = L_2$ for coupled inductors. • $L = L_1 \parallel L_2$ for uncoupled inductors.
Step 7: C1	$C1 \ge 10\mu F$ (TYPICAL); $V_{RATING} > V_{IN}+\lvert V_{OUT}\rvert$
Step 8: C_{OUT}	$C_{OUT} \ge \frac{1}{8 \bullet f^2 \bullet 0.005} \bullet \left(\frac{V_{IN(MAX)}}{V_{IN(MAX)}+\lvert V_{OUT}\rvert}\right)$
Step 9: C_{IN}	$C_{IN} \ge \frac{DC_{MAX}}{8 \bullet L \bullet f^2 \bullet 0.005}$
Step 10: C_{IMON}	$C_{IMON} \ge \frac{100\mu \bullet DC_{MAX}}{0.005 \bullet f}$
Step 11: R_{FBX}	$R_{FBX} = \frac{\lvert V_{OUT}\rvert + 9.6mV}{83.1\mu A}$
Step 12: R_T	$R_T = \frac{35,880}{f} - 1$; f in kHz and R_T in kΩ

NOTE: The final values for C_{OUT} and C_{IN} may deviate from the above equations in order to obtain desired load transient performance for a particular application. The C_{OUT} and C_{IN} equations assume zero ESR, so increase the capacitance accordingly based on the combined ESR.

APPLICATIONS INFORMATION

SETTING THE OUTPUT VOLTAGE REGULATION

The LT8710 output voltage is set by connecting an external resistor (R_{FBX}) from the converter's output, V_{OUT}, to the FBX pin. The equations below determines R_{FBX}:

$$R_{FBX} = \frac{V_{OUT} - 1.213V}{83.7\mu A};\ \text{Boost or SEPIC Converter}$$

$$R_{FBX} = \frac{|V_{OUT}| - 9.6mV}{83.1\mu A};\ \text{Inverting Converter}$$

See the Electrical Characteristics for tolerances on the FBX regulation voltage and current.

SETTING THE INPUT VOLTAGE REGULATION OR UNDERVOLTAGE LOCKOUT

By connecting a resistor divider between V_{IN}, EN/FBIN, and GND, the EN/FBIN pin provides a mean to regulate the input voltage or to create an undervoltage lockout function. Referring to error amplifier EA4 in the block diagram, when EN/FBIN is lower than the 1.607V reference, V_C is pulled low. For example, if V_{IN} is provided by a relatively high impedance source (e.g. a solar panel) and the current draw pulls V_{IN} below a preset limit, V_C will be reduced, thus reducing current draw from the input supply and limiting the input voltage drop. Note that using this function in forced continuous mode (MODE pin low) can result in current being drawn from the output and forced into the input. If this behavior is not desired then set the MODE pin high to prevent reverse current flow.

To set the minimum or regulated input voltage use:

$$V_{IN(MIN-REG)} = 1.607V \bullet \left(1 + \frac{R_{IN1}}{R_{IN2}}\right) + 17.6\mu A \bullet R_{IN1}$$

$$R_{IN1} = \frac{V_{IN(MIN-REG)} - 1.607V}{\left(\frac{1.607V}{R_{IN2}}\right) + 17.6\mu A}$$

where R_{IN1} and R_{IN2} are shown in Figure 8. For increased accuracy, set $R_{IN2} \leq 10k$. The resistor R_{IN2} is optional, but it is recommended to be used to increase the accuracy of the input voltage regulation by making the R_{IN1} current much higher than the EN/FBIN pin current.

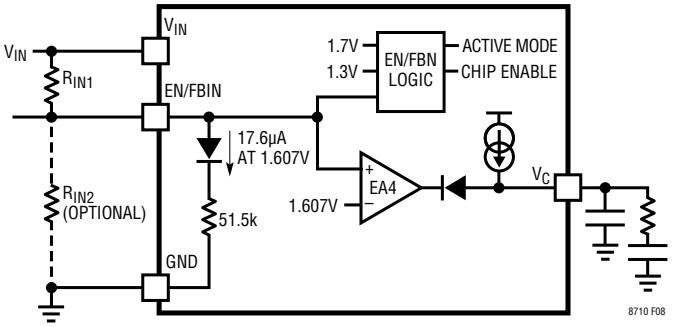


Figure 8. Configurable UVLO

This same technique can be used to create an undervoltage lockout if the LT8710 is NOT in forced continuous mode. When in discontinuous mode, forcing V_C low will stop all switching activity. Note that this does not reset the soft start function, therefore resumption of switching activity will not be accompanied by a soft-start.

Note that for very low input impedance supplies, a capacitor from EN/FBIN to ground may be needed to prevent oscillations from the input voltage regulation control loop.

At start-up, the minimum voltage on EN/FBIN must exceed 1.7V (typical) to begin a soft-start cycle. Afterwards, the EN/FBIN voltage can drop below 1.7V and the input can be regulated such that the EN/FBIN voltage is at ~1.607V. So the equation below gives the start-up V_{IN} for a desired input regulation voltage:

$$V_{IN(START-UP)} = \frac{1.7V}{1.607V} \bullet V_{IN(MIN-REG)} + 0.78\mu A \bullet R_{IN1}$$

OUTPUT CURRENT MONITORING AND LIMITING (R_{SENSE2} AND ISP-ISN AND IMON PINS)

The LT8710 has an output current monitor circuit that can be used to monitor and/or limit the output current. The current monitor circuit works as shown in Figure 9. If it is not desirable to monitor and limit the output current, simply connect the IMON pin to ground. Note that the current sense resistor connected to the ISP and ISN pins must still be used, and the value should follow the guidelines in the next couple sections.

APPLICATIONS INFORMATION

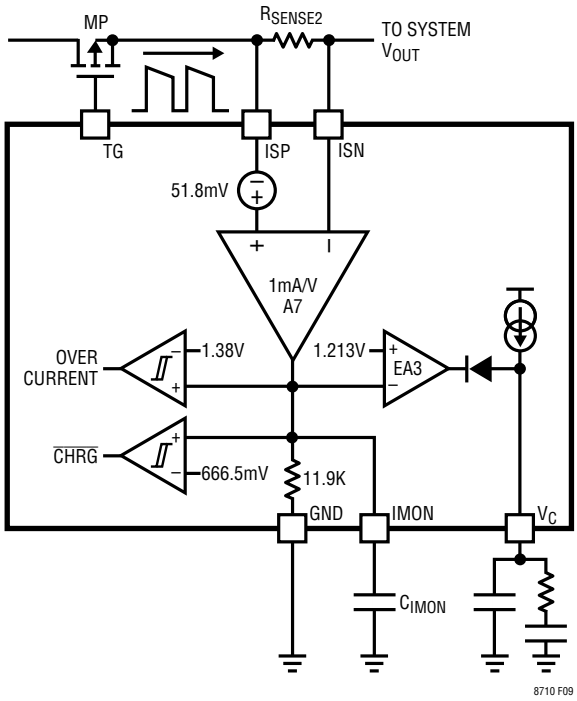


Figure 9. Output Current Monitor and Control

The current through R_{SENSE2} is sensing the current through MP which is turning on and off every clock cycle. Since the current through R_{SENSE2} is chopped, a filter capacitor connected from the IMON pin to ground is needed to filter the voltage at the IMON pin before heading to EA3. Below is the equation to calculate the required IMON pin capacitor:

$$C_{IMON} \geq \frac{100\mu A \bullet DC_{MAX}}{5mV \bullet f}$$

where DC_{MAX} is the maximum duty cycle of the converter's application (V_{IN} at the lowest of its input range) and f is the switching frequency.

To prevent start-up issues, the IMON capacitor should charge up faster than the SS capacitor. It is recommended to size the SS capacitor at least 5x greater than the IMON capacitor.

Output Current Monitoring

The voltage at the IMON pin is a gained up version of the voltage seen across the ISP and ISN pins. Below are the equations relating the R_{SENSE2} current to the IMON pin voltage. Assume the current through R_{SENSE2} is steady state and that its time average current is approximately equal to the converter's load current:

$$V_{IMON} = 11.9 \bullet (I_{RSENSE2(AVE)} \bullet R_{SENSE2} + 51.8mV)$$

$$I_{OUT} \approx I_{RSENSE2(AVE)} = \frac{\frac{V_{IMON}}{11.9} - 51.8mV}{R_{SENSE2}}$$

Output Current Limiting

As shown in Figure 9, IMON voltages exceeding 1.213V (typical) causes the V_C voltage to reduce, thus limiting the inductor current. This voltage on IMON corresponds to an average voltage of 50mV across R_{SENSE2}. Below is the equation for selecting the R_{SENSE2} resistor for limiting the output current at steady state:

$$R_{SENSE2} = \frac{50mV}{I_{OUT(LIMIT)}}$$

If it is not desirable to limit the output current, size R_{SENSE2} by setting $I_{OUT(LIMIT)}$ at least 60% higher than the maximum output current of the converter. This current sense resistor is needed if using the synchronous PFET in the converter. If the PFET is replaced with a Schottky, then R_{SENSE2} is not needed if output current limiting or monitoring isn't required.

Note that if the $INTV_{EE}$ LDO is in UVLO and SS > 1.8V (typical), then the reference voltage at EA3 reduces to 916mV, and the output current is limited to about half its set point.

Output Overcurrent

As shown in Figure 9, a comparator monitors the voltage at the IMON pin and triggers a reset condition if the IMON pin voltage exceeds 1.38V (typical). This corresponds to an average voltage of 63.6mV (typical) across the ISP and ISN pins:

$$I_{OUT(OVERCURRENT)} = \frac{63.6mV}{R_{SENSE2}}$$

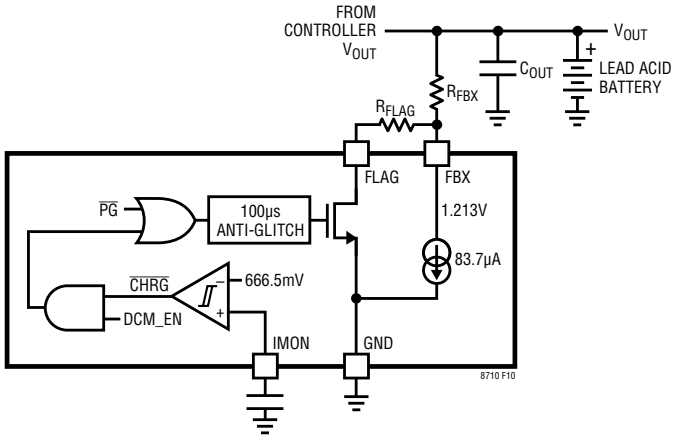
$$I_{OUT(OVERCURRENT)} = 1.27 \bullet I_{OUT(LIMIT)}$$

APPLICATIONS INFORMATION

Battery Charging and C/10

A useful application for limiting the output current is to charge a battery. When charging a battery such as a 12V lead acid battery, it may be useful to charge to a bulk and float voltage, in which case, the C/10 function of the FLAG pin can be used. For decreasing charge currents, C/10 is detected when the IMON voltage falls below 666.5mV (typical) and corresponds to an average ISP – ISN voltage of 5mV (typical). For increasing charge currents, C/10 is cleared when IMON gets above 727.5mV (typical) which corresponds to an average ISP – ISN voltage of 10mV (typical).

To set a bulk and float battery voltage, simply connect a resistor from the FLAG pin to the FBX pin. When the battery charging current is high (C/10 not detected), the target output voltage is the bulk battery voltage as set by the resistor connected between the FLAG and FBX pins. Once the charging current drops such that C/10 is detected, the target output voltage drops to the float battery voltage as set by the external FBX resistor. See Figure 10 below on the FLAG pin connections and equations for setting the bulk and float battery voltages. **Note that in order to use the C/10 feature, the MODE pin must be high to operate in DCM at light loads.**



$$R_{FBX} = \frac{V_{OUT(FLOAT)} - 1.213V}{83.7\mu A}$$

$$R_{FLAG} = R_{FBX} \bullet \frac{1.213V}{V_{OUT(BULK)} - V_{OUT(FLOAT)}}$$

Figure 10. FLAG Pin Connections and Equations for Battery Charging

Capacitor Charging

When the application is to charge a bank of capacitors such as SuperCaps, the charging current is set by R_{SENSE2} and the FLAG pin isn't necessarily needed as in the case of charging a battery.

Temperature Dependent Output Voltage Using NTC Resistor

It may be desirable to regulate the converter's output based on the ambient temperature. The $INTV_{CC}$ LDO regulated voltage is 6.3V ± 1.6% (see Electrical Characteristics), and a negative temperature coefficient (NTC) resistor can be used to sum into the FBX pin to create an output voltage that decreases with temperature. See Figure 11 for the necessary connections.

The FBX voltages regulates to 1.213V (typical) for positive output voltages. For an accurate room temperature output voltage, size the resistor divider off the $INTV_{CC}$ pin to give 1.213V such that the current through R2 is ~0 at room temperature. Choose $R_{NTC(25)} \le 10k\Omega$ and use the equations below to calculate R_1, R_{FBX}, and V_{OUT} at room temperature and R_2 for a desired V_{OUT} change over temperature.

$$R_1 = R_{NTC(25)} \frac{6.3 - 1.213V}{1.213V}$$

$$V_{OUT(25)} \cong 1.213V + 83.7\mu A \bullet R_{FBX} + \frac{R_{FBX}}{R_2} \bullet \left(1.213V - 6.3V \bullet \frac{R_1}{R_1 + R_{NTC(25)}}\right)$$

$$R_{NTC} = R_{NTC(25)} \bullet e^{\beta \bullet \left(\frac{1}{T} - \frac{1}{T_{25}}\right)}$$

$$\Delta V_{OUT} = -6.3V \bullet \frac{R_{FBX}}{R_2} \bullet R_1 \bullet \left(\frac{1}{R_1 + R_{NTC(T(MAX))}} - \frac{1}{R_1 + R_{NTC(T(MIN))}}\right)$$

$$R_2 = \frac{-6.3V}{\Delta V_{OUT}} \bullet R_{FBX} \bullet R_1 \bullet \left(\frac{1}{R_1 + R_{NTC(T(MAX))}} - \frac{1}{R_1 + R_{NTC(T(MIN))}}\right)$$

APPLICATIONS INFORMATION

where:

$R_{NTC(25)}$ = Resistance of the NTC resistor at 25°C

β = Material-specific constant of NTC resistor. Specified at two temperatures such as $\beta_{25/85}$. If more than two βs are specified, use the most appropriate for the application.

T = Absolute temperature in Kelvin

T_{25} = Room temperature in Kelvin (298.15k)

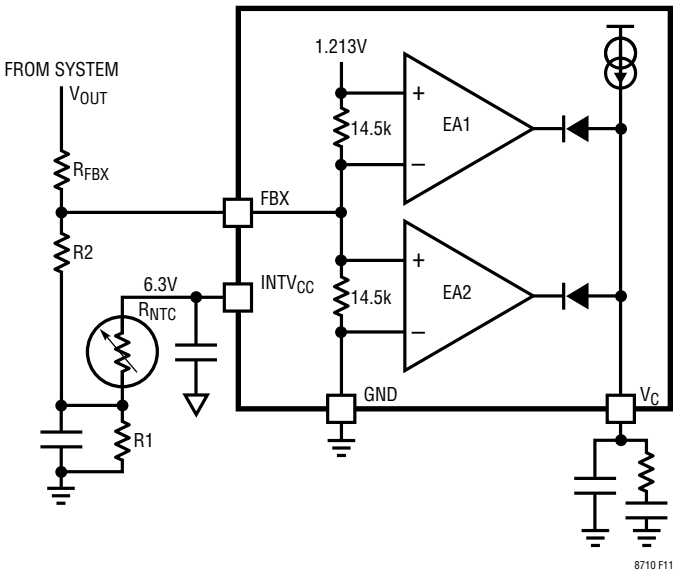


Figure 11. Temperature Dependent Output Using an NTC Resistor Divider

SWITCH CURRENT LIMIT (R_{SENSE1} AND CSP-CSN PINS)

The external current sense resistor (R_{SENSE1}) sets the maximum peak current though the external NFET switch (MN). The maximum voltage across R_{SENSE1} is 50mV (typical) at very low switch duty cycles, and then slope compensation decreases the current limit as the duty cycle increases (see the *Max Current Limit vs Duty Cycle (CSP-CSN)* plot in the Typical Performance Characteristics). The equation below gives the switch current limit for a given duty cycle and current sense resistor (find V_{CSPN} at the operating duty cycle in the plot mentioned).

$$I_{SW(LIMIT)} = \frac{V_{CSPN}}{R_{SENSE1}}$$

To provide a desired load current for any given application, R_{SENSE1} must be sized appropriately. The switch current will be at its highest when the input voltage is at the lowest of its range. The equation below calculates R_{SENSE1} for a desired output current:

$$R_{SENSE1} \le 0.74 \bullet \eta \bullet \frac{V_{CSPN}}{I_{OUT}} \bullet (1 - DC_{MAX}) \bullet \left(1 - \frac{i_{RIPPLE}}{2}\right)$$

where

η = Converter efficiency (assume ~90%)

V_{CSPN} = Max current limit voltage (see *Max Current Limit vs Duty Cycle (CSP-CSN)* plot in the Typical Performance Characteristics)

I_{OUT} = Converter load current

DC_{MAX} = Switching duty cycle at minimum V_{IN} (see Power Switch Duty Cycle in Appendix)

i_{RIPPLE} = Peak-to-peak inductor ripple current percentage at minimum V_{IN} (recommended to use 25%)

REVERSE CURRENT APPLICATIONS (MODE PIN LOW)

When the forced continuous mode is selected (MODE pin low), inductor current is allowed to reverse directions and flow from the V_{OUT} side to the V_{IN} side. This can lead to current sinking from the output and being forced into the input. The reverse current is at a maximum magnitude when V_C is lowest. The graph of *Max Current Limit vs Duty Cycle (CSP – CSN)* in the Typical Performance Characteristics section can help to determine the maximum reverse current capability.

The IMON pin voltage will indicate negative inductor currents. Refer to the equation for IMON in the Pin Functions. Note that the IMON voltage is only accurate if the dynamic voltage across R_{SENSE2} stays within –51.8mV to 500mV. If the valley inductor current goes more negative than –300mV as sensed by R_{SENSE2}, the external PFET will turn off, and the inductor current will start going more positive.

APPLICATIONS INFORMATION

Backup Power

With the use of reverse current control and input voltage regulation, the LT8710 can be used as a backup power converter as shown in Figure 12 below. With the MODE pin low to operate in FCM, when the input source is removed, the output can supply current into the input and keep the input regulated for some amount of time. The amount of time depends on the output capacitance and the load current at the input.

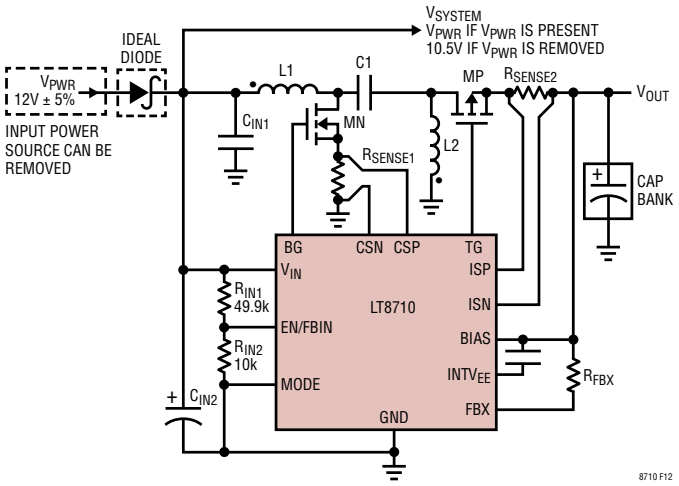


Figure 12. Backup Power Converter

Once V_{OUT} drops low enough to put the $INTV_{EE}$ LDO in UVLO (V_{OUT} at ~4.25V), the PFET will stop switching and the current will stop flowing from V_{OUT} to V_{SYSTEM}. For this type of application, it is recommended to use a PFET that is in the linear mode of operation with only 4V of gate drive.

Input Overvoltage Protection

Whenever the MODE pin is low to allow current to flow from output to input, it is strongly recommended to add a couple external components to protect the input from overvoltage as shown in Figure 13 below. With either approach, as V_{IN} approaches the OVP point, the MODE pin approaches the MODE FCM threshold (1.224V typical) and the LT8710 won't allow reverse current flow, preventing V_{IN} to go above the OVP point.

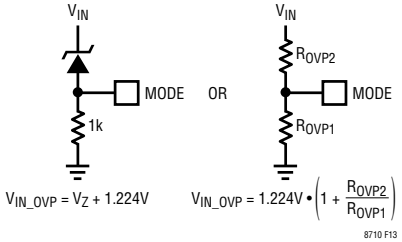


Figure 13. Input Overvoltage Protection

CURRENT SENSE FILTERING

Certain applications may require filtering of the inductor current sense signals due to excessive switching noise that can appear across R_{SENSE1} and/or R_{SENSE2}. Higher operating voltages, higher values of R_{SENSE}, and more capacitive MOSFETs will all contribute additional noise across R_{SENSE} when MOSFETs transition. The CSP/CSN and/or the ISP/ISN sense signals can be filtered by adding one of the RC networks shown in Figure 14. The filter shown in Figure 14a filters out differential noise, whereas the filter in Figure 14b filters out the differential and common mode noise at the expense of an additional capacitor and approximately twice the capacitance value. It is recommended to Kelvin the ground connection directly to the paddle of the LT8710 if using the filter in Figure 14b. The filter network should be placed as close as possible to the LT8710. Resistors greater than 10Ω should be avoided as this can increase the offset voltages at the CSP/CSN and ISP/ISN pins.

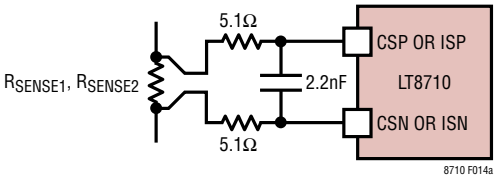


Figure 14a. Differential RC Filter on CSP/CSN and/or ISP/ISN Pins

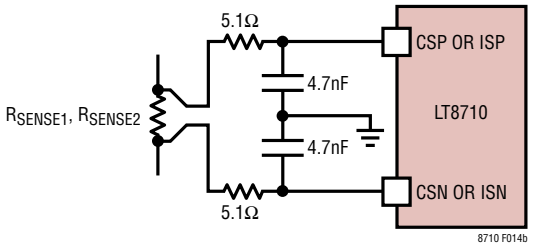


Figure 14b. Differential and Common Mode RC Filter on CSP/CSN and/or ISP/ISN Pins

APPLICATIONS INFORMATION

The RC product should be kept less than 30ns, which is simply the total series R (5.1Ω+5.1Ω in this case) times the equivalent capacitance seen across the sense pins (2.2nF for Figure 14a and 2.35nF for Figure 14b).

SWITCHING FREQUENCY

The LT8710 uses a constant frequency architecture between 100kHz and 750kHz. The frequency can be set using the internal oscillator or can be synchronized to an external clock source. Selection of the switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. For high power applications, consider operating at lower frequencies to minimize MOSFET heating from switching losses. The switching frequency can be set by placing an appropriate resistor from the RT pin to ground and tying the SYNC pin low. The frequency can also be synchronized to an external clock source driven into the SYNC pin. The following sections provide more details.

Oscillator Timing Resistor (R_T)

The operating frequency of the LT8710 can be set by the internal free-running oscillator. When the SYNC pin is driven low (< 0.4V), the frequency of operation is set by a resistor from the RT pin to ground. The oscillator frequency is calculated using the following formula:

$$f = \frac{35,880}{(R_T + 1)}$$

where f is in kHz and R_T is in k. Conversely, R_T (in k) can be calculated from the desired frequency (in kHz) using:

$$R_T = \frac{35,880}{f} - 1$$

Clock Synchronization

An external source can set the operating frequency of the LT8710 by providing a digital clock signal into the SYNC pin (R_T resistor still required). The LT8710 will operate at the SYNC clock frequency. The LT8710 will revert to its internal free-running oscillator clock when the SYNC pin is driven below 0.4V for a few free-running clock periods.

Driving SYNC high for an extended period of time effectively stops the operating clock and prevents latch SR1 from becoming set (see Block Diagram). As a result, the switching operation of the LT8710 will stop.

The duty cycle of the SYNC signal must be between 20% and 80% for proper operation. Also, the frequency of the SYNC signal must meet the following two criteria:

1. SYNC may not toggle outside the frequency range of 100kHz to 750kHz unless it is stopped below 0.4V to enable the free-running oscillator.
2. The SYNC frequency can always be higher than the free-running oscillator frequency (as set by the R_T resistor), f_{OSC}, but should not be less than 25% below f_{OSC}.

After SYNC begins toggling, it is recommended that switching activity is stopped before the SYNC pin stops toggling. Excess negative inductor current can result when SYNC stops toggling as the LT8710 transitions from the external SYNC clock source to the internal free-running oscillator clock. Switching activity can be stopped by driving the EN/FBIN pin low.

LDO REGULATORS

The LT8710 has two linear regulators to run the BG and TG gate drivers. The $INTV_{CC}$ LDO regulates 6.3V (typical) above ground, and the $INTV_{EE}$ regulator regulates 6.18V (typical) below the BIAS pin.

$INTV_{CC}$ LDO Regulator

The $INTV_{CC}$ LDO is used as the top rail for the BG gate driver for positive output converters. In the case of a negative output converter, the $INTV_{CC}$ LDO is used as the top rail for both the BG and TG gate drivers (BIAS and $INTV_{EE}$ must tie to $INTV_{CC}$ and GND respectively). An external capacitor greater than 2.2µF must be placed from the $INTV_{CC}$ pin to ground. The UVLO threshold on $INTV_{CC}$ is 4V (typical), and the LT8710 will be in reset until the LDO comes out of UVLO.

The $INTV_{CC}$ LDO can run off V_{IN} or BIAS and will intelligently select to run off the best for minimizing chip power loss, but at the same time, select the proper input for maintaining $INTV_{CC}$ as close to 6.3V as possible. For

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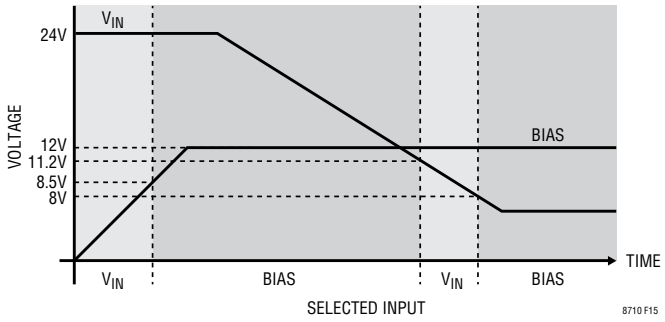

Figure 15. $INTV_{CC}$ Input Voltage Selection

example, Figure 15 is a plot that shows an application where V_{OUT}/BIAS is regulated to 12V and V_{IN} starts at 24V and ramps down to 5V and indicates that $INTV_{CC}$ is regulating from V_{IN} or BIAS.

Overcurrent protection circuitry typically limits the maximum current draw from the LDO to ~125mA and ~65mA when running from V_{IN} and BIAS respectively. When $INTV_{CC}$ is below ~3.5V during start-up or an overload condition, the typical current limit is reduced to ~25mA when running from either V_{IN} or BIAS. If the selected input voltage is greater than 20V (typical), then the current limit of the LDO reduces linearly with input voltage to limit the maximum power in the $INTV_{CC}$ pass device. See the *$INTV_{CC}$ Current Limit vs V_{IN} or BIAS* plot in the Typical Performance Characteristics. If the die temperature exceeds 175°C (typical), the current limit of the LDO drops to 0.

Power dissipated in the $INTV_{CC}$ LDO should be minimized to improve efficiency and prevent overheating of the LT8710. The current limit reduction with input voltage circuit helps prevent the part from overheating, but these guidelines should be followed. The maximum current drawn through the $INTV_{CC}$ LDO occurs under the following conditions:

1. Large (capacitive) MOSFETs being driven at high frequencies.
2. The converter's switch voltage (V_{OUT} for boost or V_{IN} + $|V_{OUT}|$ for dual inductor converters) is high, thus requiring more charge to turn the MOSFET gates on and off.

In general, use appropriately sized MOSFETs and lower the switching frequency for higher voltage applications to keep the $INTV_{CC}$ current at a minimum.

$INTV_{EE}$ LDO Regulator

The BIAS and $INTV_{EE}$ voltages are used for the top and bottom rails of the TG gate driver respectively. An external capacitor greater than 2.2µF must be placed between the BIAS and $INTV_{EE}$ pins. The UVLO threshold on the regulator (BIAS-$INTV_{EE}$) is 3.42V (typical) as long as the BIAS voltage is greater than ~3.36V. The TG pin can begin switching after the $INTV_{EE}$ regulator comes out of UVLO. For positive output converters, BIAS must be tied to the converter's output voltage. For negative output converters, BIAS must connect to the $INTV_{CC}$ pin and the $INTV_{EE}$ pin ties to ground. In this manner, the voltage of the $INTV_{EE}$ regulator is driven to the $INTV_{CC}$ voltage of 6.3V and hence the TG gate driver will have levels of 0V and 6.3V.

Overcurrent protection circuitry typically limits the maximum current draw from the regulator to ~70mA. If the BIAS voltage is greater than 20V (typical), then the current limit of the regulator reduces linearly with input voltage to limit the maximum power in the $INTV_{EE}$ pass device. See the *$INTV_{EE}$ Current Limit vs BIAS* plot in the Typical Performance Characteristics.

The same thermal guidelines from the $INTV_{CC}$ LDO Regulator section apply to the $INTV_{EE}$ regulator as well.

NON-SYNCHRONOUS CONVERTER

It may be desirable in some applications to replace the external PFET with a Schottky diode to make a non-synchronous converter. One example would be a high output voltage application because the voltage drop across the rectifier has a small affect on the efficiency of the converter. In fact, for high output voltage applications, replacing the PFET with a Schottky may result in higher efficiency because the LT8710 doesn't have to supply gate drive to the PFET. Figure 16 shows the recommended connections for using the LT8710 as a non-synchronous boost converter, however the same concept can be used for any other converter.

Note that the MODE pin must be tied high if using the LT8710 as a non-synchronous converter or else the output might not be regulated at light load. Also, the TG pin

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must be left floating or permanent damage could occur to the TG gate driver. The schematic of Figure 16 could be modified if needed. If it is not desirable to monitor and/or control the output current, R_{SENSE2} is not needed and simply tie the ISP and ISN pins to $INTV_{CC}$. The IMON pin can be left floating or can connect to ground. The BIAS and $INTV_{EE}$ pins can tie to ground if the dual input feature of the $INTV_{CC}$ LDO is not needed and V_{IN} stays above 4.5V.

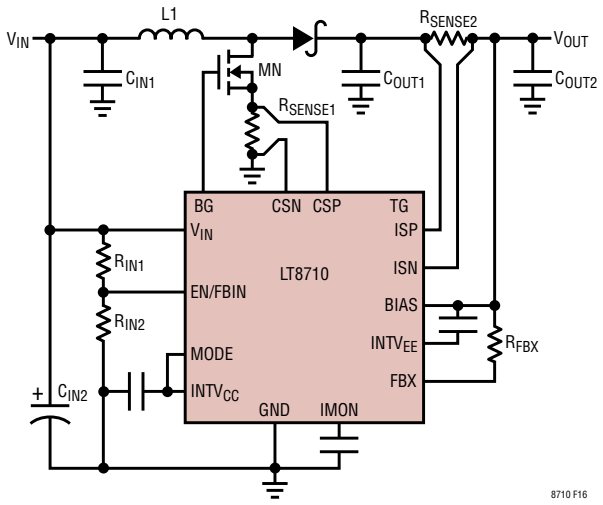

Figure 16. Simplified Schematic of a Non-Synchronous Boost Converter

LAYOUT GUIDELINES FOR BOOST, SEPIC, AND DUAL INDUCTOR INVERTING TOPOLOGIES

General Layout Guidelines

- To optimize thermal performance, solder the exposed pad of the LT8710 to the ground plane with multiple vias around the pad connecting to additional ground planes.
- High speed switching path (see specific topology below for more information) must be kept as short as possible.
- The FBX, V_C, IMON, and RT components should be placed as close to the LT8710 as possible, while being far away as practically possible from switching nodes. The ground for these components should be separated from the switch current path.
- Place bypass capacitors for the V_{IN} and BIAS pins (1µF or greater) as close as possible to the LT8710.
- Place bypass capacitors for the $INTV_{CC}$ and $INTV_{EE}$ (between BIAS and $INTV_{EE}$) pins (2.2µF or greater) as close as possible to the LT8710.
- The load should connect directly to the positive and negative terminals of the output capacitor for best load regulation.

Boost Topology Specific Layout Guidelines

- Keep length of loop (high speed switching path) governing R_{SENSE1}, MN, MP, R_{SENSE2}, C_{OUT}, and ground return as short as possible to minimize parasitic inductive spikes at the switch node during switching.

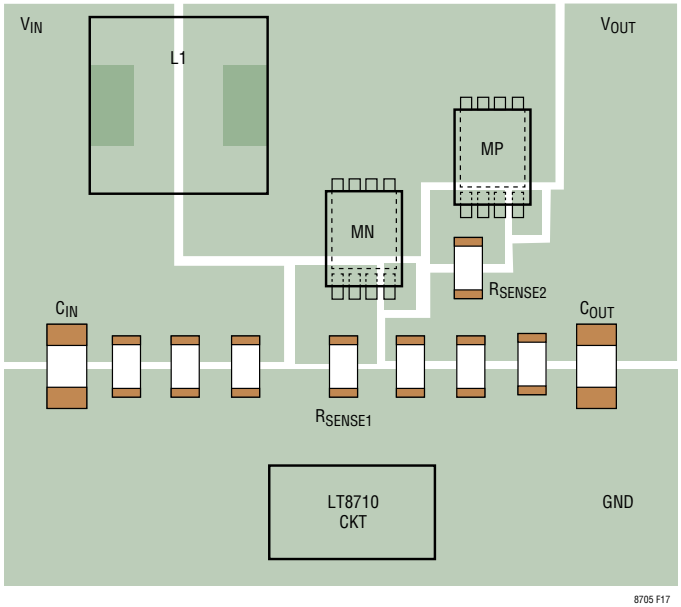

Figure 17. Suggested Component Placement for Boost Topology

SEPIC Topology Specific Layout Guidelines

- Keep length of loop (high speed switching path) governing R_{SENSE1}, MN, C1, MP, R_{SENSE2}, C_{OUT}, and ground return as short as possible to minimize parasitic inductive spikes at the switch node during switching.

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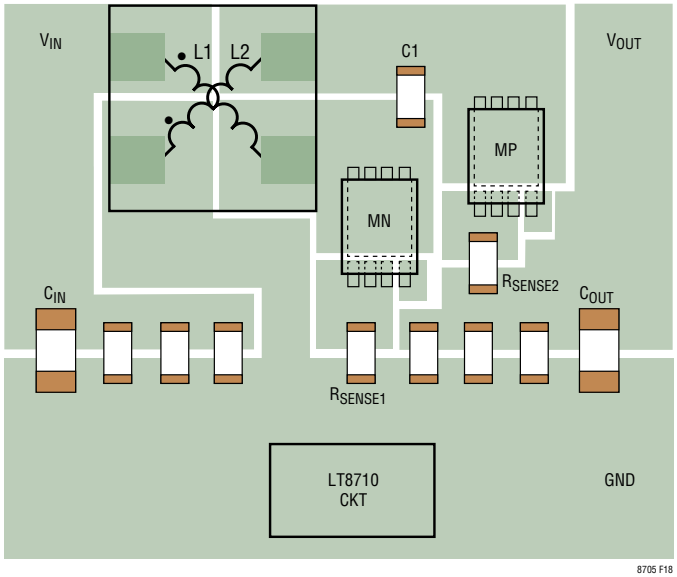

Figure 18. Suggested Component Placement for SEPIC Topology

Dual Inductor Inverting Topology Specific Layout Guidelines

- Keep ground return path from the low side of R_{SENSE1} and R_{SENSE2} (to chip) separated from C_{IN}'s and C_{OUT}'s ground return path (to chip) in order to minimize switching noise coupling into the input and output. Notice the cuts in the ground return for the low side of R_{SENSE1} and R_{SENSE2}.
- Keep length of loop (high speed switching path) governing R_{SENSE1}, MN, C1, MP, R_{SENSE2}, and ground return as short as possible to minimize parasitic inductive spikes at the switch node during switching.

Current Sense Resistor Layout Guidelines

- Route the CSP/CSN and ISP/ISN lines differentially (close together) from the chip to the current sense resistor as shown in Figure 20.
- Place the vias that connect the CSP/CSN and ISP/ISN lines directly at the terminals of the current sense resistor as shown in Figure 20.

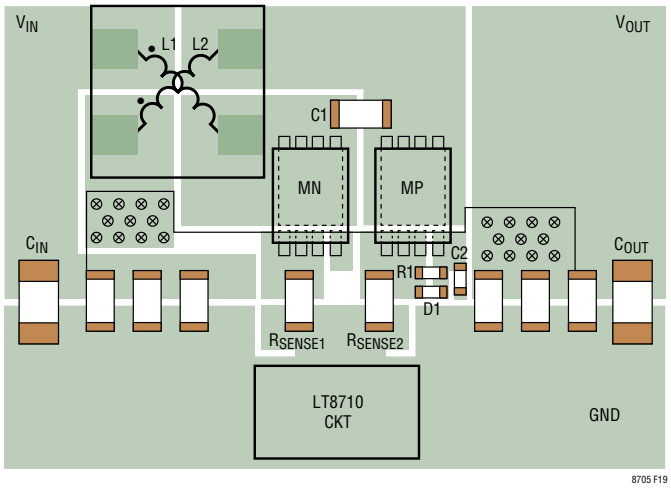

Figure 19. Suggested Component Placement for Dual Inductor Inverting Topology

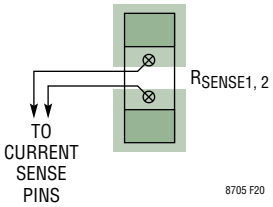

Figure 20. Suggested Routing and Connections of CSP/CSN and ISP/ISN Lines

THERMAL CONSIDERATIONS

Overview

The primary components on the board that consume the most power and produce the most heat are the power switches, MN and MP, the power inductor, and the LT8710 IC. It is imperative that a good thermal path be provided for these components to dissipate the heat generated within the packages. This can be accomplished by taking advantage of the thermal pads on the underside of the packages. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from each of these components and into a copper plane with as much area as possible. For the case of the power switches, the copper area of the drain connections shouldn't be too big as to create a large EMI surface that can radiate noise around the board.

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Power MOSFET Loss and Thermal Calculations

The LT8710 requires two external power MOSFETs, an NFET switch for the BG gate driver and a PFET switch for the TG gate driver. Important parameters for estimating the power dissipation in the MOSFETs are:

1. On-resistance (R_{DSON})
2. Gate-to-drain charge (Q_{GD})
3. PFET body diode forward voltage (V_{BD})
4. V_{DS} of the FETs during their Off-Time
5. Switch current (I_{SW})
6. Switching frequency (f)

The power loss in each power switch has a DC and AC term. The DC term is when the power switch is fully on, and the AC term is when the power switch is transitioning from on-off or off-on.

The following applies for both the NFET and PFET power switches. For a boost application, the average current through the MOSFET (I_{SW}) during its on-time, is the same as the average input current. The magnitude of the drain-to-source voltage, V_{DS}, during its off-time is approximately V_{OUT}. For a SEPIC or dual inductor inverting application, the average current through each MOSFET (I_{SW}) during its on-time, is the sum of the average input current and the output current. The $|V_{DS}|$ voltage during the off-time is approximately $V_{IN} + |V_{OUT}|$. During the non-overlap time of the gate drivers, the peak and valley inductor current is flowing through the body diode of the PFET. Below are the equations for the power loss in MN and MP.

$$P_{MOSFET} = P_{I^2R} + P_{SWITCHING}$$

$$P_{MN} = I_N{}^2 \bullet R_{DSON} + V_{DS} \bullet I_N \bullet f \bullet t_{RF} + P_{RR-N}$$

$$P_{MP} = I_P{}^2 \bullet R_{DSON} + V_{BD} \bullet \left(I_{PK} + \frac{I_{VY}}{1.6}\right) \bullet f \bullet 140ns + P_{RR-P}$$

$$I_{SW} = \frac{I_{OUT}}{(1-DC)};\quad I_{PK} = I_{SW} + \frac{i_{RIPPLE}}{2};\quad I_{VY} = I_{SW} - \frac{i_{RIPPLE}}{2}$$

$$I_N = \sqrt{DC \bullet \left(I_{SW}{}^2 + \frac{i_{RIPPLE}{}^2}{12}\right)}$$

$$I_P = \sqrt{(1-DC) \bullet \left(I_{SW}{}^2 + \frac{i_{RIPPLE}{}^2}{12}\right)}$$

$$P_{RR-N} \approx \frac{V_{DS} \bullet I_{RR} \bullet t_{RR} \bullet f}{2}$$

$$P_{RR-P} \approx \frac{V_{DS} \bullet I_{RR} \bullet t_{RR} \bullet f}{2}$$

where:

- f = Switching Frequency
- I_N = NFET RMS Current
- I_P = PFET RMS Current
- t_{RF} = Average of the rise and fall times of the NFET's drain voltage
- I_{SW} = Average switch current during its on-time
- I_{PK} = Peak inductor current
- I_{VY} = Valley inductor current
- i_{RIPPLE} = Inductor ripple current
- DC = Switch duty cycle (see Power Switch Duty Cycle section in Appendix)
- V_{BD} = PFET body diode forward voltage at I_{SW}
- V_{DS} = Voltage across the FET when it's off. V_{OUT} for a boost, V_{IN} + $|V_{OUT}|$ for a dual inductor inverting or SEPIC converter
- P_{RR-N} = PFET body diode reverse recovery power loss in the NFET
- P_{RR-P} = PFET body diode reverse recovery power loss in the PFET

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I_{RR} = Current needed to remove the PFET body diode charge

t_{RR} = Reverse recovery time of PFET body diode

Typical values for t_{RF} are 10ns to 40ns depending on the MOSFET capacitance and drain voltage. In general, the lower the Q_{GD} of the MOSFET, the faster the rise and fall times of its drain voltage. For best calculations, measure the rise and fall times in the application.

PFET body diode reverse recovery power loss is dependent on many factors and can be difficult to quantify in an application. In general, this power loss increases with higher V_{DS} and/or higher switching frequency.

Chip Power and Thermal Calculations

Power dissipation in the LT8710 chip comes from three primary sources: $INTV_{CC}$ and $INTV_{EE}$ LDOs providing gate drive to the BG and TG pins and additional input quiescent current. The average current through each LDO is determined by the gate charge of the power switches, MN and MP, and the switching frequency. Below are the equations for calculating the chip power loss followed by examples.

Noninverting Converter: The $INTV_{CC}$ LDO primarily supplies voltage for the BG gate driver. The BIAS and $INTV_{EE}$ voltages supply the top and bottom rails of the TG gate driver respectively. The chip Q current comes from the higher of V_{IN} and BIAS. Below are the chip power equations for a noninverting converter:

$P_{VCC} = 1.04 \bullet Q_{MN} \bullet f \bullet V_{SELECT}$
$P_{VEE1} = Q_{MP} \bullet f \bullet V_{BIAS}$
$P_{VEE2} = 3.1mA \bullet (1 – DC) \bullet V_{BIAS}$
$P_Q = 4mA \bullet V_{MAX}$

where:

f = Switching frequency

DC = Switch duty cycle (see Power Switch Duty Cycle section in Appendix)

Q_{MN} = Total gate charge of NFET power switch (MN) at $6.3V_{GS}$

Q_{MP} = Total gate charge of PFET power switch (MP) at $6.18V_{SG}$

V_{SELECT} = $INTV_{CC}$ LDO selected input voltage, V_{IN} or BIAS (see LDO REGULATORS section)

V_{MAX} = Higher of V_{IN} and BIAS.

Inverting Converter: Due to BIAS connecting to $INTV_{CC}$ and $INTV_{EE}$ connecting to ground (see Typical Applications), all the chip power comes from the V_{IN} pin. The $INTV_{CC}$ LDO primarily supplies voltage for both the BG and TG gate drivers. The chip Q current comes from V_{IN}. For consistency, the power that's needed to run the TG gate driver is still labeled as P_{VEE} even though the power is coming from $INTV_{CC}$. Below are the chip power equations for an inverting converter:

$P_{VCC} = 1.04 \bullet Q_{MN} \bullet f \bullet V_{IN}$
$P_{VEE1} = Q_{MP} \bullet f \bullet V_{IN}$
$P_{VEE2} = 3.15mA \bullet (1 – DC) \bullet V_{IN}$
$P_Q = 5.5mA \bullet V_{IN}$

where:

f = Switching frequency

DC = Switch duty cycle (see Power Switch Duty Cycle section in Appendix)

Q_{MN} = Total gate charge of NFET power switch (MN) at $6.3V_{GS}$

Q_{MP} = Total gate charge of PFET power switch (MP) at $6.3V_{SG}$

Chip Power Calculations Example

Table 4 calculates the power dissipation of the LT8710 for a 200kHz, 3V – 40V to 5V SEPIC application when V_{IN} is 12V. From P_{CHIP} in Table 4, the die junction temperature can be calculated using the appropriate thermal resistance and worst-case ambient temperature:

$T_J = T_A + Q_{JA} \bullet P_{CHIP}$

where T_J = die junction temperature, T_A = ambient temperature and θ_{JA} is the thermal resistance from the silicon junction to the ambient air.

The published θ_{JA} value is 38°C/W for the TSSOP exposed pad package. In practice, lower θ_{JA} values are realizable if board layout is performed with appropriate grounding

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(accounting for heat sinking properties of the board) and other considerations listed in the Layout Guidelines section. For instance, a θ_{JA} value of ~22°C/W was consistently achieved when board layout was optimized as per the suggestions in the Layout Guidelines section.

Thermal Lockout

If the die temperature reaches ~175°C, the part will go into reset, so the power switches turn off and the soft-start capacitor will be discharged. The LT8710 will come out of reset when the die temperature drops by ~5°C (typical).

Table 4. Power Calculations Example for a 200kHz, 3V to 40V to 5V/5A SEPIC (V_{IN} = 12V, MN = FDMS86500L and MP = SUD50P06-15)

DEFINITION OF VARIABLES	EQUATION	DESIGN EXAMPLE	VALUE
DC = Switch Duty Cycle	$DC \cong \frac{V_{OUT}}{V_{IN}+V_{OUT}}$	$DC \cong \frac{5V}{12V+5V}$	$DC \cong 29.4\%$
P_{VCC} = $INTV_{CC}$ LDO Power Driving the BG Gate Driver Q_{MN} = NFET Total Gate Charge at V_{GS} = 6.3V f = Switching Frequency V_{SELECT} = LDO Chooses V_{IN}	$P_{VCC} = 1.04 \bullet Q_{MN} \bullet f \bullet V_{SELECT}$	$P_{VCC} = 1.04 \bullet 73nC \bullet 200kHz \bullet 12V$	P_{VCC} = 182.2mW
P_{VEE1} = $INTV_{EE}$ LDO Power Driving the TG Gate Driver Q_{MP} = PFET Total Gate Charge at V_{SG} = 4.25V	$P_{VEE1} = Q_{MP} \bullet f \bullet V_{BIAS}$	$P_{VEE1} = 55nC \bullet 200kHz \bullet 5V$	P_{VEE1} = 55mW
P_{VEE2} = Additional TG Gate Driver Power Loss	$P_{VEE2} = 3.1mA \bullet (1 - DC) \bullet V_{BIAS}$	$P_{VEE2} = 3.1mA \bullet (1 - 0.294) \bullet 5V$	P_{VEE2} = 10.9mW
P_Q = Chip Bias Loss V_{MAX} = Higher Voltage of V_{IN} and BIAS	$P_Q = 4mA \bullet V_{MAX}$	$P_Q = 4mA \bullet 12V$	P_Q = 48mW
			P_{CHIP} = 296.1mW

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POWER SWITCH DUTY CYCLE

In order to maintain loop stability and deliver adequate current to the load, the external power NFET (MN in the Block Diagram) cannot remain on for 100% of each clock cycle. The maximum allowable duty cycle is given by:

$$DC_{MAX} = \frac{(T_P - MinOffTime)}{T_P} \bullet 100\%$$

where T_P is the clock period and MinOffTime (found in the Electrical Characteristics) is a maximum of 480ns.

Conversely, the external power NFET (MN in the Block Diagram) cannot remain off for 100% of each clock cycle, and will turn on for a minimum on time (MinOnTime) when in regulation. This MinOnTime governs the minimum allowable duty cycle given by:

$$DC_{MIN} = \frac{(MinOnTime)}{T_P} \bullet 100\%$$

where T_P is the clock period and MinOnTime (found in the Electrical Characteristics) is a maximum of 420ns.

The application should be designed such that the operating duty cycle is between DC_{MIN} and DC_{MAX}.

Duty cycle equations for several common topologies are given below where V_{ON_MP} is the voltage drop across the external power PFET (MP) when it is on, and V_{ON_MN} is the voltage drop across the external power NFET (MN) when it is on.

For the boost topology (see Figure 5):

$$DC_{BOOST} \cong \frac{V_{OUT} - V_{IN} + V_{ON\_MP}}{V_{OUT} + V_{ON\_MP} - V_{ON\_MN}}$$

For the SEPIC or dual inductor inverting topology (see Figures 6 and 7):

$$DC_{SEPIC\_\&\_INVERT} \cong \frac{|V_{OUT}| + V_{ON\_MP}}{V_{IN} + |V_{OUT}| + V_{ON\_MP} - V_{ON\_MN}}$$

The LT8710 can be used in configurations where the duty cycle is higher than DC_{MAX}, but it must be operated in the discontinuous conduction mode (MODE pin must be high) so that the effective duty cycle is reduced.

INDUCTOR SELECTION

For high efficiency, choose inductors with high frequency core material, such as ferrite, to reduce core losses. Also to improve efficiency, choose inductors with more volume for a given inductance. The inductor should have low DCR (copper-wire resistance) to reduce I^2R losses, and must be able to handle the peak inductor current without saturating. Note that in some applications, the current handling requirements of the inductor can be lower, such as in the SEPIC topology where each inductor carries a fraction of the total switch current. Molded chokes or chip inductors do not have enough core area to support peak inductor currents in the 5A to 15A range. To minimize radiated noise, use a toroidal or shielded inductor. See Table 5 for a list of inductor manufacturers.

Table 5. Inductor Manufacturers

Coilcraft	MSS1278, XAL1010, and MSD1278 Series	www.coilcraft.com
Cooper Bussmann	DRQ127, DR127, and HCM1104 Series	www.cooperbussmann.com
Vishay	IHLP Series	www.vishay.com
Würth	WE-DCT Series WE-CFWI Series	www.we-online.com

Minimum Inductance

Although there can be a trade-off with efficiency, it is often desirable to minimize board space by choosing smaller inductors. When choosing an inductor, there are three conditions that limit the minimum inductance; (1) providing adequate load current, and (2) avoidance of subharmonic oscillation, and (3) supplying a minimum ripple current to avoid false tripping of the current comparator.

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Adequate Load Current

Small value inductors result in increased ripple currents and thus, due to the limited peak switch current, decrease the average current that can be provided to the load. In order to provide adequate load current, L should be at least:

$$L_{BOOST} \geq \frac{V_{IN} \bullet DC}{2 \bullet f \bullet \left(\frac{V_{CSPN}}{R_{SENSE1}} - \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet \eta} \right)}$$ Boost Topology

or

$$L_{DUAL} \geq \frac{V_{IN} \bullet DC}{2 \bullet f \bullet \left(\frac{V_{CSPN}}{R_{SENSE1}} - \frac{|V_{OUT}| \bullet I_{OUT}}{V_{IN} \bullet \eta} - I_{OUT} \right)}$$ SEPIC or Inverting Topologies

where:

L_{BOOST} = L_1 for boost topologies (see Figure 5)

L_{DUAL} = $L_1 = L_2$ for coupled dual inductor topologies (see Figures 6 and 7)

L_{DUAL} = $L_1 \,||\, L_2$ for uncoupled dual inductor topologies (see Figures 6 and 7)

DC = Switch duty cycle (see previous section)

V_{CSPN} = Current limit voltage at the operating switch duty cycle (see *Max Current Limit vs Duty Cycle (CSP – CSN)* plot in the Typical Performance Characteristics)

R_{SENSE1} = Current sense resistor connected across the CSP-CSN pins (see Block Diagram)

η = Power conversion efficiency (assume 90%)

f = Switching frequency

I_{OUT} = Maximum output current

Negative values of L_{BOOST} or L_{DUAL} indicate that the output load current, I_{OUT}, exceeds the switch current limit capability of the converter. Decrease R_{SENSE1} to increase the switch current limit.

Avoiding Subharmonic Oscillations

The LT8710's internal slope compensation circuit will prevent subharmonic oscillations that can occur when the duty cycle is greater than 50%, provided that the inductance exceeds a minimum value. In applications that operate with duty cycles greater than 50%, the inductance must be at least:

$$L_{MIN} \geq \frac{V_{IN} \bullet R_{SENSE1} \bullet (2 \bullet DC - 1)}{40m \bullet DC \bullet f \bullet (1 - DC)}$$

where

L_{MIN} = L_1 for boost topologies (see Figure 5)

L_{MIN} = $L_1 = L_2$ for coupled dual inductor topologies (see Figures 6 and 7)

L_{MIN} = $L_1 \,||\, L_2$ for uncoupled dual inductor topologies (see Figures 6 and 7)

Maximum Inductance

Excessive inductance can reduce ripple current to levels that are difficult for the current comparator (A5 in the Block Diagram) to cleanly discriminate, thus causing duty cycle jitter and/or poor regulation. The maximum inductance can be calculated by:

$$L_{MAX} \leq \frac{V_{IN} \bullet R_{SENSE1} \bullet DC}{5m \bullet f}$$

where:

L_{MAX} = L_1 for boost topologies (see Figure 5)

L_{MAX} = $L_1 = L_2$ for coupled dual inductor topologies (see Figures 6 and 7)

L_{MAX} = $L_1 \,||\, L_2$ for uncoupled dual inductor topologies (see Figures 6 and 7)

Inductor Current Rating

The inductor(s) must have a rating greater than its (their) peak operating current to prevent inductor saturation, which would result in efficiency losses. The maximum

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inductor current (considering start-up and steady-state conditions) is given by:

$$I_{L\_PEAK} = \frac{54mV - 16mV \bullet DC^2}{R_{SENSE1}} + \frac{V_{IN} \bullet T_{MIN\_PROP}}{L}$$

where

I_{L_PEAK} = Peak inductor current in L_1 for a boost topology, or the sum of the peak inductor currents for dual inductor topologies.

T_{MIN_PROP} = 100ns (propagation delay through the current feedback loop).

For wide input voltage range applications, as the input voltage increases, the max peak inductor current also increases due to the duty cycle decreasing. It is recommended to utilize the output current limiting feature to reduce the max peak inductor current given by the following equation:

$$I_{L\_PEAK} = \frac{V_{ISPN}}{R_{SENSE2} \bullet (1 - DC)} + \frac{V_{IN} \bullet DC}{2 \bullet f \bullet L}$$

where….

V_{ISPN} = 57mV max for noninverting converters and 60mV max for inverting converters.

Note that these equations offer conservative results for the required inductor current ratings. The current ratings could be lower for applications with light loads, and if the SS capacitor is sized appropriately to limit inductor currents at start-up.

POWER MOSFET SELECTION

The LT8710 requires two external power MOSFETs, an NFET switch for the BG gate driver and a PFET switch for the TG gate driver. It is important to select MOSFETs for optimizing efficiency. For choosing an NFET and PFET, the important device parameters are:

1. Breakdown voltage (BV_{DSS})
2. Gate threshold voltage (V_{GSTH})
3. On-resistance (r_{DSON})
4. Total gate charge (Q_G)
5. Turn-off delay time ($t_{D(OFF)}$)
6. Package has exposed paddle

The drain-to-source breakdown voltage of the NFET and PFET power MOSFETs must exceed:

- $BV_{DSS} > V_{OUT}$ for boost converter
- $BV_{DSS} > V_{IN}+|V_{OUT}|$ for SEPIC or dual inductor inverting converter

If operating close to the BV_{DSS} rating of the MOSFET, check the leakage specifications on the MOSFET because leakage can decrease the efficiency of the converter.

The NFET and PFET gate-to-source drive is approximately 6.3V and 6.18V respectively, so logic level MOSFETs are required. The BG gate driver can begin switching when the $INTV_{CC}$ voltage exceeds ~4V, so ensure the selected NFET is in the linear mode of operation with 4V of gate-to-source drive to prevent possible damage to the NFET.

The TG gate driver can begin switching when the BIAS-$INTV_{EE}$ voltage exceeds ~3.42V, so it is optimal that the PFET be in the linear mode of operation with 3.42V of gate-to-source drive. However, the PFET is less likely to get damaged if it's not operating in the linear region since the drain-to-source voltage is clamped by its body diode during the NFET's off-time. Having said that, try to choose a PFET with a low body diode reverse recovery time to minimize stored charge in the PFET. The stored charge in the PFET body diode gets removed when the NFET switch turns on and can lead to efficiency hits especially in applications where the V_{DS} of the PFET (during off-time) is high. For these applications, it may be beneficial to put a Schottky diode across the PFET to reduce the amount of charge in the PFET body diode. In applications where the output voltage is high in magnitude, it may be better to replace the PFET with a Schottky diode since the converter may be more efficient with a Schottky.

Power MOSFET on-resistance and total gate charge go hand-in-hand and are typically inversely proportional to each other; the lower the on-resistance, the higher total gate charge. Choose MOSFETs with an on-resistance to give a voltage drop to be less than 300mV at the peak

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current. At the same time, choose MOSFETs with a lower total gate charge to reduce LT8710 power dissipation and MOSFET switching losses.

The turn-off delay time ($t_{D(OFF)}$) of available NFETs is generally smaller than the LT8710's non-overlap time. However, the turn-off time of the available PFETs should be looked at before deciding on a PFET for a given application. The turn-off time must be less than the non-overlap time of the LT8710 or else the NFET and PFET could be on at the same time and damage to external components may occur. If the PFET turn-off delay time as specified in the data sheet is less than the LT8710 non-overlap time, then the PFET is good to use. If the turn-off delay time is longer than the non-overlap time, it doesn't necessarily mean it can't be used. It may be unclear how the PFET manufacturer measures the turn-off delay time, so it is best to measure the PFET turn-off delay time with respect to the PFET gate voltage.

Finally, both the NFET and PFET power MOSFETs should be in a package with an exposed paddle for the drain connection to be able to dissipate heat. The on-resistance of MOSFETs is proportional to temperature, so it's more efficient if the MOSFETs are running cool with the help of the exposed paddle. See Table 6 for a list of power MOSFET manufacturers.

Table 6. Power MOSFET (NFET and PFET) Manufacturers

Fairchild Semiconductor	www.fairchildsemi.com
On-Semiconductor	www.onsemi.com
Vishay	www.vishay.com
Diodes Inc.	www.diodes.com

INPUT AND OUTPUT CAPACITOR SELECTION

Input and output capacitance is necessary to suppress voltage ripple caused by discontinuous current moving in and out of the regulator. A parallel combination of capacitors is typically used to achieve high capacitance and low ESR (equivalent series resistance). Tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Capacitors with low ESR and high ripple current ratings, such as OS-CON and POSCAP are also available.

Ceramic capacitors should be placed near the regulator input and output to suppress high frequency switching noise. A minimum 1µF ceramic capacitor should also be placed from V_{IN} to GND and from BIAS to GND as close to the LT8710 pins as possible. Due to their excellent low ESR characteristics, ceramic capacitors can significantly reduce ripple voltage and help reduce power loss in the higher ESR bulk capacitors. X5R or X7R dielectrics are preferred, as these materials retain their capacitance over wide voltage and temperature ranges. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired operating voltage.

Input Capacitor, C_{IN}

The input capacitor, C_{IN}, sees the ripple current of the input inductor, L_1, which eases the capacitance requirements of C_{IN}. Below is the equation for calculating the capacitance of C_{IN} for 0.5% input voltage ripple:

$$C_{IN} > \frac{DC}{8 \bullet L \bullet f^2 \bullet 0.005}$$

where:

DC = Switch duty cycle (see Power Switch Duty Cycle section)

L = L_{BOOST} or L_{DUAL} (see Inductor Selection section)

f = Switching frequency

The worst-case for the input capacitor (largest capacitance needed) is when the input voltage is at its lowest because the duty cycle is the highest. Keep in mind that the voltage rating of the input capacitor needs to be greater than the maximum input voltage. This equation calculates the capacitance value during steady-state operation and may need to be adjusted for desired transient response. Also, this assumes no ESR, so the input capacitance may need to be larger depending on the equivalent ESR of the input capacitor(s).

Output Capacitor, C_{OUT}

The output capacitor, C_{OUT}, in a boost or SEPIC topology has chopped current flowing through it, whereas the output capacitor in a dual inductor inverting topology sees the

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inductor ripple current. Below is the equation for calculating the capacitance of C_{OUT} for 0.5% output voltage ripple:

$$C_{OUT} > \frac{I_{OUT} \bullet DC}{f \bullet 0.005 \bullet V_{OUT}}$$ Boost or SEPIC Topologies

or

$$C_{OUT} > \frac{1-DC}{8 \bullet L \bullet f^2 \bullet 0.005}$$ Dual Inductor Inverting Topology

where:

I_{OUT} = Maximum output current of converter

DC = Switch duty cycle (see Power Switch Duty Cycle section)

L = L_{BOOST} or L_{DUAL} (see Inductor Selection section)

f = Switching frequency

The worst-case for the output capacitor (largest capacitance needed) is when the output regulation voltage is relatively low. This equation calculates the capacitance value during steady-state operation and may need to be adjusted for desired transient response. Also, this assumes no ESR, so the output capacitance may need to be larger depending on the equivalent ESR of the output capacitor(s). See Table 7 for a list of ceramic capacitor manufacturers.

Table 7. Ceramic Capacitor Manufacturers

TDK	www.tdk.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com

COMPENSATION – ADJUSTMENT

To compensate the feedback loop of the LT8710, a series resistor capacitor network in parallel with an optional single capacitor should be connected from the V_C pin to GND. For most applications, choose a series capacitor in the range of 1nF to 10nF with 4.7nF being a good starting value. The optional parallel capacitor should range in value from 47pF to 220pF with 100pF being a good starting value. The compensation resistor, R_C, is usually in the range of 5k to 50k. A good technique to compensate a new application is to use a 100k potentiometer in place of the series resistor R_C. With the series and parallel capacitors at 4.7nF and 100pF respectively, adjust the potentiometer while observing the transient response and the optimum value for R_C can be found. The series capacitor can be reduced or increased from 4.7nF to speed up the converter or slow down the converter, respectively. For the circuit in Figure 7, a 3.3nF series cap was used. Figures 21a to 21c illustrate this process for the circuit of Figure 7 with a load current stepped between 2A and 5.5A with an input voltage of 9V. Figure 21a shows the transient response with R_C equal to 1k. The phase margin is poor as evidenced by the excessive ringing in the output voltage and inductor current. In Figure 21b, the value of R_C is increased to 4k, which results in a more damped response. Figure 21c shows the results when R_C is increased further to 11.5k. The transient response is nicely damped and the compensation procedure is complete.

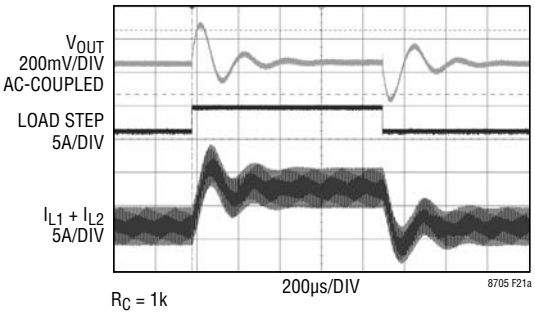

Figure 21a. Transient Response Shows Excessive Ringing

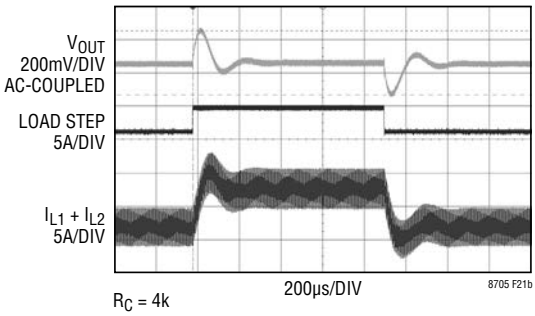

Figure 21b. Transient Response is Better

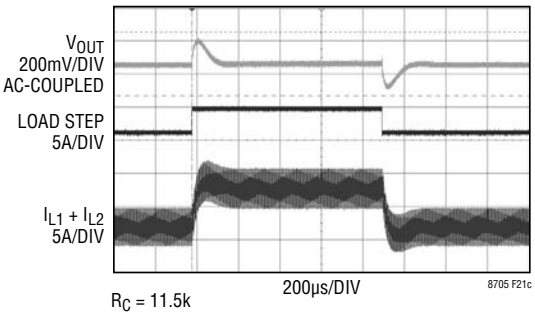

Figure 21c. Transient Response is Well Damped

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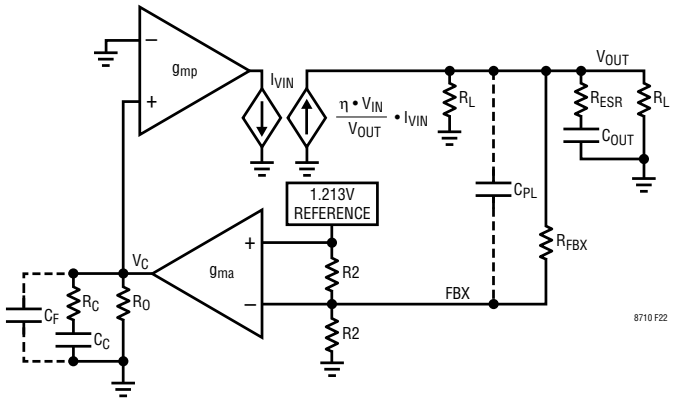
COMPENSATION – THEORY

Like all other current mode switching regulators, the LT8710 needs to be compensated for stable and efficient operation. Two feedback loops are used in the LT8710: a fast current loop which does not require compensation, and a slower voltage loop which does. Standard bode plot analysis can be used to understand and adjust the voltage feedback loop.

As with any feedback loop, identifying the gain and phase contribution of the various elements in the loop is critical. Figure 22 shows the key equivalent elements of a boost converter. Because of the fast current control loop, the power stage of the IC, inductor and PFET have been replaced by a combination of the equivalent transconductance amplifier g_{mp} and the current controlled current source (which converts I_{VIN} to $\frac{\eta V_{IN}}{V_{OUT}} I_{VIN}$). G_{mp} acts as a current source where the peak input current, I_{VIN}, is proportional to the V_C voltage and current sense resistor, R_{SENSE1}.



C_C: COMPENSATION CAPACITOR
C_{OUT}: OUTPUT CAPACITOR
C_{PL}: PHASE LEAD CAPACITOR
C_F: HIGH FREQUENCY FILTER CAPACITOR
g_{ma}: TRANSCONDUCTANCE AMPLIFIER INSIDE IC
g_{mp}: POWER STAGE TRANSCONDUCTANCE AMPLIFIER
R_C: COMPENSATION RESISTOR
R_L: OUTPUT RESISTANCE DEFINED AS $V_{OUT}/I_{LOADMAX}$
R_O: OUTPUT RESISTANCE OF g_{ma}
R2, R_{FBX}: FEEDBACK RESISTOR DIVIDER NETWORK
R_{ESR}: OUTPUT CAPACITOR ESR
η: CONVERTER EFFICIENCY (~90% AT HIGHER CURRENTS)

Figure 22. Boost Converter Equivalent Model

Note that the maximum output currents of g_{mp} and g_{ma} are finite. The external current sense resistor, R_{SENSE1}, sets the value of:

$$g_{mp} \approx \frac{1}{6 \bullet R_{SENSE1}}$$

The error amplifier, g_{ma}, is nominally about 200µmhos with a source and sink current of about 12µA and 19µA respectively.

From Figure 22, the DC gain, poles and zeros can be calculated as follows:

DC GAIN:

$$A_{DC} = g_{ma} \bullet R_O \bullet g_{mp} \bullet \eta \bullet \frac{V_{IN}}{V_{OUT}} \bullet \frac{R_L}{2} \bullet \frac{0.5 \bullet R_2}{R_{FBX} + 0.5 \bullet R_2}$$

$$\text{Output Pole: } P1 = \frac{2}{2 \bullet \pi \bullet R_L \bullet C_{OUT}}$$

$$\text{Error Amp Pole: } P2 = \frac{1}{2 \bullet \pi \bullet (R_O + R_C) \bullet C_C}$$

$$\text{Error Amp Zero: } Z1 = \frac{1}{2 \bullet \pi \bullet R_C \bullet C_C}$$

$$\text{ESR Zero: } Z2 = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}}$$

$$\text{RHP Zero: } Z3 = \frac{V_{IN}^2 \bullet R_L}{2 \bullet \pi \bullet V_{OUT}^2 \bullet L}$$

$$\text{High Frequency Pole: } P3 > \frac{f_S}{3}$$

$$\text{Phase Lead Zero: } Z4 = \frac{1}{2 \bullet \pi \bullet R_{FBX} \bullet C_{PL}}$$

$$\text{Phase Lead Pole: } P4 = \frac{1}{2 \bullet \pi \bullet \frac{R_{FBX} \bullet 0.5 \bullet R_2}{R_{FBX} + 0.5 \bullet R_2} \bullet C_{PL}}$$

$$\text{Error Amp Filter Pole: } P5 = \frac{1}{2 \bullet \pi \bullet \frac{R_C \bullet R_O}{R_C + R_O} \bullet C_F}, C_F < \frac{C_C}{10}$$

The current mode zero (Z3) is a right half plane zero which can be an issue in feedback control design, but is manageable with proper external component selection.

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Using the circuit in Figure 24 with a 4A load as an example, Table 9 shows the parameters used to generate the bode plot shown in Figure 23.

Table 9: Bode Plot Parameters

PARAMETER	VALUE	UNITS	COMMENT
R_L	3	Ω	Application Specific
C_{OUT}	88	µF	Application Specific
R_{ESR}	2	mΩ	Application Specific
R_O	350	kΩ	Not Adjustable
C_C	3300	pF	Adjustable
C_F	100	pF	Optional/Adjustable
C_{PL}	0	pF	Optional/Adjustable
R_C	18	kΩ	Adjustable
R_{FBX}	130	kΩ	Adjustable
R2	14.5	kΩ	Not Adjustable
V_{OUT}	12	V	Application Specific
V_{IN}	5	V	Application Specific
g_{ma}	200	µmho	Not Adjustable
g_{mp}	167	mho	Application Specific
L	1.3	µH	Application Specific
f_{OSC}	400	kHz	Adjustable

From Figure 23, the phase is –135° when the gain reaches 0dB giving a phase margin of 45°. The crossover frequency is 20kHz, which is about three times lower than the frequency of the RHP zero Z3 to achieve adequate phase margin.

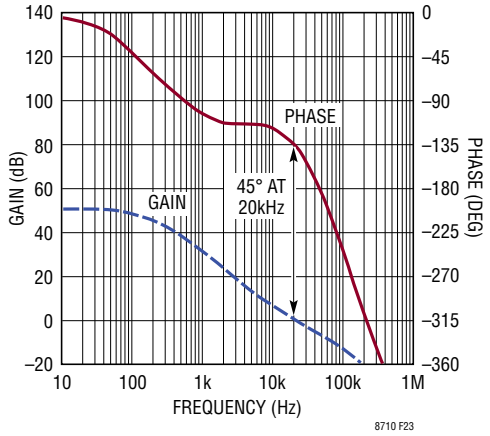


Figure 23. Bode Plot for Example Boost Converter

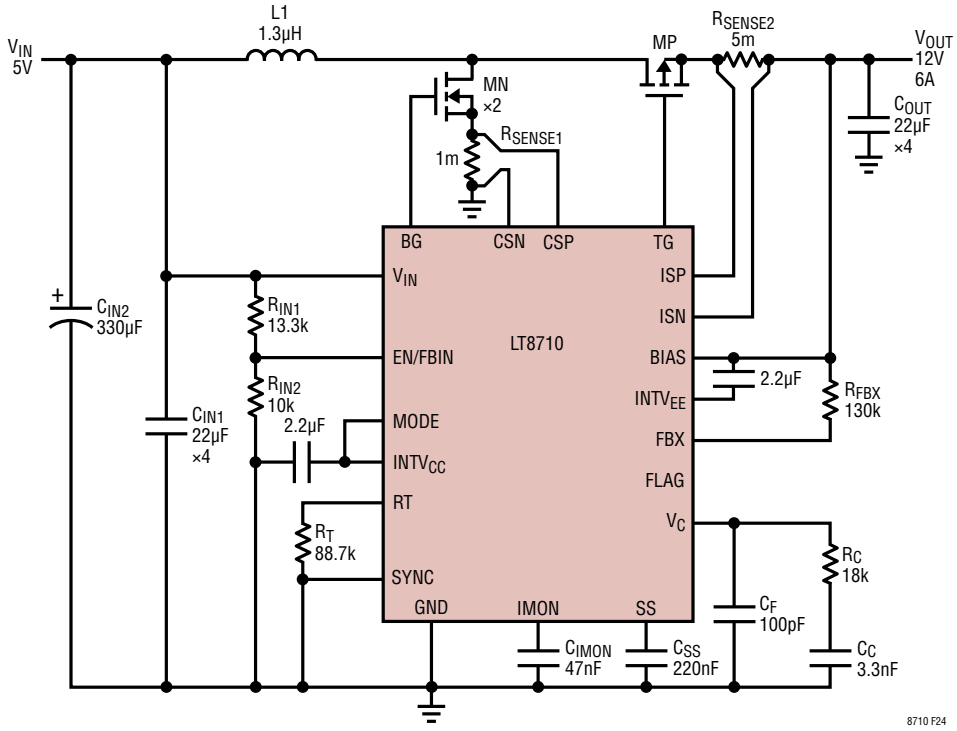
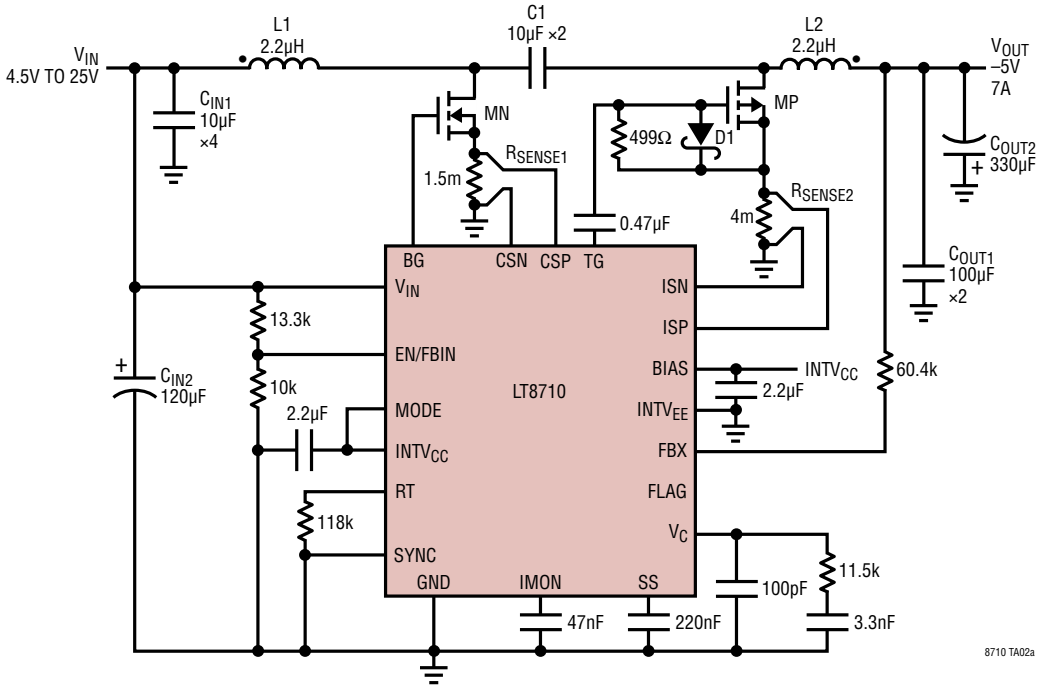


Figure 24. 5V to 12V Boost Converter

TYPICAL APPLICATION

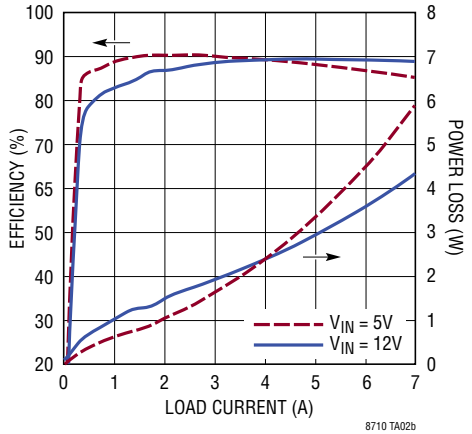
300kHz, 4.5V to 25V Input to –5V Output Delivers Up to 7A Output Current



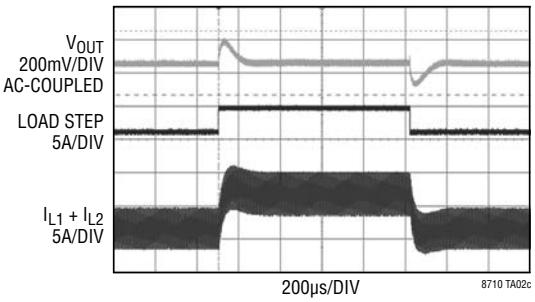
L1, L2: WÜRTH 2.2µH WE-CFWI 74485540220
MN: FAIRCHILD FDMS8333L
MP: FAIRCHILD FDD4141
R_{SENSE1}: 1.5mΩ 2010
R_{SENSE2}: 4mΩ 2512
D1: NXP PMEG2010EA

C_{IN1}: 10µF, 50V, 1210, X7S
C_{IN2}: OSCON 120µF, 35V, 35SVPF120M
C_{OUT1}: 100µF, 6.3V, 1812, X5R
C_{OUT2}: OSCON 330µF, 16V, 16SEQP330M
C1: 10µF, 50V, 1210, X7S

Efficiency and Power Loss

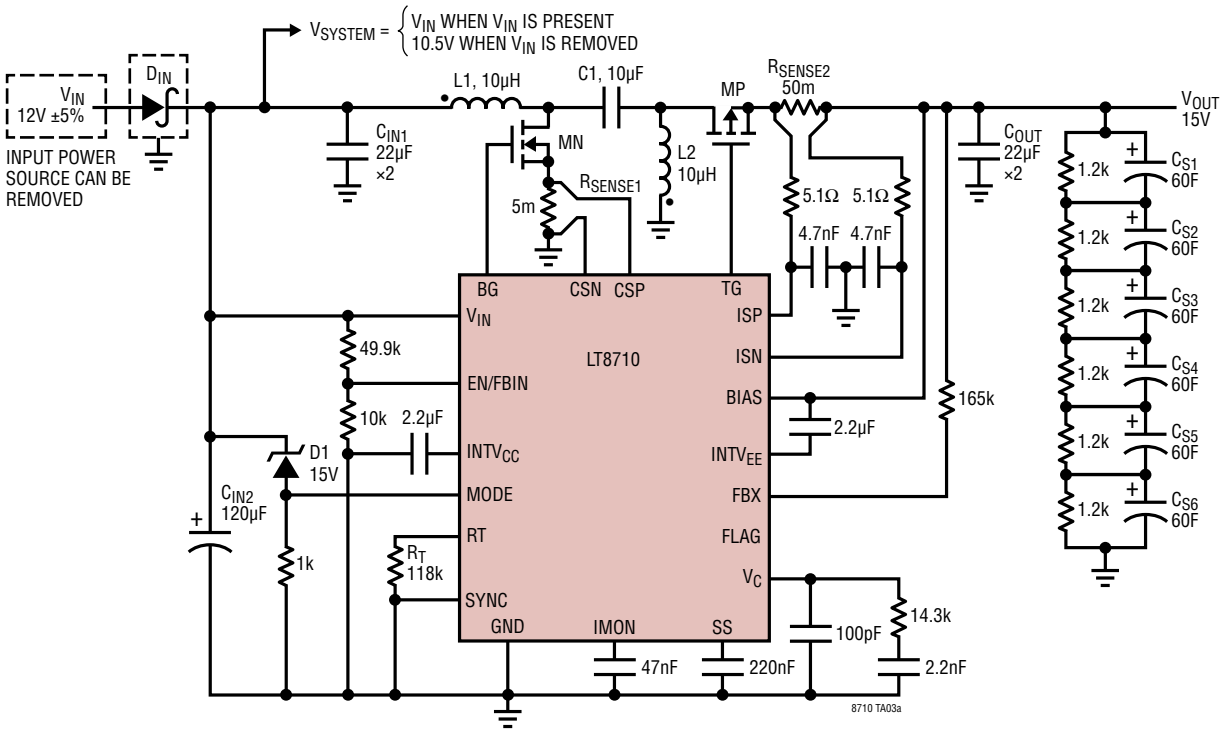


Transient Response with 2A to 5.5A to 2A Output Load Step (V_{IN} = 12)



TYPICAL APPLICATION

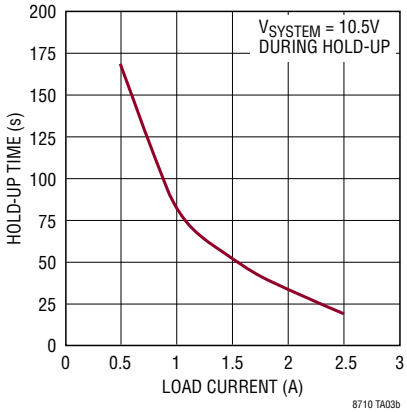
300kHz, SuperCap Backup Power



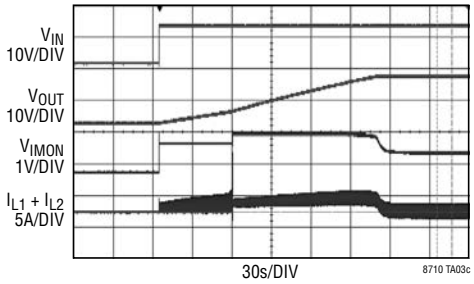
L1, L2: COILCRAFT 10µH MSD1278-103ML
MN: FAIRCHILD FDMC8327L
MP: VISHAY Si7611DN
R_{SENSE1}: 5mΩ 2010
R_{SENSE2}: 50mΩ 2512
D_{IN}: APPROPRIATE SCHOTTKY DIODE OR IDEAL DIODE SUCH AS LTC4358, LTC4352, LTC4412, ETC.

C_{IN1}: 22µF, 25V, 1812, X7R
C_{OUT}: 22µF, 25V, 1812, X7R
C1: 10µF, 25V, 1210, X7R
C_{S1-6}: POWERSTOR HB1840-2R5606-R
D1: CENTRAL SEMI CMDZ5245B-LTZ

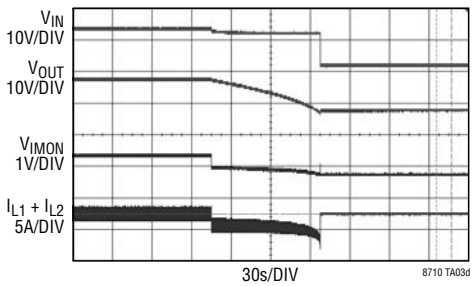
System Hold-Up Time vs System Load Current



SuperCaps Charging When V_{IN} Is Applied

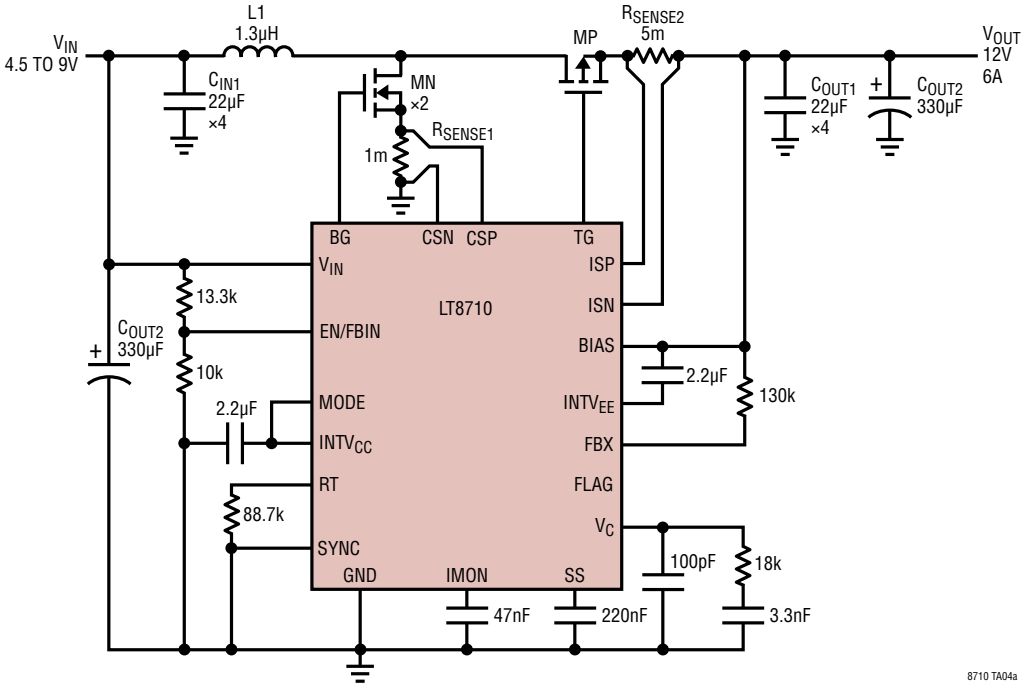


SuperCaps Hold-Up System at 10.5V for ~83s When V_{IN} Is Removed (I_{SYSTEM} = 1A)



TYPICAL APPLICATION

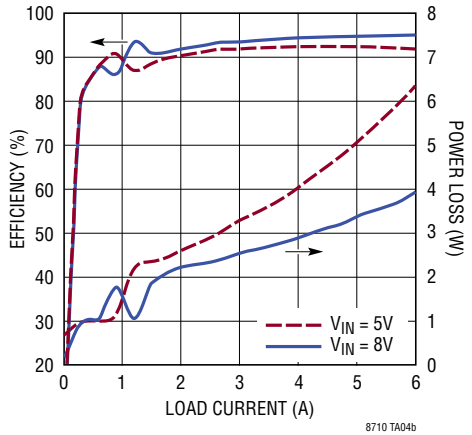
400kHz, 12V Boost Converter Delivers Up to 6A from a 4.5V to 9V Input



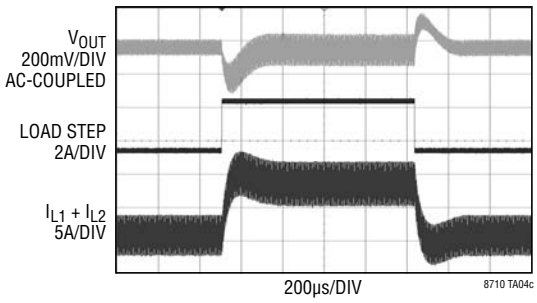
L1: WÜRTH 1.3µH WE-HCI 7443551130
MN: VISHAY SiR802DP
MP: VISHAY Si7635DP
R_{SENSE1}: 1mΩ 2512
R_{SENSE2}: 5mΩ 2512

C_{IN1}: 22µF, 16V, 1206, X5R
C_{IN2}: OSCON 330µF, 16V, 16SEQP330M
C_{OUT1}: 22µF, 25V, 1812, X7R
C_{OUT2}: OSCON 330µF, 16V, 16SEQP330M

Efficiency and Power Loss

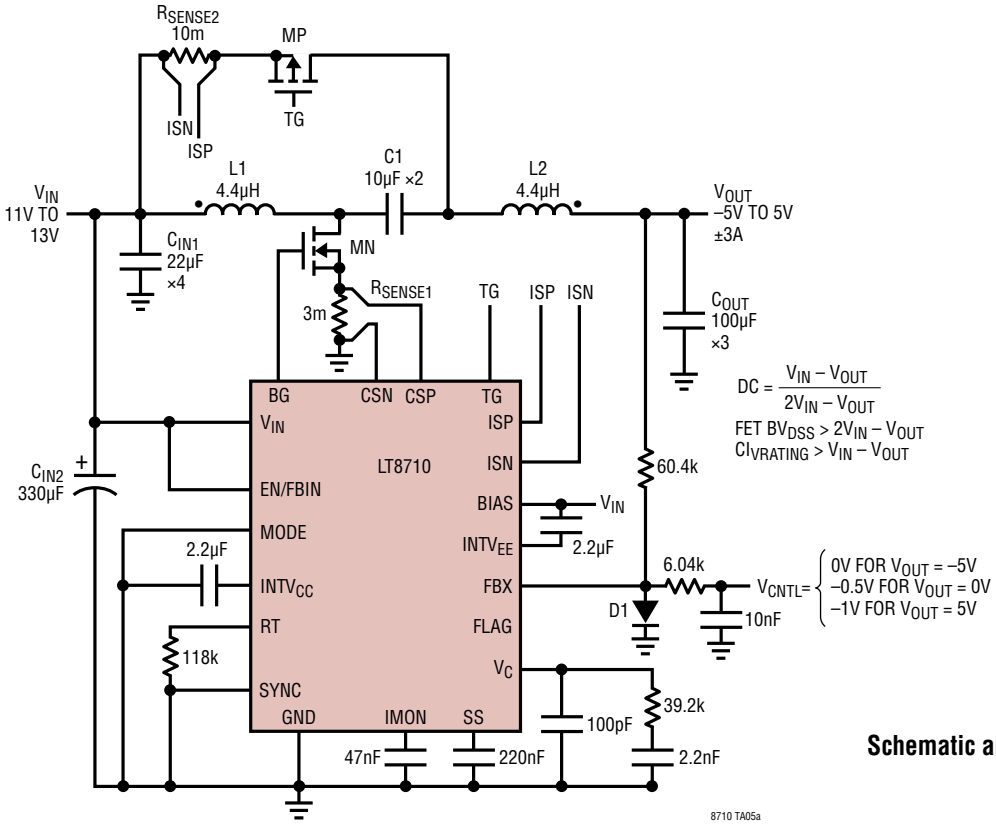


Transient Response with 2A to 5A to 2A Output Load Step (V_{IN} = 5V)



TYPICAL APPLICATION

300kHz, –5V to 5V Output Cleanly Transitions Through 0V with 3A Source and Sink Capability*

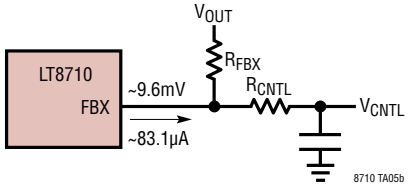


L1, L2: WÜRTH 4.4µH WE-CFWI 74485540440
MN: FAIRCHILD FDMS8333L
MP: FAIRCHILD FDD4141
R_{SENSE1}: 3mΩ 2010
R_{SENSE2}: 10mΩ 2512

C_{IN1}: 22µF, 25V, 1812, X7R
C_{IN2}: OSCON 330µF, 16V, 16SEQP330M
C_{OUT}: 100µF, 6.3V, 1812, X5R
C1: 10µF, 25V, 1210, X7R
D1: CENTRAL SEMI CMPD1001

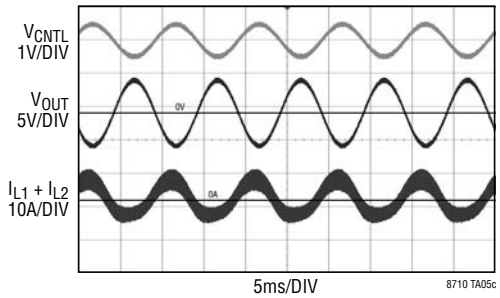
* PATENT PENDING

Schematic and Equations for Calculating V_{OUT}

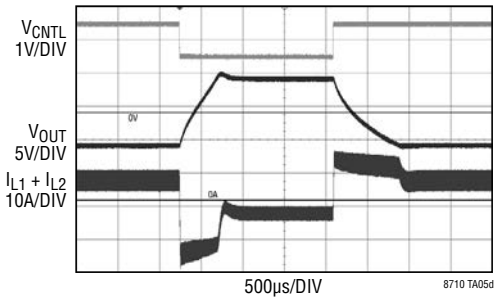


$$V_{OUT} = 9.6mV - 83.1\mu A \bullet R_{FBX} - \frac{R_{FBX}}{R_{CNTL}} (V_{CNTL} - 9.6mV)$$

V_{OUT} Cleanly Transitions Through 0V with a 1V, 100Hz Sine Wave CNTL Signal (R_{LOAD} = 2Ω)

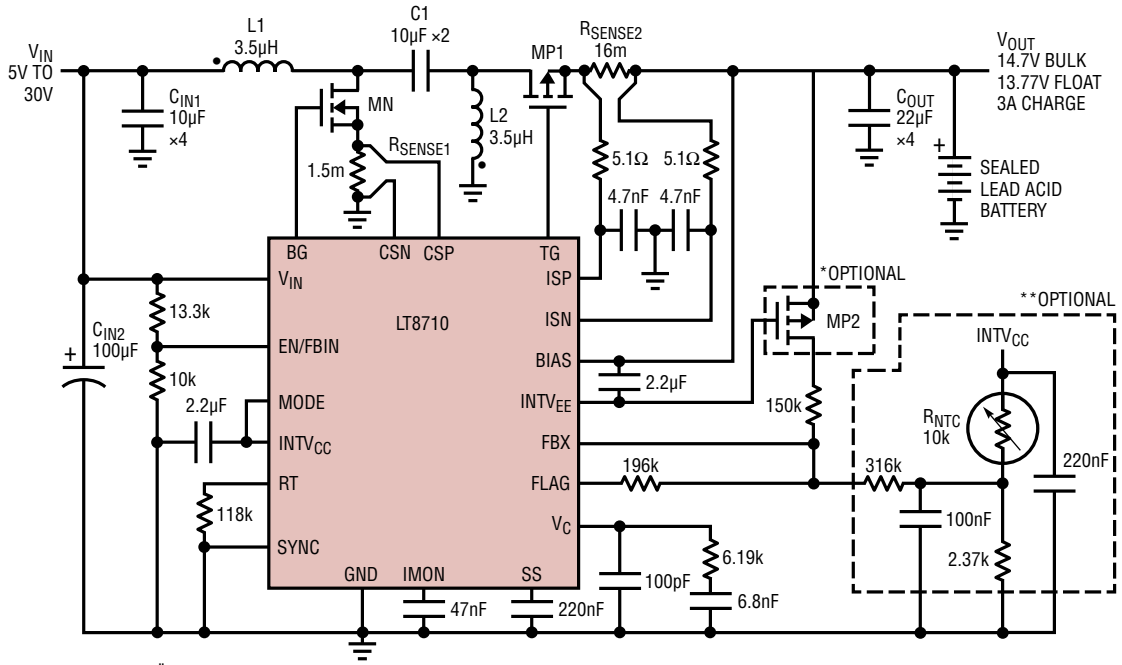


Transient Response with Stepping V_{CNTL} from 0V to –1V to 0V with 2Ω Output Load



TYPICAL APPLICATION

300kHz, 3A Sealed Lead Acid Battery Charger with an Optional Negative Temp-Co Bulk and Float Battery Voltage



L1, L2: WÜRTH 3.5µH WE-CFWI 74485540350
MN: FAIRCHILD FDMS86500L
MP1: VISHAY SUD50P06-15
R_{SENSE1}: 1.5mΩ 2010
R_{SENSE2}: 16mΩ 2512
C_{IN1}: 10µF, 50V, 1210, X7S
C_{OUT}: 22µF, 25V, 1812, X7R
C1: 10µF, 50V, 1210, X7S
MP2: VISHAY Si2343CDS
R_{NTC}: MURATA NCP18XH103F03RB

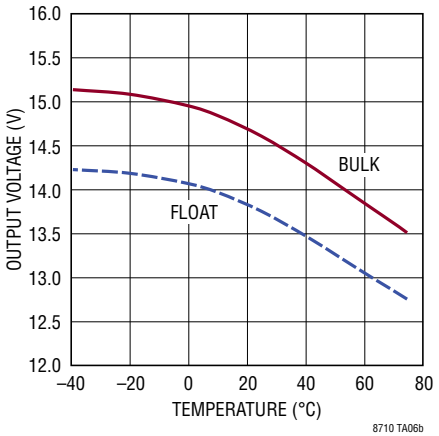
SEE THE BATTERY CHARGING AND C/10 SECTION IN APPLICATIONS INFORMATION FOR MORE INFORMATION ON BATTERY CHARGING

* MP2 DISCONNECTS FBX PIN CURRENT DRAW FROM BATTERY WHEN LT8710 IS IN SHUTDOWN

** PLACE 316kΩ AND 100nF AS CLOSE TO THE FBX PIN AS POSSIBLE. ALSO, CONNECT ALL GROUNDS OF THESE COMPONENTS TO THE LT8710 GROUND

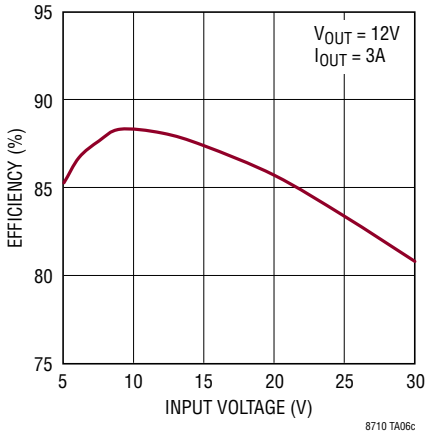
8710 TA06a

Bulk and Float Output Voltage with **Optional Components



8710 TA06b

Efficiency vs Input Voltage

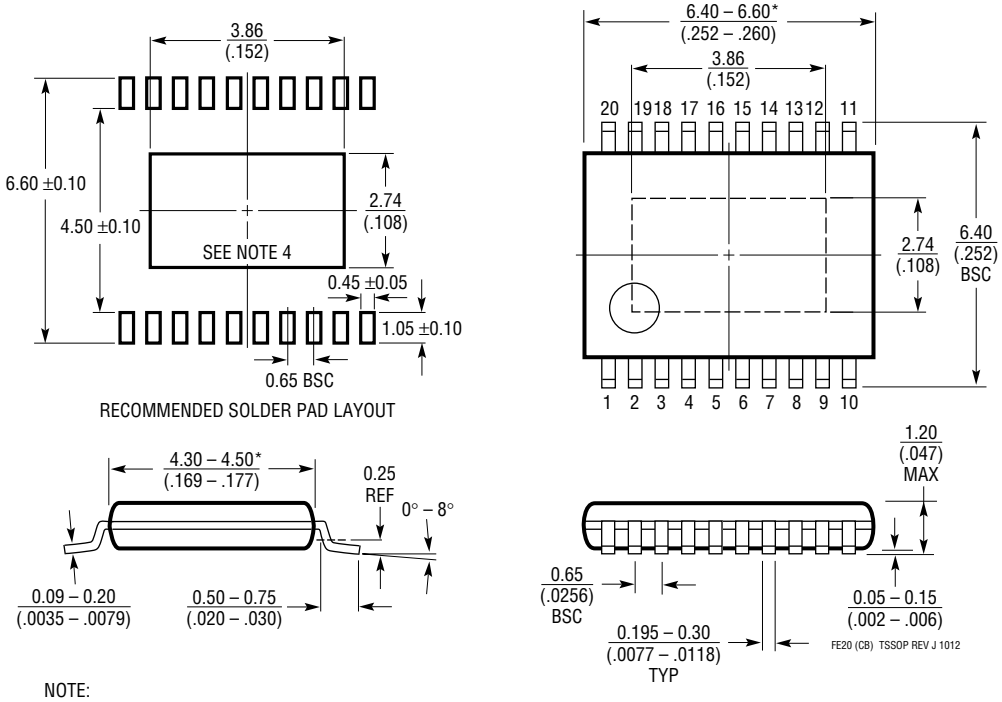


8710 TA06c

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

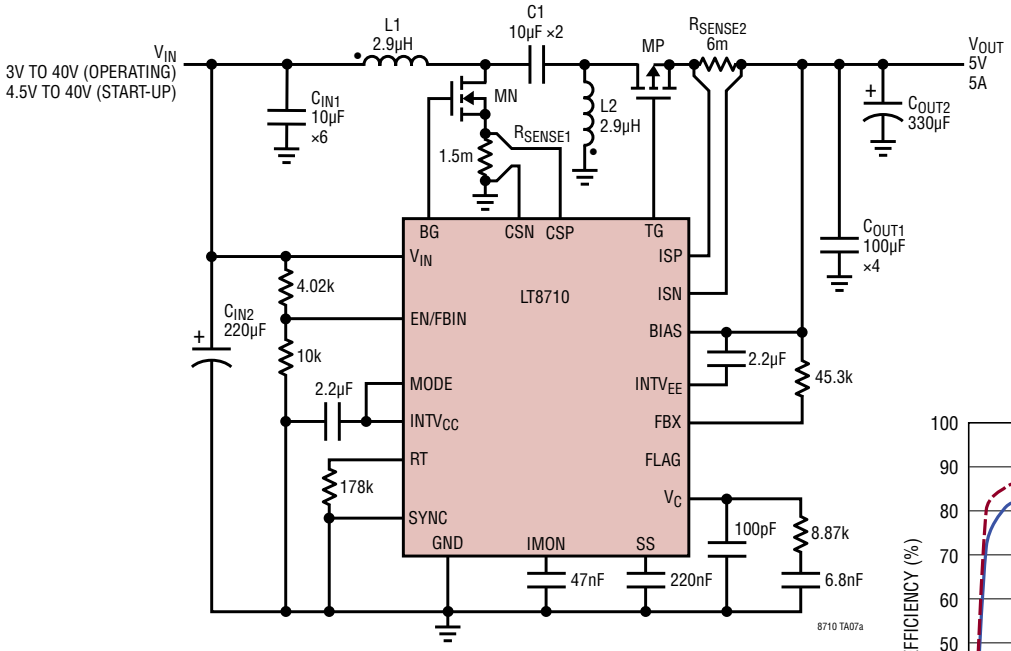
FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev J)
Exposed Pad Variation CB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

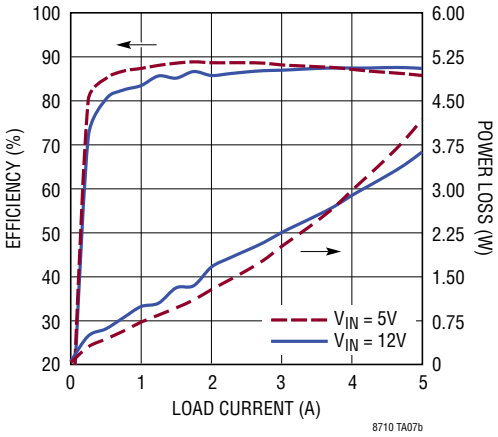
TYPICAL APPLICATION

200kHz, Wide Input Range SEPIC Converter Generates a 5V Output with Up to 5A Output Current



L1, L2: WÜRTH 2.9µH WE-CFWI 74485540290
MN: FAIRCHILD FDMS86500L
MP: VISHAY SUD50P06-15
R_{SENSE1}: 1.5mΩ 2010
R_{SENSE2}: 6mΩ 2512
C_{IN1}: 10µF, 50V, 1210, X7S
C_{OUT1}: 100µF, 6.3V, 1812, X5R
C_{OUT2}: OSCON 330µF, 16V, 16SEQP330M
C1: 10µF, 50V, 1210, X7S

Efficiency and Power Loss



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3757A	Boost, Flyback, SEPIC and Inverting Controller	2.9V ≤ V_{IN} ≤ 40V, 100kHz to 1MHz Programmable Operating Frequency, 3mm × 3mm DFN-10 and MSOP-10E Packages
LT3758A	Boost, Flyback, SEPIC and Inverting Controller	5.5V ≤ V_{IN} ≤ 100V, 100kHz to 1MHz Programmable Operating Frequency, 3mm × 3mm DFN-10 and MSOP-10E Packages
LT3759	Boost, SEPIC and Inverting Controller	1.6V ≤ V_{IN} ≤ 42V, 100kHz to 1MHz Programmable Operating Frequency, MSOP-12E Package
LT3957A	Boost, Flyback, SEPIC and Inverting Converter with 5A, 40V Switch	3V ≤ V_{IN} ≤ 40V, 100kHz to 1MHz Programmable Operating Frequency, 5mm × 6mm QFN Package
LT3958	Boost, Flyback, SEPIC and Inverting Converter with 3.3A, 84V Switch	5V ≤ V_{IN} ≤ 80V, 100kHz to 1MHz Programmable Operating Frequency, 5mm × 6mm QFN Package
LT3959	Boost, SEPIC and Inverting Converter with 6A, 40V Switch	1.6V ≤ V_{IN} ≤ 40V, 100kHz to 1MHz Programmable Operating Frequency, 5mm × 6mm QFN Package
LTC3786	Low I_Q Synchronous Step-Up Controller	4.5V (Down to 2.5V After Start-Up) ≤ V_{IN} ≤ 38V, V_{OUT} Up to 60V, 55µA Quiescent Current, 3mm × 3mm QFN-16, MSOP-16E

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