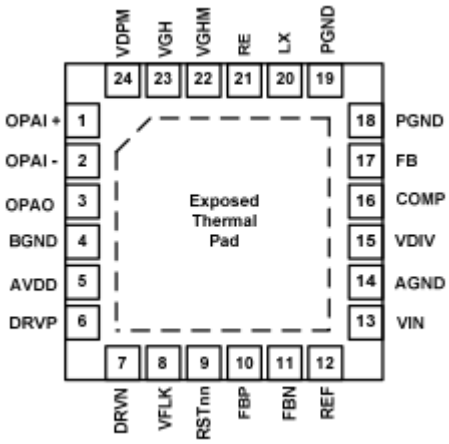
General Description

The EC9232 is an integrated power supply solution optimized for small to medium size thin-film transistor (TFT) liquid crystal displays (LCD's). The boost converter operates at the frequency of 1.2MHz. The integrated N channel FET has a typical current limit of 3.0A and can support output voltages up to 20V. The gate-on and gate-off charge pumps provide regulated TFT-LCD gate-on and gate-off supplies. Both outputs can be adjusted by external resistive voltage-dividers. The GPM is a flicker compensation circuit to reduce the coupling effect of gate lines; the gate-shaping timing is controlled by the timing-controller to modulate the Gate-On voltage, VGHM. It also can delay the Gate-On voltage during power-on to achieve a correct power-on sequence for gate driver ICs. Both the power-on delay time and the falling time of the Gate-On voltage are programmable by external capacitor and resistor. The integrated operational amplifier is typically used for LCD VCOM driving; the output can sink or source up to 350mA short-circuit current. This operational amplifier features fast slew rate (40V/us), wide bandwidth (20MHz), and rail-to-rail outputs as well. A built-in voltage detector generates a reset signal when the input voltage drops below a specified level. The reset signal is active low, and the detecting level is decided by an external resistor divider. The EC9232 is available in a thin 24-pin 4x4 mm VQFN green package.

Features

- 2.5V to 5.5V input supply
- Current-mode boost regulator
  - 1.2MHz switching frequency
  - Integrated 20V/3.0A 160mΩ FET
  - Fast transient response to pulsed load
  - High efficiency up to 90%
  - Adjustable high-accuracy output voltage(±1%)
  - Over current protection
  - Over voltage protection
- VGH positive charge pump controller
- VGL negative charge pump controller
- Integrated high performance operational amplifier
  - ±350mA output short-circuit current
  - 40V/us fast slew rate
  - 20MHz Bandwidth
  - rail-to-rail output
- Low-voltage detection circuit
- GPM controller
  - Adjustable falling time
  - Adjustable delay
- Thermal shutdown
- Thin 4x4 mm 24-lead VQFN package

VQFN-24 Pin Configuration



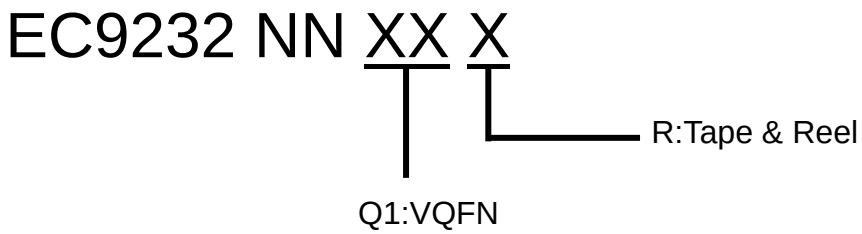
Applications

- TFT LCD for Notebooks
- TFT LCD for Monitors
- Car Navigation Display
- Portable equipment

Pin Description

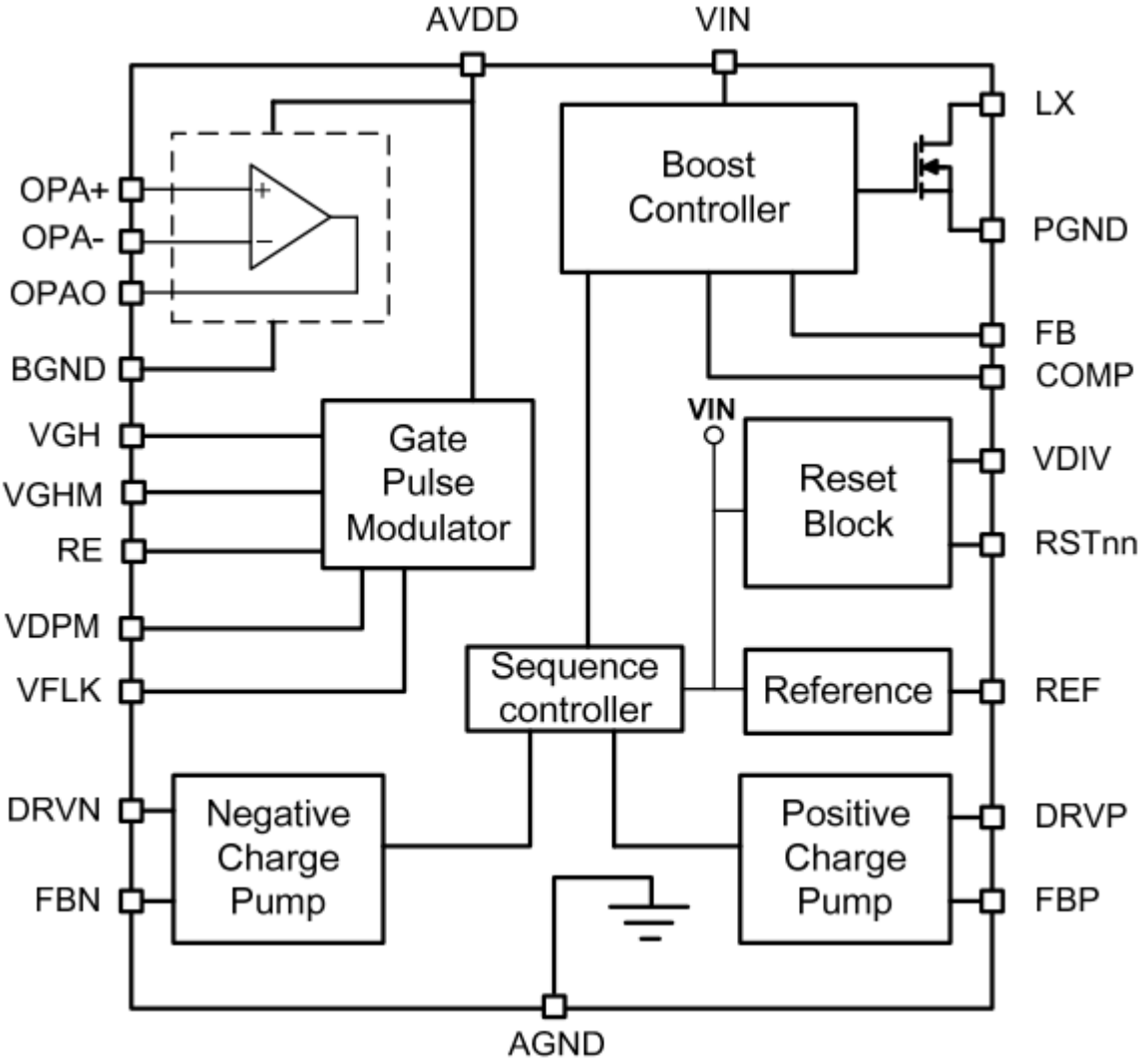
Number	Name	Pin Description
1	OPA+	Operational amplifier non-inverting input.
2	OPA-	Operational amplifier inverting input.
3	OPAO	Operational amplifier output.
4	BGND	Ground for operational amplifier and charge pumps.
5	AVDD	Charge pump supply and operational amplifier supply.
6	DRVP	Positive charge pump driving output.
7	DRVN	Negative charge pump driving output.
8	VFLK	Timing control pin for charging or discharging VGHM.
9	RSTnn	Voltage detector output for reset, active low. RSTnn is an open-drain output.
10	FBP	Positive charge pump feedback sense input.
11	FBN	Negative charge pump feedback sense input.
12	REF	Reference output. All power outputs are disabled until REF exceeds its UVLO
13	VIN	Supply for PWM, reference and other circuits.
14	AGND	Analog ground.
15	VDIV	Voltage detector divider input.
16	COMP	Boost converter error amplifier compensation node.
17	FB	Boost converter feedback voltage sense input.
18,19	PGND	Boost converter power ground (source of the internal NMOS switch).
20	LX	Boost converter switching node (drain of the internal NMOS switch).
21	RE	Switch input to discharge VGHM.
22	VGHM	Supply voltage for Gate Driver.
23	VGH	Input to charge VGHM.
24	VDPM	GPM startup delay input; charged with a constant 5μA current.
-	TP	Thermal Pad, connect to AGND.

Ordering Information

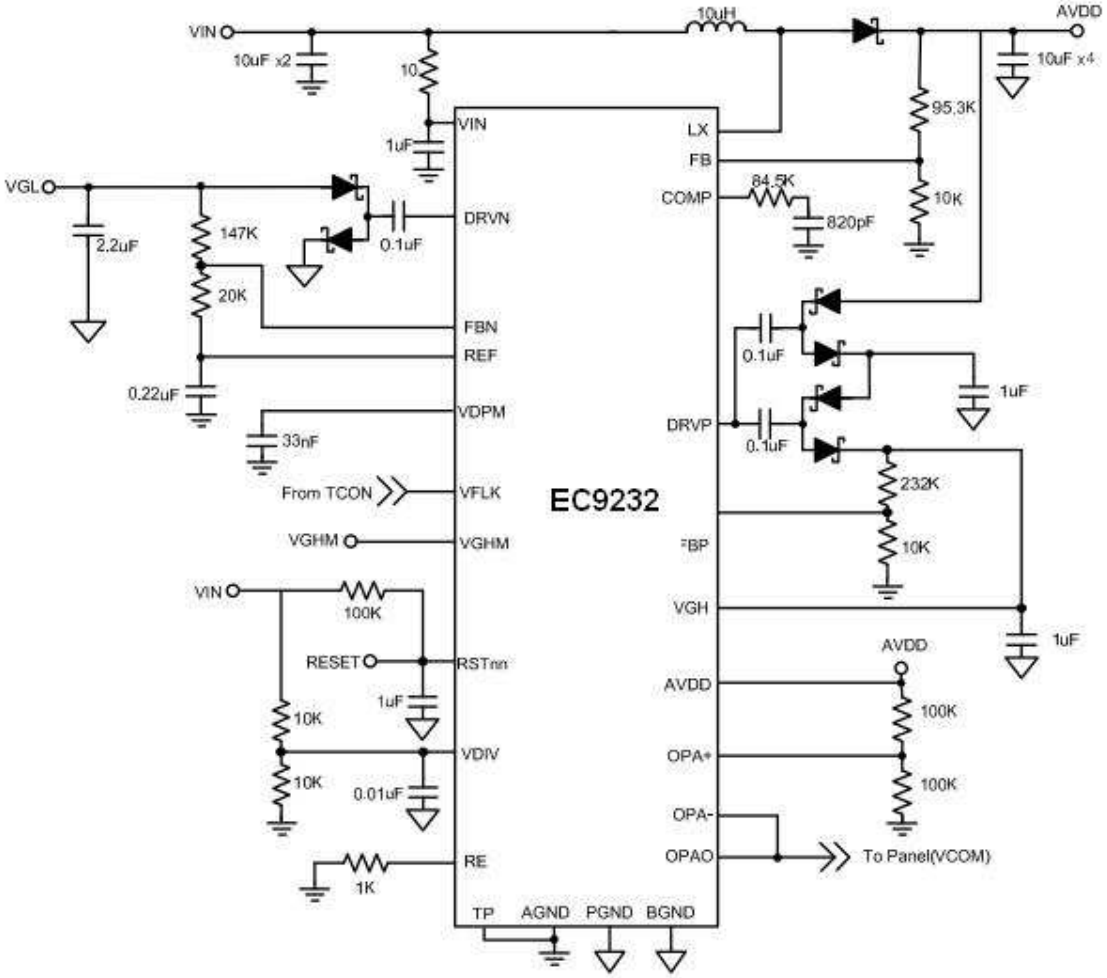


Part Number	Package	Marking	Marking Information
EC9232NNQ1R	VQFN 24L	9232 LLLLL	1. LLLLL：Lot No

Function Block Diagram



Typical Application Diagram



Absolute Maximum Ratings

Input Supply Voltage, VIN	-0.3V to 6.5V
Voltages on RSTnn, VDIV, VFLK	-0.3V to 6.5V
Voltages on AVDD, LX	-0.3V to 22V
Voltages on VGH, VGHM, RE	-0.3V to 38V
Voltages on FB, FBP, FBN, COMP, REF, VDPM	-0.3V to (VIN+0.3V)
Voltages on DRVP, DRVN, OPA+,OPA-, OPAO	-0.3V to (AVDD+0.3V)
Storage temperature range	-65℃ to 150℃
Lead temperature (soldering, 10s maximum)	260℃
ESD, Human body mode	2kV
ESD, Machine mode	200V

Note1: All voltages are referenced to ground with PGND and AGND pins grounded.
Note2: “ABSOLUTE MAXIMUM RATINGS” indicate limits beyond which permanent damage to the device may occur. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. For guaranteed specifications and test conditions, see the “ELECTRICAL SPECIFICATIONS”.

Recommended Operation Conditions

Junction temperature range	-40℃ to 125℃
Ambient temperature range	-40℃ to 85℃

Power Dissipation Ratings

Package	Thermal Resistance, Θ_{JA}	Power Rating (T_A < 25 ℃)	Power Rating (25 < T_A < 85 ℃)	Power Rating (T_A = 85℃)
24-ld QFN	44℃ /W	2.28W	(125 - T_A) / 44 W	0.9W

Electrical Specifications

(V_{IN}=5V, AV_{DD} = 13V, T_A=25℃, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
System Supply						
Input Supply Voltage	V_{IN}		2.5	--	5.5	V
VIN Under Voltage Lockout Threshol	V_{UVLO}	V_{IN} falling	2.05	2.15	2.25	V
		V_{IN} rising	2.15	2.25	2.35	V
VIN Quiescent current	I_Q	V_{FB} = 1.35V, LX no switching	--	0.6	0.9	mA
		V_{FB} = 1.15V, LX switching	--	3	4.5	mA
Thermal shutdown	T_{SHDN}		--	160	--	℃
Main Boost Regulator						
Output Voltage Range	AV_{DD}		VIN	-	18	V
FB Regulation Voltage	V_{FB}	FB=COMP,C_{COMP}=1nF	1.238	1.25	1.262	V
FB Fault Trip Level		Falling edge	0.95	1	1.05	V
FB Load Regulation		0< I_{LOAD} < full, transient only		-1		%
FB Line Regulation		V_{IN} = 2.5 to 5.5V		0.05	0.15	%/V
FB Input Bias Current		V_{FB} = 1.25V	-40	0	40	nA
FB Transconductance	G_m	ΔI=±5uA at COMP, FB = COMP		85		uA/V
FB Voltage Gain	A_V	FB to COMP		1500		V/V
LX Current Limit		V_{FB} =1.1V, duty cycle = 75%	2.5	3	3.5	A
LX On-Resistance	R_{ds_LX}	I_{LX} = 200mA		0.16		Ω
LX Leakage Current		V_{LX} = 19V, T_A = +25℃		0.01	20	uA
Current-Sense Transresistance			0.1	0.2	0.3	V/A
Soft-Start Period	T_{SS1}			14		ms
Reference						
REF OUTPUT Voltage	V_{REF}	I_{REF}=50uA	1.238	1.25	1.262	V
REF under Voltage Lockout Threshold	V_{REF_UVLO}	V_{REF} falling		0.86		
		V_{REF} rising		1.08		
REF Load Regulation	I_{REF}	0<I_{LOAD} <100uA		1	5	mV
REF Line Regulation		I_{REF} = 100uA		2	5	mV
Oscillator and Timing						
Frequency	F_{OSC}		1000	1200	1400	KHz
Oscilllator Maximum Duty Cycle	DUTY		86	90	94	%
Duration to Trigger Fault Condition		FB or FBP or FBN below	47	55	65	ms
VDPM Capacitor Charge Current	I_{DPM}	During startup V_{VDPM}	4	5	6	uA
VDPM Turn-on threshold	I_{VDPM}	During startup V_{VDPM}	1.22	1.25	1.28	v

Positive Charge-Pump Regulator						
AVDD Supply Range	V_{AVDD}		6		18	V
Operating Frequency	F_{OSC_CP}		500	600	700	KHz
FBP Regulation Voltage	V_{FBP}		1.23	1.25	1.27	V
FBP Input Bias Current	I_{FBP_BIAS}	V_{FBP} =1.5V, T_A = +25℃	-40	-	40	nA
DRVP P-Ch On-Resistance	R_{DRVPP}			3	6	Ω
DRVP N-Ch On-Resistance	R_{DRVPN}			3	6	Ω
FBP Fault Trip Level		Falling edge	0.95	1	1.05	V
Soft-Start Period	T_{SS2}			3.4		ms
Negative Charge-Pump Regulator						
AVDD Supply Range	V_{AVDD}		6		18	V
Operating Frequency	F_{OSC_CP}		500	600	700	KHz
FBN Regulation Voltage	V_{FBN}		235	250	265	mV
FBN Input Bias Current	I_{FBN_BIAS}	V_{FBN} = 0V, T_A = +25℃	-40	-	40	nA
DRVN P-Ch On-Resistance	R_{DRVNP}			3	6	Ω
DRVN N-Ch On-Resistance	R_{DRVNN}			3	6	Ω
FBN Fault Trip Level		Rising edge	0.4	0.45	0.5	V
Soft-Start Period	T_{SS3}			3.4		ms
Operational Amplifier						
AVDD Supply Range	V_{AVDD}		6		18	V
V_{AVDD} Overvoltage Threshold	V_{OVP}		19	20	21	V
AVDD Under Voltage Lockout Threshold	V_{AVDD_UVLO}		3.8	4	4.2	V
AVDD Supply Current	I_{AVDD}	Buffer configuration, V_{OPA+}=V_{AVDD}/2,no load		2		mA
Input Offset Voltage	V_{OS}	V_{OPA-}, V_{OPA+}=V_{AVDD}/2, T_A = +25℃		2	15	mV
Input Bias Current	I_{BIAS}	V_{OPA-}, V_{OPA+}=V_{AVDD}/2, T_A = +25℃	-40		40	nA
Input Common-Mode Voltage Range			0		VAVDD	V
Output-Voltage-Swing High	VOH	Buffer configuration, OPAO I_{OUT} =25 mA	V_{AVDD} - 350			mV
Output-Voltage-Swing Low	VOL	Buffer configuration, OPAO I_{OUT} = -25μA			350	mV
Slew Rate	SR	V_{OUT}20% to 80% with CL=10pF, RL=10k		40		V/us
-3dB Bandwidth	BW	CL=10pF, RL=10k		40		MHz
Short-Circuit Current	ISCC	V_{OPA+}=V_{AVDD}/2 , short output to BGND (sourcing)		350		mA
		V_{OPA+}=V_{AVDD}/2 , short output to AVDD (sinking)		350		mA

Settling Time	Tsetling	Buffer configuration, V_{OPA+}=5.5V to7.5V,with No output loading		220		ns
Reset Control						
VDIV Threshold	V_{DIV}	Falling edge at VIN=5V	1.225	1.25	1.275	V
		Falling edge at VIN=1.8V	1.213	1.25	1.287	
VDIV Input current		TA=+25℃	-40	0	40	nA
VDIV Hysteresis	△ V_{DIV}			50		mV
RSTnn Output Voltage	V_{RST}	I_{SINK} = 1mA			0.2	V
Reset Blanking Time	T_{BLK}			163		ms
GPM Control						
VGH Input Voltage Range	V_{VGH}				36	V
VGH Input Current	I_{VGH}	VDPM=1.5V,VFLK=HIGH			600	uA
		VDPM=1.5V,VFLK=LOW			300	
VFLK Input Low Voltage	V_{IL}				0.6	V
VFLK Input high Voltage	V_{IH}		2			V
VFLK Input Current		VFLK Input Current	-40		40	nA
Propagation Delay of VFLK to VGHM rising	Tdelay	VGH=25V		100		ns
VGH to VGHM Switch on Resistance	Rds_high	VDM=1.5V,VFLK=HIGH		15	30	Ω
RE to VGM Switch on Resistance	Rds_low	VDM=1.5V,VFLK=LOW		30	60	Ω
VGHM-to –GND Pull-down Resistance	R_{VGHM}	VDPM=0V		2.5		KΩ

Application Information

The EC9232 offers an all-in-one solution for TFT LCD. The chip includes a high-efficiency boost converter with a 20V/3A on-chip N-channel transistor for biasing of the LCD, a regulated positive charge pump, a regulated negative charge pump, a VCOM buffer and a gate pulse modulation circuit. A voltage detector circuit generates a reset signal when the input voltage falls below the preset threshold.

TFT LCD Boost Converter (AVDD)

The LCD panel AVDD supply is generated from a high-efficiency PWM boost converter operating with current mode control, and the switching frequency is 1.2MHz. During the on-period, TON, the synchronous FET connects one end of the inductor to ground, therefore increasing the inductor current. After the FET turns off, the inductor switching node, LX, is charged to a positive voltage by the inductor current. The freewheeling diode turns on and the inductor current flows to the output capacitor. The converter operates in the continuous conduction mode (CCM) when the average input current IIN is at least one-half of the inductor peak- to-peak ripple current, ΔI_{LPP}.

$$I_{IN} \geq \frac{\Delta I_{LPP}}{2}$$

$$\Delta I_{LPP} = \frac{(AVDD - V_{IN}) \times V_{IN}}{L \times F_{OSC} \times AVDD}$$

The output voltage, AVDD, is determined by the duty cycle, D, of the power FET on-time and the input voltage, V_{IN}.

$$AVDD = \frac{V_{IN}}{1 - D}$$

The average load current, I_{LOAD}, can be calculated from the power conservation law.

$$\eta \times V_{IN} \times I_{IN} = AVDD \times I_{LOAD}$$

where η is the power conversion efficiency. For a lower load current, the inductor current would decay to zero during the free-wheeling period and the output node would be disconnected from the inductor for the remaining portion of the switching period. The converter would operate in the discontinuous conduction mode (DCM). Current mode control is well known for its robustness and fast transient response. An inner current feedback loop sets the on-time and the duty cycle such that the current through the inductor equals to the current computed by the compensator. This loop acts within one switching cycle. A slope compensation ramp is added to suppress sub-harmonic oscillations. An outer voltage feedback loop subtracts the voltage on the FB pin from the internal reference voltage and feeds the difference to the compensator operational transconductance (Gm) amplifier. This amplifier is compensated by an external R-C network to allow the user to optimize the transient response and loop stability for the specific application conditions.

Compensator Selection

This current mode boost converter has a current sense loop and a voltage feedback loop. The current sense loop does not need any compensation. The voltage feedback loop is compensated by an external series R-C network R_{COMP} and C_{COMP} from COMP pin to ground. R_{COMP} sets the high-frequency loop gain and the unity gain bandwidth of the loop which determines the transient response. C_{COMP} together with R_{COMP} determine the phase margin which relates to loop stability.

Users can adjust R_{COMP} and C_{COMP} by the following equations to reach fast transient response and better regulation.

$$R_{COMP} \cong \frac{312.5 \times V_{IN} \times V_{BOOST} \times C_{OUT}}{L_{BOOST} \times I_{BOOST}}$$

$$C_{COMP} \cong \frac{V_{BOOST} \times C_{OUT}}{10 \times I_{BOOST} \times R_{COMP}}$$

For example, when V_{IN}=5V, V_{BOOST}=13.2V, C_{OUT}=40uF, L_{BOOST}=10uH, I_{BOOST}=1A, we put 84.5k for R_{COMP} and 820pF for C_{COMP} in Typical Application Diagram.

Output Capacitor Selection

The output voltage ripple due to converter switching is determined by the output capacitor total capacitance, C_{OUT}, and the output capacitor total effective series resistance, ESR.

$$AVDD_{RIPPLE} = \frac{D \times I_{LOAD}}{F_{OSC} \times C_{OUT}} + I_{PK} \times ESR$$

$$I_{PK} = I_{IN} + \frac{\Delta I_{LPP}}{2}$$

The first ripple component can be reduced by increasing C_{OUT} since FOSC is fixed 1.2MHz(typical). Changing C_{OUT} may require adjustment of compensation R and C in order to provide adequate phase margin and loop bandwidth. The second ripple component can be reduced by selecting low-ESR ceramic capacitors and using several smaller capacitors in parallel instead of just one large capacitor.

Inductor Selection

To prevent magnetic saturation of the inductor core the inductor has to be rated for a maximum current larger than I_{PK} in a given application. Since the chip provides current limit protection of 3A (typ) it is generally recommended that the inductor be rated at least for 3A.

Selection of the inductor requires trade-off between the physical size (footprint x height) and its electrical properties (current rating, inductance, resistance). Within a given footprint and height, an inductor with larger inductance typically comes with lower current rating and often larger series resistance. Larger inductance typically requires more turns on the winding, a smaller core gap or a core material with a larger relative permeability. An inductor with a larger physical size has better electrical properties than a smaller inductor.

It is desirable to reduce the ripple current I_{LPP} in order to reduce voltage noise on the input and output capacitors. In practice, the inductor is often much larger than the capacitors and it is easier and cheaper to increase the size of the capacitors. The ripple current I_{LPP} is then chosen the largest possible while at the same time not degrading the maximum input and output current that the converter can operate with before reaching the current limit of the chip or the rated current of the inductor.

$$I_{PK} = I_{IN} + \frac{\Delta I_{LPP}}{2} \le I_{MAX}$$

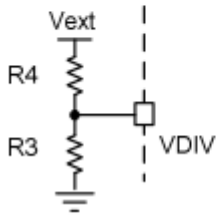
For example, I_{LPP} could be set to 20% of I_{MAX}.

Voltage Detector Circuit

During power-up, once V_{IN} exceeds V_{UVLO} (2.25V typical), the controller initiates a 163ms blanking period during which the input voltage at V_{DIV} is ignored and the RSTnn pin is floated to high impedance. An external pull up resistor should pull RSTnn high. After this blanking period, the V_{DIV} function is enabled, with RSTnn driven low if V_{DIV} falls below V_{DIV}, or floated high if V_{DIV} rises above V_{DIV}.To the external voltage Vext, the rising and falling detection thresholds V_{DET},High and V_{DET},Low, respectively are set by the external voltage divider R3, R4.

$$V_{DET,High} = \frac{R_4 + R_3}{R_3}(V_{DIV} + \Delta V_{DIV})$$

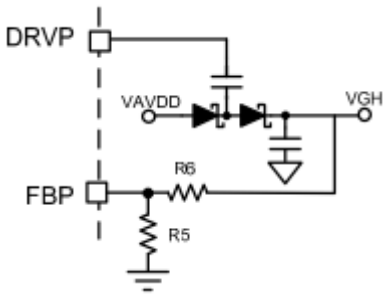
$$V_{DET,Low} = \frac{R_4 + R_3}{R_3} V_{DIV}$$



Positive Charge Pump (VGH)

The positive charge pump is used to generate the TFT LCD gate on voltage. The output voltage, VGH, can be set by an external resistive divider. Voltage VFBP is typically 1.25V. A single stage charge pump can produce an output voltage less than approximately twice the charge pump input voltage AVDD. The maximum voltage VGH should not exceed 36V if it is used to supply the GPM circuit. The output voltage VGH is regulated as the following equation.

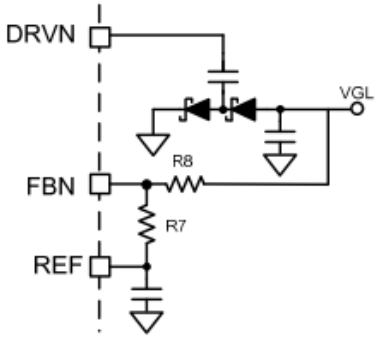
$$VGH = V_{FBP} \times \frac{R5 + R6}{R5}$$



Negative Charge Pump (VGL)

The negative charge pump is used to generate the TFT LCD gate off voltage. The output voltage, VGL, is set with an external resistive divider from its output to REF with the midpoint connected to FBN. The error amplifier compares the feedback signal from FBN with an internal reference 250mV. The output voltage VGL is regulated as the following equation.

$$VGL = V_{FBN} - \frac{R8}{R7}(V_{REF} - V_{FBN})$$



Gate-pulse modulator (GPM)

The GPM is a flicker compensation circuit to reduce the coupling effect of gate lines, and is controlled by timing controller to modulate VGHM, the Gate-On voltage. This block is not activated until the below 3 conditions are satisfied:

1) The input voltage exceeds its UVLO,

2) No fault condition is detected, and 3) V_{DPM} exceeds its turn-on threshold. Once GPM activates and V_{FLK} is high, the internal switch between V_{GH} and V_{GHM} turns on and the switch between V_{GHM} and RE turns off. If V_{FLK} is low, the internal switch between V_{GH} and V_{GHM} turns off and the switch between V_{GHM} and RE turns on. At that time, the falling time and delay time of the Gate-On voltage are programmable by an external resistor connected between RE and GND.

Operational Amplifier

The operational amplifier is typically used for LCD V_{COM} buffer. The V_{COM} buffer generates the bias supply for the back plane of an LCD screen which is capacitively coupled to the pixel drive voltage. The purpose of the V_{COM} buffer is to hold the bias voltage steady while pixel voltage changes dynamically. The buffer is designed to sustain up to ±350mA of output short-circuit current. In transients, it can deliver up to 350mA at which point the over current protection circuit limits the output current. Excessive current draw over a period of time may cause the chip temperature to rise and set off the over temperature protection circuit.

Soft-Start Function

The IC employs a internal soft-start function to minimize inrush current and voltage overshoot, and ensure a well-defined startup behaviour. The soft-start time of the boost controller is 14ms (typ), and the soft-start time of positive and negative charge pump is 3.4ms (typ).

Under Voltage Protection

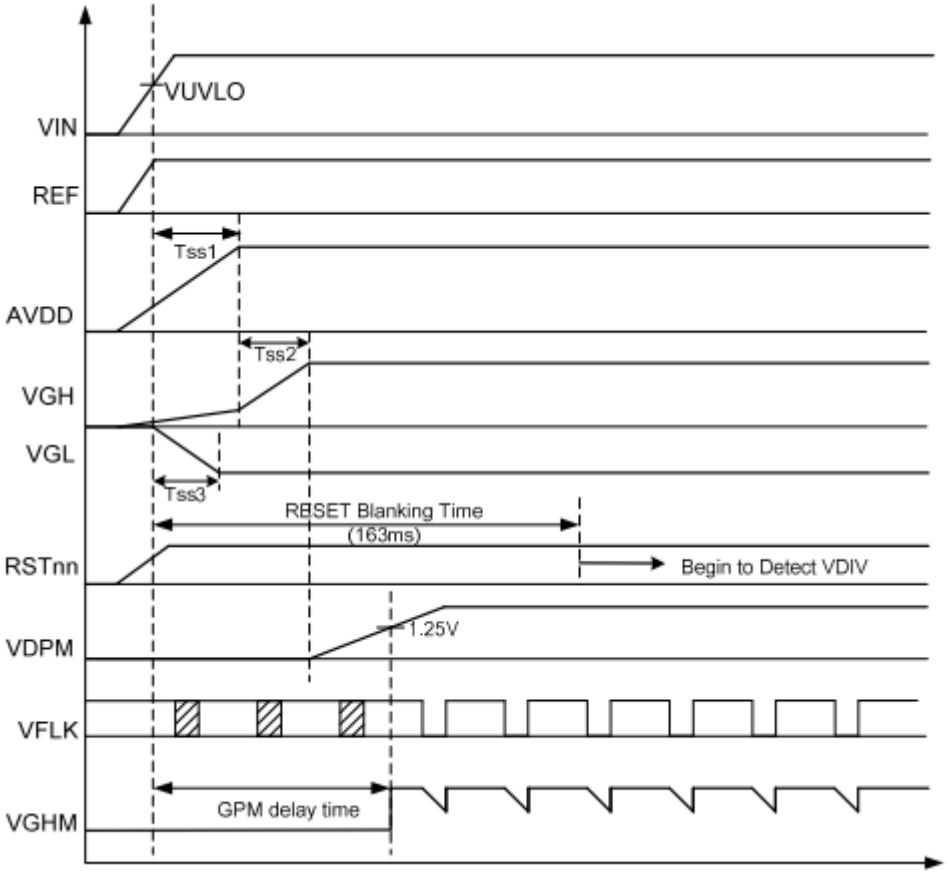
During steady-state operation, if the feedback voltage pin FB is below 1V of the nominal value, the EC9232 activates an internal fault timer. If any condition indicates a continuous fault for the fault timer duration (55ms typ), the IC sets the fault latch to shut down all its outputs except the reference. Once the fault condition is removed, cycle the VIN (below the UVLO falling threshold) to clear the fault latch and reactivate the device.
The fault-detection circuit is disabled during the soft-start ramp.

The positive and negative charge pump controller also provide the under voltage protection function during steady-state operation. If F_{BP} voltage is lower than 1V (typ) or F_{BN} voltage is higher than 0.45V (typ), and the fault duration is over 55ms (typ), the IC sets the fault latch to shut down all its outputs as well.

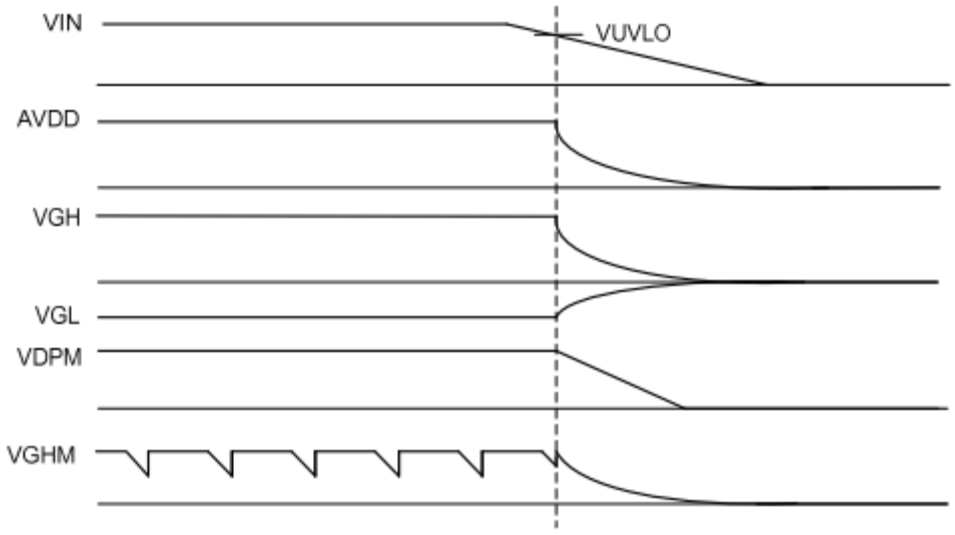
Thermal-Overload Protection

The EC9232 provides a Thermal-Overload Protection to prevents excessive power dissipation from overheating the IC. When the junction temperature exceeds TJ = 160℃, a thermal sensor activates the fault protect ion, which shuts down all outputs except the reference. To resume normal function, the temperature must cool down by 15℃ and cycle the IC power to clear the fault l atch.

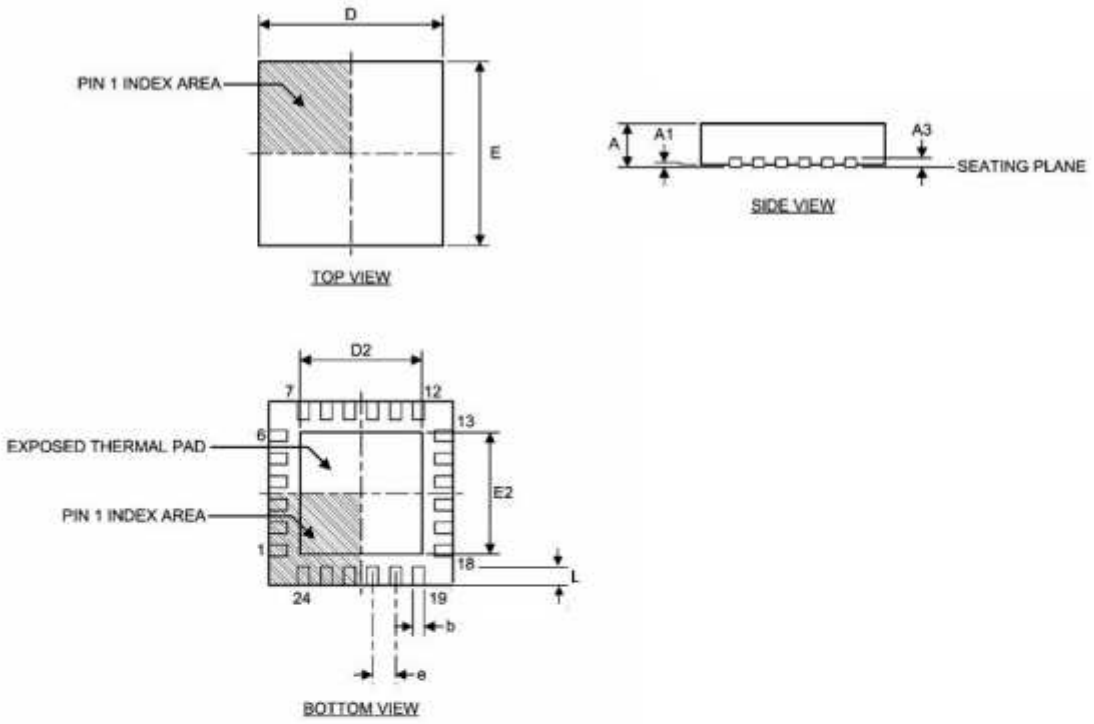
Startup Sequence



Power-off Sequence



Package Outline Drawing (VQFN-24 4x4 mm)



DIMENSION	MIN (mm)	MAX (mm)
A	0.80	1.00
A1	0	0.05
A3	0.20 REF	
b	0.18	0.30
D	4.00 BSC	
D2	2.40	2.75
E	4.00 BSC	
E2	2.40	2.75
e	0.50 BSC	
L	0.35	0.45

Notes:
1) All dimensions are in millimeters.
2) Dimensions comply with JEDEC MO-220K, VGGD-6.