3.5A-Capable, Slew-Rate-Controlled Load Switch with True Reverse Current Blocking

Features

- **Input Voltage Operating Range:1.5V to 5.5V**
- **Typical $R_{DS(ON)}$**
  - **– 21mΩ at V_{IN} =5.5V**
  - **– 23mΩ at V_{IN} =4.5V**
  - **– 41mΩ at V_{IN} =1.8V**
  - **– 90mΩ at V_{IN} =1.5V**
- **Slew Rate/Inrush Control with t_R = 1.8ms(Typ)**
- **3.5A Maximum Continuous Current Capability**
- **Low Off Switch Current <1mA**
- **True Reverse Current Blocking(TRCB)**
- **Logic CMOS IO Meets JESD76 Standard for GPIO Interface and Related Power Supply Requirements**
- **ESD Protected**
  - **– Human Body Model >8kV**
  - **– Charged Device Model >1.5kV**
  - **– IEC 61000-4-2 Air Discharge >15kV**
  - **– IEC 61000-4-2 Contact Discharge >8kV**
- **Tiny small WLCSP1.2x0.8-6 and VTDFN1.6x1.2-4 Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

General Description

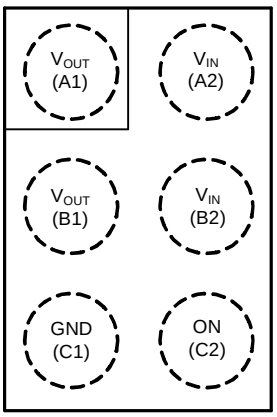
The APL3222 advanced load management switch targets applications requiring a highly integrated solution. It disconnects loads powered from the DC power rail (<6V) with stringent off-state current targets and high load capacitances (up to 100µF). The APL3222 consists of slew-rate controlled low-impedance MOSFET switch (23mΩ typical) and integrated analog features. The slew-rate controlled turn-on characteristic prevents inrush current and the resulting excessive voltage droop on power rails. The APL3222 has a True Reverse Current Blocking (TRCB) function that obstructs unwanted reverse current from VOUT to VIN during both ON and OFF states.

The exceptionally low off-state current drain (<1µA maximum) facilitates compliance with standby power requirements. The input voltage range operates from 1.5V to 5.5V_{DC} to support a wide range of applications in consumer, optical, medical, storage, portable, and industrial device power management. Switch control is managed by a logic input (active HIGH) capable of interfacing directly with low-voltage control signal / General-Purpose Input / Output (GPIO) without an external pull-down resistor.

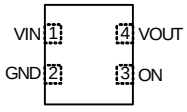
The device is packaged in advanced, fully "green" compliant, 1.2mm x 0.8mm, Wafer-Level Chip-Scale Package (WLCSP) with backside lamination.

Pin Configuration

Top View



WLCSP1.2x0.8-6



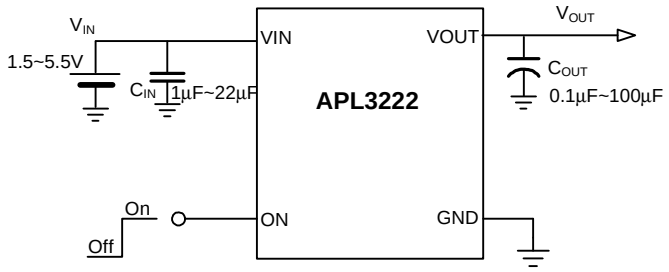
VTDFN-1.6x1.2
(Top View)

Applications

- **Smart Phones**
- **Tablets PCs**
- **Portable Devices**

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Simplified Application Circuit



Ordering and Marking Information

APL3222 □□□ — □□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

Package Code
HA : WLCSP1.2x0.8-6 QF : VTDFN1.6x1.2-4
Operating Junction Temperature
I : - 40 to 85 C
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device

APL3222 HA:	2X	X - Date Code
APL3222 QF:	L2 X	X - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{IN}	VIN to GND Voltage	-2 ~ 7	V
V_{OUT}	VOUT to GND Voltage	-2 ~ 7	V
V_{ON}	ON to GND Voltage	-2 ~ 7	V
I_{SW}	Maximum Continuous Switch Current	0 ~ 3.5	A
T_J	Maximum Junction Temperature	-40 ~ 150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)	260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance in free air (Note 2)		°C/W
	WLCSP1.2X0.8-6	TBD	
	VTDFN1.6x1.2-4	100	
θ_{JC}	Junction-to-Case Thermal Resistance in free air (Note 2)		°C/W
	WLCSP1.2X0.8-6	TBD	
	VTDFN1.6x1.2-4	TBD	

Note 2 : θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note3)

Symbol	Parameter	Range	Unit
V_{IN}	VIN Input Voltage	1.5 ~ 5.5	V
I_{SW}	Continuous Switch Current	0 ~ 3.5	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3 : Refer to the typical application circuit

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}= 1.5~5.5V,T_A= -40~85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL3222			Unit
			Min	Typ	Max	
Basic Operation						
V_{IN}	Input Voltage		1.5	-	5.5	V
$I_{Q(OFF)}$	Off Supply Current	V_{ON}=GND, V_{OUT}=Open	-	-	1	µA
I_{SD}	Shutdown Current	V_{ON}=GND, V_{OUT}=GND,T_A=-40 to +85 °C	-	0.2	3.6	µA
I_Q	Quiescent Current	I_{OUT}=0mA	-	-	20	µA
R_{ON}	On Resistance	V_{IN}=5.5V, I_{OUT}=3A	-	22	-	mΩ
		V_{IN}=5.5V, I_{OUT}=2A	-	21.5	-	
		V_{IN}=5.5V, I_{OUT}=1A, T_A=25 °C	-	21.0	28.0	
		V_{IN}=4.5V, I_{OUT}=3A	-	24.0	-	
		V_{IN}=4.5V, I_{OUT}=2A	-	23.5	-	
		V_{IN}=4.5V, I_{OUT}=1A, T_A=25 °C	-	23.0	30.0	
		V_{IN}=3.3V, I_{OUT}=500mA, T_A=25 °C	-	26.0	-	
		V_{IN}=2.5V, I_{OUT}=500mA, T_A=25 °C	-	30.0	-	
		V_{IN}=1.8V, I_{OUT}=250mA, T_A=25 °C	-	41.0	-	
		V_{IN}=1.5V, I_{OUT}=250mA, T_A=25 °C	-	90.0	110.0	
V_{IH}	ON Input Logic High Voltage	V_{IN}=1.5V to 5.5V	0.9	-	-	V
V_{IL}	ON Input Logic Low Voltage	V_{IN}=1.8V to 5.5V	-	-	0.55	V
		V_{IN}=1.5V to 1.8V	-	-	0.26	
I_{ON}	ON Input Leakage	V_{ON}= V_{IN} or GND	-	-	4.3	µA
R_{ON_PD}	Pull-Down Resistance at ON Pin	V_{IN}= V_{ON} = 1.5V to 5.5V, T_A=-40 to +85 °C	1.29	1.3	1.61	MΩ

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Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}= 1.5~5.5V,T_A= -40~85°C. Typical values are at T_A=25°C.

Symbol	Parameter	Test Conditions	APL3222			Unit
			Min	Typ	Max	
True Reverse Current Blocking						
V_{T_RCB}	RCB Protection Trip Point	V_{OUT} - V_{IN}	-	55	-	mV
V_{R_RCB}	RCB Protection Release Trip Point	V_{IN} - V_{OUT}	-	30	-	mV
	RCB Hysteresis		-	85	-	mV
I_{SD_OUT}	V_{OUT} Shutdown Current	V_{ON} = 0V, V_{OUT} = 5.5V, V_{IN} = Short to GND	-	-	2	µA
t_{RCB_ON}	RCB Response Time, Device ON	V_{OUT} - V_{IN}=100mV, V_{ON} = High	-	0.7	-	µs
t_{RCB_OFF}	RCB Response Time, Device OFF	V_{OUT} - V_{IN}=100mV, V_{ON} = Low	-	0.7	-	µs
Dynamic Characteristics						
t_{ON}	Turn-On Time	V_{IN}=3.3V, R_L=5Ω, C_L=150µF, T_A=25 °C	1	1.8	2.5	ms
t_{DOFF}	Turn-Off Delay	V_{IN}=4.5V, R_L=150Ω, C_L=100µF, T_A=25 °C	-	2.5	-	
t_F	V_{OUT} Fall Time		-	34	-	
t_{OFF}	Turn-Off Time		-	36.5	-	

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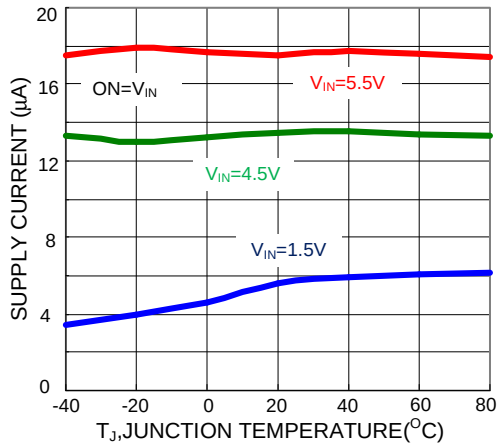
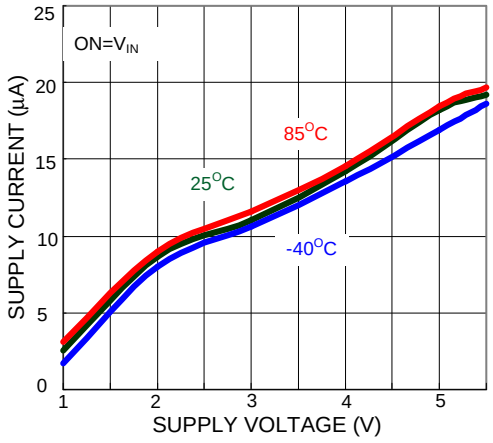
Typical Operating Characteristics

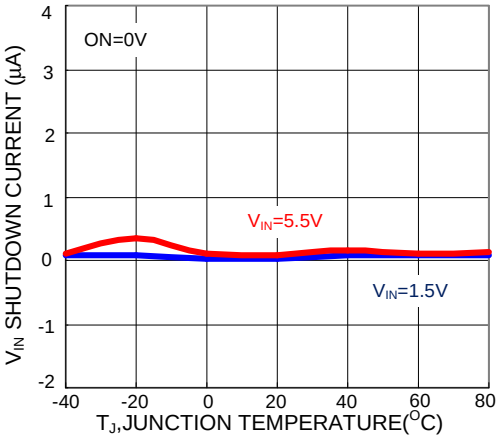
Quiescent Current



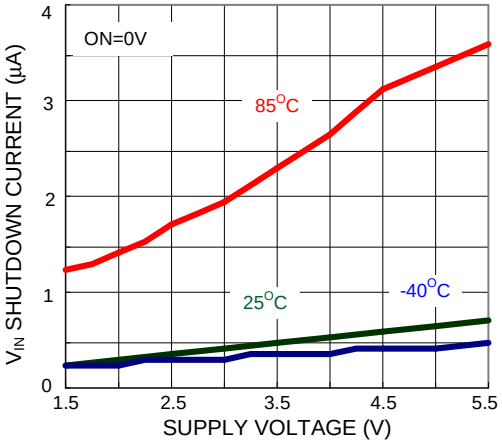
Quiescent Current



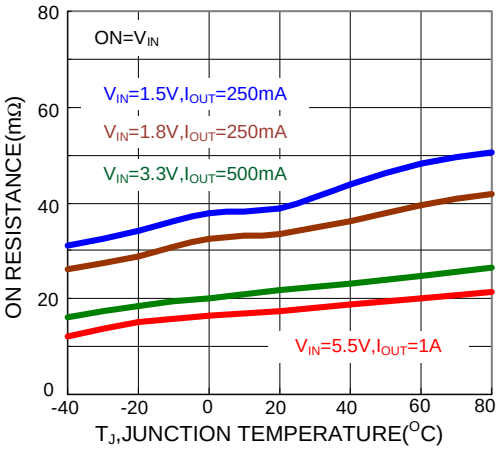
Shutdown Current



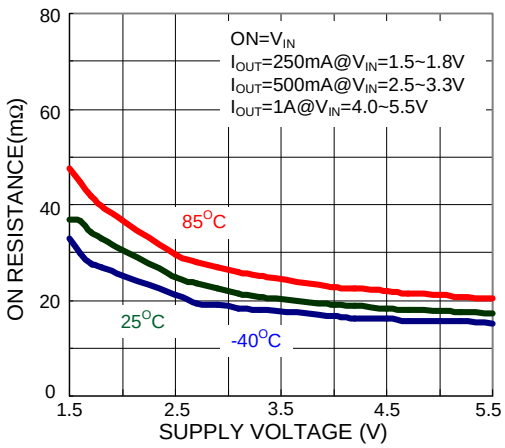
Shutdown Current



On Resistance



On Resistance



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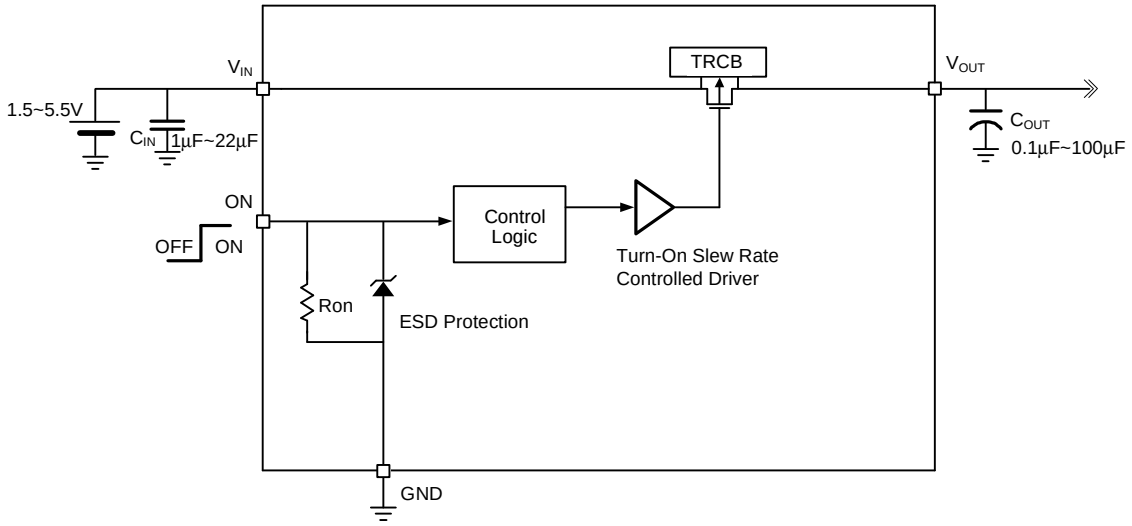
Pin Description

PIN			Function
VTDFN1.6x1.2-4	WLCSP1.2x0.8-6	NAME	
4	A1,B1	V_{OUT}	Switch Output.
1	A2,B2	V_{IN}	Supply Input: Input to the Power Switch.
2	C1	GND	Ground.
3	C2	ON	ON/OFF Control, Active High, GPIO Compatible.

Block Diagram / Typical Application Circuit



Application Information

The APL3222 is a low-RON P-channel load switch with controlled turn-on and True Reverse Current Blocking (TRCB). The core is a 23mΩ P-channel MOSFET and controller capable of functioning over a wide input operating range of 1.5 to 5.5V. The ON pin, an active-HIGH, GPIO/CMOS-compatible input; controls the state of the switch. TRCB functionality blocks unwanted reverse current during both ON and OFF states when higher VOUT than VIN is applied.

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush current when the switch turns on into a discharged load capacitor; a capacitor must be placed between the VIN and GND pins. At least 1μF ceramic capacitor, CIN, placed close to the pins is usually sufficient. Higher-value CIN can be used to reduce the voltage drop in higher-current applications.

Inrush Current

Inrush current occurs when the device is turned on. Inrush current is dependent on output capacitance and slew rate control capability, as expressed by:

$$I_{INRUSH} = C_{OUT} \times \frac{V_{IN} - V_{INITIAL}}{t_R} + I_{LOAD} \quad .....(1)$$

where:
COUT: Output capacitance;
tR: Slew rate or rise time at VOUT;
VIN: Input voltage;
VINITIAL: Initial voltage at COUT, usually GND; and
ILOAD: Load current.
Higher inrush current causes higher input voltage drop, depending on the distributed input resistance and input capacitance. High inrush current can cause problems. APL3222 has a 2.7ms of slew rate capability under 4.5VIN at 1000μF of COUT and 5Ω of RL so inrush current can be minimized and no input voltage drop appears. Table 1 show the values and actual waveform with CIN=10μF, COUT=100μF, no load current.

Table1. Inrush Current by Input Voltage

V_{IN}(V)	t_R(ms)	Inrush Current(mA)	
		Measured	Calculated with 2.7ms t_R
1.5	1.62	76	56
3.3	2.03	140	122
5.0	2.33	196	185

Output Capacitor

At least 0.1μF capacitor, COUT, should be placed between the VOUT and GND pins. This capacitor prevents parasitic board inductance from forcing VOUT below GND when the switch is on.

True Reverse Current Blocking

The true reverse current blocking feature protects the input source against current flow from output to input regardless of whether the load switch is on or off.

Board Layout

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effect that parasitic trace inductance on normal and short-circuit operation. Using wide traces or large copper planes for all pins (VIN, VOUT, ON, and GND) minimizes the parasitic electrical effects and the case-to-ambient thermal impedance.

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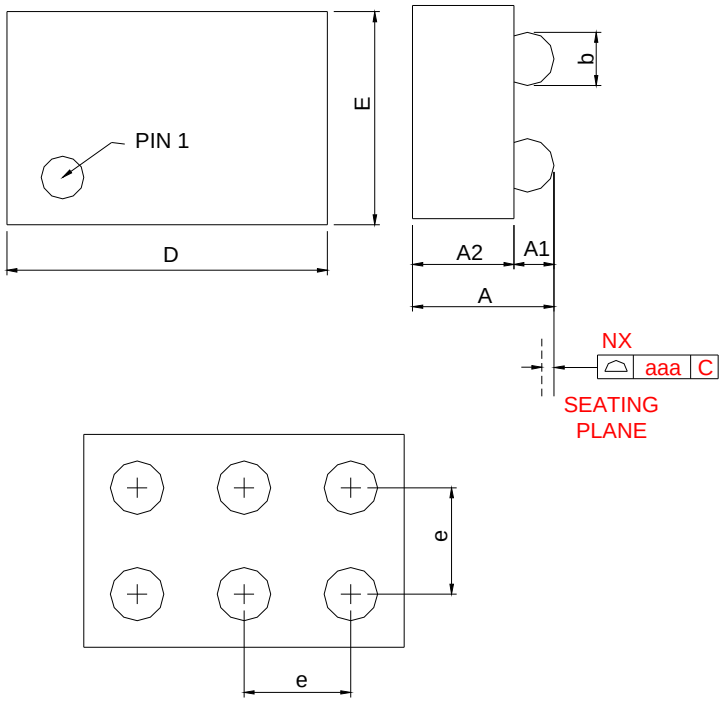
Package Information

WLCSP0.8x1.2-6



SYMBOL	WLCSP0.8x1.2-6					
	MILLIMETERS			INCHES		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.40	0.50	0.60	0.016	0.0197	0.024
A1	0.15	0.20	0.25	0.006	0.0079	0.010
b	0.23	0.26	0.29	0.009	0.0102	0.011
D	1.16	1.20	1.24	0.046	0.0472	0.049
E	0.76	0.80	0.84	0.030	0.0315	0.033
e	0.40 BSC			0.016 BSC		
aaa	0.08			0.003		

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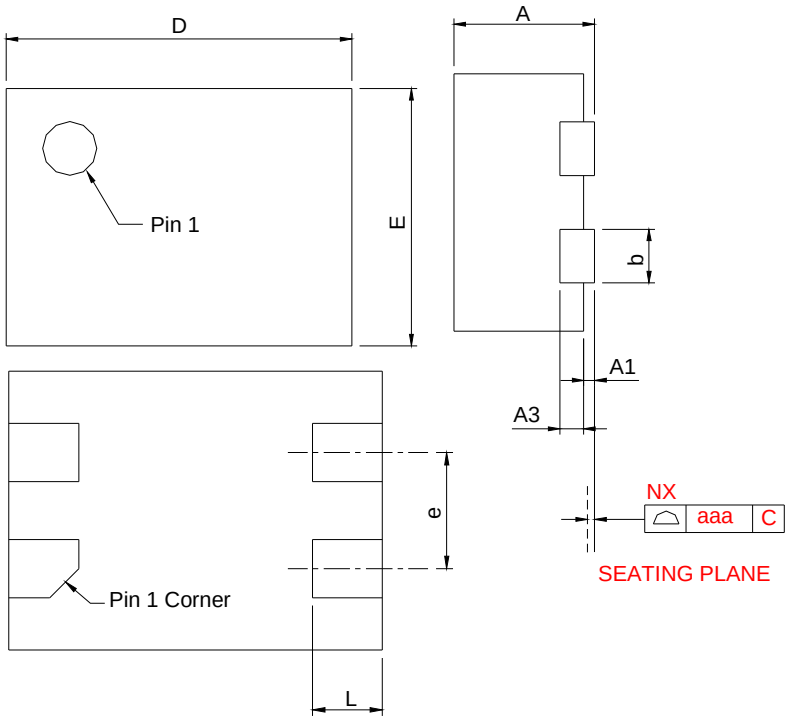
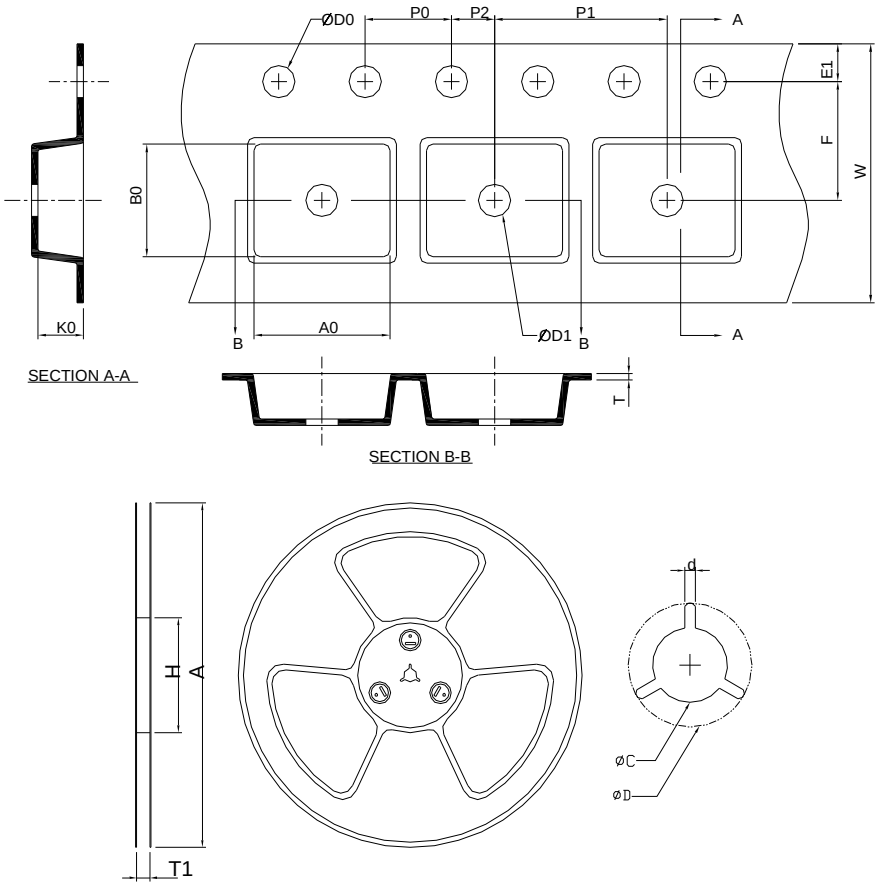
Package Information

VTDFN1.2x1.6-4



SYMBOL	VTDFN1.2x1.6-4A			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.50	0.60	0.020	0.024
A1	0.00	0.05	0.000	0.002
A3	0.11 REF		0.004 REF	
b	0.20	0.30	0.008	0.012
D	1.55	1.65	0.061	0.065
E	1.15	1.25	0.045	0.049
e	0.50 BSC		0.020 BSC	
L	0.25	0.35	0.010	0.014
aaa	0.08		0.003	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
VTDFN1.6x1.2	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.20	1.75±0.10	3.50±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.4	1.4±0.20	1.8±0.20	0.75±0.20
Application	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
WLCSP1.2X0.8	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	1.07±0.05	1.42±0.05	0.74±0.05

(mm)

Devices Per Unit

Package Type	Unit	Quantity
VTDFN1.6x1.2	Tape & Reel	3000
WLCSP1.2X0.8	Tape & Reel	3000

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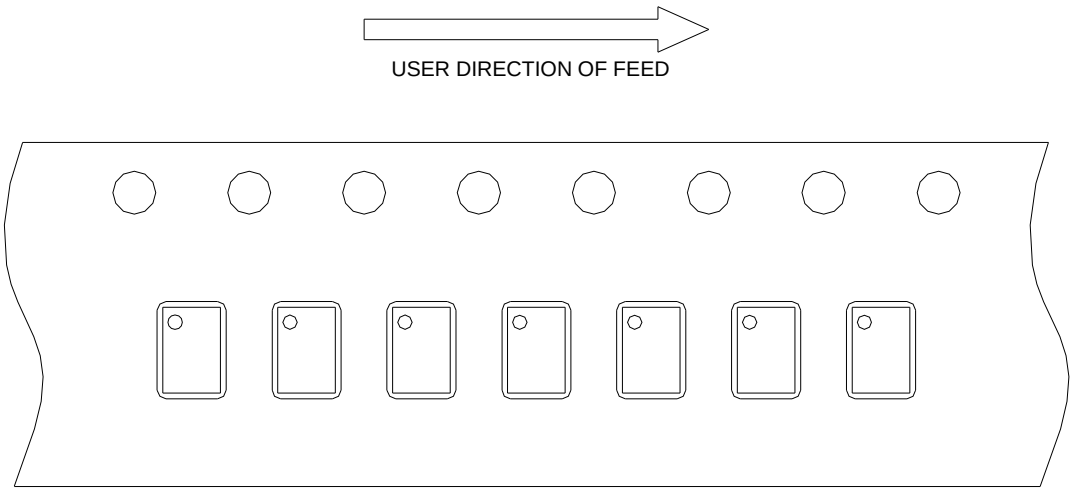
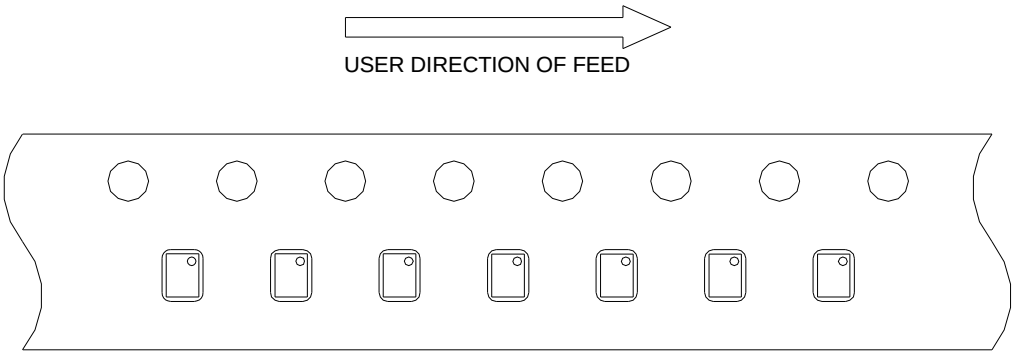
Taping Dircetion Information

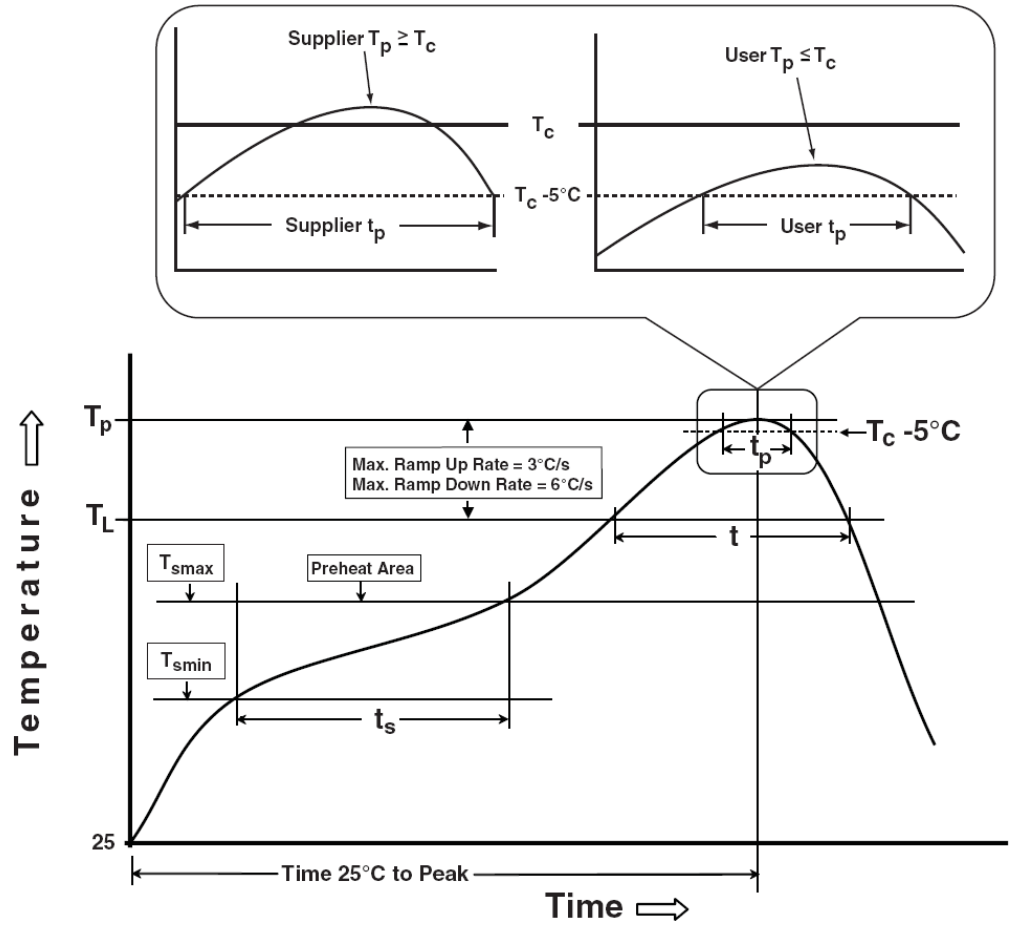
WLCSP1.2x0.8-6



VTDFN1.2x1.6-4



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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Customer Service

Anpec Electronics Corp.
Head Office :
No.6, Dusing 1st Road, SBIP,
Hsin-Chu, Taiwan
Tel : 886-3-5642000
Fax : 886-3-5642050

Taipei Branch :
2F, No. 11, Lane 218, Sec 2 Jhongsing Rd.,
Sindian City, Taipei County 23146, Taiwan
Tel : 886-2-2910-3838
Fax : 886-2-2917-3838