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RENESAS

MOS INTEGRATED CIRCUIT
μ**PD780833Y**

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD780833Y is a member of the μPD780833Y Subseries of the 78K/0 Series, and incorporates a rich lineup of peripheral hardware, including a J1850 (CLASS2) bus controller, A/D converter, timer, serial interface, and interrupt controller.

A flash memory version, the μPD78F0833Y, and various development tools are also available.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

      μ**PD780833Y Subseries User's Manual:**   **U13892E**

      78K/0 Series User's Manual Instructions: **U12326E**

FEATURES

- On-chip J1850 (CLASS2) bus controller
- On-chip ROM and RAM

Item / Part Number	Program Memory Internal ROM	Data Memory Internal High-Speed RAM	Data Memory Internal Expansion RAM	Package
μPD780833Y	60 KB	1024 bytes	2048 bytes	80-pin plastic QFP (14 $\times$ 14)

- Minimum instruction execution time can be changed from high speed (0.48 μs) to low speed (7.68 μs)
- I/O ports: 65 (N-ch open-drain: 3, TTL input/CMOS output: 8)
- 8-bit resolution A/D converter: 8 channels $\times$ 2
- Serial interface: 4 channels
- Timer: 7 channels
- Power supply voltage: V_{DD} = 4.5 to 5.5 V

APPLICATIONS

Car audios, etc.

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ORDERING INFORMATION

Part Number	Package
μPD780833YGC-×××-8BT	80-pin plastic QFP (14 × 14)

Remark ××× indicates ROM code suffix.

78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.

Products in mass production

Products under development

Y subseries products support I²C bus.
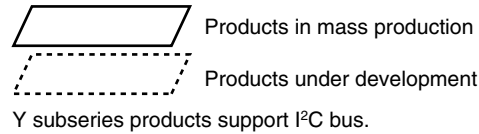
78K/0 Series

Control

100-pin	μPD78075B		EMI-noise reduced version of the μPD78078
100-pin	μPD78078	μPD78078Y	μPD78054 with added timer and enhanced external interface
100-pin	μPD78070A	μPD78070AY	ROMless version of the μPD78078
100-pin		μPD780018AY	μPD78078Y with enhanced serial I/O and limited functions
80-pin	μPD780058	μPD780058Y	μPD78054 with enhanced serial I/O
80-pin	μPD78058F	μPD78058FY	EMI-noise reduced version of the μPD78054
80-pin	μPD78054	μPD78054Y	μPD78018F with added UART and D/A converter and enhanced I/O
80-pin	μPD780065		μPD780024A with increased RAM capacity
64-pin	μPD780078	μPD780078Y	μPD780034A with added timer and enhanced serial I/O
64-pin	μPD780034A	μPD780034AY	μPD780024A with enhanced A/D converter
64-pin	μPD780024A	μPD780024AY	μPD78018F with enhanced serial I/O
64-pin	μPD78014H		EMI-noise reduced version of the μPD78018F
64-pin	μPD78018F	μPD78018FY	Basic subseries for control
42/44-pin	μPD78083		On-chip UART, capable of operating at low voltage (1.8 V)

Inverter control

64-pin	μPD780988	On-chip inverter controller and UART. Reduced EMI noise.

VFD drive

100-pin	μPD780208	μPD78044F with enhanced I/O and VFD C/D. Display output total: 53
80-pin	μPD780232	For panel control. On-chip VFD C/D. Display output total: 53
80-pin	μPD78044H	μPD78044F with added N-ch open-drain I/O. Display output total: 34
80-pin	μPD78044F	Basic subseries for driving VFD. Display output total: 34

LCD drive

120-pin	μPD780338		μPD780308 with enhanced display function and timer. Segment signal output: 40 pins max.
120-pin	μPD780328		μPD780308 with enhanced display function and timer. Segment signal output: 32 pins max.
120-pin	μPD780318		μPD780308 with enhanced display function and timer. Segment signal output: 24 pins max.
100-pin	μPD780308	μPD780308Y	μPD78064 with enhanced SIO, and increased ROM, RAM capacity
100-pin	μPD78064B		EMI-noise reduced version of the μPD78064
100-pin	μPD78064	μPD78064Y	Basic subseries for driving LCDs, on-chip UART

Bus interface supported

100-pin	μPD780948		On-chip D-CAN controller
80-pin	μPD78098B		μPD78054 with added IEBus™ controller. Reduced EMI noise.
80-pin		μPD780701Y	On-chip D-CAN/IEBus controller
80-pin		μPD780833Y	On-chip controller compliant with J1850 (CLASS2)

Meter control

100-pin	μPD780958	For industrial meter control
80-pin	μPD780852	On-chip automobile meter controller/driver
80-pin	μPD780824	For automobile meter driver. On-chip D-CAN controller

Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are the same.

The major functional differences among the subseries are shown below.

Function / Subseries Name		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-Bit	16-Bit	Watch	WDT							
Control	μPD78078Y	48 K to 60 K	4 ch	1 ch	1 ch	1 ch	8 ch	—	2 ch	3 ch (UART: 1 ch, I²C: 1 ch)	88	1.8 V	√
	μPD78070AY	—									61	2.7 V	
	μPD780018AY	48 K to 60 K							—	3 ch (I²C: 1 ch)	88		
	μPD780058Y	24 K to 60 K	2 ch						2 ch	3 ch (Time division UART: 1 ch, I²C: 1 ch)	68	1.8 V	
	μPD78058FY	48 K to 60 K								3 ch (UART: 1 ch, I²C: 1 ch)	69	2.7 V	
	μPD78054Y	16 K to 60 K										2.0 V	
	μPD780078Y	48 K to 60 K		2 ch			—	8 ch	—	4 ch (UART: 2 ch, I²C: 1 ch)	52	1.8 V	
	μPD780034AY	8 K to 32 K		1 ch						3 ch (UART: 1 ch, I²C: 1 ch)	51		
	μPD780024AY						8 ch	—					
	μPD78018FY	8 K to 60 K								2 ch (I²C: 1 ch)	53		
LCD drive	μPD780308Y	48 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	3 ch (Time division UART: 1 ch, I²C: 1 ch)	57	2.0 V	—
	μPD78064Y	16 K to 32 K								2 ch (UART: 1 ch, I²C: 1 ch)			
Bus interface supported	μPD780701Y	60 K	3 ch	2 ch	1 ch	1 ch	16 ch	—	—	4 ch (UART: 1 ch, I²C: 1 ch)	67	3.5 V	—
	μPD780833Y										65	4.5 V	

Data Sheet U15012EJ1V0DS

FUNCTION OVERVIEW

Item		μPD780833Y
Internal memory	ROM	60 KB
	High-speed RAM	1024 bytes
	Expansion RAM	2048 bytes
Memory space		64 KB
General-purpose registers		8 bits $\times$ 32 registers (8 bits $\times$ 8 registers $\times$ 4 banks)
Minimum instruction execution time		On-chip variable function of minimum instruction execution time 0.48 μs/0.96 μs/1.92 μs/3.84 μs/7.68 μs (@4.19 MHz operation)
Instruction set		• 16-bit operation • Multiply/divide (8 bits $\times$ 8 bits,16 bits $\div$ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjust, etc.
I/O ports		Total: 65 • CMOS input: 54 • TTL input/CMOS output: 8 • N-ch open-drain I/O: 3
A/D converter		8-bit resolution $\times$ 8 channels $\times$ 2
Serial interface		• 3-wire serial I/O mode: 2 channels • UART mode: 1 channel • I^{2}C bus mode: 1 channel
Timer		• 16-bit timer/event counter: 2 channels • 8-bit timer/event counter: 3 channels • Watch timer: 1 channel • Watchdog timer: 1 channel
Timer outputs		5 (8-bit PWM output capable: 3)
Clock output		32.8 kHz, 65.5 kHz, 130.9 kHz, 261.9 kHz, 523.6 kHz, 1.05 MHz, 2.10 MHz, 4.19 MHz (@4.19 MHz operation with system clock)
Bus controller		Bus interface compliant with J1850 (CLASS2)
Vectored interrupt source	Maskable	Internal: 19, external: 9
	Non-maskable	Internal: 1
	Software	1
Power supply voltage		V_{DD} = 4.5 to 5.5 V
Operating ambient temperature		T_A = −40 to +85°C
Package		80-pin plastic QFP (14 $\times$ 14)

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- **80-pin plastic QFP (14 × 14)**
  µPD780833YGC-×××-8BT

Top pins (left to right, 80–61): AVSS0, P97/ANI70, P96/ANI60, P95/ANI50, P94/ANI40, P93/ANI30, P92/ANI20, P91/ANI10, P90/ANI00, AVREF0, AVDD0, VDD1, VSS1, X1, X2, IC, RESET, C2TX, C2RX, P67

Left side (pins 1–20):

Pin	Signal
1	P70/PCL
2	P71/SDA0
3	P72/SCL0
4	P73/TO01
5	P74/TI001
6	P75/TI011
7	P00/INTP0
8	P01/INTP1
9	P02/INTP2
10	P03/INTP3
11	AVREF1
12	P80/ANI01
13	P81/ANI11
14	P82/ANI21
15	P83/ANI31
16	P84/ANI41
17	P85/ANI51
18	P86/ANI61
19	P87/ANI71
20	AVSS1

Right side (pins 41–60):

Pin	Signal
60	P66
59	P65
58	P64
57	P27/TI51/TO51
56	P26/ASCK0/TI52/TO52
55	P25/TxD0
54	P24/RxD0
53	P23/TI50/TO50
52	P07/INTP7
51	P06/INTP6
50	P05/INTP5
49	P04/INTP4
48	P22/SCK31
47	P21/SO31
46	P20/SI31
45	P57
44	P56
43	P55
42	P54
41	P53

Bottom pins (left to right, 21–40): P40, P41, P42, P43, P44, P45, P46, P47, P30/SI30, P31/SO30, P32/SCK30, VDD0, VSS0, P33, P34/TO00, P35/TI000, P36/TI010, P50, P51, P52

Cautions 1. Connect the IC (Internally Connected) pin directly to VSS0 or VSS1.

    2. Connect the AVDD0 pin to VDD0.

    3. Connect the AVSS0 and AVSS1 pins to VSS0.

ANI00 to ANI70,:	Analog input	P90 to P97:	Port 9
ANI01 to ANI71		PCL:	Programmable clock
ASCK:	Asynchronous serial clock	RxD0:	Receive data
AV_{DD0}:	Analog power supply	$\overline{RESET}$:	Reset
AV_{REF0}, AV_{REF1}:	Analog reference voltage	$\overline{SCK30}$, $\overline{SCK31}$:	Serial clock
AV_{SS0}, AV_{SS1}:	Analog ground	SCL0:	Serial clock
C2RX:	CLASS2 receive data	SDA0:	Serial data
C2TX:	CLASS2 transmit data	SI30, SI31:	Serial input
IC:	Internally connected	SO30, SO31:	Serial output
INTP0 to INTP7:	External interrupt input	TI000, TI010, TI001,:	Timer input
P00 to P07:	Port 0	TI011, TI50, TI51, TI52	
P20 to P27:	Port 2	TO00, TO01, TO50,:	Timer output
P30 to P36:	Port 3	TO51, TO52	
P40 to P47:	Port 4	TxD0:	Transmit data
P50 to P57:	Port 5	V_{DD0}, V_{DD1}:	Power supply
P64 to P67:	Port 6	V_{SS0}, V_{SS1}:	Ground
P70 to P75:	Port 7	X1, X2:	Crystal
P80 to P87:	Port 8		

2. BLOCK DIAGRAM
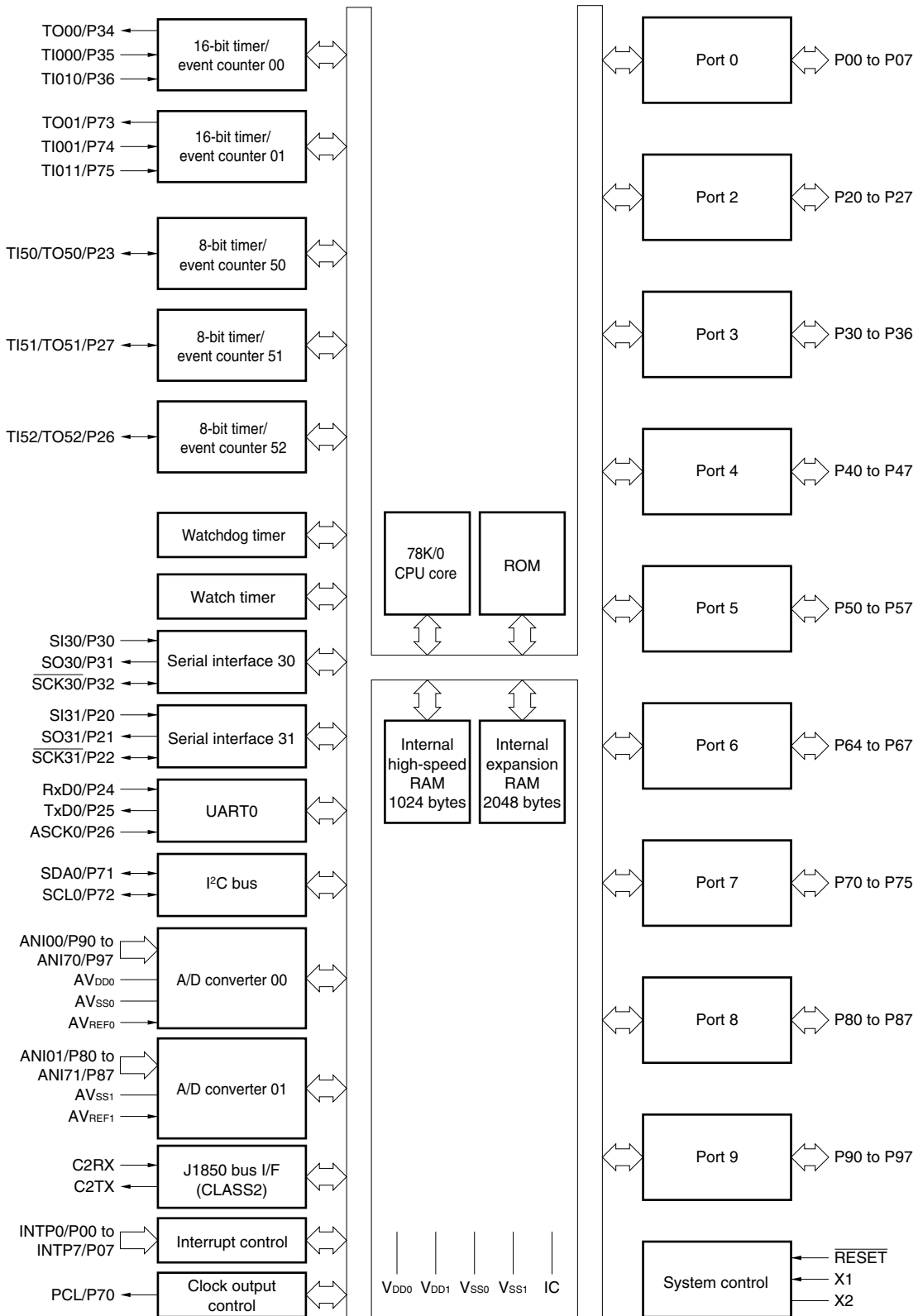
3. PIN FUNCTIONS

3.1 Port Pins (1/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P00 to P07	I/O	Port 0 8-bit I/O port Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by means of software.		Input	INTP0 to INTP7
P20	I/O	Port 2 8-bit I/O port Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by means of software.		Input	SI31
P21					SO31
P22					$\overline{\text{SCK31}}$
P23					TI50/TO50
P24					RxD0
P25					TxD0
P26					ASCK0/TI52/TO52
P27					TI51/TO51
P30	I/O	Port 3 7-bit I/O port Input/output can be specified in 1-bit units.	Use of an on-chip pull-up resistor can be specified by means of software.	Input	SI30
P31					SO30
P32					$\overline{\text{SCK30}}$
P33			N-ch open-drain I/O port LEDs can be driven directly.		—
P34			Use of an on-chip pull-up resistor can be specified by means of software.		TO00
P35					TI000
P36					TI010
P40 to P47	I/O	Port 4 8-bit I/O port Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by means of software. The interrupt request flag (KRIF) is set to 1 by falling edge detection.		Input	—
P50 to P57	I/O	Port 5 8-bit I/O port TTL level input/CMOS output Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by means of software.		Input	—
P64 to P67	I/O	Port 6 4-bit I/O port Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by means of software.		Input	—

3.1 Port Pins (2/2)

Pin Name	I/O	Function		After Reset	Alternate Function
P70	I/O	Port 7 6-bit I/O port Input/output can be specified in 1-bit units.	Use of an on-chip pull-up resistor can be specified by means of software.	Input	PCL
P71			N-ch open-drain I/O port		SDA0
P72					SCL0
P73			Use of an on-chip pull-up resistor can be specified by means of software.		TO01
P74					TI001
P75					TI011
P80 to P87	I/O	Port 8 8-bit I/O port Input/output can be specified in 1-bit units.		Input	ANI01 to ANI71
P90 to P97	I/O	Port 9 8-bit I/O port Input/output can be specified in 1-bit units.		Input	ANI00 to ANI70

3.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0 to INTP7	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified	Input	P00 to P07
SI30	Input	Serial interface SIO30 serial data input	Input	P30
SI31		Serial interface SIO31 serial data input		P20
SO30	Output	Serial interface SIO30 serial data output	Input	P31
SO31		Serial interface SIO31 serial data output		P21
SDA0	I/O	Serial interface IIC0 serial data input/output	Input	P71
$\overline{\text{SCK30}}$	I/O	Serial interface SIO30 serial clock input/output	Input	P32
$\overline{\text{SCK31}}$		Serial interface SIO31 serial clock input/output		P22
SCL0		Serial interface IIC0 serial clock input/output		P72
RxD0	Input	Serial data input for asynchronous serial interface	Input	P24
TxD0	Output	Serial data output for asynchronous serial interface	Input	P25
ASCK0	Input	Serial clock input for asynchronous serial interface	Input	P26/TI52/TO52
TI000	Input	External count clock input to 16-bit timer/event counter 00 Capture trigger input to capture register (CR000 and CR010) of 16-bit timer/event counter 00	Input	P35
TI010		Capture trigger input to capture register (CR000) of 16-bit timer/event counter 00		P36
TI001		External count clock input to 16-bit timer/event counter 01 Capture trigger input to capture register (CR001 and CR011) of 16-bit timer/event counter 01		P74
TI011		Capture trigger input to capture register (CR001) of 16-bit timer/event counter 01		P75
TI50		External count clock input to 8-bit timer/event counter 50		P23/TO50
TI51		External count clock input to 8-bit timer/event counter 51		P27/TO51
TI52		External count clock input to 8-bit timer/event counter 52		P26/ASCK0/TO52

3.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
TO00	Output	16-bit timer/event counter 00 output	Input	P34
TO01		16-bit timer/event counter 01 output		P73
TO50		8-bit timer/event counter 50 output		P23/TI50
TO51		8-bit timer/event counter 51 output		P27/TI51
TO52		8-bit timer/event counter 52 output		P26/ASCK0/TI52
PCL	Output	Clock output	Input	P70
ANI00 to ANI70	Input	A/D converter (AD00) analog input	Input	P90 to P97
ANI01 to ANI71		A/D converter (AD01) analog input		P80 to P87
AV$_{REF0}$	—	A/D converter (AD00) reference voltage input	—	—
AV$_{REF1}$		A/D converter (AD01) analog power supply and reference voltage input		—
AV$_{DD0}$		A/D converter (AD00) analog power supply		—
AV$_{SS0}$		A/D converter (AD00) ground potential. Set the same potential as that of V$_{SS0}$ or V$_{SS1}$.		—
AV$_{SS1}$		A/D converter (AD01) ground potential. Set the same potential as that of V$_{SS0}$ or V$_{SS1}$.		—
C2RX	Input	CLASS2 data input		—
C2TX	Output	CLASS2 data output		—
$\overline{RESET}$	Input	System reset input		—
X1	Input	Crystal connection for oscillation		—
X2	—			—
V$_{DD0}$		Positive power supply for ports		—
V$_{DD1}$		Positive power supply (except ports)		—
V$_{SS0}$		Ground potential of ports		—
V$_{SS1}$		Ground potential (except ports)		—
IC		Internally connected. Connect directly to V$_{SS0}$ or V$_{SS1}$.		—

3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.

For the I/O circuit configuration of each type, see Figure 3-1.

Table 3-1. Types of Pin I/O Circuits and Recommended Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0 to P07/INTP7	8-C	I/O	Input: Independently connect to V_{SS0} via a resistor. Output: Leave open.
P20/SI31			Input: Independently connect to V_{DD0} or V_{SS0} via a resistor. Output: Leave open.
P21/SO31	5-H		
P22/$\overline{SCK31}$	8-C		
P23/TI50/TO50			
P24/RxD0			
P25/TxD0	5-H		
P26/ASCK0/TI52/TO52	8-C		
P27/TI51/TO51			
P30/SI30			
P31/SO30	5-H		
P32/$\overline{SCK30}$	8-C		
P33	13-P		Input: Independently connect to V_{DD0} via a resistor. Output: Leave open.
P34/TO00	5-H		Input: Independently connect to V_{DD0} or V_{SS0} via a resistor. Output: Leave open.
P35/TI000	8-C		
P36/TI010			
P40 to P47	5-H		Input: Independently connect to V_{DD0} via a resistor. Output: Leave open.
P50 to P57	5-T		Input: Independently connect to V_{DD0} or V_{SS0} via a resistor. Output: Leave open.
P64 to P67	5-H		
P70/PCL			
P71/SDA0	13-R		Input: Independently connect to V_{DD0} via a resistor. Output: Leave open.
P72/SCL0			
P73/TO01	5-H		Input: Independently connect to V_{DD0} or V_{SS0} via a resistor. Output: Leave open.
P74/TI001	8-C		
P75/TI011			
P80/ANI01 to P87/ANI71	11-E		
P90/ANI00 to P97/ANI70			
C2RX	2	Input	Connect to V_{SS0} via a resistor.
C2TX	3-B	Output	Leave open.
$\overline{RESET}$	2	Input	—
AV_{DD0}	—	—	Connect to V_{DD0}.
AV_{REF0}			
AV_{REF1}			
AV_{SS0}			Connect to V_{SS0}.
AV_{SS1}			
IC			Connect directly to V_{SS0} or V_{SS1}.

Figure 3-1. Pin I/O Circuits
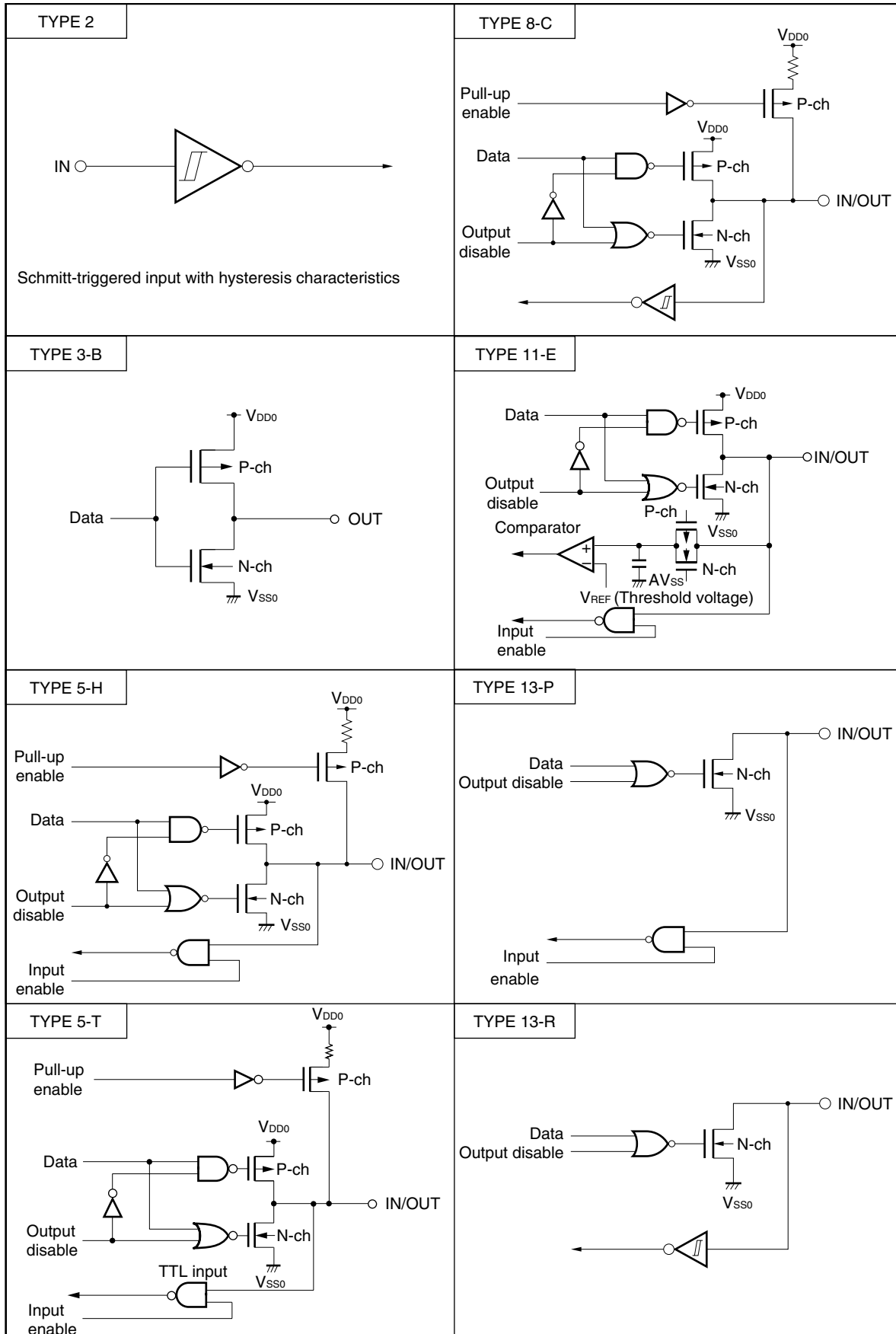
4. MEMORY SPACE

Figure 4-1 shows the memory map of the μPD780833Y.

Figure 4-1. Memory Map
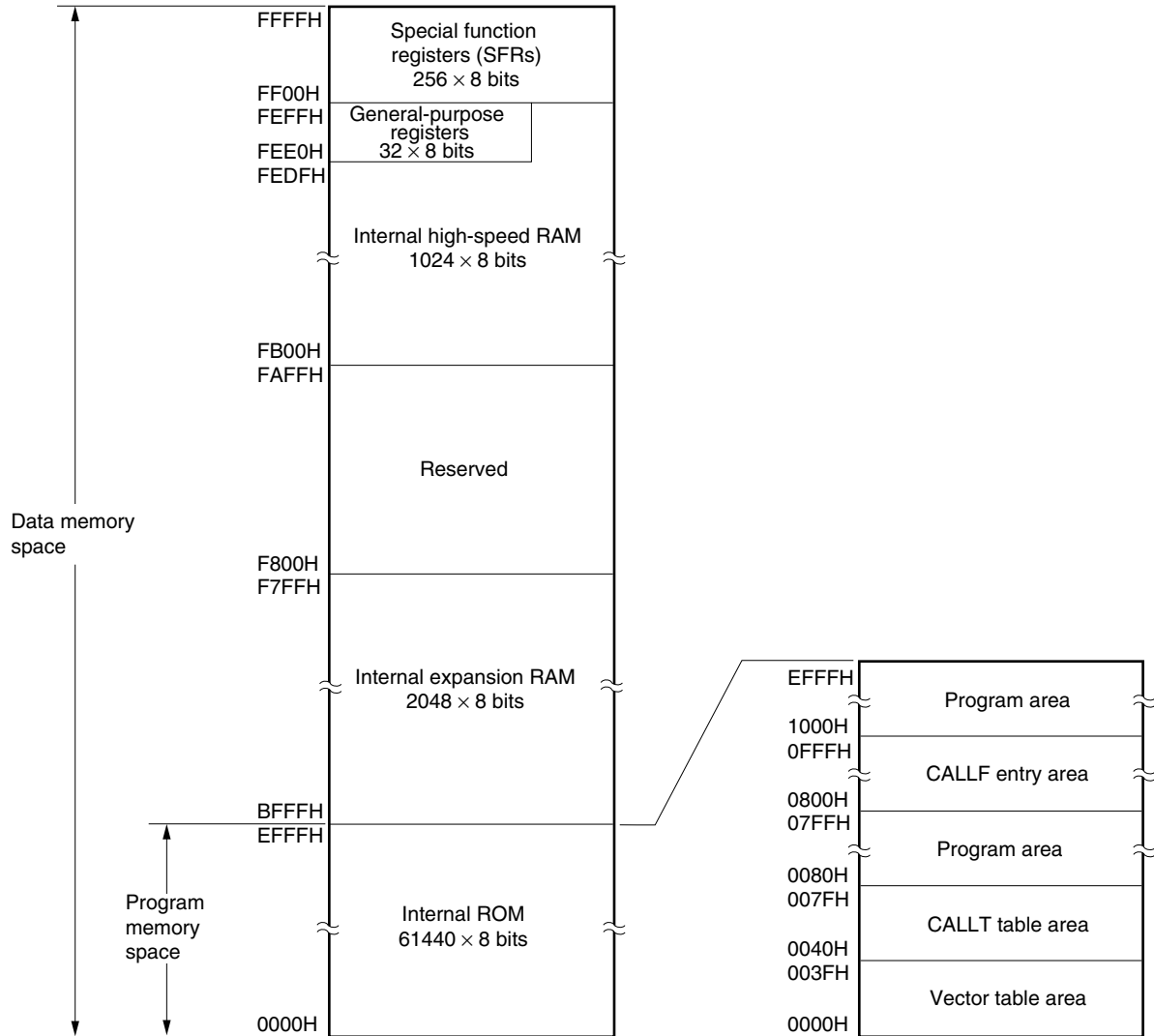
5. PERIPHERAL HARDWARE FUNCTION FEATURES

5.1 Ports

The following 3 types of I/O ports are available.

- CMOS I/O (ports 0, 2 to 4, 6 to 9 (excluding P33, P71, and P72)): 54
- TTL input/CMOS output (port 5): 8
- N-channel open-drain I/O (P33, P71, P72): 3

  Total: 65

Table 5-1. Port Functions

Name	Pin Name	Function
Port 0	P00 to P07	I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by means of software.
Port 2	P20 to P27	I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by means of software.
Port 3	P30 to P32, P34 to P36	I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by means of software.
	P33	N-ch open-drain I/O port. Input/output can be specified in 1-bit units. LEDs can be driven directly.
Port 4	P40 to P47	I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by means of software. The interrupt request flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	TTL-level input/CMOS output port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by means of software.
Port 6	P64 to P67	I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by means of software.
Port 7	P70, P73 to P75	I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by means of software.
Port 8	P80 to P87	I/O port. Input/output can be specified in 1-bit units.
Port 9	P90 to P97	I/O port. Input/output can be specified in 1-bit units.

5.2 Clock Generator

A system clock generator is incorporated.

The minimum instruction execution time can be changed.

- 0.48 μs/0.95 μs/1.91 μs/3.81 μs/7.63 μs (at 4.19 MHz operation with system clock)

Figure 5-1. Block Diagram of Clock Generator
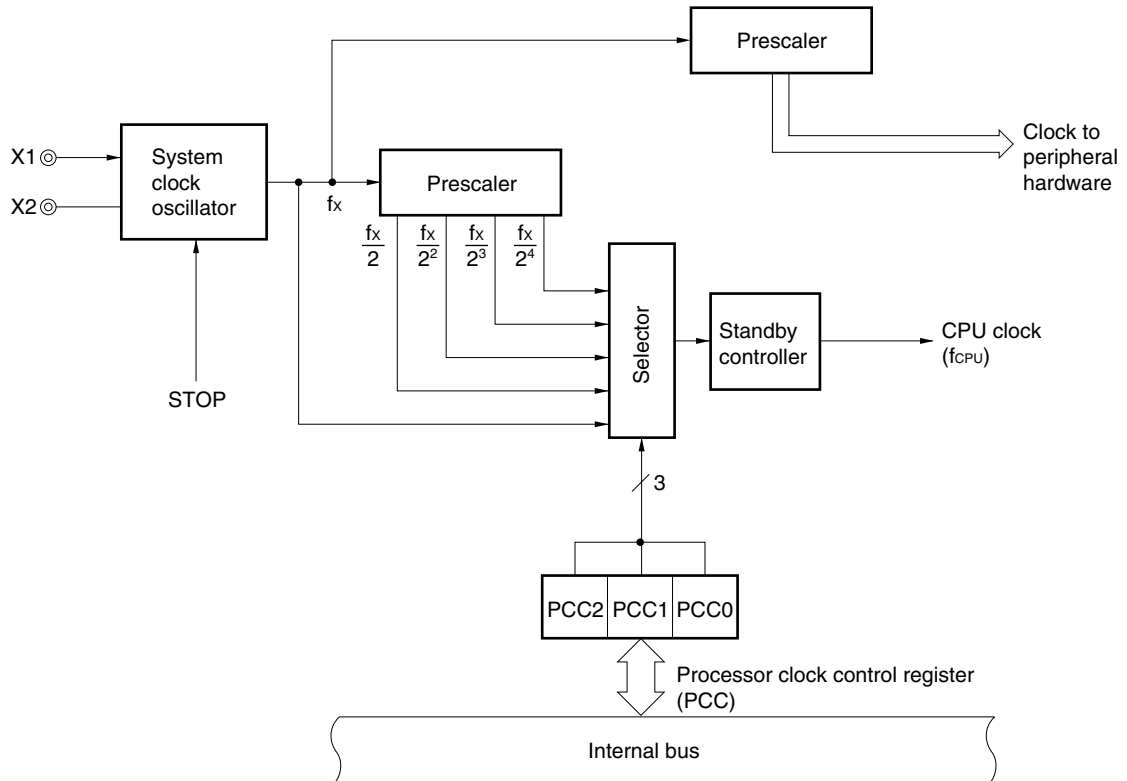
5.3 Timer

Seven timer channels are incorporated.

- 16-bit timer/event counter: 2 channels
- 8-bit timer/event counter: 3 channels
- Watch timer: 1 channel
- Watchdog timer: 1 channel

Table 5-2. Operations of Timer/Event Counter

		16-Bit Timer/Event Counter 00, 01	8-Bit Timer/Event Counter 50, 51, 52	Watch Timer	Watchdog Timer
Operation mode	Interval timer	2 channels	3 channels	1 channel[Note 1]	1 channel[Note 2]
	External event counter	2 channels	3 channels	—	—
Function	Timer outputs	2	3	—	—
	PWM outputs	—	3	—	—
	PPG outputs	2	—	—	—
	Pulse width measurement	4 inputs	—	—	—
	Square-wave outputs	2	3	—	—
	One-shot pulse outputs	2	—	—	—
	Interrupt sources	4	3	2	1

Notes 1. The watch timer can perform both watch timer and interval timer functions at the same time.

2. The watchdog timer has the watchdog timer and interval timer functions. However, use the watchdog timer by selecting either the watchdog timer function or the interval timer function.

Figure 5-2. Block Diagram of 16-Bit Timer/Event Counter 00
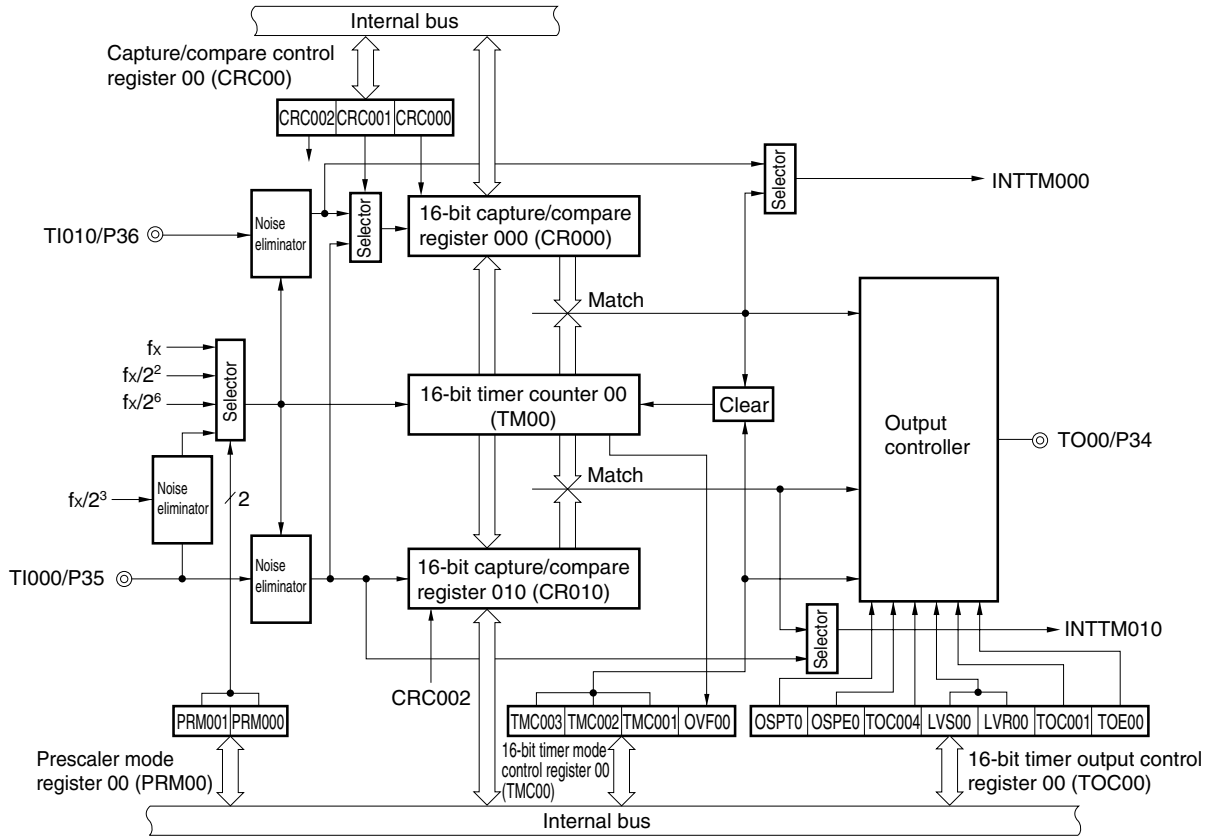
Figure 5-3. Block Diagram of 16-Bit Timer/Event Counter 01
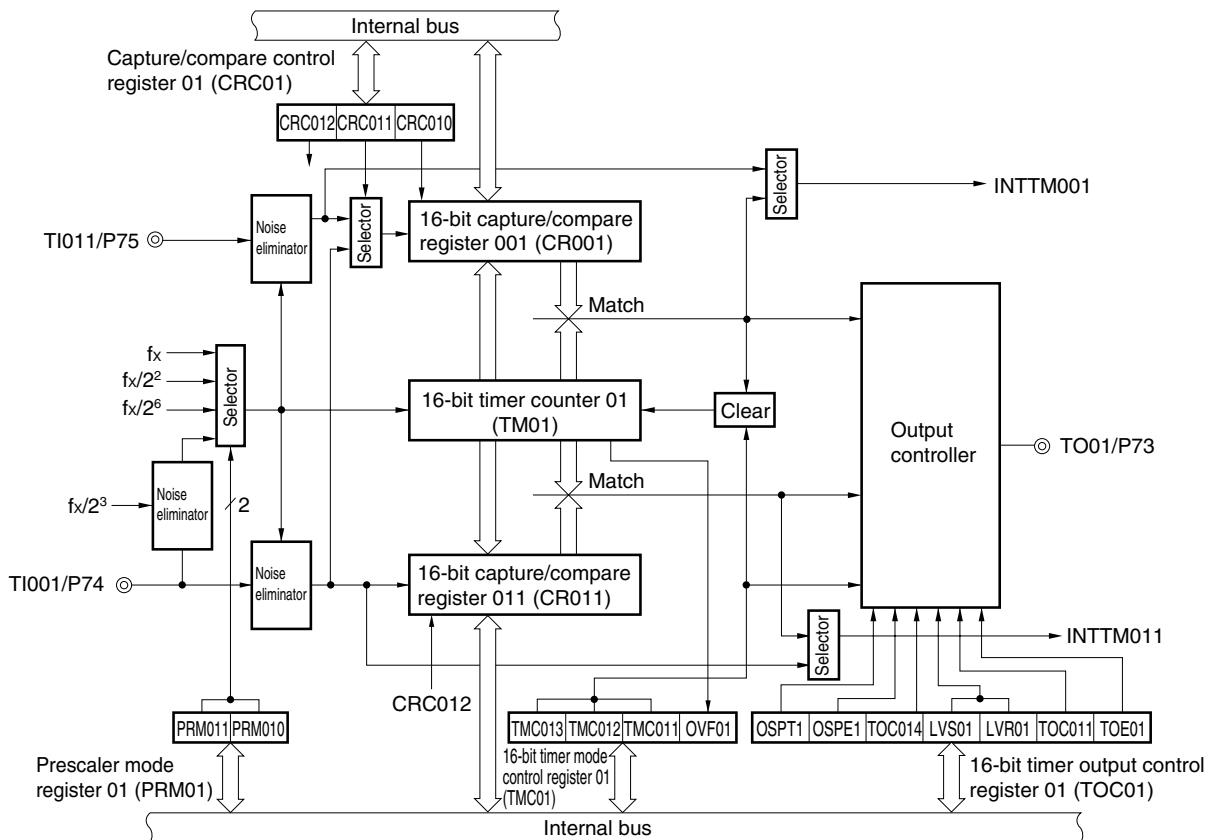
Figure 5-4. Block Diagram of 8-Bit Timer/Event Counter 50
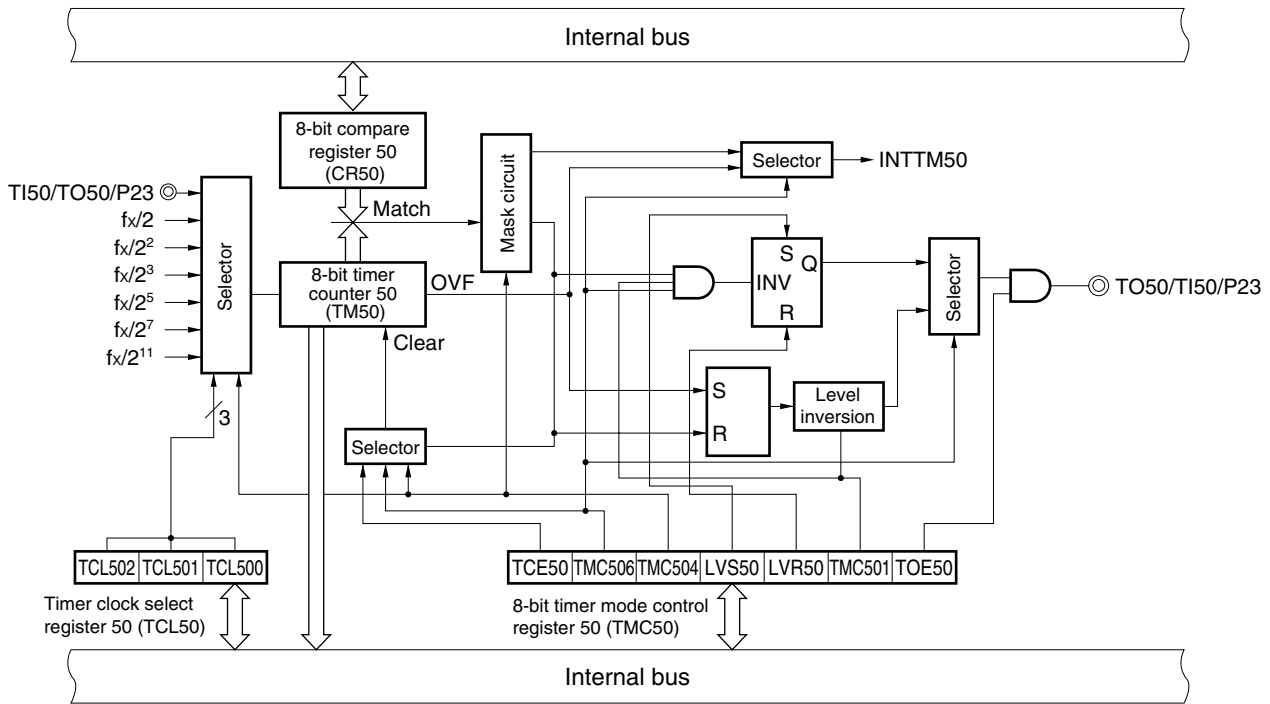
Figure 5-5. Block Diagram of 8-Bit Timer/Event Counter 51
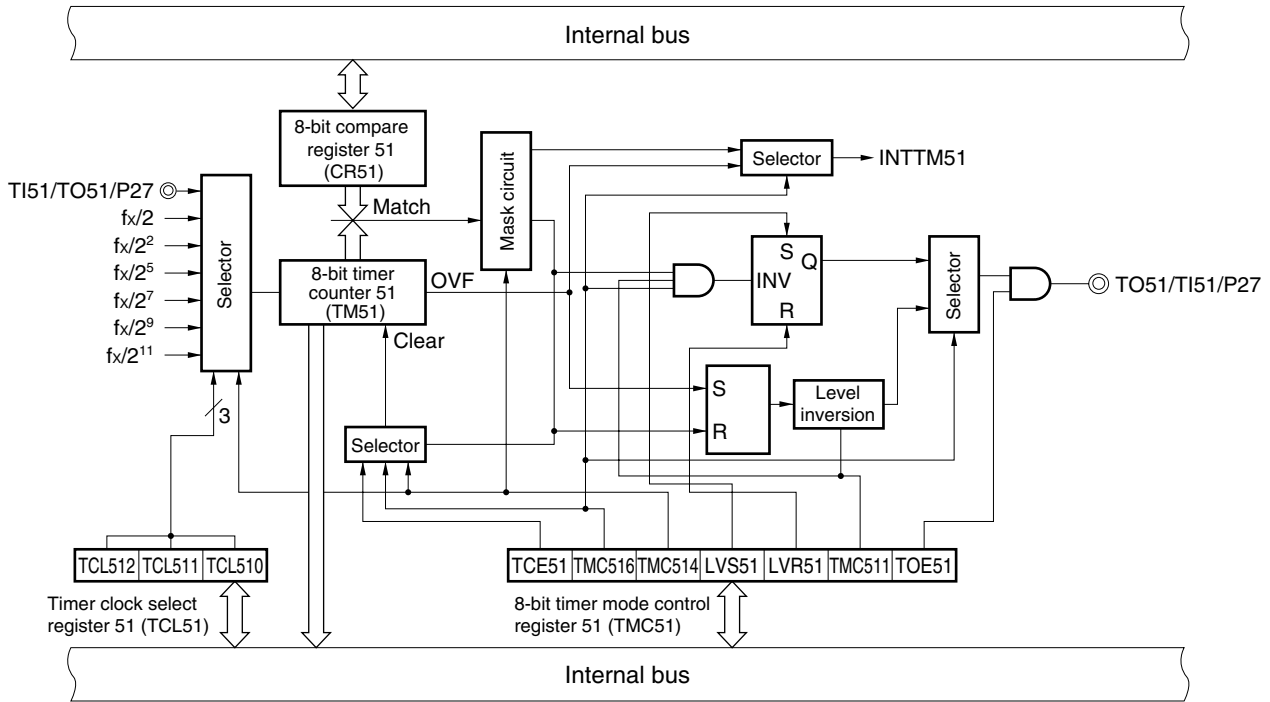
Figure 5-6. Block Diagram of 8-Bit Timer/Event Counter 52
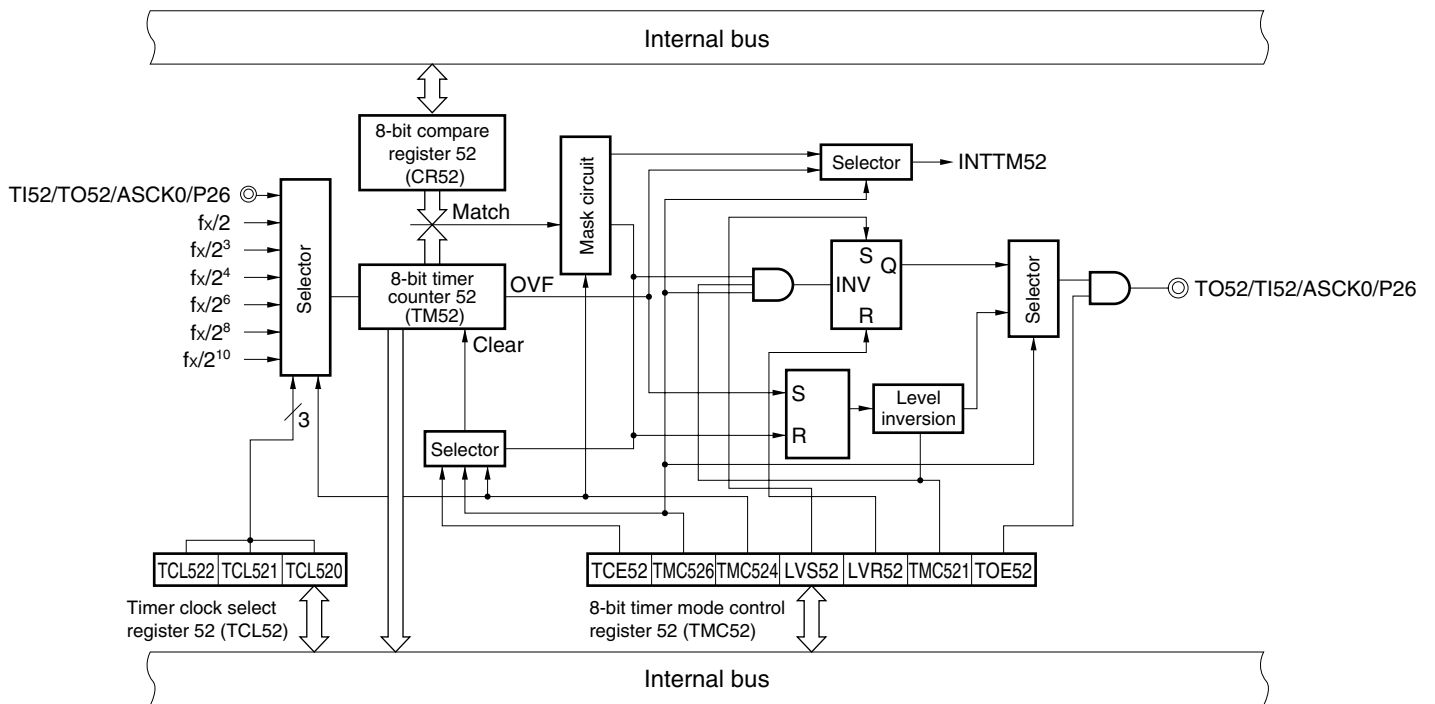
Figure 5-7. Block Diagram of Watch Timer
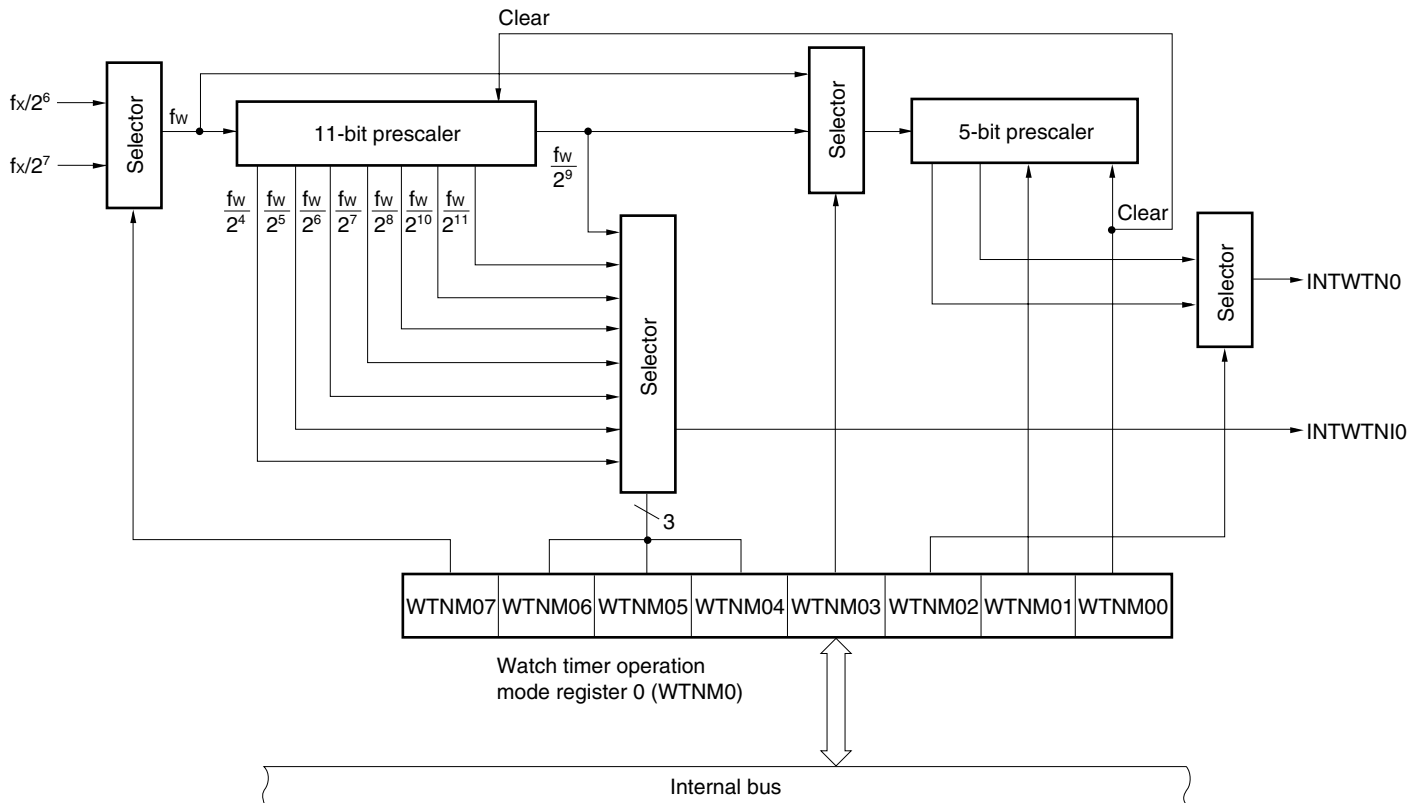
Figure 5-8. Block Diagram of Watchdog Timer
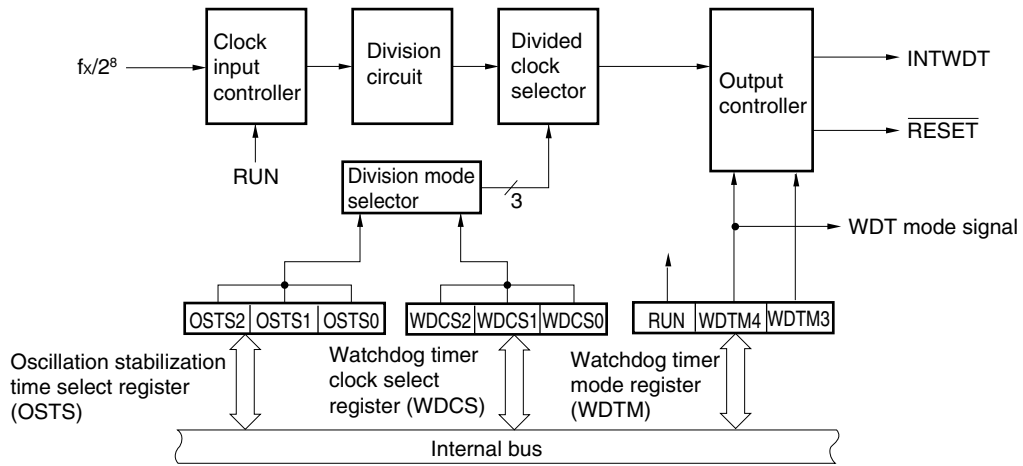
5.4 Clock Output Controller

A clock output/buzzer output controller (CKU) is incorporated.

Clocks with the following variation of frequency can be output as clock output.

- 32.8 kHz/65.6 kHz/131 kHz/262 kHz/524 kHz/1.05 MHz/2.10 MHz/4.19 MHz (at 4.19 MHz operation with system clock)

Figure 5-9. Block Diagram of Clock Output Controller
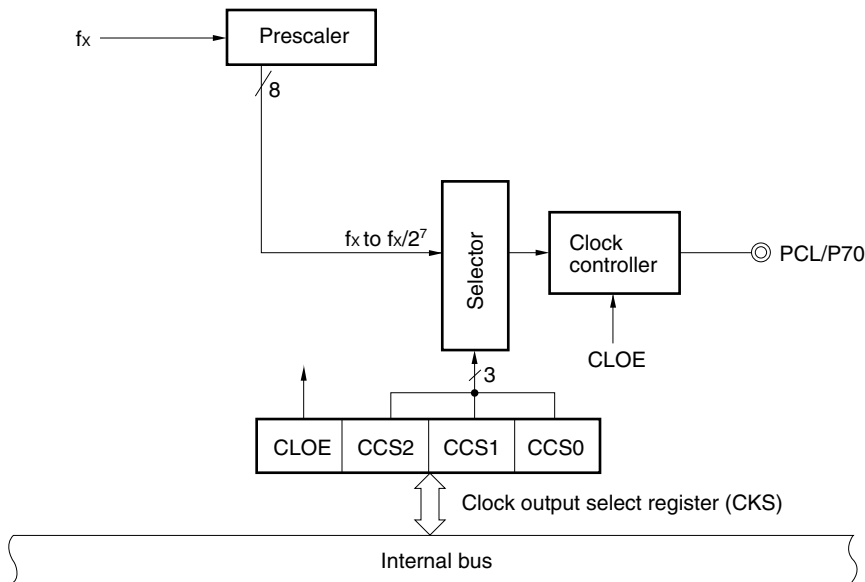
5.5 A/D Converter

Two A/D converters of 8-bit resolution $\times$ 8 channels (AD00 and AD01) are incorporated.

An A/D conversion operation can only be started by software.

Figure 5-10. Block Diagram of A/D Converter (AD00)
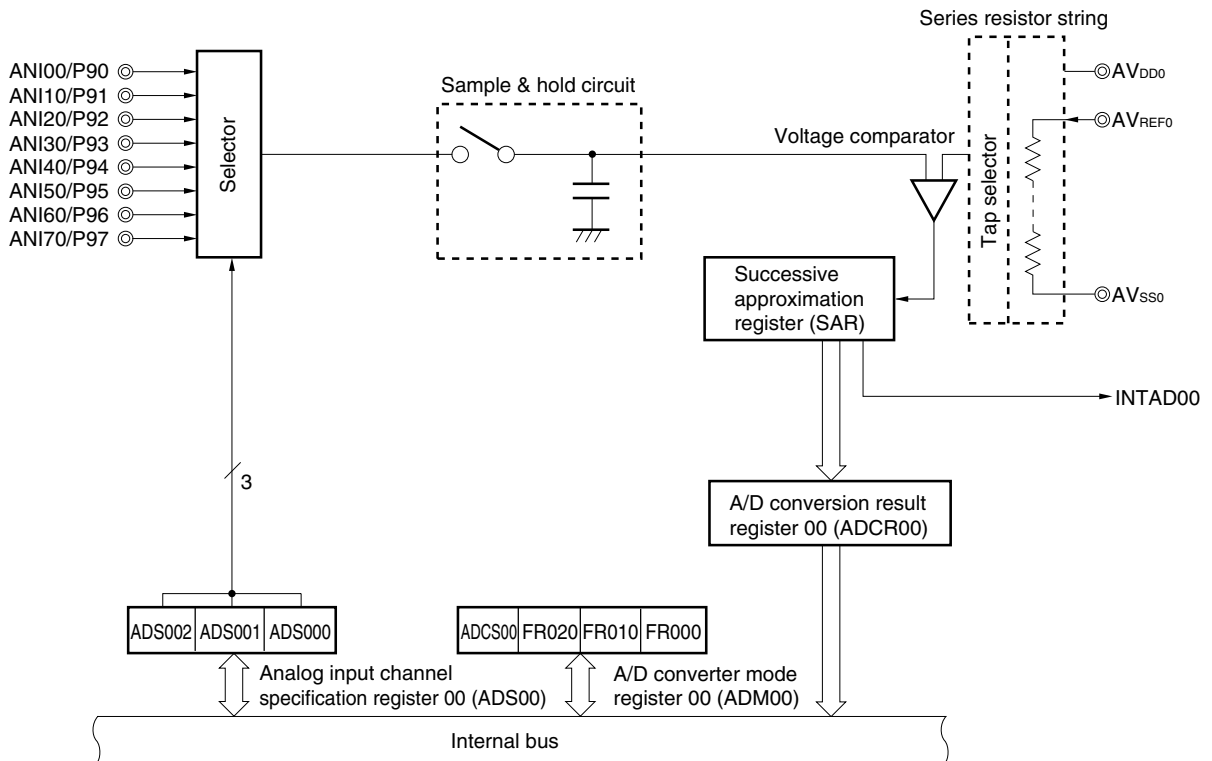
Figure 5-11. Block Diagram of A/D Converter (AD01)

NEC
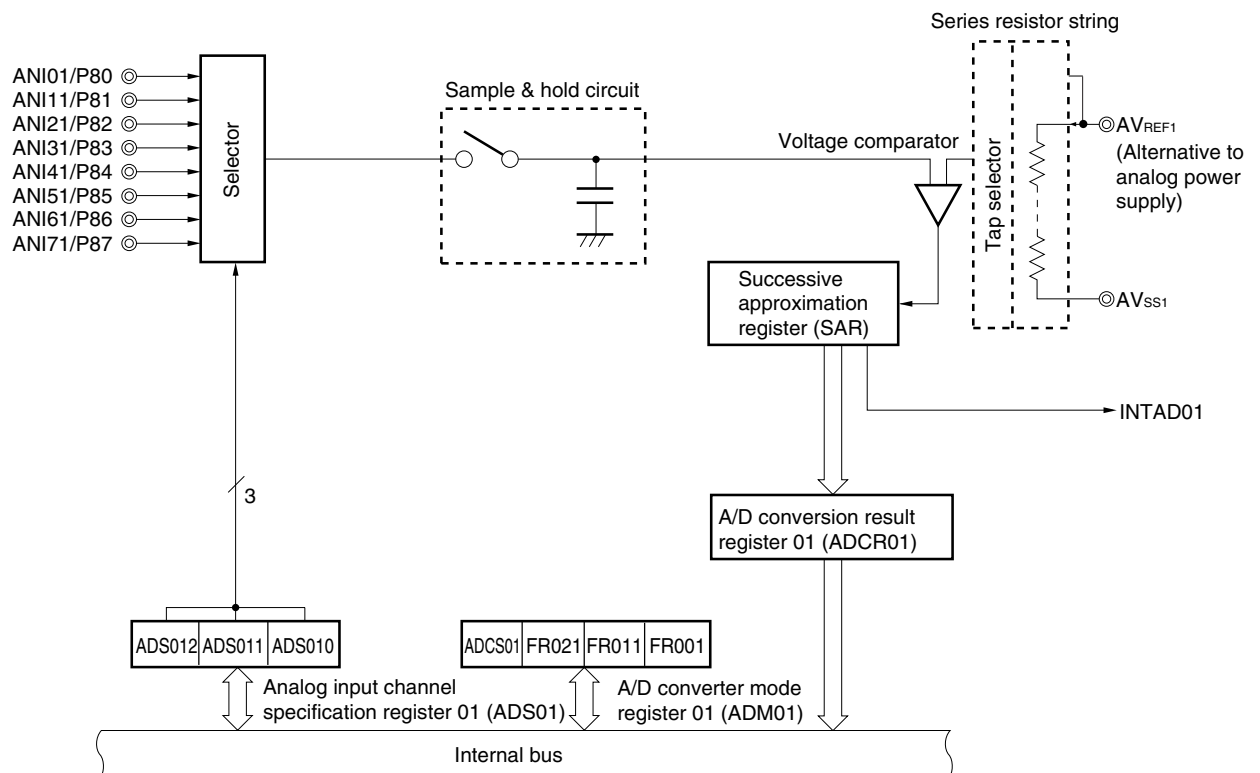
5.6 Serial Interface

Four serial interface channels are incorporated.

- Serial interface UART0
- Serial interface SIO30, 31
- Serial interface IIC0

(1) Serial interface UART0

The serial interface UART0 operates in asynchronous serial interface (UART) mode.

- **Asynchronous serial interface (UART) mode**

  This mode enables full-duplex operation wherein one byte of data following the start bit is transmitted and received.

  The on-chip UART-dedicated baud rate generator enables communication using a wide range of selectable baud rates. In addition, a baud rate can be also defined by dividing the clock input to the ASCK0 pin.

  The UART-dedicated baud rate generator can also be used to generate a MIDI-standard baud rate (31.25 Kbps).

Figure 5-12. Block Diagram of Serial Interface UART0
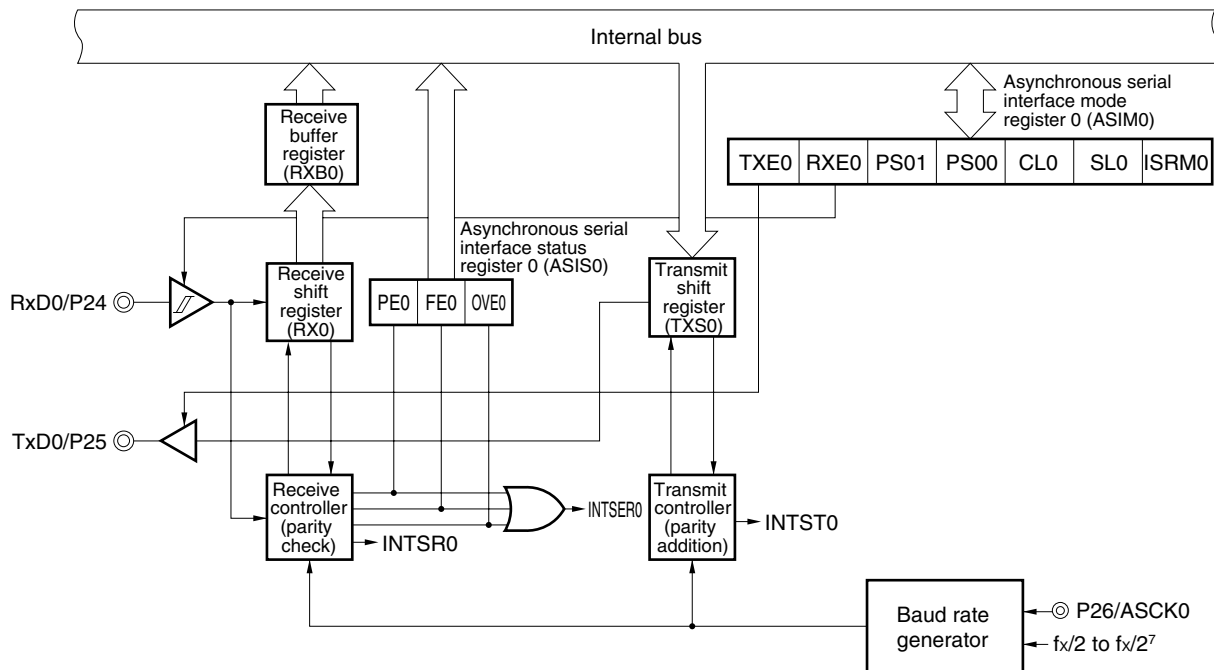
(2) Serial interface SIO30 and 31

The serial interfaces SIO30 and 31 operate in 3-wire serial I/O mode.

- **3-wire serial I/O mode (fixed as MSB first)**

    This is an 8-bit data transfer mode using three lines: a serial clock line ($\overline{\text{SCK3n}}$), a serial output line (SO3n), and a serial input line (SI3n).

    Since simultaneous transmit and receive operations are possible in the 3-wire serial I/O mode, the processing time for data transfer is reduced.

    The first bit of the 8-bit data in the serial transfer is fixed as MSB.

    The 3-wire serial I/O mode is useful for connection to peripheral I/O devices that include a clocked serial interface, display controllers, etc.

    Remark   n = 0, 1

Figure 5-13. Block Diagram of Serial Interface SIO30
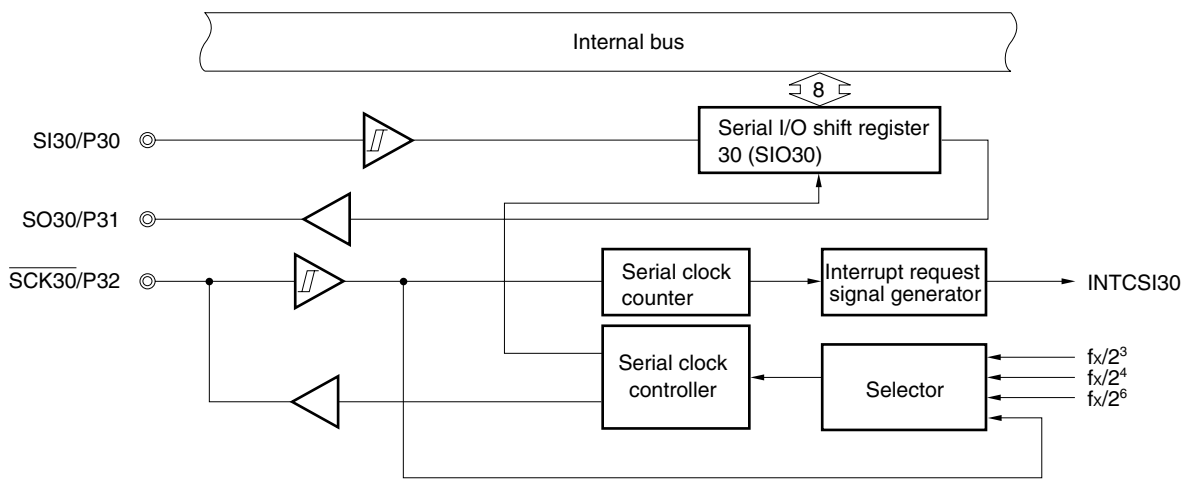
Figure 5-14. Block Diagram of Serial Interface SIO31
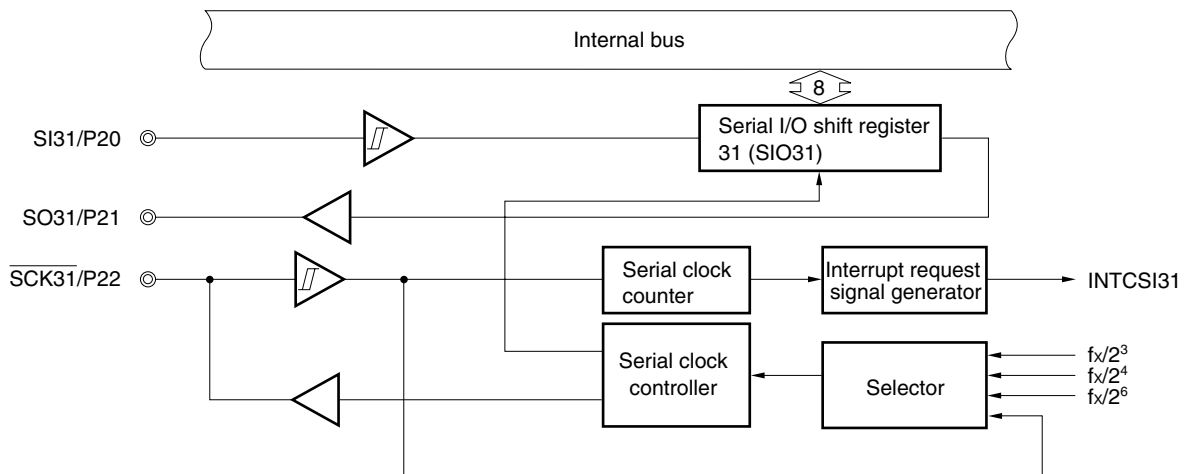
(3) Serial interface IIC0

The serial interface IIC0 operates in the I²C (Inter IC) bus mode (multimaster supported).

• **I²C bus mode (multimaster supported)**

This is an 8-bit data transfer mode using two lines: a serial clock line (SCL0) and a serial data bus line (SDA0).

This mode complies with the I²C bus format, and can output "start condition", "data", and "stop condition" during transmission via the serial data bus. This data are automatically detected by hardware during reception.

Since SCL0 and SDA0 are open-drain outputs in IIC0, pull-up resistors for the serial clock line and the serial data bus line are required.

Figure 5-15. Block Diagram of Serial Interface IIC0
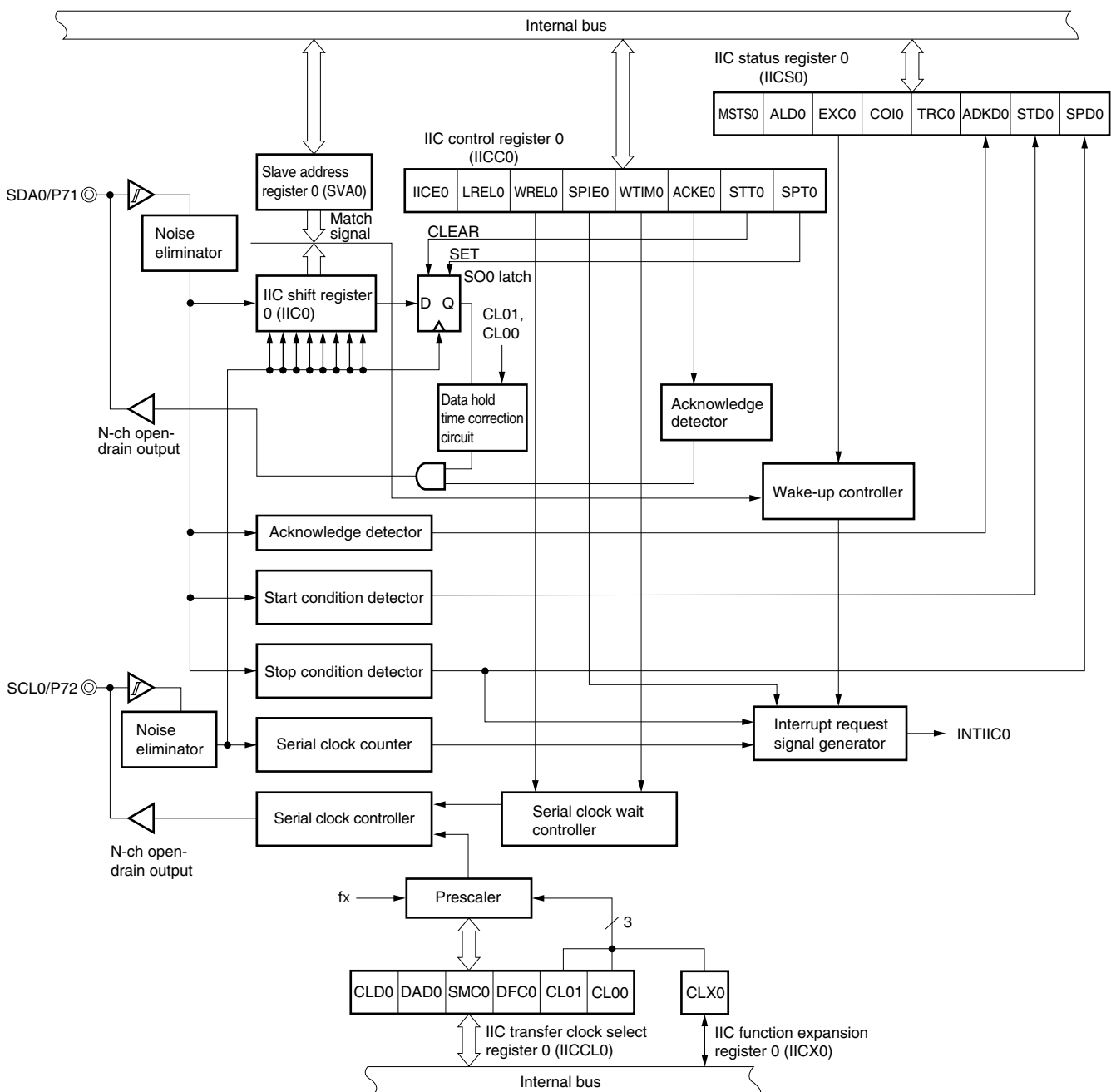
5.7 J1850 (CLASS2) Bus Controller

The μPD780833Y includes a bus controller compliant with J1850 (CLASS2).

The protocol of J1850 (CLASS2) is the variable pulse width modulation (VPW) method. The protocol conforms to the rules stated below.

(1)   The potential level is changed at each bit.

(2)   A logical value, 1 or 0, is determined by the potential level and pulse width.

(3)   A logical value of 0 takes precedence.

A message begins with an SOF (start of frame) symbol and contains one to 11 bytes of data except in block mode, in which the data length is not limited. Data is transmitted serially in descending order of bits, that is, bit 7 is transmitted first, and bit 0 is transmitted last. The last bit, bit 0, is followed by the cyclic redundancy check (CRC) field. A message is concluded with an EOF (end of frame). The break signal is a single pulse. Examples of a message and symbols are shown below.

Figure 5-16. Example of Message
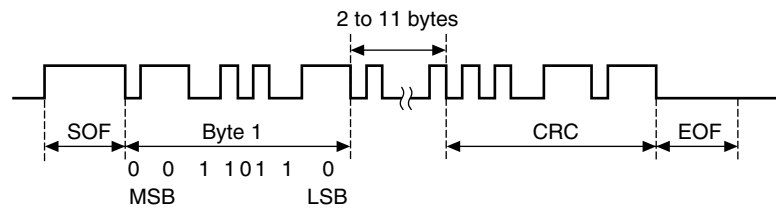
Table 5-3. Examples of Symbols

Symbol Name	Symbol (Example of Symbols in Normal Transmission Mode)
SOF (Start Of Frame)	Active 200 μs
Logical state 0	64 μs passive 128 μs active
Logical state 1	64 μs active 128 μs passive
EOF (End Of Frame)	Passive > 280 μs
Break signal	Active > 768 μs

6. INTERRUPT FUNCTIONS

A total of 30 interrupt sources are provided, divided into the following three types.
- Non-maskable: 1
- Maskable: 28
- Software: 1

Table 6-1. Interrupt Source List (1/2)

Interrupt Type	Default Priority[Note 1]	Interrupt Source Name	Interrupt Source Trigger	Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
Non-maskable	—	INTWDT	Watchdog timer overflow (with watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (with interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTP4			000EH	
	6	INTP5			0010H	
	7	INTP6			0012H	
	8	INTP7			0014H	
	9	INTSER0	UART0 reception error generation	Internal	0016H	(B)
	10	INTSR0	End of UART0 reception		0018H	
	11	INTST0	End of UART0 transmission		001AH	
	12	INTCSI30	End of SIO30 transfer		001CH	
	13	INTCSI31	End of SIO31 transfer		001EH	
	14	INTIIC0	End of IIC0 transfer		0020H	
	15	INTC2	CLASS2 wake-up request, reception completion, sleep enable, reception error		0022H	
	16	INTWTNI0	Reference time interval signal from watch timer		0024H	
	17	INTTM000	Match between TM00 and CR000 (when compare register is specified). Valid edge detection of TI000 pin (when capture register is specified).		0026H	
	18	INTTM010	Match between TM00 and CR010 (when compare register is specified). Valid edge detection of TI010 pin (when capture register is specified).		0028H	

Notes 1. The default priority is the priority order when two or more maskable interrupt requests are generated simultaneously. 0 is the highest and 27 is the lowest.
2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1, respectively.

Remark Two watchdog timer interrupt sources (INTWDT) are available: a non-maskable interrupt and a maskable interrupt (internal), either of which can be selected.

Table 6-1. Interrupt Source List (2/2)

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Maskable	19	INTTM001	Match between TM01 and CR001 (when compare register is specified). Valid edge detection of TI001 pin (when capture register is specified).	Internal	002AH	(B)
	20	INTTM011	Match between TM01 and CR011 (when compare register is specified). Valid edge detection of TI011 pin (when capture register is specified).		002CH	
	21	INTAD00	End of A/D converter (AD00) conversion		002EH	
	22	INTAD01	End of A/D converter (AD01) conversion		0030H	
	23	INTWTN0	Watch timer overflow		0034H	
	24	INTKR	Port 4 falling edge detection	External	0036H	(D)
	25	INTTM50	Match between TM50 and CR50	Internal	0038H	(B)
	26	INTTM51	Match between TM51 and CR51		003AH	
	27	INTTM52	Match between TM52 and CR52		003CH	
Software	—	BRK	BRK instruction execution	—	003EH	(E)

Notes 1. The default priority is the priority order when two or more maskable interrupt requests are generated simultaneously. 0 is the highest and 27 is the lowest.

2. Basic configuration types (A) to (E) correspond to (A) to (E) in Figure 6-1, respectively.

Remark Two watchdog timer interrupt sources (INTWDT) are available: a non-maskable interrupt and a maskable interrupt (internal), either of which can be selected.

Figure 6-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt

```
                                    ┌──────────────────────────┐
                                    │      Internal bus        │
                                    └──────────────────────────┘
                                                  ▲
                                                  │
                          ┌──────────┐      ┌──────────────┐
Interrupt   ●────────────▶│ Priority │─────▶│ Vector table │
request     │             │controller│      │   address    │
            │             └──────────┘      │  generator   │
            │                               └──────────────┘
            │
            └──────────────────────────────▶ Standby release
                                             signal
```

(B) Internal maskable interrupt

```
   ┌───────────────────────────────────────────────────────────────┐
   │                        Internal bus                            │
   └───────────────────────────────────────────────────────────────┘
         ▲         │             │      │      │                ▲
         │         ▼             ▼      ▼      ▼                │
       ┌────┐   ┌────┐        ┌────┐ ┌────┐ ┌────┐              │
       │ MK │   │    │        │ IE │ │ PR │ │ISP │              │
       └────┘   └────┘        └────┘ └────┘ └────┘              │
         │                       │     │      │                │
         │                       └─────┼──────┘                │
         ▼                             ▼                        │
Interrupt ┌────┐                ┌──────────┐      ┌──────────────┐
request ─▶│ IF │──▷o──●────────▶│ Priority │─────▶│ Vector table │
          └────┘                │controller│      │   address    │
                                └──────────┘      │  generator   │
                                      │           └──────────────┘
                                      └──────────▶ Standby release
                                                   signal
```
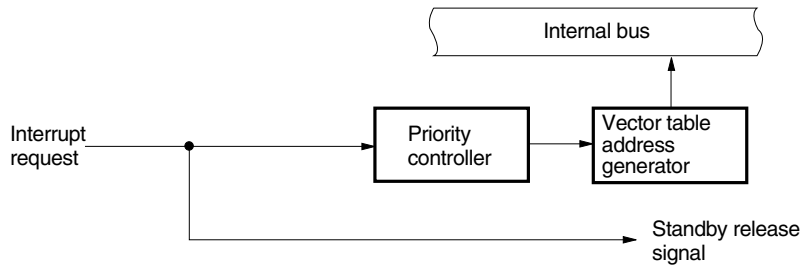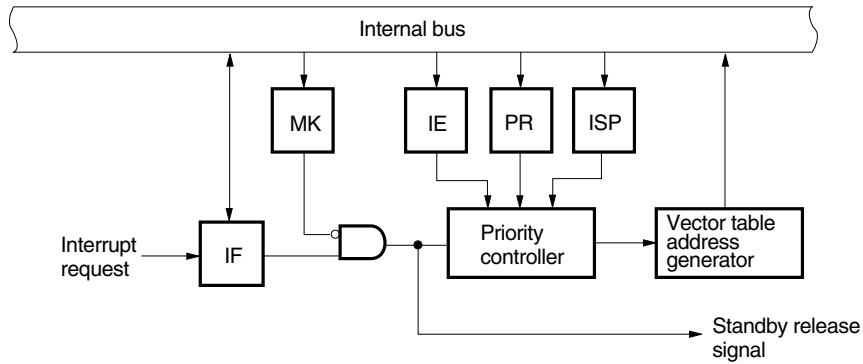
(C) External maskable interrupt (INTP0 to INTP7)

```
   ┌────────────────────────────────────────────────────────────────────┐
   │                           Internal bus                             │
   └────────────────────────────────────────────────────────────────────┘
        │     │                    │         │     │     │            ▲
        ▼     ▼                    ▼         ▼     ▼     ▼            │
  ┌──────────────────┐  ┌────┐   ┌────┐   ┌────┐┌────┐┌────┐         │
  │External interrupt│  │    │   │ MK │   │ IE ││ PR ││ISP │         │
  │edge enable       │  │    │   └────┘   └────┘└────┘└────┘         │
  │register          │  │ IF │     │        │     │    │            │
  │(EGP, EGN)        │  │    │     │        └─────┼────┘            │
  └──────────────────┘  │    │     │              ▼                 │
        │               │    │     ▼        ┌──────────┐   ┌──────────────┐
Interrupt ┌──────────┐  │    │  ▷o──●──────▶│ Priority │──▶│ Vector table │
request ─▶│   Edge   │─▶│    │              │controller│   │   address    │
          │ detector │  └────┘              └──────────┘   │  generator   │
          └──────────┘                            │        └──────────────┘
                                                  └────────▶ Standby release
                                                             signal
```
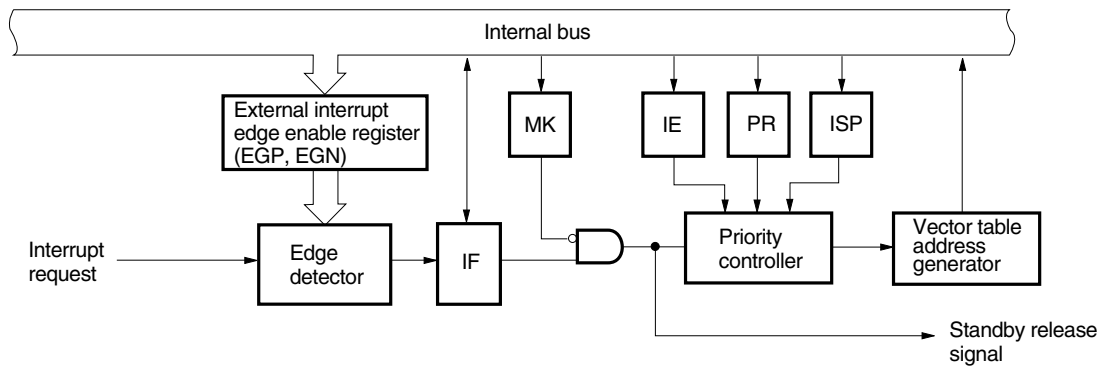
Figure 6-1. Basic Configuration of Interrupt Function (2/2)

(D) External maskable interrupt (INTKR)
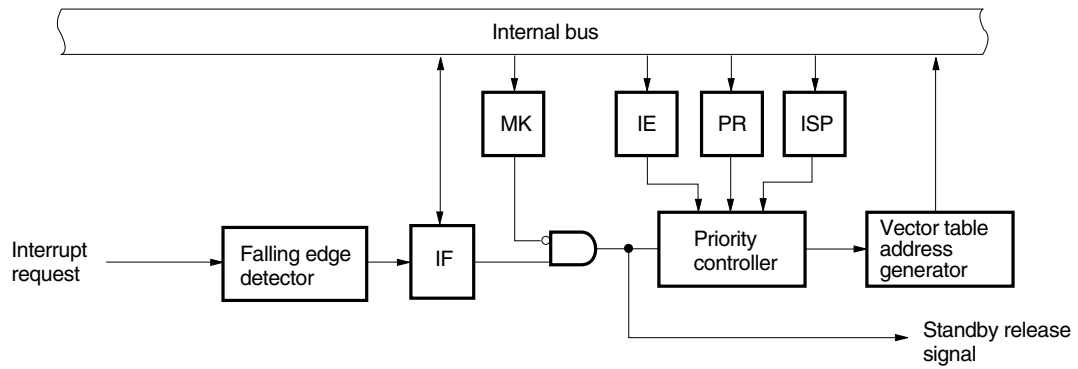
(E) Software interrupt
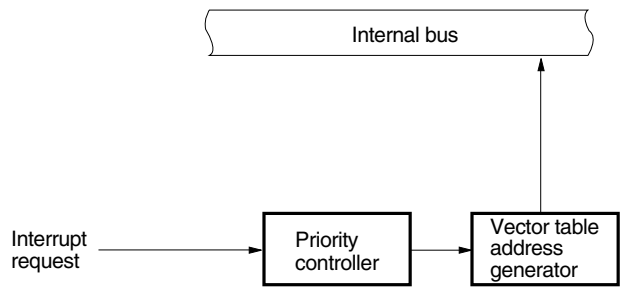
IF: Interrupt request flag
IE: Interrupt enable flag
ISP: In-service priority flag
MK: Interrupt mask flag
PR: Priority specification flag

7. STANDBY FUNCTIONS

The following two standby functions are provided to reduce the current consumption.

- • HALT mode: The CPU operating clock is stopped. The average current consumption can be reduced by intermittent operation in combination with the normal operating mode.
- • STOP mode: The system clock oscillation is stopped. All operations using the system clock are stopped, so that the system operates with ultra-low power consumption.

Figure 7-1. Standby Function
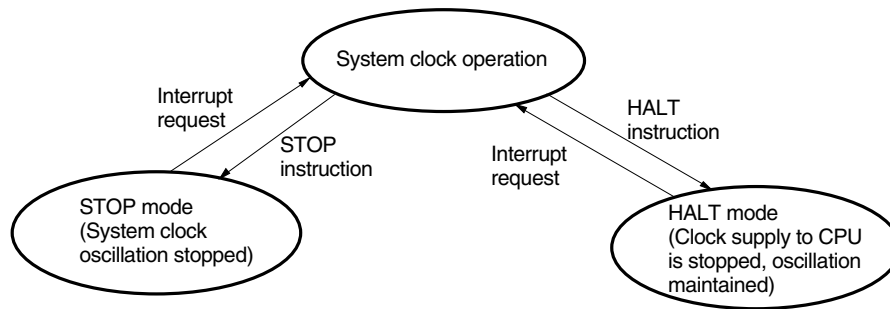
8. RESET FUNCTIONS

The following two reset methods are available.

- • External reset by $\overline{\text{RESET}}$ signal input
- • Internal reset by watchdog timer loop time detection

9. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

Second operand / First operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] / [HL + B] / [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

First operand \ Second operand	#word	AX	rp^Note	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW^Note						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE or HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

First operand \ Second operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instructions/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

First operand \ Second operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

10. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}	V_{DD} = AV_{DD} = AV_{REF}		−0.3 to +6.5	V
	AV_{DD}				
	AV_{REF}				
	AV_{SS}			−0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, P80 to P87, P90 to P97, C2RX, X1, X2, $\overline{RESET}$		−0.3 to V_{DD} + 0.3	V
	V_{I2}	P33	N-ch open-drain	−0.3 to +16	V
Output voltage	V_O	P00 to P07, P20 to P27, P30 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, P80 to P87, P90 to P97, C2TX		−0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	ANI00 to ANI70 ANI01 to ANI71	Analog input pin	AV_{SS} − 0.3 to AV_{REF} + 0.3 and −0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin for P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70, P73 to P75, P80 to P87, P90 to P97, C2TX		−10	mA
		Total for all pins		−30	mA
Output current, low[Note]	I_{OL}	Per pin for P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, P80 to P87, P90 to P97, C2TX	Peak value	20	mA
			rms value	10	mA
		P33 pin	Peak value	30	mA
			rms value	15	mA
		Total for all pins	Peak value	100	mA
			rms value	60	mA
Operating ambient temperature	T_A			−40 to +85	$^\circ$C
Storage temperature	T_{stg}			−65 to +150	$^\circ$C

Note The rms value should be calculated as follows: [rms value] = [Peak value] $\times \sqrt{\text{Duty}}$

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

System Clock Oscillator Characteristics (T$_A$ = −40 to +85°C, V$_{DD}$ = 4.5 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f$_X$)[Note 1]		4.0		8.4	MHz
		Oscillation stabilization time[Note 2]				4	ms
Crystal resonator		Oscillation frequency (f$_X$)[Note 1]		4.0		4.2	MHz
		Oscillation stabilization time[Note 2]				10	ms

Notes 1. Indicates only oscillator characteristics.

2. Time required to stabilize oscillation after reset or STOP mode release.

Caution **When using the system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.**

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V$_{SS1}$.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

Remark For the resonator selection and oscillator constant, customers are requested to either evaluate the oscillation themselves or apply to the resonator manufacturer for evaluation.

Capacitance (T$_A$ = 25°C, V$_{DD}$ = V$_{SS}$ = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C$_{IN}$	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
Output capacitance	C$_{OUT}$	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C$_{IO}$	f = 1 MHz Unmeasured pins returned to 0 V.	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, P80 to P87, P90 to P97			15	pF
			P33			20	pF

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T$_A$ = −40 to +85°C, V$_{DD}$ = AV$_{DD}$ = AV$_{REF}$ = 4.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V$_{IH1}$	P21, P25, P31, P34, P40 to P47, P64 to P67, P70 to P73, P80 to P87, P90 to P97		0.7V$_{DD}$		V$_{DD}$	V
	V$_{IH2}$	P00 to P07, P20, P22 to P24, P26, P27, P30, P32, P35, P36, P74, P75, $\overline{\text{RESET}}$		0.8V$_{DD}$		V$_{DD}$	V
	V$_{IH3}$	P50 to P57		2.3		V$_{DD}$	V
	V$_{IH4}$	P33 (N-ch open drain)		0.7V$_{DD}$		15	V
	V$_{IH5}$	X1, X2		V$_{DD}$ − 0.5		V$_{DD}$	V
	V$_{IH6}$	C2RX		0.8V$_{DD}$		V$_{DD}$ + 0.2	V
Input voltage, low	V$_{IL1}$	P21, P25, P31, P34, P40 to P47, P64 to P67, P70 to P73, P80 to P87, P90 to P97		0		0.3V$_{DD}$	V
	V$_{IL2}$	P00 to P07, P20, P22 to P24, P26, P27, P30, P32, P35, P36, P74, P75, C2RX, $\overline{\text{RESET}}$		0		0.2V$_{DD}$	V
	V$_{IL3}$	P50 to P57		0		0.75	V
	V$_{IL4}$	P33 (N-ch open drain)		0		0.3V$_{DD}$	V
	V$_{IL5}$	X1, X2		0		0.4	V
Output voltage, high	V$_{OH1}$	I$_{OH}$ = −1 mA	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70, P73 to P75, P80 to P87, P90 to P97, C2TX	V$_{DD}$ − 1.0		V$_{DD}$	V
	V$_{OH2}$	I$_{OH}$ = −100 μA		V$_{DD}$ − 0.5		V$_{DD}$	V
Output voltage, low	V$_{OL1}$	I$_{OL}$ = 15 mA	P33		0.4	2.0	V
	V$_{OL2}$	I$_{OL}$ = 1.6 mA	P71, P72			0.4	V
	V$_{OL3}$	I$_{OL}$ = 1 mA	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70, P73 to P75, P80 to P87, P90 to P97, C2TX			1.0	V
	V$_{OL4}$	I$_{OL}$ = 500 μA				0.5	V
Input leakage current, high	I$_{LIH1}$	V$_{IN}$ = V$_{DD}$	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, P80 to P87, P90 to P97, C2RX, $\overline{\text{RESET}}$			3	μA
	I$_{LIH2}$		X1			20	μA
	I$_{LIH3}$	V$_{IN}$ = 15 V	P33			80	μA
Input leakage current, low	I$_{LIL1}$	V$_{IN}$ = 0 V	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, P80 to P87, P90 to P97, C2RX, $\overline{\text{RESET}}$			−3	μA
	I$_{LIL2}$		X1			−20	μA
	I$_{LIL3}$		P33			−3**Note**	μA

Note A low-level input leakage current of −200 μA (MAX.) flows through P33 for only 1 clock after executing a read instruction to port 33 (P33). Other than that period, −3 μA (MAX.) flows.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = AV_{REF} = 4.5 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output leakage current, high	I_{LOH}	V_{OUT} = V_{DD}	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70, P73 to P75, P80 to P87, P90 to P97, C2TX			3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V	P00 to P07, P20 to P27, P30 to P36, P40 to P47, P50 to P57, P64 to P67, P70 to P75, P80 to P87, P90 to P97, C2TX			–3	μA
Software pull-up resistance	R_1	V_{IN} = 0 V	P00 to P07, P20 to P27, P30 to P32, P34 to P36, P40 to P47, P50 to P57, P64 to P67, P70, P73 to P75	15	30	90	kΩ
Supply current[Note 1]	I_{DD1}	4.19 MHz crystal oscillation operating mode[Note 2]			4	9	mA
		8.38 MHz crystal oscillation operating mode[Note 2]			8	18	mA
	I_{DD2}	4.19 MHz crystal oscillation HALT mode[Note 3]			400	700	μA
		8.38 MHz crystal oscillation HALT mode[Note 3]			700	1200	μA
	I_{DD3}	STOP mode			0.1	30	μA

Notes 1. Refers to total current flowing to the internal power supplies (V_{DD1} and V_{SS1}). The current flowing to AV_{REF}, AV_{DD}, and the ports (on-chip pull-up resistors) is not included.

2. High-speed mode operation (when the processor clock control register (PCC) is set to 00H)

3. Low-speed mode operation (when the processor clock control register (PCC) is set to 04H). The WTN0 operating current and CLASS2 signal receive wait status operating current (when bit 5 (C2SC1) and bit 4 (C2SC0) of the class 2 clock selection register (C2CLK) are set to 00B) are included.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of port pins.

AC Characteristics

(1) Basic operation (T$_A$ = –40 to +85°C, V$_{DD}$ = 4.5 to 5.5 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Cycle time (minimum instruction execution time)	T$_{CY}$	When using ceramic resonator	0.238		8	μs
		When using crystal resonator	0.476		8	μs
TI000, TI010, TI001, TI011 input high-/low-level width	t$_{TIH0}$ t$_{TIL0}$		2/f$_{sam}$ + 0.1^{Note}			μs
TI50, TI51, TI52 input frequency	f$_{TI5}$		0		2.5	MHz
TI50, TI51, TI52 input high-/low-level width	t$_{TIH5}$ t$_{TIL5}$		160			ns
Interrupt request input high-/low-level width	t$_{INTH}$ t$_{INTL}$	INTP0 to INTP7, P40 to P47	10			μs
$\overline{\text{RESET}}$ low-level width	t$_{RSL}$		10			μs

Note Selection of f$_{sam}$ = f$_X$, f$_X$/4, f$_X$/64 is available with bits 0 and 1 (PRM0n0, PRM0n1) of prescaler mode register 0n (PRM0n). However, if the TI00n valid edge is selected as the count clock, the value becomes f$_{sam}$ = f$_X$/8 (n = 0, 1).

(2) Serial interface (T$_A$ = –40 to +85°C, V$_{DD}$ = 4.5 to 5.5 V)

(a) SIO3 3-wire serial I/O mode (internal clock output): SIO30, SIO31

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK3}}$ cycle time	t$_{KCY1}$		952			ns
$\overline{\text{SCK3}}$ high-/low-level width	t$_{KH1}$, t$_{KL1}$		t$_{KCY1}$/2 − 50			ns
SI3 setup time (to $\overline{\text{SCK3}}\uparrow$)	t$_{SIK1}$		100			ns
SI3 hold time (from $\overline{\text{SCK3}}\uparrow$)	t$_{KSI1}$		400			ns
Delay time from $\overline{\text{SCK3}}\downarrow$ to SO3 output	t$_{KSO1}$	C = 100 pF**Note**			300	ns

Note C is the load capacitance of the $\overline{\text{SCK3}}$ and SO3 output lines.

(b) SIO3 3-wire serial I/O mode (external clock input): SIO30, SIO31

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{SCK3}}$ cycle time	t$_{KCY2}$		800			ns
$\overline{\text{SCK3}}$ high-/low-level width	t$_{KH2}$, t$_{KL2}$		400			ns
SI3 setup time (to $\overline{\text{SCK3}}\uparrow$)	t$_{SIK2}$		100			ns
SI3 hold time (from $\overline{\text{SCK3}}\uparrow$)	t$_{KSI2}$		400			ns
Delay time from $\overline{\text{SCK3}}\downarrow$ to SO3 output	t$_{KSO2}$	C = 100 pF**Note**			300	ns

Note C is the load capacitance of the SO3 output line.

(c) UART0 (dedicated baud rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					131250	bps

(d) UART0 (external clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK0 cycle time	t$_{KCY3}$		800			ns
ASCK0 high-/low-level width	t$_{KH3}$, t$_{KL3}$		400			ns
Transfer rate					39063	bps

(e) I²C bus mode

Parameter		Symbol	Standard Mode		High-Speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{SCL}	0	100	0	400	kHz
Bus free time (between stop and start condition)		t_{BUF}	4.7		1.3		μs
Hold time[Note 1]		$t_{HD:STA}$	4.0		0.6		μs
SCL0 clock low-level width		t_{LOW}	4.7		1.3		μs
SCL0 clock high-level width		t_{HIGH}	4.0		0.6		μs
Start/restart condition setup time		$t_{SU:STA}$	4.7		0.6		μs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	5.0		—	—	μs
	I²C bus		0[Note 2]		0[Note 2]	0.9[Note 3]	μs
Data setup time		$t_{SU:DAT}$	250		100[Note 4]		ns
SDA0 and SCL0 signal rise time		t_R		1000		300	ns
SDA0 and SCL0 signal fall time		t_F		300		300	ns
Stop condition setup time		$t_{SU:STO}$	4.0		0.6		μs
Capacitive load per bus line		Cb		400		400	pF

Notes 1. On start condition output, the first clock pulse is generated after this hold period.

2. To fill the undefined area of the SCL0 falling edge, it is necessary for the device to provide at least 300 ns of hold time internally for the SDA0 signal (on $V_{IHmin.}$ of SCL0 signal).

3. If the device does not extend the SCL0 signal low hold time (t_{LOW}), only the maximum data hold time $t_{HD:DAT}$ needs to be satisfied.

4. The high-speed mode I²C bus is available in the standard mode I²C bus system. At this time, the conditions described below must be satisfied.
- If the device does not extend the SCL0 signal low state hold time
  $t_{SU:DAT} \geq 250$ ns
- If the device extends the SCL0 signal low state hold time
  Be sure to transmit the next data bit to the SDA0 line before the SCL0 line is released ($t_{Rmax.} + t_{SU:DAT}$ = 1000 + 250 = 1250 ns by standard mode I²C bus specification).

(3)   CLASS2 (T$_A$ = –40 to +85°C, V$_{DD}$ = 4.5 to 5.5 V)

(a)   Internal clock count limit

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Internal clock cycle time	t$_{CCLK}$		467		510	ns

(b)   In normal mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Rise time propagation delay (from C2TX$\uparrow$ to C2RX$\uparrow$)	t$_{PDR}$				62t$_{CCLK}$	μs
Fall time propagation delay (from C2TX$\downarrow$ to C2RX$\downarrow$)	t$_{PDF}$				62t$_{CCLK}$	μs

(c)   In quadruple-speed mode

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Rise time propagation delay (from C2TX$\uparrow$ to C2RX$\uparrow$)	t$_{PDRX}$				8t$_{CCLK}$	μs
Fall time propagation delay (from C2TX$\downarrow$ to C2RX$\downarrow$)	t$_{PDFX}$				8t$_{CCLK}$	μs

(d)   Transmission/reception pulse width (in normal mode)

Symbol	t$_{XMIN}$	t$_{XNOM}$	t$_{XMAX}$	t$_{RMIN}$	t$_{RMAX}$	Unit
When Passive: 0, Active: 1	60	64	68	37	91 or below	μs
When Passive: 1, Active: 0	122	128	134	100	157 or below	μs
When Active is SOF	193	200	207	170	230	μs
When Passive is EOF	271	280	289	249	320 or below	μs
Idle point				320 or above	8t$_{CCLK}$	μs
When Active is Break	768			249 or above		μs

(e)   Transmission/reception pulse width (in quadruple-speed mode)

Symbol	t$_{XMIN}$	t$_{XNOM}$	t$_{XMAX}$	t$_{RMIN}$	t$_{RMAX}$	Unit
When Passive: 0, Active: 1	15	16	17	10	22	μs
When Passive: 1, Active: 0	30	32	34	25	39	μs
When Active is SOF	48	50	52	43	57	μs
When Passive is EOF	68	70	72	63	80	μs
Idle point				80	8t$_{CCLK}$	μs
When Passive: 0, Active: 1	768			63		μs

AC Timing Test Points (Excluding X1 Input)

0.8V$_{DD}$

0.2V$_{DD}$

Test points

0.8V$_{DD}$

0.2V$_{DD}$

Clock Timing

$1/f_X$

t_{XL}　　t_{XH}

X1 input

V_{IH5} (MIN.)
V_{IL5} (MAX.)

TI Timing

t_{TIL0}　　t_{TIH0}

TI000, TI010, TI001, TI011

$1/f_{TI5}$

t_{TIL5}　　t_{TIH5}

TI50, TI51, TI52
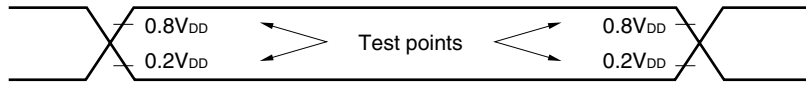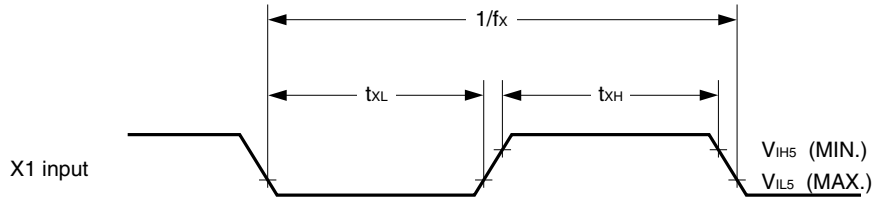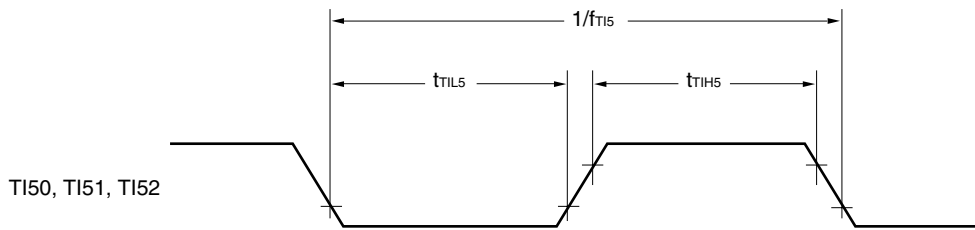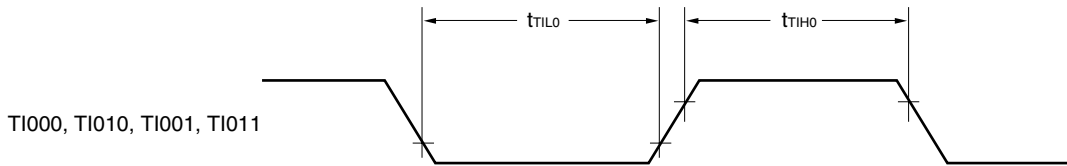
Interrupt Request Input Timing

t_{INTL}　　t_{INTH}

INTP0 to INTP7
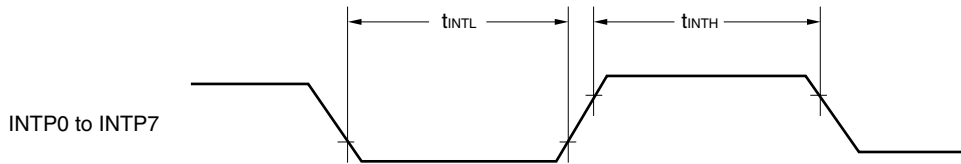
RESET Input Timing

t_{RSL}

RESET
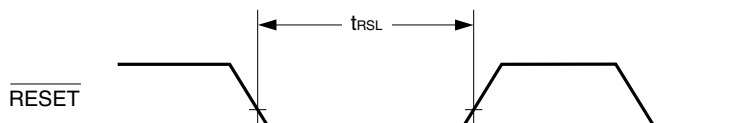
Serial Transfer Timing

3-wire serial I/O mode:
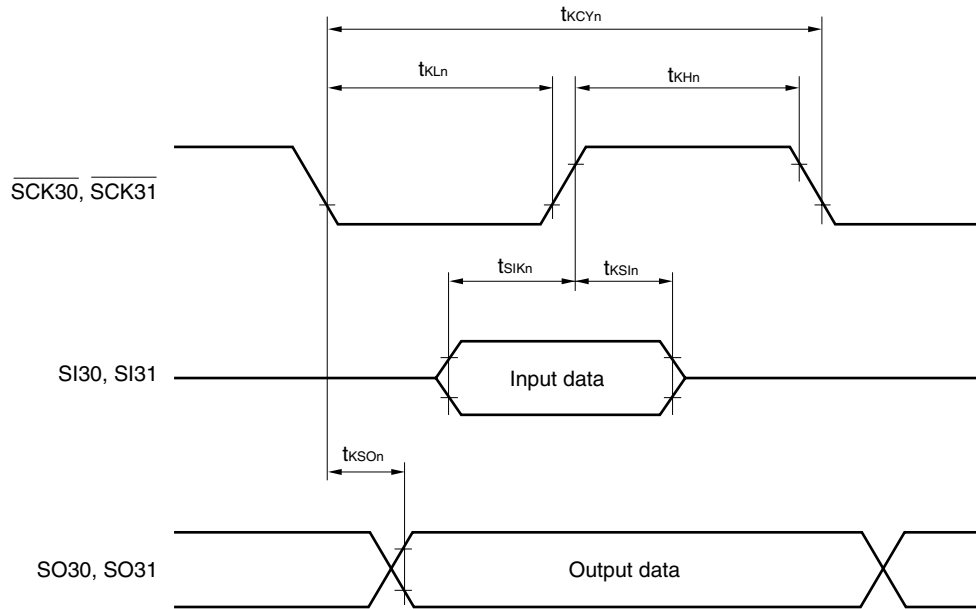
UART mode (external clock input):
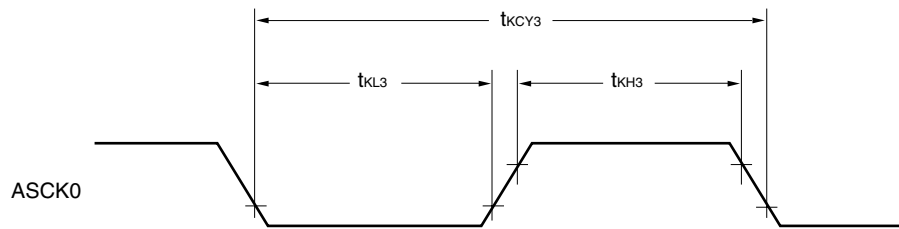
I²C bus mode:
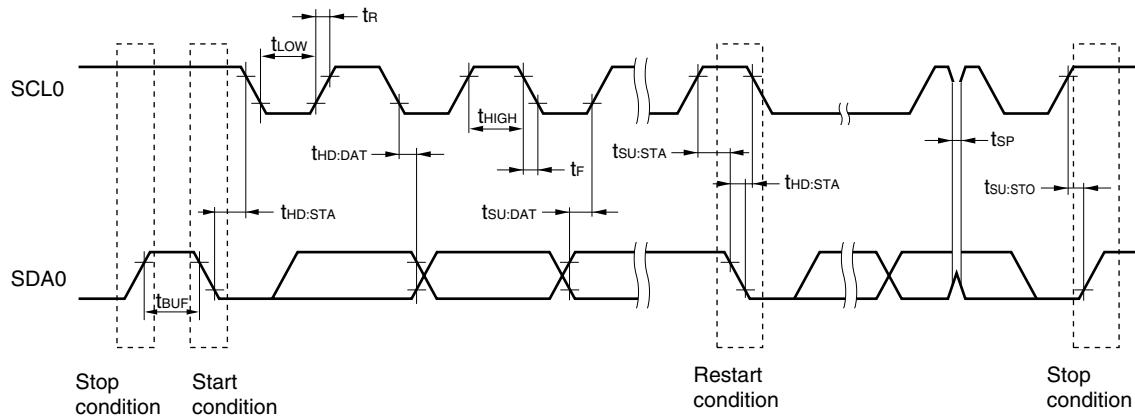
CLASS2 propagation waveform (example of short pulse width)

C2TX

t_{PDR} 64 μs–t_{PDF} t_{PDF} 64 μs–t_{PDR} t_{PDR}

C2RX

64 μs   64 μs

C2TX

t_{PDRX} 16 μs–t_{PDFX} t_{PDFX} 16 μs–t_{PDRX} t_{PDRX}

C2RX

16 μs   16 μs
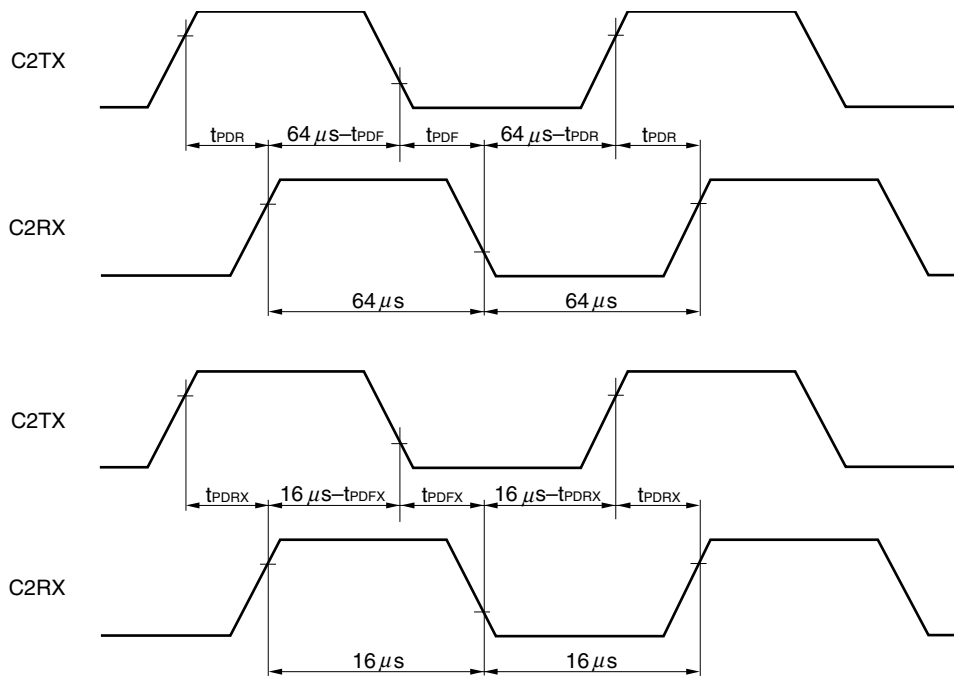
Remarks 1. The meanings of the symbols in the above figure are as follows:

     t_{PDR}:   Rise time propagation delay in normal mode of the CLASS2 transceiver

     t_{PDF}:   Fall time propagation delay in normal mode of the CLASS2 transceiver

     t_{PDRX}: Rise time propagation delay in quadruple-speed mode of the CLASS2 transceiver

     t_{PDFX}: Fall time propagation delay in quadruple-speed mode of the CLASS2 transceiver

   2. The values of t_{PDR}, t_{PDF}, t_{PDRX}, and t_{PDFX}, can be specified using the class 2 rise time propagation delay correction register (C2PDR) and class 2 fall time propagation delay correction register (C2PDF).

A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = AV_{REF} = 4.5 to 5.5 V, V_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error**Note**					±0.6	%FSR
Conversion time	t_{CONV}		14		100	μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
AV_{REF} resistance	R_{AIREF}		9.5	15	37	kΩ

Note Excludes quantization error (±0.2%FSR). It is indicated as a ratio to the full-scale value.

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		2.0		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{\text{RESET}}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note**		ms

Note Selection of $2^{12}/f_X$, $2^{14}/f_X$, $2^{15}/f_X$, $2^{16}/f_X$, and $2^{17}/f_X$ is possible with bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Data Retention Timing (STOP Mode Release by $\overline{\text{RESET}}$)
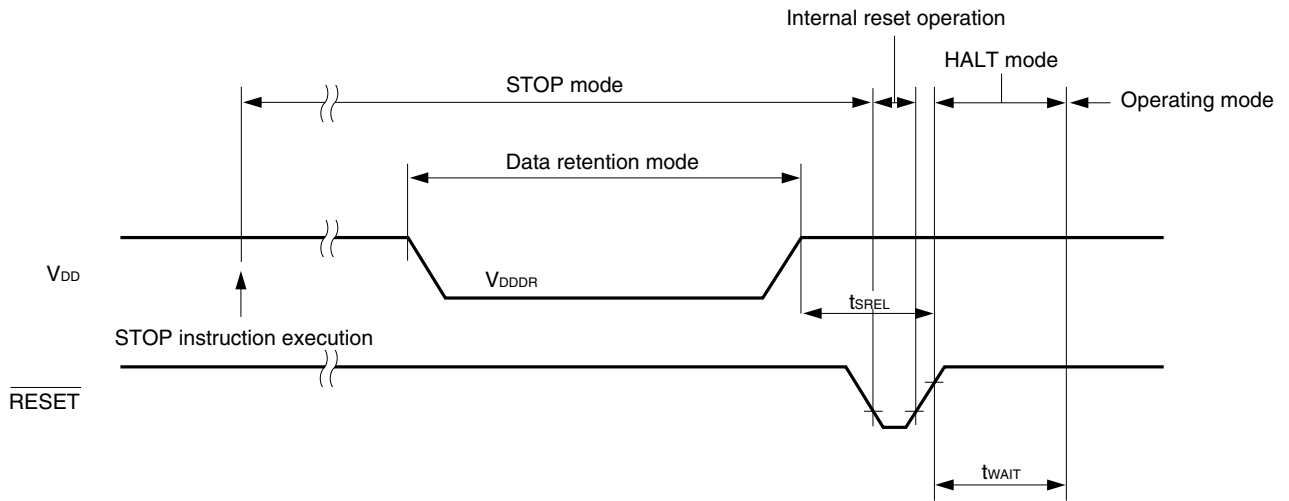
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)

NEC
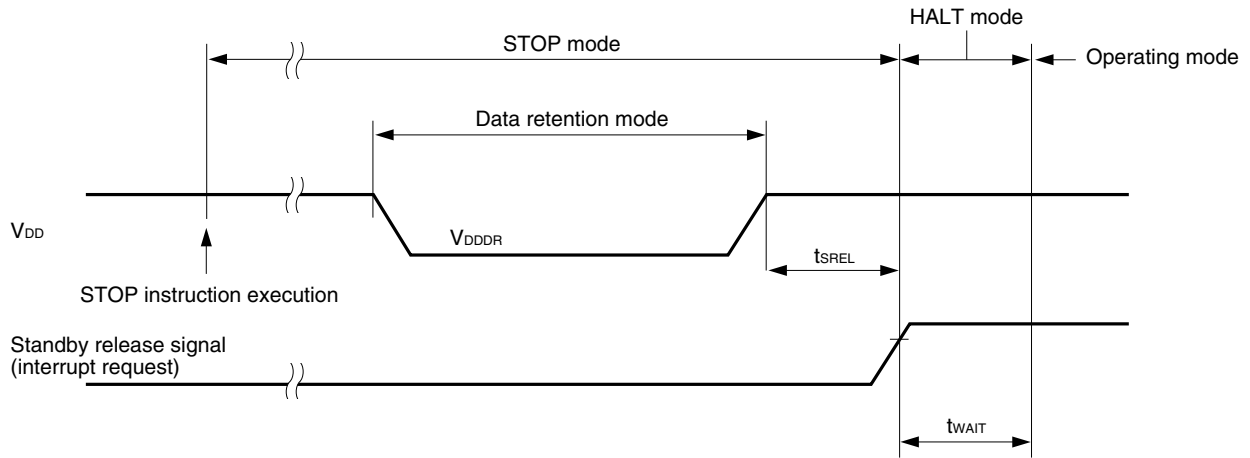
11. PACKAGE DRAWING

80-PIN PLASTIC QFP (14x14)

detail of lead end
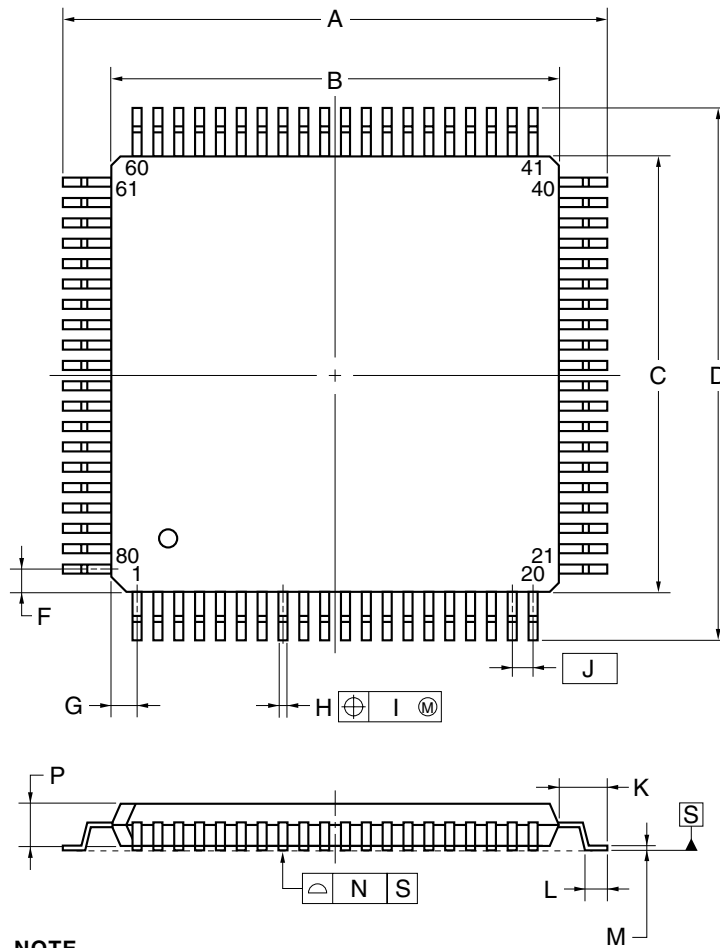
NOTE

Each lead centerline is located within 0.13 mm of
its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.20±0.20
B	14.00±0.20
C	14.00±0.20
D	17.20±0.20
F	0.825
G	0.825
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.60±0.20
L	0.80±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.40±0.10
Q	0.125±0.075
R	$3°^{+7°}_{-3°}$
S	1.70 MAX.

P80GC-65-8BT-1

12. RECOMMENDED SOLDERING CONDITIONS

For the solder mounting method and soldering conditions of the μPD780833Y, contact an NEC sales representative.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD780833Y.
Also refer to **(5) Cautions on using development tools**.

(1) Language processing software

RA78K0	Assembler package common to 78K/0 Series
CC78K0	C compiler package common to 78K/0 Series
DF780833	Device file for μPD780833Y Subseries
CC78K0-L	C compiler library source file common to 78K/0 Series

(2) Flash memory writing tools

Flashpro II (Part No.: FL-PR2) Flashpro III (Part No.: FL-PR3, PG-FP3)	Flash programmer dedicated to on-chip flash memory microcontrollers
FA-80GC	Adapter for flash memory writing used by connecting the Flashpro II or Flashpro III. This is for 80-pin plastic QFP (GC-8BT type).

(3) Debugging tool
   • When using in-circuit emulator IE-78K0-NS

IE-78K0-NS	In-circuit emulator common to 78K/0 Series
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-70000-98-IF-C	Interface adapter when using PC-9800 series as host machine (excluding notebook PCs) (C bus supported)
IE-70000-CD-IF-A	PC card and interface cable when using notebook PC as host machine (PCMCIA socket supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT™ compatible as host machine (ISA bus supported)
IE-70000-PCI-IF-A	Adapter necessary when using on-chip PCI bus PC as host machine
IE-780833-NS-EM4	Emulation board to emulate μPD780833Y Subseries
IE-78K0-NS-P02	I/O board necessary when using IE-780833-NS-EM4
NP-80GC	Emulation probe for 80-pin plastic QFP (GC-8BT type)
EV-9200GC-80	Conversion socket to connect target system on which an 80-pin plastic QFP (GC-8BT type) can be mounted and NP-80GC
ID78K0-NS	Integrated debugger for IE-78K0-NS
SM78K0	System simulator common to 78K/0 Series
DF780833	Device file for μPD780833Y Subseries

• **When using in-circuit emulator IE-78001-R-A**

IE-78001-R-A	In-circuit emulator common to 78K/0 Series
IE-70000-98-IF-C	Interface adapter when using PC-9800 series as host machine (excluding notebook PCs) (C bus supported)
IE-70000-PC-IF-C	Interface adapter when using IBM PC/AT compatible as host machine (ISA bus supported)
IE-70000-PCI-IF-A	Adapter necessary when using on-chip PCI bus PC as host machine
IE-78000-R-SV3	Interface adapter and cable when using EWS as host machine
IE-780833-NS-EM4	Emulation board to emulate μPD780833Y Subseries
IE-78K0-NS-P02	I/O board necessary when using IE-780833-NS-EM4
IE-78K0-R-EX1	Emulation probe conversion board necessary to use IE-780833-NS-EM4 + IE-78K0-NS-P02 on IE-78001-R-A
EP-78230GC-R	Emulation probe for 80-pin plastic QFP (GC-8BT type)
EV-9200GC-80	Conversion socket to connect target system board manufactured for 80-pin plastic QFP (GC-8BT type) and EP-78230GC-R
ID78K0	Integrated debugger for IE-78001-R-A
SM78K0	System simulator common to 78K/0 Series
DF780833	Device file for μPD780833Y Subseries

(4) Real-time OS

RX78K0	Real-time OS for 78K/0 Series
MX78K0	OS for 78K/0 Series

(5) Cautions on using development tools
- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780833.
- The CC78K0 and RX78K0 are used in combination with the RA78K0 and the DF780833.
- The FL-PR2, FL-PR3, FA-80GC, and NP-80GC are products of Naito Densei Machida Mfg. Co., Ltd. (+81-44-822-3813).
- For third-party development tools, see the **Single-chip Microcontroller Development Tool Selection Guide (U11069E)**.
- The host machines and OSs supporting each software are as follows.

Host Machine [OS] / Software	PC PC-9800 series [Japanese Windows^{TM}] IBM PC/AT compatible [Japanese/English Windows]	EWS HP9000 series 700^{TM} [HP-UX^{TM}] SPARCstation^{TM} [SunOS^{TM}, Solaris^{TM}] NEWS^{TM} (RISC) [NEWS-OS^{TM}]
RA78K0	$\sqrt{}$ **Note**	$\sqrt{}$
CC78K0	$\sqrt{}$ **Note**	$\sqrt{}$
ID78K0-NS	$\sqrt{}$	—
ID78K0	$\sqrt{}$	$\sqrt{}$
SM78K0	$\sqrt{}$	—
RX78K0	$\sqrt{}$ **Note**	$\sqrt{}$
MX78K0	$\sqrt{}$ **Note**	$\sqrt{}$

Note DOS-based software

Conversion Socket (EV-9200GC-80) Drawing and Footprints

Figure A-1. EV-9200GC-80 Drawing (for Reference Only)

No.1 pin index
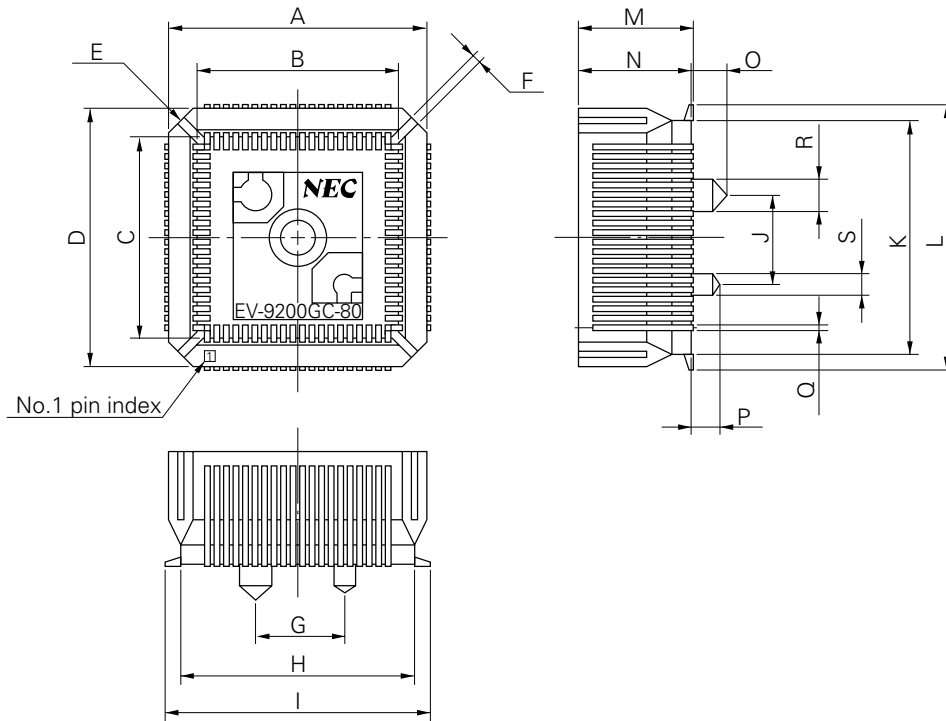
EV-9200GC-80-G1E

ITEM	MILLIMETERS	INCHES
A	18.0	0.709
B	14.4	0.567
C	14.4	0.567
D	18.0	0.709
E	4-C 2.0	4-C 0.079
F	0.8	0.031
G	6.0	0.236
H	16.0	0.63
I	18.7	0.736
J	6.0	0.236
K	16.0	0.63
L	18.7	0.736
M	8.2	0.323
N	8.0	0.315
O	2.5	0.098
P	2.0	0.079
Q	0.35	0.014
R	ϕ2.3	ϕ0.091
S	ϕ1.5	ϕ0.059

Figure A-2. EV-9200GC-80 Footprints (for Reference Only)
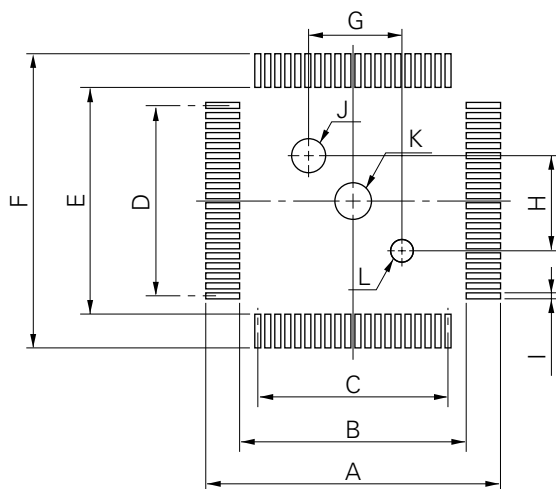
EV-9200GC-80-P1E

ITEM	MILLIMETERS	INCHES
A	19.7	0.776
B	15.0	0.591
C	$0.65\pm0.02 \times 19 = 12.35\pm0.05$	$0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$
D	$0.65\pm0.02 \times 19 = 12.35\pm0.05$	$0.026^{+0.001}_{-0.002} \times 0.748 = 0.486^{+0.003}_{-0.002}$
E	15.0	0.591
F	19.7	0.776
G	6.0 ± 0.05	$0.236^{+0.003}_{-0.002}$
H	6.0 ± 0.05	$0.236^{+0.003}_{-0.002}$
I	0.35 ± 0.02	$0.014^{+0.001}_{-0.001}$
J	$\phi2.36\pm0.03$	$\phi0.093^{+0.001}_{-0.002}$
K	$\phi2.3$	$\phi0.091$
L	$\phi1.57\pm0.03$	$\phi0.062^{+0.001}_{-0.002}$

Caution   Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (C10535E).

APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to devices

Document Name	Document No.
μPD780833Y Subseries User's Manual	U13892E
μPD780833Y Data Sheet	This document
μPD78F0833Y Data Sheet	U15013E
78K/0 Series User's Manual Instructions	U12326E

Documents related to development tools (user's manuals)

Document Name		Document No.
RA78K0 Assembler Package	Operation	U11802E
	Language	U11801E
	Structured Assembly Language	U11789E
CC78K0 C Compiler	Operation	U11517E
	Language	U11518E
IE-78K0-NS		U13731E
IE-78K0-R-EX1		To be prepared
IE-780833-NS-EM4		To be prepared
SM78K0S, SM78K0 System Simulator Windows Based	Operation	U14611E
SM78K Series System Simulator Ver. 2.10 or later	External Part User Open Interface Specifications	To be prepared
ID78K0-NS Integrated Debugger Ver. 2.00 or later Windows Based	Operation	U14379E
ID78K0 Integrated Debugger Windows Based	Guide	U11649E
	Reference	U11539E

Caution   The related documents listed above are subject to change without notice. Be sure to read the latest version of each document before designing.

Documents related to embedded software (user's manuals)

Document Name		Document No.
78K/0 Series Real-time OS	Fundamentals	U11537E
	Installation	U11536E
78K/0 Series OS MX78K0	Fundamental	U12257E

Other related documents

Document Name	Document No.
SEMICONDUCTOR SELECTION GUIDE Products & Packages (CD-ROM)	X13769X
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

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NOTES FOR CMOS DEVICES

① **PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② **HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ **STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability

- Ordering information

- Product release schedule

- Availability of related technical literature

- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)

- Network requirements

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