ADS92x4R Dual, Low Latency, Simultaneous-Sampling SAR ADC

1 Features

- High Resolution, High Throughput:
  - ADS9224R: 16 Bit, 3 MSPS
  - ADS9234R: 14 Bit, 3 MSPS
- Fast Response Time With Low Latency: 333 ns
- Higher Performance Over Wide Analog Bandwidth:
  - ADS9224R: 83-dB SINAD at 1.4 MHz
  - ADS9234R: 80-dB SINAD at 1.4 MHz
- Two Simultaneously Sampled channels
- Unipolar, Fully Differential Inputs
- Wide Common-Mode Voltage Range
- Excellent DC and AC Performance:
  - ADS9224R:
    - 16-Bit NMC DNL, ±2-LSB Max INL
    - 93.5-dB SNR, –110-dB THD
    - 80-dB CMRR
  - ADS9234R:
    - 14-Bit NMC DNL, ±1-LSB Max INL
    - 85.6-dB SNR, –106-dB THD
    - 75-dB CMRR
- Integrated Reference and Reference Buffers
- Integrated REFby2 Buffer for Setting Common Mode
- Integrated Data Averaging
- Enhanced-SPI Interface for MCUs and FPGAs:
  - Wide Read Cycle to Read Data With MCUs
  - CRT for Data Transfers With Digital Isolators
  - DDR Modes for FPGAs
- Parallel Byte Mode for Easy Interface
- Extended Temperature Range: –40°C to +125°C
- Small Footprint: 5-mm × 5-mm VQFN

2 Applications

- Optical Encoders: Incremental and Absolute
- SONAR Receivers
- Optical Networking: EDFA Gain Control Loop
- Power Quality Measurement
- Digital Power Supply
- I/Q Demodulators
- Medical Imaging: CT Scanners, MRI Scanners

3 Description

The ADS92x4R is a pin-compatible, high-speed, dual, simultaneous-sampling, analog-to-digital converters (ADC) with an integrated reference and reference buffer. The device can operate on a single 5-V supply and supports unipolar, fully differential analog input signals with excellent DC and AC specifications.

The device supports SPI-compatible serial (enhanced-SPI) and byte-wide parallel interfaces, making the device easy to pair with a diversity of microcontrollers, digital signal processors (DSPs), and field-programmable gate arrays (FPGAs).

The device comes in a space-saving, 5-mm × 5-mm, VQFN package. The ADS92x4R is specified for the extended temperature range of –40°C to +125°C.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS92x4R	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

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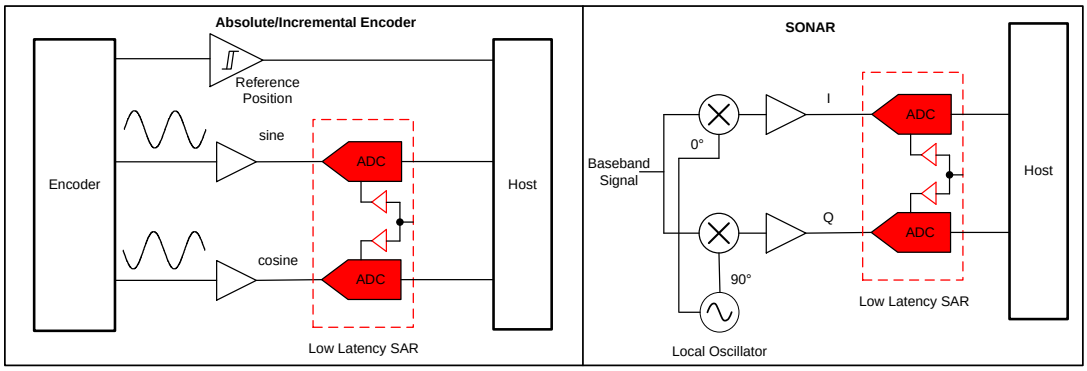
Typical Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2018	*	Initial release.

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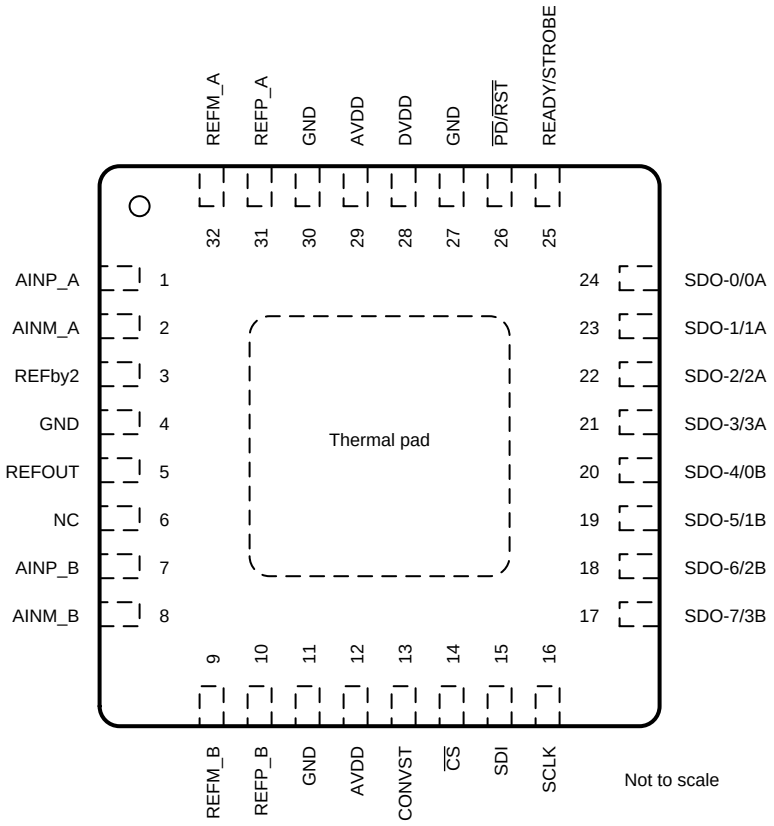
5 Pin Configuration and Functions

RHB Package
5-mm × 5-mm, 32-Pin VQFN
Top View



Pin Functions

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
AINM_A	2	Analog input	Negative analog input for channel A.
AINP_A	1	Analog input	Positive analog input for channel A.
AINM_B	8	Analog input	Negative analog input for channel B.
AINP_B	7	Analog input	Positive analog input for channel B.
AVDD	12, 29	Power supply	Analog power-supply pin. Connect a 1-µF decoupling capacitor between pin 12 and pin 11. Connect pins 12 and 29 together. Connect a 1-µF decoupling capacitor between pin 29 and pin 30.
CONVST	13	Digital input	Conversion start input pin. A CONVST rising edge starts the conversion for ADC_A and ADC_B.
$\overline{CS}$	14	Digital input	Chip-select input pin; active low. The device takes control of the data bus when $\overline{CS}$ is low. The SDO-x pins go to Hi-Z when $\overline{CS}$ is high.
DVDD	28	Power supply	Interface power-supply pin. Connect a 1-µF decoupling capacitor between pin 27 and pin 28.
GND	4, 11, 27, 30	Power supply	Ground
NC	6	—	No external connection
$\overline{PD}/\overline{RST}$	26	Digital input	Asynchronous reset or power-down input pin. See the *Reset or Power-Down* section.
READY/STROBE	25	Digital output	Indicates data ready or strobe output for data capture.

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Pin Functions (continued)

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
REFby2	3	Analog output	REFby2 buffer output. Connect a 1-µF decoupling capacitor between pin 3 and pin 4.
REFOUT	5	Analog output	Internal reference output. Connect a 1-µF decoupling capacitor between pin 5 and pin 4.
REFM_A	32	Analog output	Negative output of reference buffer A. Negative reference input for ADC_A. Externally connect to the device GND.
REFM_B	9	Analog output	Negative output of reference buffer B. Negative reference input for ADC_B. Externally connect to the device GND.
REFP_A	31	Analog output	Positive output of reference buffer A. Positive reference input for ADC_A. Connect a 10-µF decoupling capacitor between pin 31 and pin 32.
REFP_B	10	Analog output	Positive output of reference buffer B. Positive reference input for ADC_B. Connect a 10-µF decoupling capacitor between pin 9 and pin 10.
SCLK	16	Digital input	Clock input pin for the serial interface.
SDI	15	Digital input	Serial data input pin. This pin is used to program the device registers.
SDO-0/0A	24	Digital output	SPI mode: data output 0 for channel A. Parallel byte mode: least significant bit (LSB) from the data byte.
SDO-1/1A	23	Digital output	SPI mode: data output 1 for channel A. Parallel byte mode: LSB+1 from the data byte.
SDO-2/2A	22	Digital output	SPI mode: data output 2 for channel A. Parallel byte mode: LSB+2 from the data byte.
SDO-3/3A	21	Digital output	SPI mode: data output 3 for channel A. Parallel byte mode: LSB+3 from the data byte.
SDO-4/0B	20	Digital output	SPI mode: data output 0 for channel B. Parallel byte mode: LSB+4 from the data byte.
SDO-5/1B	19	Digital output	SPI mode: data output 1 for channel B. Parallel byte mode: LSB+5 from the data byte.
SDO-6/2B	18	Digital output	SPI mode: data output 2 for channel B. Parallel byte mode: LSB+6 from the data byte.
SDO-7/3B	17	Digital output	SPI mode: data output 3 for channel B. Parallel byte mode: most significant bit (MSB) from the data byte.
Thermal pad	Pad	Power supply	Exposed thermal pad. TI recommends connecting this pin to the printed circuit board (PCB) ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Analog supply voltage	AVDD to GND	–0.3	6	V
Digital supply voltage	DVDD to GND	–0.3	6	V
Digital input voltage	$\overline{CS}$, CONVST, SDI, SCLK, $\overline{PD}$/$\overline{RST}$ to GND	–0.3	DVDD + 0.3	V
Analog input voltage	AINP_A, AINP_B to GND	–0.3	AVDD + 0.3	V
Analog input voltage	AINM_A, AINM_B to GND	–0.3	AVDD + 0.3	V
Input or output current to any pin except power supply pin		–10	10	mA
Maximum virtual junction temperature	T_J		150	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Analog supply voltage	4.5	5	5.5	V
DVDD	Digital supply voltage operating range	1.65	3.3	5.5	V
	Digital supply voltage for SCLK > 20 MHz	2.35	3.3	5.5	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		ADS92x4R RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	29	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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6.5 Electrical Characteristics: ADS92x4R

all minimum and maximum specifications are at T_A = –40°C to +125°C, AVDD = 4.5 V to 5.5 V, DVDD = 2.35 to 5.5 V and f_{SAMPLE} = 3 MSPS (unless otherwise noted); Typical values are at T_A= 25°C, AVDD = 5 V, and DVDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
FSR	Full-scale input voltage (1)	V_{REF} = 2.5 V	-4.096		4.096	V
V_{IN}	Absolute input voltage (AINP or AINM to GND)	V_{REF} = 2.5 V	0		4.096	V
V_{CM}	Common-mode input range	V_{REF} = 2.5 V	1.848		2.248	V
I_{IN}	Analog input leakage current			±1		µA
C_i	Input capacitance	Sample Mode		16		pF
		Hold Mode		1		
SAMPLING DYNAMICS						
t_{CYCLE}	Cycle time		333			ns
f_{SAMPLE}	Sampling rate				3	MSPS
t_{ACQ}	Acquisition time		140			ns
t_A	Aperture delay			8		ns
	t_A mismatch			40		ps
t_{JITTER}	Aperture jitter			2		ps
BW	Analog input bandwidth	-3dB Input Signal		100		MHz
		-0.1 dB Input Signal		20		MHz
VOLTAGE REFERENCE OUTPUT						
V_{REF} (2)	REFOUT voltage	T_A = 25°C	2.498	2.5	2.502	V
$\Delta V_{REF}/\Delta T$	V_{REF} drift			5	20	ppm/°C
$\Delta V_{REF}/\Delta AVDD$	V_{REF} line regulation	AVDD variation 4.5 V to 5.5 V		200		µV/V
I_{REFOUT}	REFOUT output current capability	$\lvert\Delta V_{REF}\rvert$ < 2 mV		1.5		µA
C_{REFOUT}	REFOUT capacitor	For specified performance		1		µF
$t_{wkup-\ REFOUT}$	REFOUT wake-up time	C_{REFOUT} = 1 µF		10		ms
INTERNAL REFERENCE BUFFER						
G_{REFBUF}	Reference buffer Gain			1.6384		V/V
$E_{O-REFBUF}$	Reference buffer output offset (V_{REFP_x} - V_{REF})	At T_A = 25°C		±500		µV
		T_A = -40°C to 125°C	–1	0	1	mV
$\Delta E_{O-REFBUF}/\Delta T$	Reference buffer output offset temperature drift			10		µV/°C
(V_{REFP_A} - V_{REFP_B})	Reference buffer output mismatch	T_A = -40°C to 125°C	–500	±50	500	µV
C_{REFP_x}	Reference buffer output capacitor	For specified performance, between each pair of REFP and REFM	7	10	27	µF
$t_{REFBUF-SETTLE}$	Reference buffer output settling time	C_{REFP_x} = 10 µF		25		ms
REFby2 OUTPUT						
V_{REFby2}	REFby2 uutput voltage	EN_REFBY2_OFFSET = 0, V_{REF} = 2.5 V	2.043	2.048	2.053	V
		EN_REFBY2_OFFSET = 1, V_{REF} = 2.5 V	2.133	2.148	2.163	V
I_{REFby2}	REFby2 output current capability			±3		mA
	REFby2 output capacitor		1			µF

(1) Ideal input span; does not include gain or offset error.
(2) Does not include the variation in voltage resulting from solder shift effects.

Electrical Characteristics: ADS92x4R (continued)

all minimum and maximum specifications are at T_A = –40°C to +125°C, AVDD = 4.5 V to 5.5 V, DVDD = 2.35 to 5.5 V and f_{SAMPLE} = 3 MSPS (unless otherwise noted); Typical values are at T_A= 25°C, AVDD = 5 V, and DVDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	REFby2 output noise	With specified output capacitor		10		μV_{RMS}
Digital Outputs						
V_{OH}	High level output voltage	I_{OH} = 500 µA source	0.8 × DVDD		DVDD	V
V_{OL}	Low level output voltage	I_{OL} = 500 µA sink	0		0.2 × DVDD	V
Digital Inputs						
V_{IH}	High level input voltage	DVDD > 2.3 V	0.7 × DVDD		DVDD +0.3	V
V_{IL}	Low level intput voltage	DVDD > 2.3 V	–0.3		0.3 × DVDD	V
V_{IH}	High level input voltage	DVDD ≤ 2.3 V	0.8 × DVDD		DVDD +0.3	V
V_{IL}	Low level intput voltage	DVDD ≤ 2.3 V	–0.3		0.2 × DVDD	V
Power Supply						
AVDD	Analog supply voltage		4.5	5	5.5	V
DVDD	Digital supply voltage		1.65	3.3	5.5	V
I_{AVDD}	Analog supply current	AVDD = 5 V, f_{SAMPLE} = 3 MSPS		24		mA
		AVDD = 5 V, No Conversion		8		mA
		AVDD = 5 V, Power down ($\overline{PD}/\overline{RST}$ Low)		1		µA
I_{DVDD}	Digital supply current	DVDD = 3.3 V, $C_{SDO-x/y}$ = 10 pF		0.75		mA
PSRR(3)	Power supply rejection ratio	100mVp-p Ripple on AVDD of frequency < 100kHz		70		dB

(3) All specifications expressed in decibels (dB) refer to the full-scale input (FSR) and are tested with an input signal 0.5 dB below full-scale, unless otherwise specified.

6.6 Electrical Characteristics: ADS9224R

all minimum and maximum specifications are at T_A = –40°C to +125°C, AVDD = 4.5 V to 5.5 V, DVDD = 2.35 to 5.5 V, and f_{SAMPLE} = 3 MSPS (unless otherwise noted); Typical values are at T_A= 25°C, AVDD = 5 V, and DVDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ACCURACY						
	Resolution, no missing codes		16			bit
DNL	Differential nonlinearity		–0.99	±0.5	0.99	LSB
INL	Integral nonlinearity		–2	±1	2	LSB
E_O	Offset error		–6	±1	6	LSB
G_E	Cummulative gain error for ADC_x and REFBUF_x		–0.05	±0.01	0.05	%FSR
$\Delta G_E/\Delta T$	Gain drift			5		ppm/°C
	Transition noise	Mid-code, PFS-1000, NFS+1000		TBD		LSB
CMRR(1)	Common-mode rejection ratio	F_{IN} = dc to 1-MHz, V_{IN} = 100 mVp-p		80		dB
AC ACCURACY						
SNR(1)	Signal-to-noise ratio	F_{IN} = 2 kHz	89	93.5		dB
		F_{IN} = 100 kHz		90.5		dB
		F_{IN} = 1400 kHz		88.5		dB

(1) All specifications expressed in decibels (dB) refer to the full-scale input (FSR) and are tested with an input signal 0.5 dB below full-scale, unless otherwise specified.

ADVANCE INFORMATION

Electrical Characteristics: ADS9224R (continued)

all minimum and maximum specifications are at T_A = –40°C to +125°C, AVDD = 4.5 V to 5.5 V, DVDD = 2.35 to 5.5 V, and f_{SAMPLE} = 3 MSPS (unless otherwise noted); Typical values are at T_A= 25°C, AVDD = 5 V, and DVDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SINAD(1) (2)	Signal-to-noise plus distortion	F_{IN} = 2 kHz		90.8		dB
		F_{IN} = 100 kHz		90.3		dB
		F_{IN} = 1400 kHz		83		dB
THD(1) (2)	Total harmonic distortion	F_{IN} = 2 kHz		–110		dB
		F_{IN} = 100 kHz		–105		dB
		F_{IN} = 1400 kHz		-85		dB
SFDR(1)	Spurious-free dynamic range	F_{IN} = 2 kHz		115		dB
		F_{IN} = 100 kHz		110		dB
		F_{IN} = 1400 kHz		90		dB
ISOXT(1)	Channel-to-channel isolation	F_{IN_ADCA} = 15 kHz at 10% FSR, F_{IN_ADCB} = 25 kHz at 100% FSR		–110		dB

(2) Calculated on the first nine harmonics of the input frequency.

6.7 Electrical Characteristics: ADS9234R

all minimum and maximum specifications are at T_A = –40°C to +125°C, AVDD = 4.5 V to 5.5 V, DVDD = 2.35 to 5.5 V, and f_{SAMPLE} = 3 MSPS (unless otherwise noted); Typical values are at T_A= 25°C, AVDD = 5 V, and DVDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ACCURACY						
	Resolution, no missing codes		14			bit
DNL	Differential nonlinearity		–0.99	±0.15	0.99	LSB
INL	Integral nonlinearity		–1	±0.3	1	LSB
E_O	Offset error		–2.5	±0.8	2.5	LSB
G_E	Cummulative gain error for ADC_x and REFBUF_x		–0.05	±0.01	0.05	%FSR
$\Delta G_E/\Delta T$	Gain drift			5		ppm/°C
	Transition noise	Mid-code, PFS-1000, NFS+1000		TBD		LSB
CMRR(1)	Common mode rejection ratio	F_{IN} = dc to 1-MHz, V_{IN} = 100 mVp-p		75		dB
AC ACCURACY						
SNR(1)	Signal-to-noise ratio	F_{IN} = 2 kHz	82	85.6		dB
		F_{IN} = 100 kHz		84		dB
		F_{IN} = 1400 kHz		82		dB
SINAD(1) (2)	Signal-to-noise plus distortion	F_{IN} = 2 kHz		85.6		dB
		F_{IN} = 100 kHz		84		dB
		F_{IN} = 1400 kHz		80		dB
THD(1) (2)	Total harmonic distortion	F_{IN} = 2 kHz		–106		dB
		F_{IN} = 100 kHz		–105		dB
		F_{IN} = 1400 kHz		–85		dB
SFDR(1)	Spurious-free dynamic range	F_{IN} = 2 kHz		108		dB
		F_{IN} = 100 kHz		107		dB
		F_{IN} = 1400 kHz		90		dB
ISOXT(1)	Channel-to-channel isolation	F_{IN_ADCA} = 15 kHz at 10% FSR, F_{IN_ADCB} = 25 kHz at 100% FSR		–110		dB

(1) All specifications expressed in decibels (dB) refer to the full-scale input (FSR) and are tested with an input signal 0.5 dB below full-scale, unless otherwise specified.
(2) Calculated on the first nine harmonics of the input frequency.

ADVANCE INFORMATION

6.8 Timing Requirements

all minimum and maximum specifications are at T_A = –40°C to +125°C, AVDD = 4.5 V to 5.5 V, DVDD = 2.35 V to 5.5 V, and f_{SAMPLE} = 3 MSPS (unless otherwise noted); typical values are at T_A = 25°C, AVDD = 5 V, and DVDD = 3.3 V

		MIN	NOM	MAX	UNIT
Conversion Control and Data Transfer (See Figure 1 and Figure 2)					
$t_{D\_CONVST\_CS}$	Delay time: CONVST high to $\overline{CS}$ Falling for zero cycle latency (zone 1 transfer)	t_{DRDY} (1)			ns
$t_{D\_CONVST\_CS}$	Delay time: CONVST high to $\overline{CS}$ falling for zone 2 transfer	15		180	ns
t_{WL_CONVST}	Pulse duration : CONVST low	15			ns
t_{WH_CONVST}	Pulse duration : CONVST high	15			ns
t_{CYCLE}	Time between two adjacent CONVST rising edges for zero cycle latency (zone 1 transfer)		$t_{DRDY}+t_{READ}$ (2)		ns
t_{CYCLE}	Time between two adjacent CONVST rising edges for zone 2 transfer	333			ns
SPI-compatible and Parallel Byte Protocols (See Figure 3)					
t_{CLK}	Serial clock time period	1/ f_{CLK}			
t_{PH_CLK}	SCLK high time	0.45 × t_{CLK}		0.55 × t_{CLK}	ns
t_{PL_CLK}	SCLK low time	0.45 × t_{CLK}		0.55 × t_{CLK}	ns
t_{SU_CSCK}	Setup time: $\overline{CS}$ faling to first SCLK capture edge	12			ns
t_{SU_CKDI}	Setup Time: SDI data valid to SCLK capture edge	1.5			ns
t_{HT_CKDI}	Hold Time: SCLK capture edge to previous data valid on SDI	1.5			ns
t_{HT_CKCS}	Delay Time: last SCLK capture edge to $\overline{CS}$ rising	7			ns
f_{CLK}	Serial clock frequecny for SPI protocols with single data rate			60	MHz
f_{CLK}	Serial clock frequecny for SPI protocols with double data rate			22	MHz
f_{CLK}	Serial clock frequecny for parallel byte protocol			45	MHz
Clock Re-Timer protocol with STROBE = SCLK (External Clock)(3)(See Figure 4)					
f_{CLK}	Serial clock frequency with single data rate			60	MHz
f_{CLK}	Serial clock frequency with double data rate			22	MHz
Asynchronous Reset and Power Down Timing (See Figure 6)					
t_{WL-RST}	Pulse duration (Low) for reset	50		500	ns
$t_{WL-PD-min}$	Minimum pulse duration (Low) for power down	1000			ns

(1) See Switching Characteristics
(2) See Protocols for Reading From the Device for t_{READ}
(3) Other parameters are the same as the SPI-compatible and Parallel Byte Protocols.

ADVANCE INFORMATION

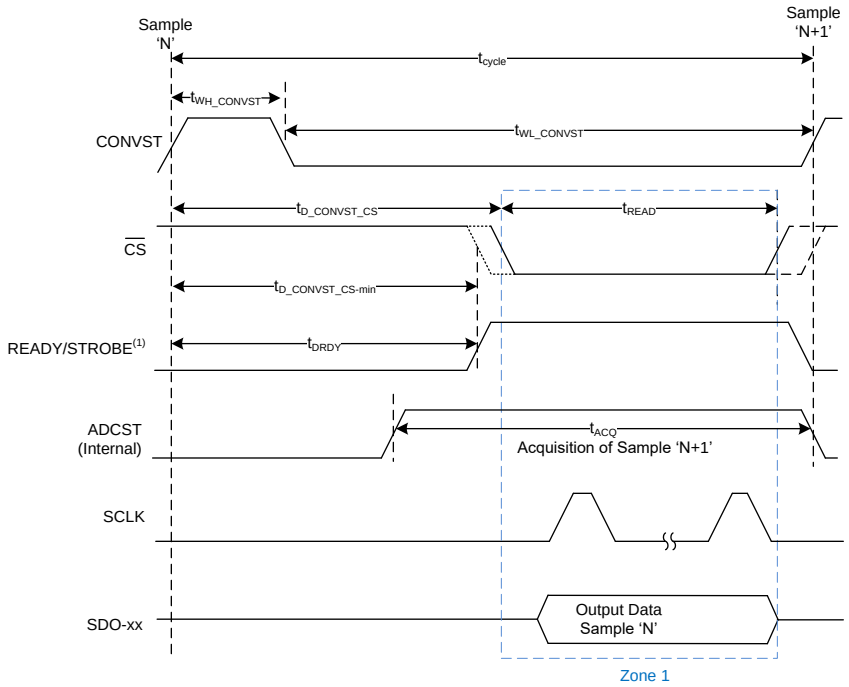
6.9 Switching Characteristics

all minimum and maximum specifications are at T_A = –40°C to +125°C, AVDD = 4.5 V to 5.5 V, DVDD = 2.35 V to 5.5 V, and f_{Sample} = 3 MSPS (unless otherwise noted); typical values are at T_A= 25°C, AVDD = 5 V, and DVDD = 3.3 V

		MIN	TYP	MAX	UNIT
Conversion Control and Data Transfer (See Figure 1 and Figure 2)					
t_{DRDY}	Data ready time for present sample: CONVST high to READY high with zero cycle latency (zone 1 transfer) for ADS9224x (16-bit)			300	ns
	Data ready time for present sample: CONVST high to READY high with zero cycle latency (zone 1 transfer) for ADS9234x (14-bit)			285	ns
SPI-compatible and Parallel Byte Protocols (See Figure 3)					
t_{DEN_CSDO}	Delay time: $\overline{CS}$ falling to data valid on SDO-x			12	ns
t_{DZ_CSDO}	Delay time: $\overline{CS}$ rising edge to SDO-x tristate			12	ns
t_{D_CKDO}	Delay time: SCLK launch edge to next data valid on SDO-x for SPI-compatible protocols with single data rate	TBD		15.8	ns
t_{D_CKDO}	Delay time: SCLK launch edge to next data valid on SDO-x for SPI-compatible protocols with double data rate	TBD		21	ns
t_{D_CKDO}	Delay time: SCLK launch edge to next data valid on SDO-x for parallel byte protocol	TBD		21	ns
Clock Re-Timer protocol with STROBE = SCLK (External Clock)(1)(See Figure 4)					
$t_{OFF\_STROBE\_DO}$	Time offset: STROBE edge to next data valid on SDO-x	-2.5		2.5	ns
$t_{D\_CS\_READY}$	Delay time: $\overline{CS}$ rising to READY displaying internal device state			13.5	ns
$t_{D\_CKSTROBE\_r}$	Delay time: SCLK rising edge to STROBE rising			21.5	ns
$t_{D\_CKSTROBE\_f}$	Delay time: SCLK falling edge to STROBE falling			21.5	ns
t_{PH_STROBE}	Strobe output high time	0.45 × t_{STR}		0.55 × t_{STR}	ns
t_{PL_STROBE}	Strobe output low time	0.45 × t_{STR}		0.55 × t_{STR}	ns
Clock Re-Timer protocol with STROBE = Internal Clock.(1)(See Figure 5)					
$t_{D\_CS\_STROBE}$	Delay time : $\overline{CS}$ falling to 1st STROBE rising	15		50	ns
$t_{OFF\_STROBE\_DO}$	Time offset : STROBE edge to next data valid on SDO-x	-2.5		2.5	ns
$t_{D\_CS\_READY}$	Delay time: $\overline{CS}$ rising to READY displaying internal device state			13.5	ns
t_{INTCLK}	INTCLK period		15		ns
t_{STR}	STROBE period (INTCLK)		15		ns
	INTCLK/2		30		ns
	INTCLK/4		60		ns
t_{WH_STR}	STROBE high period	0.45 × t_{STR}		0.55 × t_{STR}	ns
t_{WL_STR}	STROBE low period	0.45 × t_{STR}		0.55 × t_{STR}	ns
Asynchronous Reset and Power Down Timing (See Figure 6)					
$t_{RST-WKUP}$	Wake up time from reset			1	µs
$t_{PD-WKUP}$ (2)	Wake up time from power down		25		ms

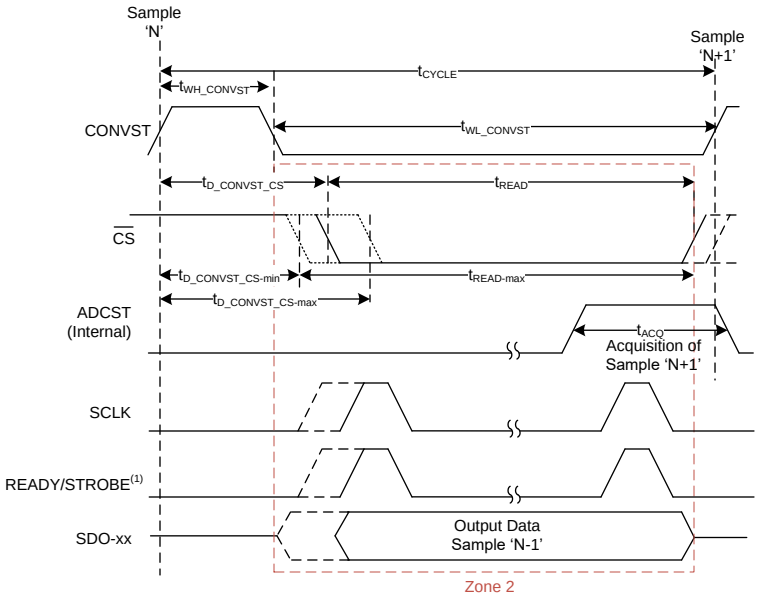
(1) Other parameters are the same as the SPI-compatible and Parallel Byte Protocols.
(2) With C_{REFP_x} = 10µF

ADVANCE INFORMATION



(1) The READY output is required for data transfer with zero cycle latency. The STROBE output is required only for clock re-timer (CRT) protocols.

Figure 1. Conversion Control and Data Transfer With Zero Cycle Latency (Zone 1 Transfer)



(1) The READY output is not required for zone 2 data transfer. The STROBE output is required only for clock re-timer protocols.

Figure 2. Conversion Control and Data Transfer With Wider Read Cycle (Zone 2 Transfer)

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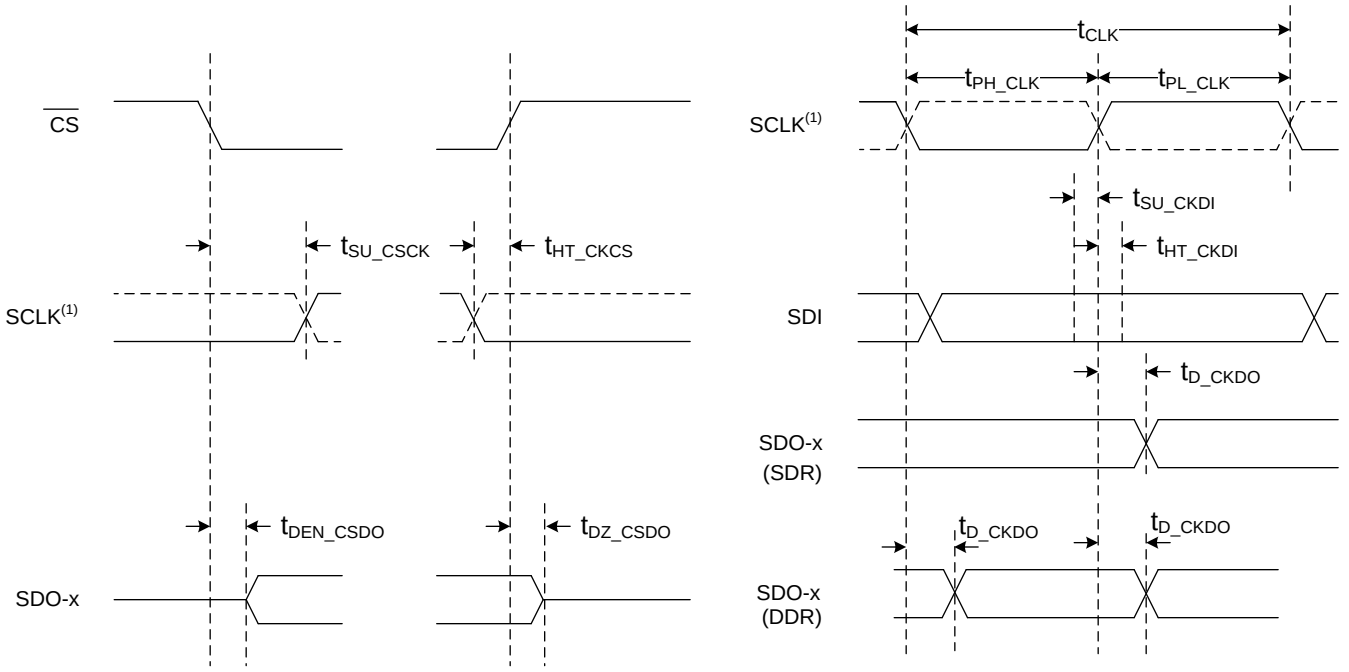

(1) The SCLK polarity, launch edge, and capture edge depend on the SPI protocol selected. DDR is not supported with the parallel byte protocol.

Figure 3. SPI-Compatible and Parallel Byte Protocols Timing

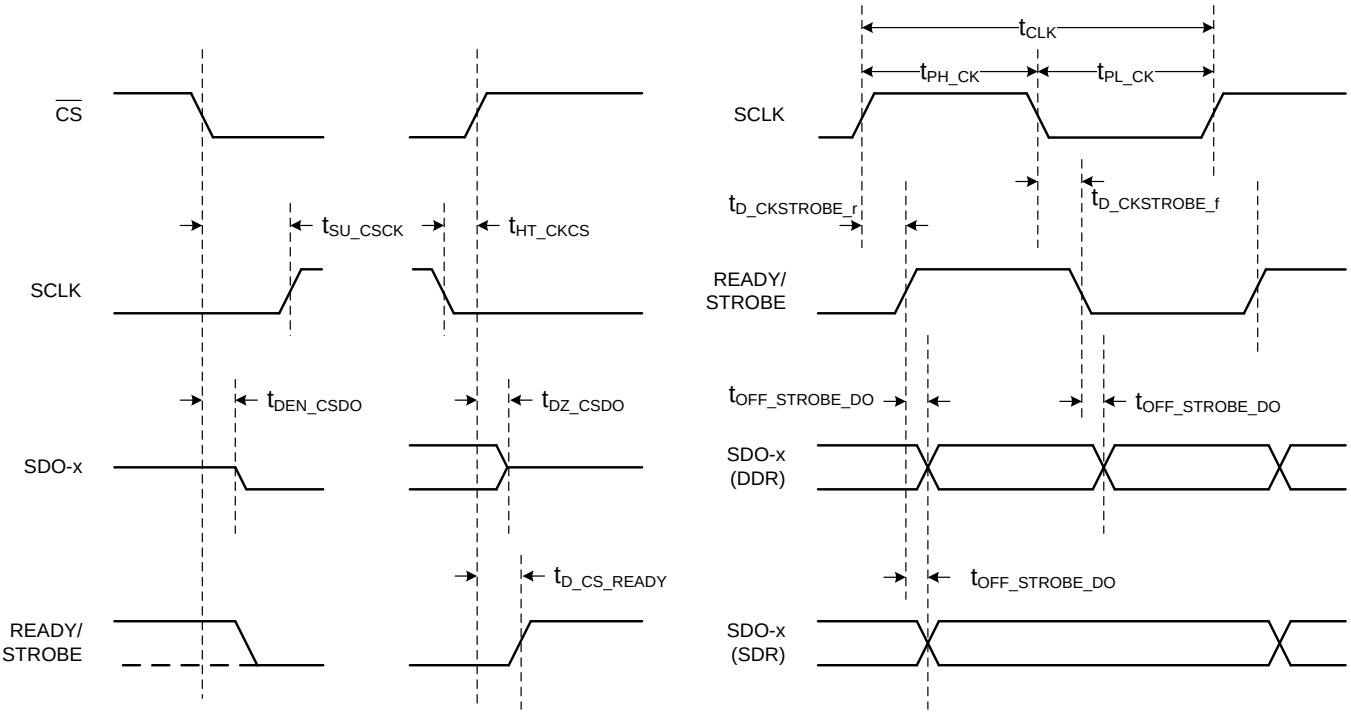

Figure 4. Clock Re-Timer Protocol (External Clock) Timing

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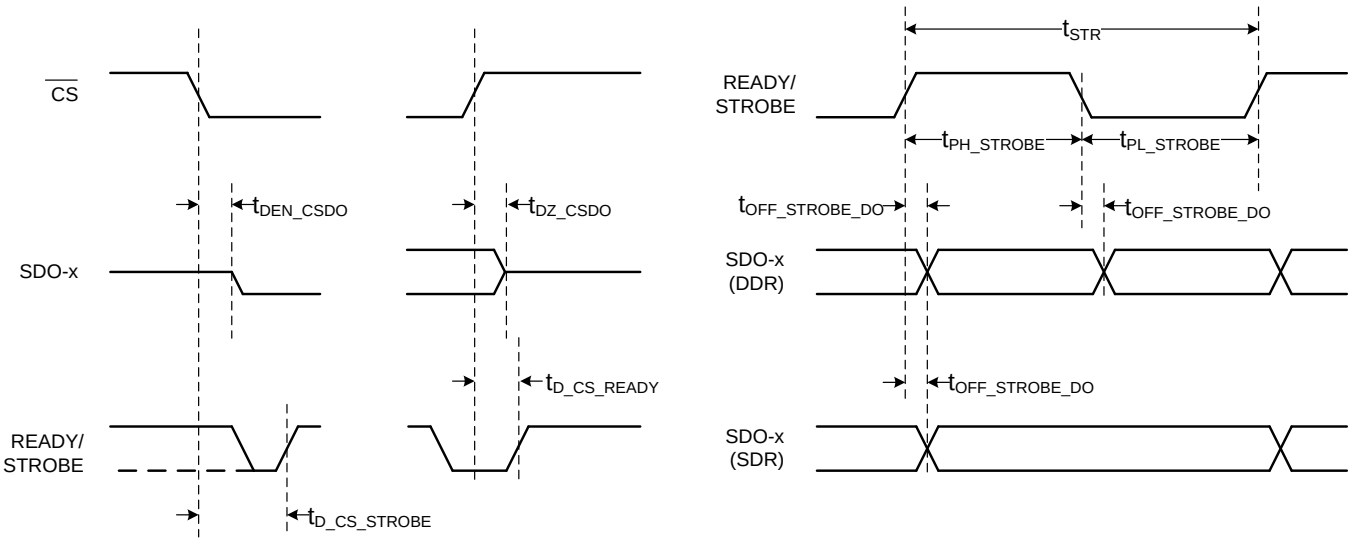

Figure 5. Clock Re-Timer Protocol (Internal Clock) Timing

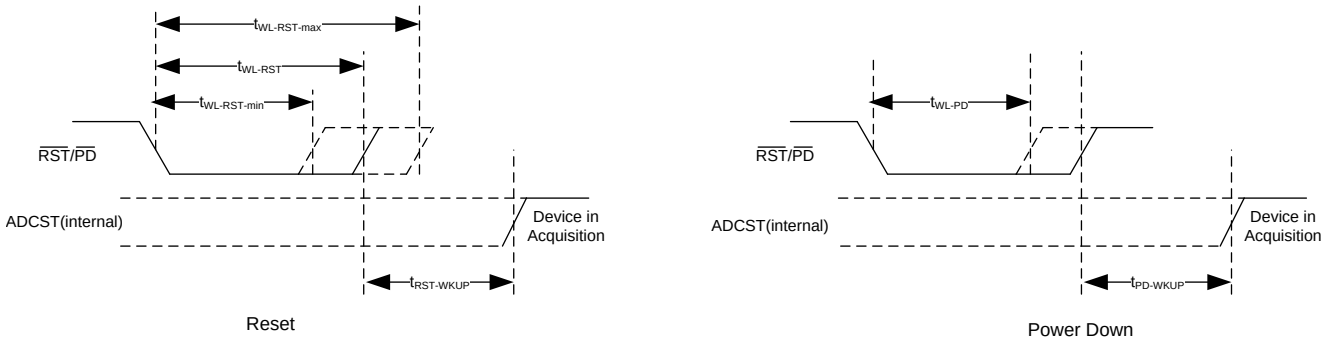

Figure 6. Asynchronous Reset and Power-Down Timing

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7 Detailed Description

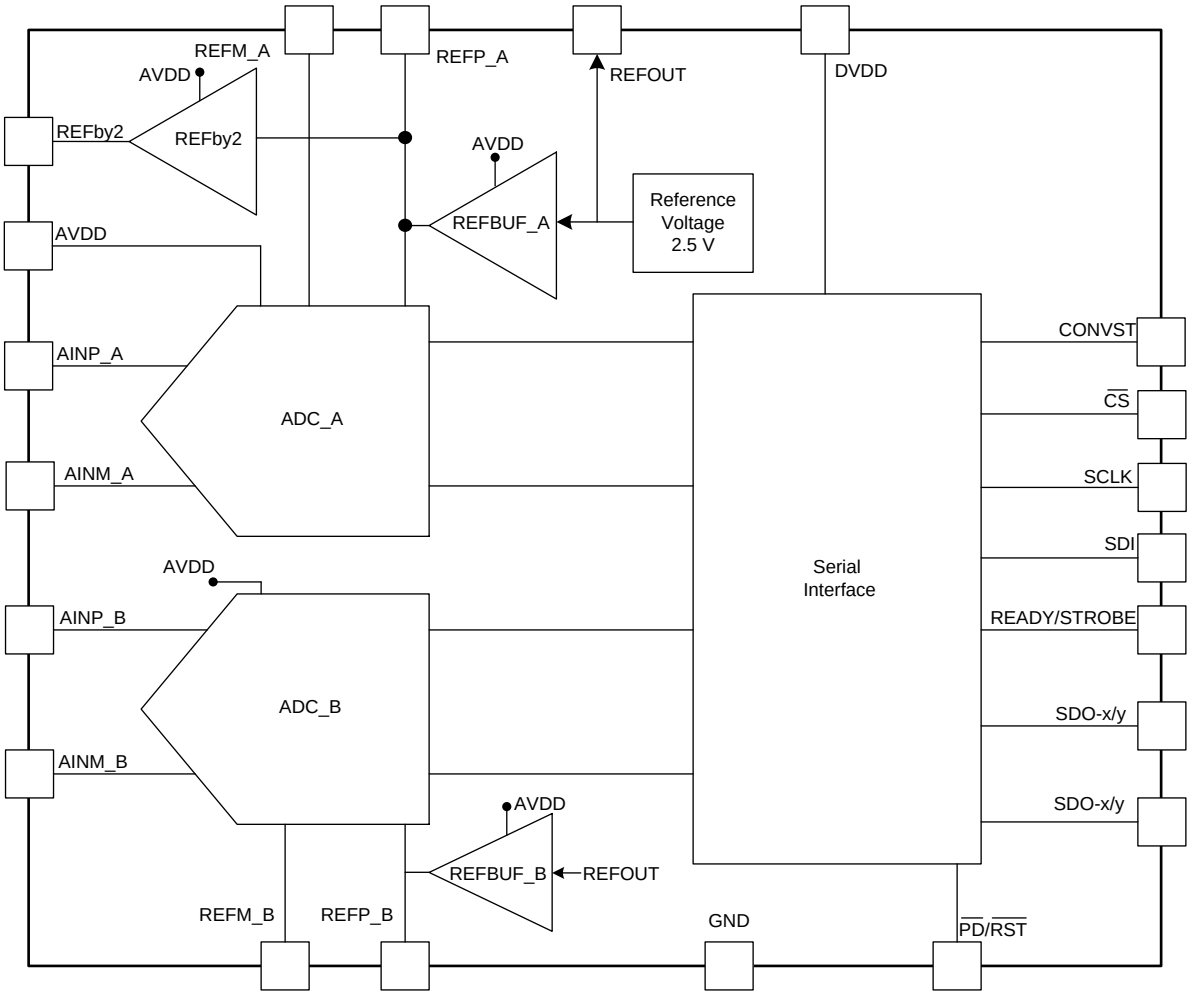
7.1 Overview

The device belongs to a family of dual, high-speed, simultaneous-sampling, analog-to-digital converters (ADCs). The device supports fully differential input signals and a full-scale input range equal to 3.2678 × V_{REF}.

When a conversion is initiated, the input between the AINP_x and AINM_x pins is sampled on the internal capacitor array. The device uses an internal clock to perform conversions. During the conversion process, both analog inputs are disconnected from the internal circuit. At the end of conversion process, the device reconnects the sampling capacitors to the AINP_x and AINM_x pins and enters an acquisition phase. The device includes reference buffers to provide the charge required by the ADCs during conversion. The device includes a reference voltage for the ADCs.

The enhanced serial programming interface (SPI) digital interface is backward-compatible with traditional SPI protocols. Configurable features simplify board layout, timing, and firmware and support high throughput at lower clock speeds, thus allowing an easy interface with a variety of microcontrollers, digital signal processors (DSPs), and field-programmable gate arrays (FPGAs). The device also provides a byte mode and a wide read cycle to reduce the clock frequency required for data transfer. The device includes a clock re-timer (CRT) to enable data transfer through digital isolators. The device also supports double data rate (DDR) with SPI-compatible serial interface modes and with a clock re-timer.

7.2 Functional Block Diagram



ADVANCE INFORMATION

7.3 Feature Description

From a functional perspective, the device is comprised of seven modules: two converters (ADC_A, ADC_B), two reference buffers (REFBUF_A, REFBUF_B), the REFby2 buffer, the reference voltage, and the serial interface, as shown in the *Functional Block Diagram* section.

The converter module samples and converts the analog input into an equivalent digital output code. The reference buffers provide the charge required by the converters for the conversion process. The serial interface module facilitates communication and data transfer between the device and the host controller. The REFby2 buffer provides the common-mode voltage for the amplifiers input driving the analog of the device. The reference voltage is used by the converters for conversion process.

7.3.1 Converter Modules

As shown in Figure 7, both converter modules sample the analog input signal (provided between the AINP_x and AINM_x pins), compare this signal with the reference voltage (between the pair of REFP_x and REFM_x pins), and generate an equivalent digital output code. The converter modules receive PD/RST and the CONVST inputs from the interface module, and output the ADCST signal and the conversion result back to the interface module.

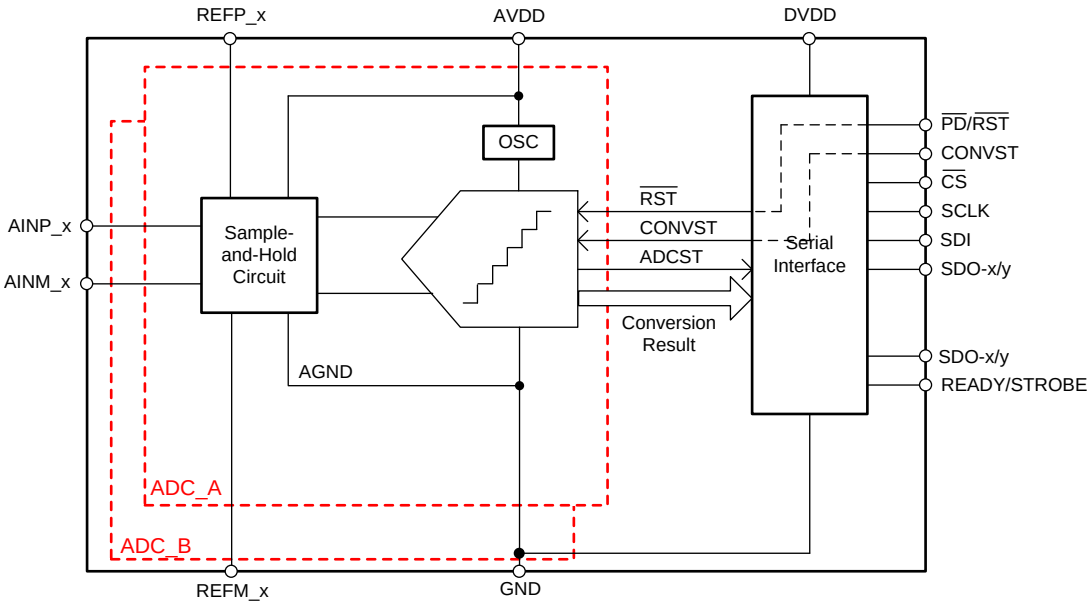


Figure 7. Converter Modules

7.3.1.1 Analog Input With Sample-and-Hold

This device supports unipolar, fully differential, analog input signals. Figure 8 shows a small-signal equivalent circuit of the sample-and-hold circuit. Each sampling switch is represented by a resistance (R_{S1} and R_{S2}, typically 120 Ω) in series with an ideal switch (SW_1 and SW_2). The sampling capacitors, C_{S1} and C_{S2}, are typically 16 pF.

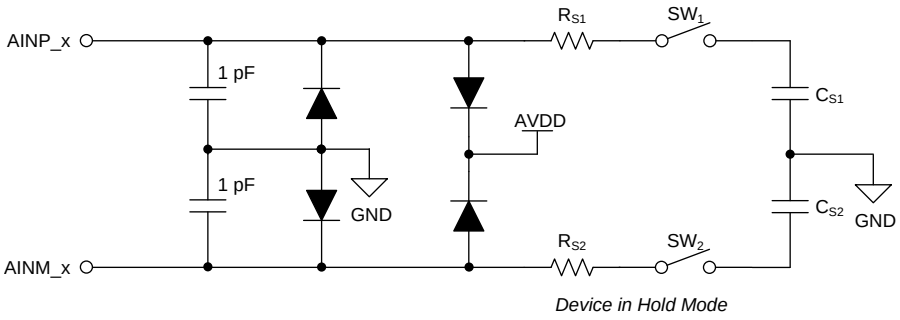


Figure 8. Analog Input Structure for Converter Module

ADVANCE INFORMATION

Feature Description (continued)

During the acquisition process, both inputs are individually sampled on C_{S1} and C_{S2}, respectively. During the conversion process, both converters convert for the respective voltage difference between the sampled values: $V_{AINP\_x} – V_{AINM\_x}$.

Equation 1 and Equation 2 provide the full-scale input range (FSR) and common-mode voltage (VCM), supported at the analog inputs for reference voltage (V_{REF}) on the REFOUT pin.

$$FSR = ±1.6384 × V_{REF} = 3.2768 × V_{REF} \quad (1)$$

$$V_{CM} = 0.8192 × V_{REF} ± 0 .2 V \quad (2)$$

7.3.1.2 ADC Transfer Function

This device supports unipolar, fully differential input signals. The device output is in two's compliment format. Table 1 and Figure 9 show the ideal transfer characteristics for the device. Equation 3 gives the least significant bit (LSB) for the ADC.

$$1 \text{ LSB} = FSR / 2^R \quad (3)$$

where

- FSR is defined in Equation 1
- R = Resolution of the device

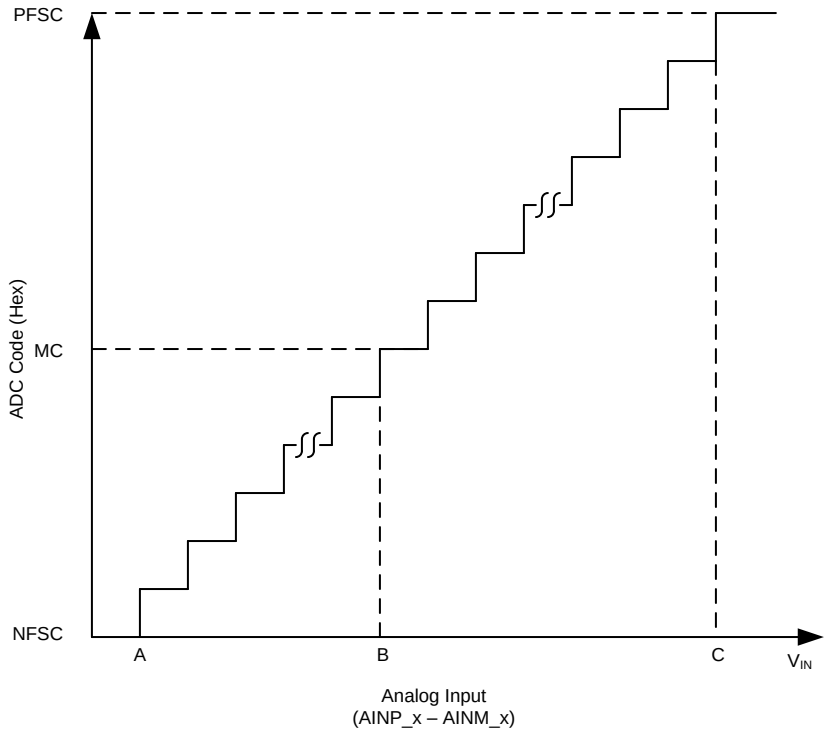


Figure 9. Ideal Transfer Characteristics

Table 1. Transfer Characteristics

STEP	INPUT VOLTAGE (AINP_x-AINM_x)	CODE	DESCRIPTION	IDEAL OUTPUT CODE (R = 16)	IDEAL OUTPUT CODE (R = 14)
A	≤ –(1.6384 × V_{REF} – 1 LSB)	NFSC	Negative full-scale code	8000	2000
B	0 LSB to 1 LSB	MC	Mid code	0000	0000
C	≥ (1.6384 × V_{REF} – 1 LSB)	PFSC	Positive full-scale code	7FFF	1FFF

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7.3.2 Internal Reference Voltage

The device features an internal reference source with a nominal output value of 2.5 V. The REFOUT pin is an output with the internal reference value. A 1-µF decoupling capacitor (C_{REFOUT}), as shown in Figure 10, is recommended to be placed between the REFOUT pin and GND pin. The capacitor must be placed as close to the REFOUT pin as possible. The output impedance of the internal band-gap circuit creates a low-pass filter with this capacitor to band-limit the noise of the reference. The initial accuracy specification for the internal reference can be degraded if the die is exposed to any mechanical or thermal stress. Heating the device when being soldered to a printed circuit board (PCB) and any subsequent solder reflow is a primary cause for shifts in the V_{REF} value.

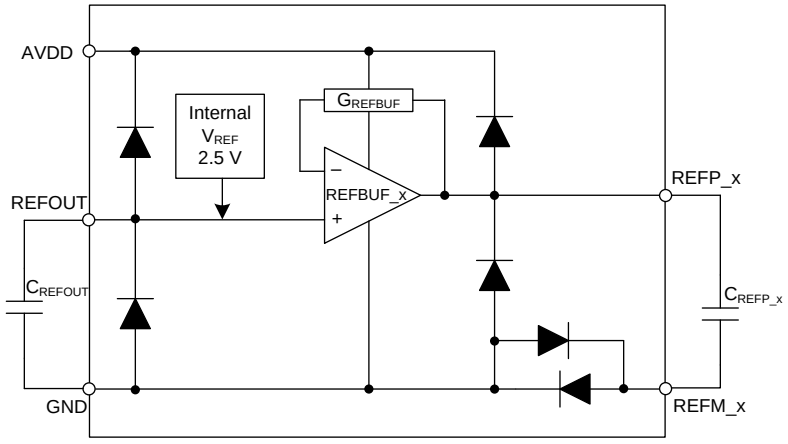

Figure 10. Connection Diagram for Reference and Reference Buffers

7.3.3 Reference Buffers

On the CONVST rising edge, both converters start converting the sampled value on the analog input, and the internal capacitors are switched to the REFP_x pins. Most of the switching charge required during the conversion process is provided by the external decoupling capacitor C_{REFP_x}. If the charge lost from C_{REFP_x} is not replenished before the next CONVST rising edge, the subsequent conversion occurs with this different reference voltage and causes a proportional error in the output code. To eliminate these errors, the internal reference buffers of the device maintains the voltage on the REFP_x pins. The reference buffers have a gain of G_{REFBUF}, as specified in the *Specifications* section. The voltage at the REFP_x pins can be calculated as $V_{REFP\_x} = G_{REFBUF} \times V_{REF}$.

All performance characteristics of the device are specified with the internal reference buffer and a specified value of C_{REFP_x}. As shown in Figure 10, place a decoupling capacitor C_{REFP_x} between the REFP_x pins and the REFM_x pin as close to the device as possible.

7.3.4 REFby2 Buffer

The device includes a REFby2 buffer for setting the common-mode voltage required by the converter modules. The REFby2 output can be provided to the V_{OCM} pin of the fully differential amplifiers (similar to the THS4551). The REFby2 output can be increased by 100 mV (for specifications of the REFby2 output, see the *Specifications* section) for providing headroom from GND for the fully differential amplifier. To increase the REFby2 output, set the EN_REFby2_OFFSET bit to 1 in the REFby2_OFFSET register. Figure 11 depicts a block diagram for the REFby2 buffer.

ADVANCE INFORMATION

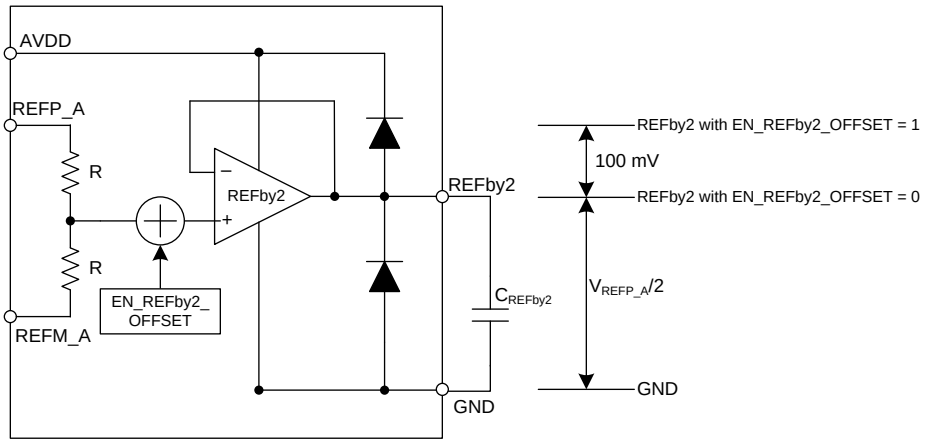

Figure 11. REFby2 Buffer

7.3.5 Data Averaging

The device can be configured to average two or four samples and provide the averaged value as output data. To configure the data averaging, configure the DATA_AVG_CFG register.

7.3.5.1 Averaging of Two Samples

To enable averaging of two samples, set the EN_DATA_AVG bits in the DATA_AVG_CFG register to 10b. In this mode, the device averages two samples and provides the average of two samples as output data. The output data rate reduces by a factor of two. In this mode, the host must provide two pulses separated by a time of t_{CYCLE} (see t_{CYCLE} for a zone 2 transfer in the *Specifications* section) on the CONVST pin. The device sets the READY pin high after a time of t_{DRDY} (see t_{DRDY} in the *Specifications* section) from the second rising edge on the CONVST pin. After the READY pin is set high, the host can read the data by using one of the protocols for reading from the device. The host can read the data while providing the two CONVST pulses for acquiring the next two samples. The host must keep $t_{READ} < [2 \times t_{CYCLE}]$. Figure 12 provides the timing for the averaging of two samples.

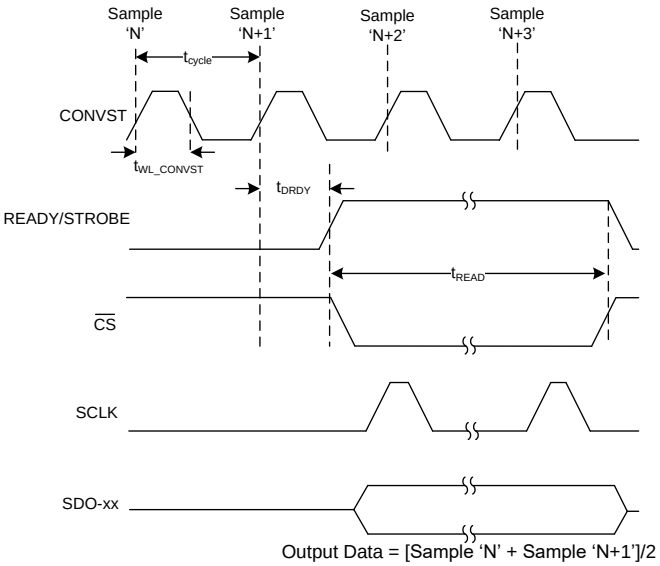

Figure 12. Timing for Averaging of Two Samples

7.3.5.2 Averaging of Four Samples

To enable averaging of four samples, set the EN_DATA_AVG bits in the DATA_AVG_CFG register to 11b. In this mode, the device averages four samples and provides the average of four samples as output data. The output data rate reduces by a factor of four. In this mode, the host must provide four pulses separated by a time of t_{CYCLE} (see t_{CYCLE} for a zone 2 transfer in the *Specifications* section) on the CONVST pin. The device sets the READY pin high after a time of t_{DRDY} (see t_{DRDY} in the *Specifications* section) from the fourth rising edge on the CONVST pin. After the READY pin is set high, the host can read the data by using one of the protocols for reading from the device. The host can read the data while providing the four CONVST pulses for acquiring the next four samples. The host must keep $t_{READ} < [4 \times t_{CYCLE}]$. Figure 13 provides the timing for the averaging of four samples.

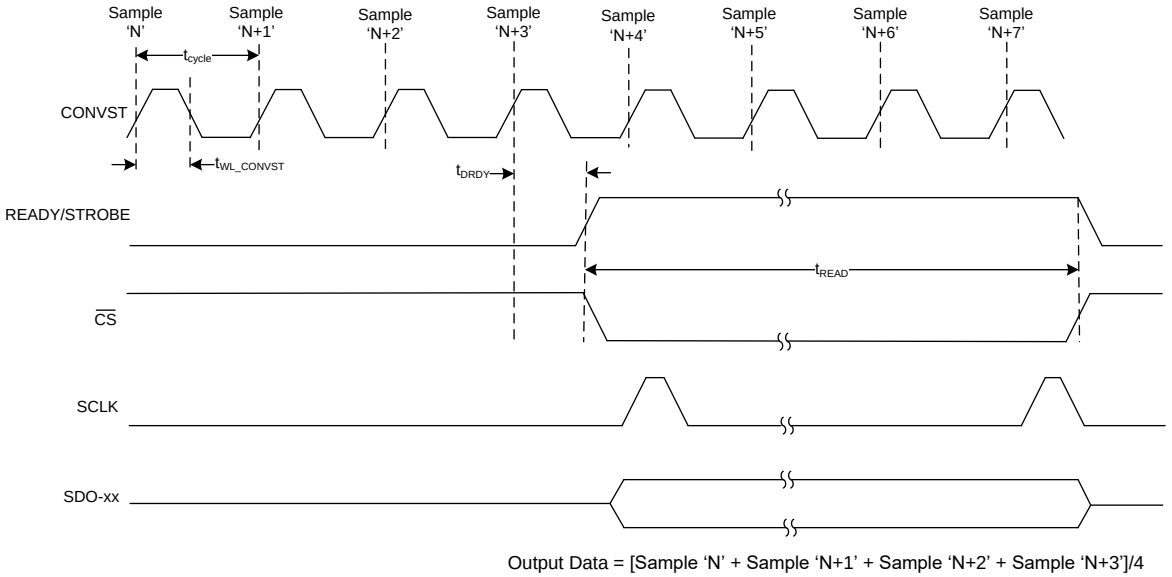

Figure 13. Timing for Averaging of Four Samples

7.4 Device Functional Modes

As shown in Figure 14, this device supports three functional states: RST or power-down, ACQ, and CNV. The device state is determined by the status of the CONVST and PD/RST control signals provided by the host controller.

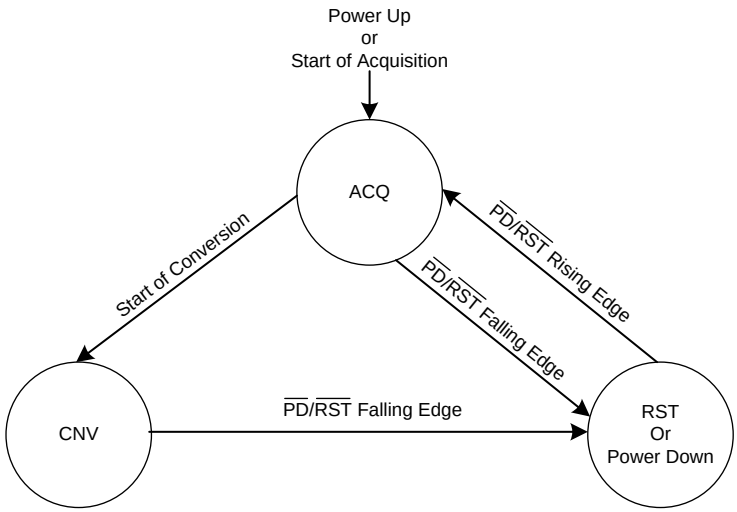

Figure 14. Device Functional States

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Device Functional Modes (continued)

7.4.1 ACQ State

In ACQ state, the device acquires the analog input signal. The device enters ACQ state at power-up, when coming out of power down, after any asynchronous reset, and by the ADCST signal (internal). A $\overline{PD}/\overline{RST}$ falling edge takes the device from ACQ state to RST state. A CONVST rising edge takes the device from ACQ state to CNV state.

7.4.2 CNV State

The device moves from ACQ state to CNV state and starts conversion on a rising edge of a CONVST pin. The conversion process uses an internal clock. The host must provide a minimum time of t_{CYCLE} between two subsequent start of conversions.

7.4.3 Reset or Power-Down

The $\overline{PD}/\overline{RST}$ pin is an asynchronous digital input for the device. The pulse duration (low) on the $\overline{PD}/\overline{RST}$ pin decides the state for the device (reset or power-down). Figure 15 provides the timing diagram for these states. On power-up or after reset the device supports the SPI-00-S protocol for configuring the device and the SPI-00-S-SDR protocol for reading the data from the device. See the *Protocols for Reading From the Device* and *Protocols for Configuring the Device* sections for details.

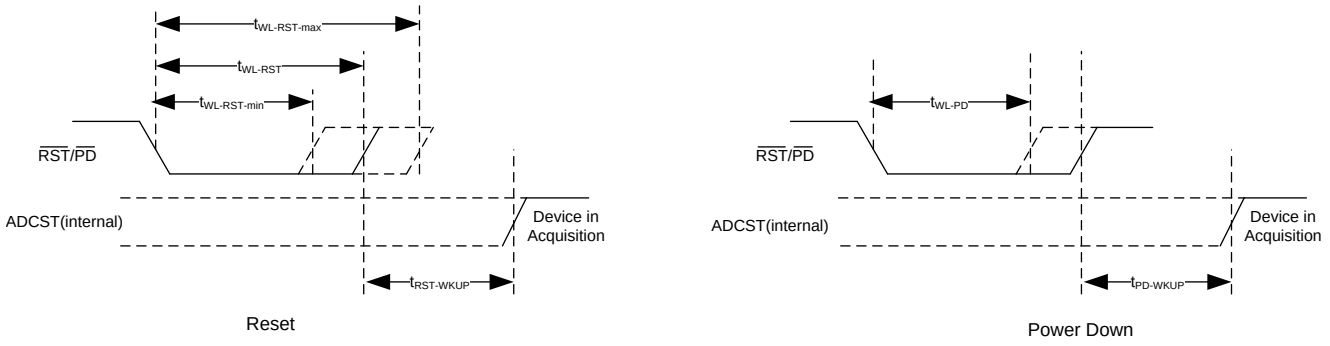

Figure 15. Reset or Power Down

7.4.3.1 Reset

To enter reset state, the host controller pulls and keeps the $\overline{PD}/\overline{RST}$ pin low for a duration of t_{WL_RST} ($t_{WL\_RST\text{-}min} \le t_{WL\_RST} \le t_{WL\_RST\text{-}max}$).

In reset state, the device terminates the ongoing conversion or acquisition process and all configuration registers (see the *Register Maps* section) are reset to their default values.

To exit reset state, the host controller pulls the $\overline{PD}/\overline{RST}$ pin high. After a delay of $t_{RST\text{-}WKUP}$, the device enters ACQ state.

7.4.3.2 Power-Down

To enter power-down state, the host controller pulls and keeps the $\overline{PD}/\overline{RST}$ pin low for a minimum duration of t_{WL_PD}.

In power-down state, all device blocks are powered down and all configuration registers (see the *Register Maps* section) are reset to their default values.

To exit power-down state, the host controller pulls the $\overline{PD}/\overline{RST}$ pin high. After a delay of $t_{PD\text{-}WKUP}$, the device powers up and enters ACQ state.

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Device Functional Modes (continued)

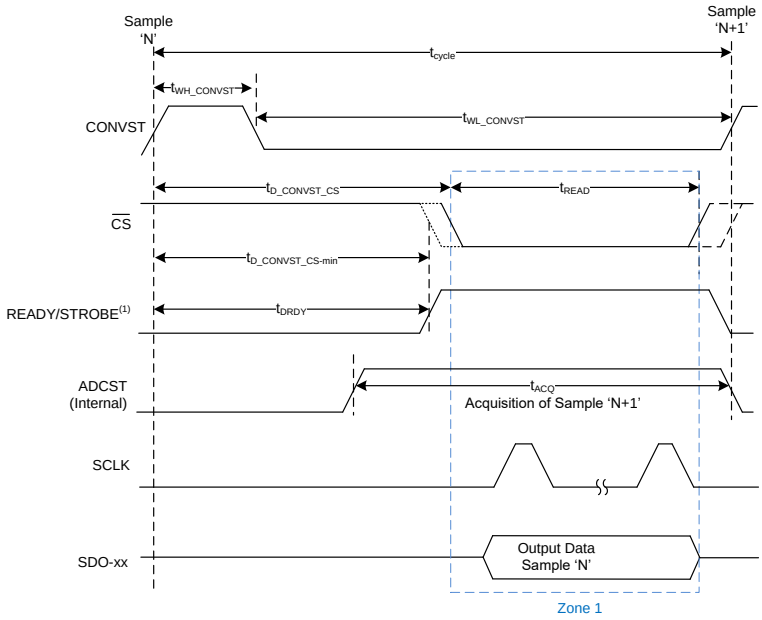
7.4.4 Conversion Control and Data Transfer Frame

The device supports two modes of conversion control and data transfer, one with zero cycle latency (zone 1 transfer) and another with a wide read cycle (zone 2 transfer).

7.4.4.1 Conversion Control and Data Transfer Frame With Zero Cycle Latency (Zone 1 Transfer)

In this mode of conversion control and data transfer, the device starts conversion on the rising edge of CONVST. The CONVST pin can be pulled low after a minimum time of t_{WH_CONVST}. After the conversion is finished, the rising edge of the READY/STROBE pin indicates that the data are ready and the data can be read by the host. After the READY pin is set high, as shown in Figure 16, the host must pull $\overline{CS}$ low and provide clocks on the SCLK pin to read the data in zone 1 without cycle latency. For a zone 1 transfer, the host must provide a minimum delay time of $t_{D\_CONVST\_CS}$ (= t_{DRDY}) between the rising edge of CONVST and the falling edge of $\overline{CS}$.

The data for the present sample (sample N) is provided by the device on the SDO pins. After all bits are read, the host can pull the $\overline{CS}$ pin high to end the data transfer frame. After pulling $\overline{CS}$ high, the host can pull the CONVST pin high to start the next conversion. The host must keep the SDI pin low (NOP0) or high (NOP1) for conversion control and for getting conversion results from the device. In this mode of conversion control, the time between two adjacent rising edges of the CONVST signal (t_{CYCLE}) is determined as $t_{CYCLE} = t_{DRDY} + t_{READ}$.



(1) The READY output is required for data transfer with zero cycle latency. The STROBE output is required only for clock re-timer (CRT) protocols. See the *READY/STROBE Output* section for details.

(2) For t_{READ} with different data transfer protocols; see the *Protocols for Reading From the Device* section.

(3) $f_{Sample} = 1 / t_{cycle}$.

Figure 16. Conversion Control and Data Transfer Frame With Zero Cycle Latency (Zone 1 Transfer)

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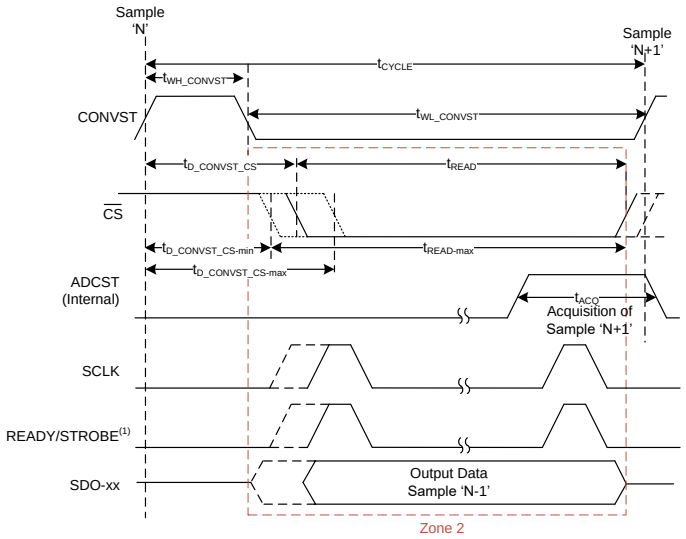
Device Functional Modes (continued)

7.4.4.2 Conversion Control and Data Transfer Frame With Wide Read Cycle (Zone 2 Transfer)

In this mode of conversion control and data transfer, the device starts conversion on the rising edge of CONVST. The CONVST pin can be pulled low after a minimum time of t_{WH_CONVST}. After a time of $t_{D\_CONVST\_CS}$ (see $t_{D\_CONVST\_CS}$ for zone 2 transfer in the *Specifications* section), the host must pull $\overline{CS}$ low and provide clocks on the SCLK pin to read the data in zone 2. As shown in Figure 17, a zone 2 transfer provides more read time (t_{read}). The read time available for reading data is maximized when $t_{D\_CONVST\_CS}$ is set to the minimum permissible value. The data for the previous sample (sample N-1) is provided by the device on the SDO pins. After all bits are read, the host can pull the $\overline{CS}$ pin high to end the data transfer frame. After pulling $\overline{CS}$ high, the host can pull the CONVST pin high to start the next conversion. In this mode of conversion control, a minimum time of t_{CYCLE} (see t_{CYCLE} for zone 2 transfer in the *Specifications* section) is required between two adjacent rising edges of the CONVST signal. The host must keep the SDI pin low (NOP0) or high (NOP1) for conversion control and for getting conversion results from the device.



(1) The READY output is not required for zone 2 data transfer. The STROBE output is required only for clock re-timer (CRT) protocols. See the *READY/STROBE Output* section for details.

(2) For t_{READ} with different data transfer protocols; see the *Protocols for Reading From the Device* section.

(3) $f_{Sample} = 1 / t_{cycle}$.

Figure 17. Conversion Control and Data Transfer Frame With Wide Read Cycle (Zone 2 Transfer)

NOTE

For optimum performance with zone 2 transfer, TI recommends masking the READY output by setting the READY_MASK bit in the OUTPUT_DATA_WORD_CFG register and using a data transfer protocol with a bus width of more than 2 SDOs or the parallel byte protocol to keep [$t_{D\_CONVST\_CS}$ + t_{READ}] below 150 ns. See the *Protocols for Reading From the Device* section for details on different protocols for reading the data.

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7.5 READY/STROBE Output

The READY/STROBE pin has multiple functions. The READY and STROBE signals are multiplexed to this pin. When CS is low, STROBE is output and when CS is high, READY is output.

7.5.1 READY Output

After power-up or after exiting power-down (a rising edge on $\overline{PD}/\overline{RST}$), the READY signal is set high. After a time of 0.9 ms, this signal goes low, indicating that the device is initialized and the registers can be configured. However, conversions can only be performed with the desired accuracy only after a time of $t_{PD-WKUP}$ (see the *Specifications* section). After power-up, READY indicates that data are available for readout. READY is set low at the next falling edge of $\overline{CS}$. For zone 2 transfer, TI recommends masking the READY output by setting the READY_MASK bit in the OUTPUT_DATA_WORD_CFG register.

7.5.2 STROBE Output

In clock re-timer protocols, the device sends out data on the SDO lines with synchronized clock on the STROBE line. The data are synchronized to the rising edges of the STROBE pulses. In CRT protocols, the host can use the STROBE output for latching the data. The STROBE for the CRT protocols is either derived from the external SCLK provided by the host or from the internal oscillator. The STROBE signal is held low for protocols other than the CRT protocols.

7.6 Programming

7.6.1 Output Data Word

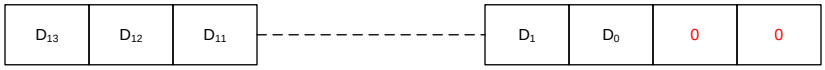
The output data word, as shown in Table 2, consists of a conversion result of N bits, where N is the width of the output data word. The output data word is provided on data lines (SDO-xx) for each ADC.

Table 2. Output Data Word

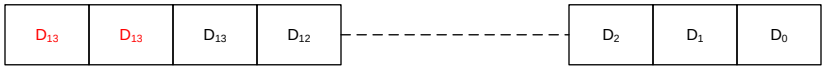
DEVICE	RESOLUTION OF DEVICE (R)	WIDTH OF OUTPUT DATA WORD (N)	CONTENT OF OUTPUT DATA WORD(1)(2)	MSB OF CONVERSION RESULT WITH LEFT ALIGNMENT	MSB OF CONVERSION RESULT WITH RIGHT ALIGNMENT
ADS9224R	16	16	16-bit conversion in 2's compliment format	D_{N-1} (= D_{15})	D_{N-1} (= D_{15})
ADS9234R	14	16	14-bit conversion in 2's compliment format	D_{N-1} (= D_{15})	D_{N-3} (= D_{13})

(1) The device provides register data in the output data word during register read operation.
(2) When a fixed pattern data is enabled, the device provides a fixed pattern in the output data word.

For ADS9234R devices with 14-bit resolution, the output data word can be left-aligned or right-aligned by configuring the DATA_RIGHT_ALIGNED bit. With left alignment, the device appends zeros in the end of the output data word. With right alignment, the device appends MSBs in the beginning of the output data word. Figure 18 shows the data alignment in the data output word.



Left Aligned Data with Zeros appended at the end



Right Aligned Data with MSBs appended in the beginning (Sign Extension)

Figure 18. Data Alignment for ADS9234R Devices

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7.6.2 Data Transfer Protocols

This device features an enhanced-SPI digital interface that allows the host controller to operate at slower SCLK speeds and still achieve the required throughput and response time. The enhanced-SPI digital interface module offers three options to reduce the SCLK speed required for data transfer:

- Increase the width of the output data bus (dual SDO, quad SDO, or parallel byte)
- Enable double data rate (DDR) transfer
- Wider read cycle by extending the data transfer window (zone 2 transfer)

These three options can be combined to achieve further reduction in SCLK speed.

7.6.2.1 Protocols for Reading From the Device

The protocols for the data-read operation can be broadly classified into five categories:

1. Legacy, SPI-compatible protocols (SPI-xy-S-SDR)
2. SPI-compatible protocols with bus width options and single data rate (SPI-xy-D-SDR and SPI-xy-Q-SDR)
3. SPI-compatible protocols with bus width options and double data rate (SPI-x1-S-DDR, SPI-x1-D-DDR, and SPI-x1-Q-DDR)
4. Clock re-timer (CRT) protocols (CRT-S-SDR, CRT-D-SDR, CRT-Q-SDR, CRT-S-DDR, CRT-D-DDR, and CRT-Q-DDR)
5. Parallel byte protocol (PB-xy-AB-SDR, PB-xy-AA-SDR)

7.6.2.1.1 Legacy, SPI-Compatible Protocols (SPI-xy-S-SDR)

The device supports legacy, SPI-compatible protocols with all combinations of clock phase and polarity. In this data transfer protocol, the device provides data from ADC_A on SDO-0A and data from ADC_B on SDO-0B. On power-up or after reset, the device supports the SPI-00-S-SDR protocol for reading data from the device. Table 3 provides the details of different legacy SPI protocols to read data from the device.

Table 3. SPI-xy-S-SDR Protocols for Reading From Device

PROTOCOL (1)	SCLK POLARITY (CPOL (2))	SCLK PHASE (CPHA (2)(3)(4))	MSB LAUNCH EDGE	BUS WIDTH	t_{READ} (5)(6)	TIMING DIAGRAM
SPI-00-S-SDR	Low (CPOL= 0)	Rising (CPHA = 0)	$\overline{CS}$ falling	1	[15.5 × t_{CLK} + k]	Figure 19
SPI-01-S-SDR	Low (CPOL= 0)	Falling (CPHA = 1)	1st SCLK rising	1	[15.5 × t_{CLK} + k]	Figure 20
SPI-10-S-SDR	High (CPOL= 1)	Falling (CPHA = 0)	$\overline{CS}$ falling	1	[15.5 × t_{CLK} + k]	Figure 19
SPI-11-S-SDR	High (CPOL= 1)	Rising (CPHA = 1)	1st SCLK falling	1	[15.5 × t_{CLK} + k]	Figure 20

(1) For legacy SPI-compatible protocols, set the SDO_PROTOCOL bits in PROTOCOL_CFG register to 000b.
(2) Configure the SPI_CPOL and SPI_CPHA bits in the PROTOCOL_CFG register for the desired CPOL and CPHA.
(3) With SCLK ≥ 30 MHz, TI recommends data capture on the launch edge for the next bit.
(4) With SCLK < 30 MHz, data can be captured either on the same edge as the SCLK phase or on the launch edge for the next bit.
(5) t_{READ} is the read time for reading the 16-bit output data word. k = (t_{SU_CSCK} + t_{HT_CKCS}).
(6) For ADS9234R devices, the read time for reading the 14-bit output data word is [13.5 × t_{CLK} + k].

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Figure 19 and Figure 20 show timing diagrams for the SPI-00-S-SDR, SPI-10-SDR and SPI-01-S-SDR, SPI-11-SDR protocols, respectively.

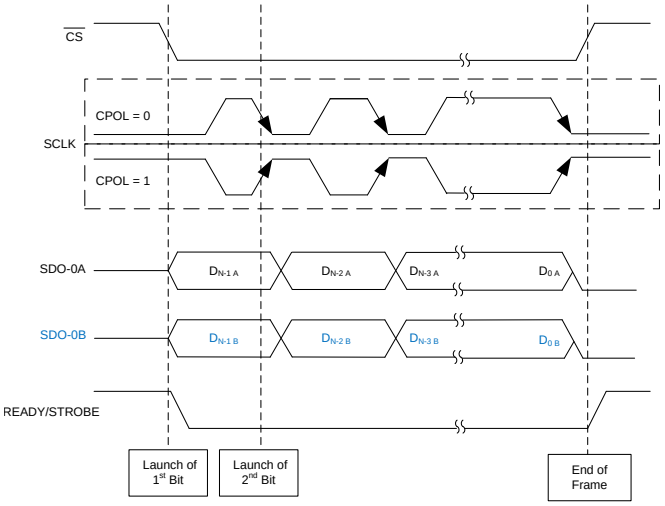

Figure 19. SPI-00-S-SDR and SPI-10-SDR Protocols

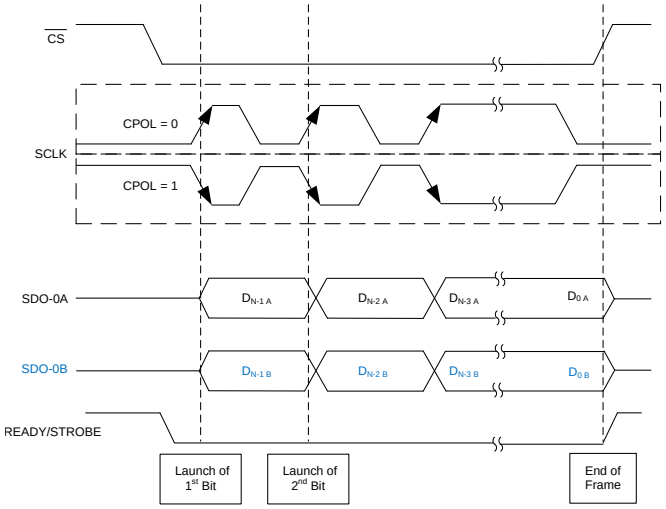

Figure 20. SPI-01-S-SDR and SPI-11-SDR Protocols

7.6.2.1.2 SPI-Compatible Protocols With Bus Width Options and Single Data Rate (SPI-xy-D-SDR and SPI-xy-Q-SDR)

In this data transfer protocol, the bus width of reading data from each ADC can be increased to two SDOs or four SDOs. All combinations of clock phase and polarity are supported. The read time required for reading the output data word reduces with increases in bus width and, thus, t_{CYCLE} for zone 1 transfer reduces. The SDOs that are not enabled by the BUS_WIDTH register are set to tri-state. Table 4 provides the details of different SPI protocols with bus width options and single data rate to read data from the device.

Table 4. SPI-xy-D-SDR and SPI-xy-Q-SDR Protocols for Reading From Device

PROTOCOL(1)	SCLK POLARITY (CPOL)(2)	SCLK PHASE (CPHA)(3)(4)	MSB LAUNCH EDGE	BUS WIDTH(5)	t_{READ}(6)(7)	TIMING DIAGRAM
SPI-00-D-SDR	Low (CPOL = 0)	Rising (CPHA = 0)	$\overline{CS}$ falling	2	[7.5 × t_{CLK} + k]	Figure 21
SPI-01-D-SDR	Low (CPOL = 0)	Falling (CPHA = 1)	1st SCLK rising	2	[7.5 × t_{CLK} + k]	Figure 22
SPI-10-D-SDR	High (CPOL = 1)	Falling (CPHA = 0)	$\overline{CS}$ falling	2	[7.5 × t_{CLK} + k]	Figure 21
SPI-11-D-SDR	High (CPOL = 1)	Rising (CPHA = 1)	1st SCLK falling	2	[7.5 × t_{CLK} + k]	Figure 22
SPI-00-Q-SDR	Low (CPOL = 0)	Rising (CPHA = 0)	$\overline{CS}$ falling	4	[3.5 × t_{CLK} + k]	Figure 23
SPI-01-D-SDR	Low (CPOL = 0)	Falling (CPHA = 1)	1st SCLK rising	4	[3.5 × t_{CLK} + k]	Figure 24
SPI-10-D-SDR	High (CPOL = 1)	Falling (CPHA = 0)	$\overline{CS}$ falling	4	[3.5 × t_{CLK} + k]	Figure 23
SPI-11-D-SDR	High (CPOL = 1)	Rising (CPHA = 1)	1st SCLK falling	4	[3.5 × t_{CLK} + k]	Figure 24

(1) For SPI-compatible protocols with bus width options and SDR, set the SDO_PROTOCOL bits in the PROTOCOL_CFG register to 000b.
(2) Configure the SPI_CPOL and SPI_CPHA bits in the PROTOCOL_CFG register for the desired CPOL and CPHA.
(3) With SCLK ≥ 30 MHz, TI recommends data capture on the launch edge for the next bit.
(4) With SCLK < 30 MHz, data can be captured either on the same edge as the SCLK phase or on the launch edge for the next bit.
(5) For configuring the bus width, configure the BUS_WIDTH register.
(6) t_{READ} is the read time for reading the 16-bit output data word. k = (t_{SU_CSCK} + t_{HT_CKCS}).
(7) For ADS9234R devices, the read time for reading the 14-bit output data word is [6.5 × t_{CLK} + k] for a bus width of 2 and [3.5 × t_{CLK} + k] for a bus width of 4.

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Figure 21, Figure 22, Figure 23, and Figure 24 show timing diagrams for the SPI-00-D-SDR and SPI-10-D-SDR, SPI-01-D-SDR and SPI-11-D-SDR, SPI-00-Q-SDR and SPI-10-Q-SDR, and SPI-01-Q-SDR and SPI-11-Q-SDR protocols, respectively.

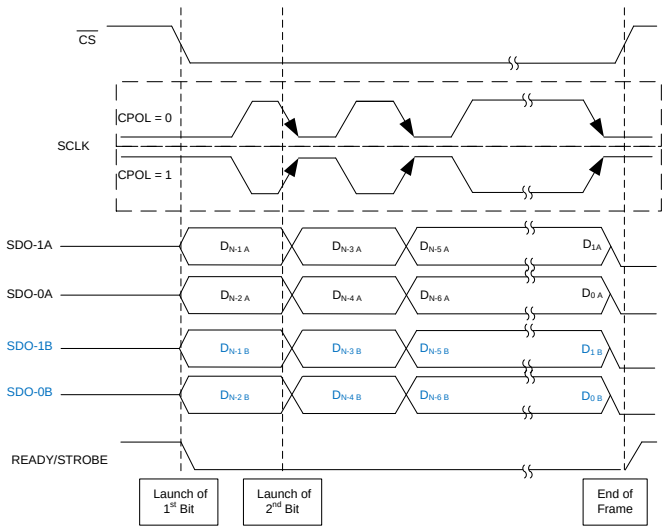

Figure 21. SPI-00-D-SDR and SPI-10-D-SDR Protocols

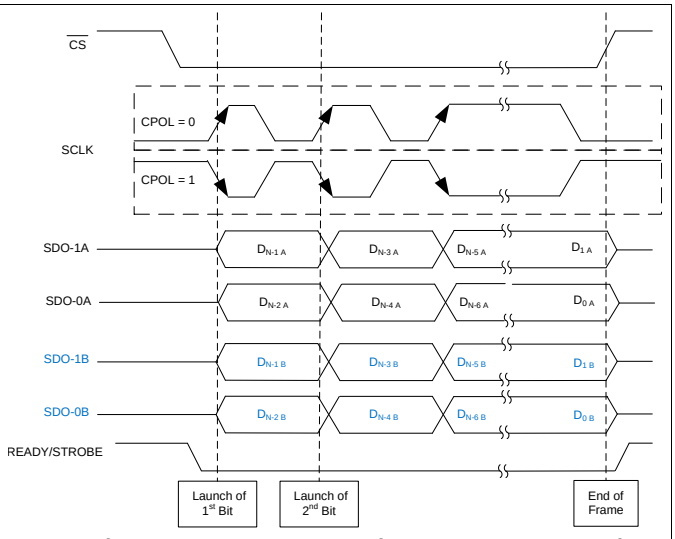

Figure 22. SPI-01-D-SDR and SPI-11-D-SDR Protocols

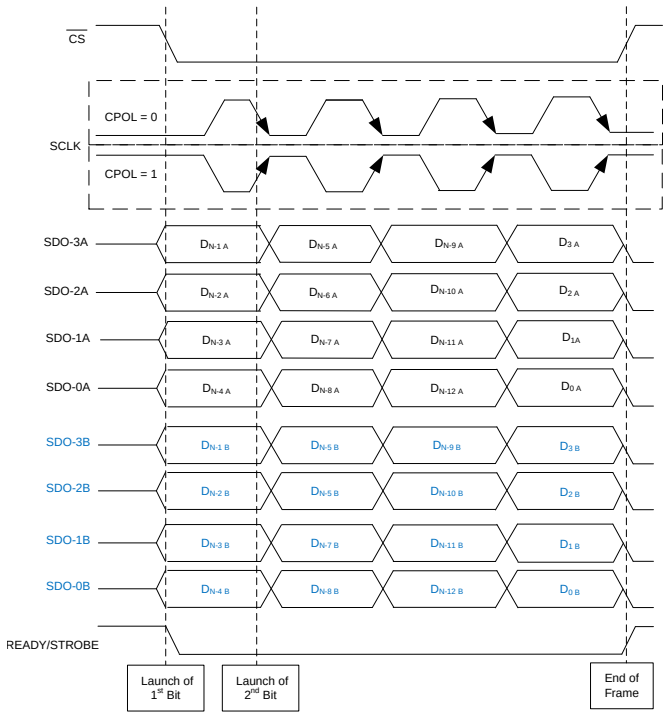

Figure 23. SPI-00-Q-SDR and SPI-10-Q-SDR Protocols

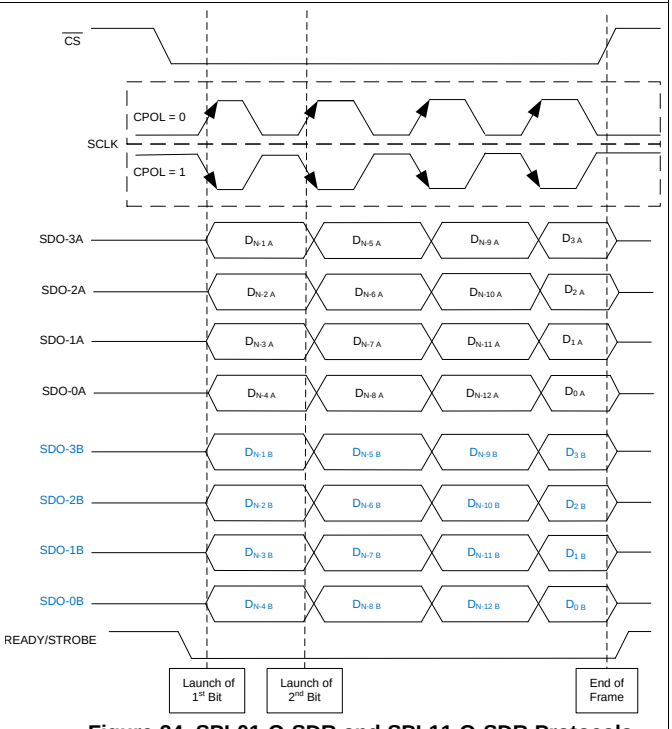

Figure 24. SPI-01-Q-SDR and SPI-11-Q-SDR Protocols

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7.6.2.1.3 SPI-Compatible Protocols With Bus Width Options and Double Data Rate (SPI-x1-S-DDR, SPI-x1-D-DDR, SPI-x1-Q-DDR)

In this data transfer protocol, the data rate for data transfer can be increased to double data rate. With double data rate, the device launches data on both edges (rising and falling) of the SCLK. The device supports both polarities of the clock and only one phase of clock (CPHA = 1). The read time required for reading the output data word reduces with increases in bus width and data rate. The SDOs that are not enabled by the BUS_WIDTH register are set to tri-state. Table 5 provides the details of different SPI protocols with bus width options and double data rate to read data from the device.

Table 5. SPI-x1-S-DDR, SPI-x1-D-DDR, and SPI-x1-Q-DDR Protocols for Reading From Device

PROTOCOL(1)	SCLK POLARITY (CPOL)(2)	SCLK PHASE(2)	MSB LAUNCH EDGE	BUS WIDTH(3)	t_{READ}(4)(5)	TIMING DIAGRAM
SPI-01-S-DDR	Low (CPOL = 0)	Falling (CPHA = 1)	1st SCLK rising	1	[9 × t_{CLK} + k]	Figure 25
SPI-11-S-DDR	High (CPOL = 1)	Rising (CPHA = 1)	1st SCLK falling	1	[9 × t_{CLK} + k]	Figure 25
SPI-01-D-DDR	Low (CPOL = 0)	Falling (CPHA = 1)	1st SCLK rising	2	[5 × t_{CLK} + k]	Figure 26
SPI-11-D-DDR	High (CPOL = 1)	Rising (CPHA = 1)	1st SCLK falling	2	[5 × t_{CLK} + k]	Figure 26
SPI-01-Q-DDR	Low (CPOL = 0)	Falling (CPHA = 1)	1st SCLK rising	4	[3 × t_{CLK} + k]	Figure 27
SPI-11-Q-DDR	High (CPOL = 1)	Rising (CPHA = 1)	1st SCLK falling	4	[3 × t_{CLK} + k]	Figure 27

(1) For SPI-compatible protocols with bus width options and DDR, set the SDO_PROTOCOL bits in the PROTOCOL_CFG register to 001b.
(2) Configure the SPI_CPOL bits in the PROTOCOL_CFG register for the desired CPOL. The device supports CPHA = 1 only for SPI-compatible protocols with bus width options and DDR.
(3) For configuring the bus width, configure the BUS_WIDTH register.
(4) t_{READ} is the read time for reading the 16-bit output data word. k = (t_{SU_CSCK} + t_{HT_CKCS}).
(5) For ADS9234R devices, the read time for reading the 14-bit output data word is [7.5 × t_{CLK} + k] for a bus width of 1, [3.5 × t_{CLK} + k] for a bus width of 2, and [3 × t_{CLK} + k] for a bus width of 4.

Figure 25, Figure 26, and Figure 27 illustrate timing diagrams for the SPI-01-S-DDR and SPI-11-S-DDR, SPI-01-D-DDR and SPI-11-D-DDR, and SPI-01-Q-DDR and SPI-11-Q-DDR protocols, respectively.

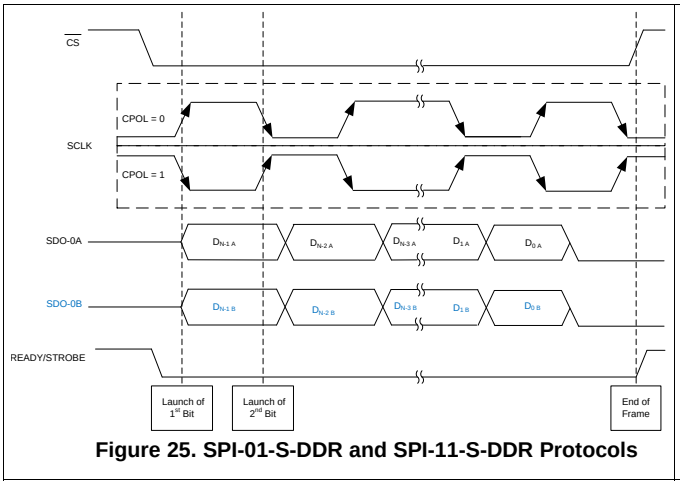

Figure 25. SPI-01-S-DDR and SPI-11-S-DDR Protocols

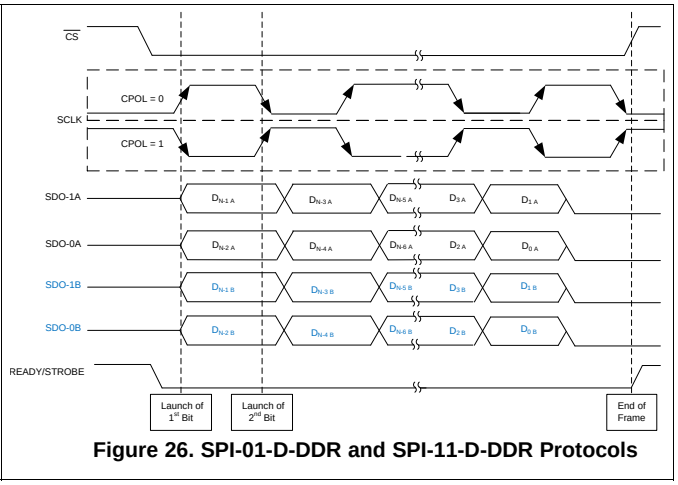

Figure 26. SPI-01-D-DDR and SPI-11-D-DDR Protocols

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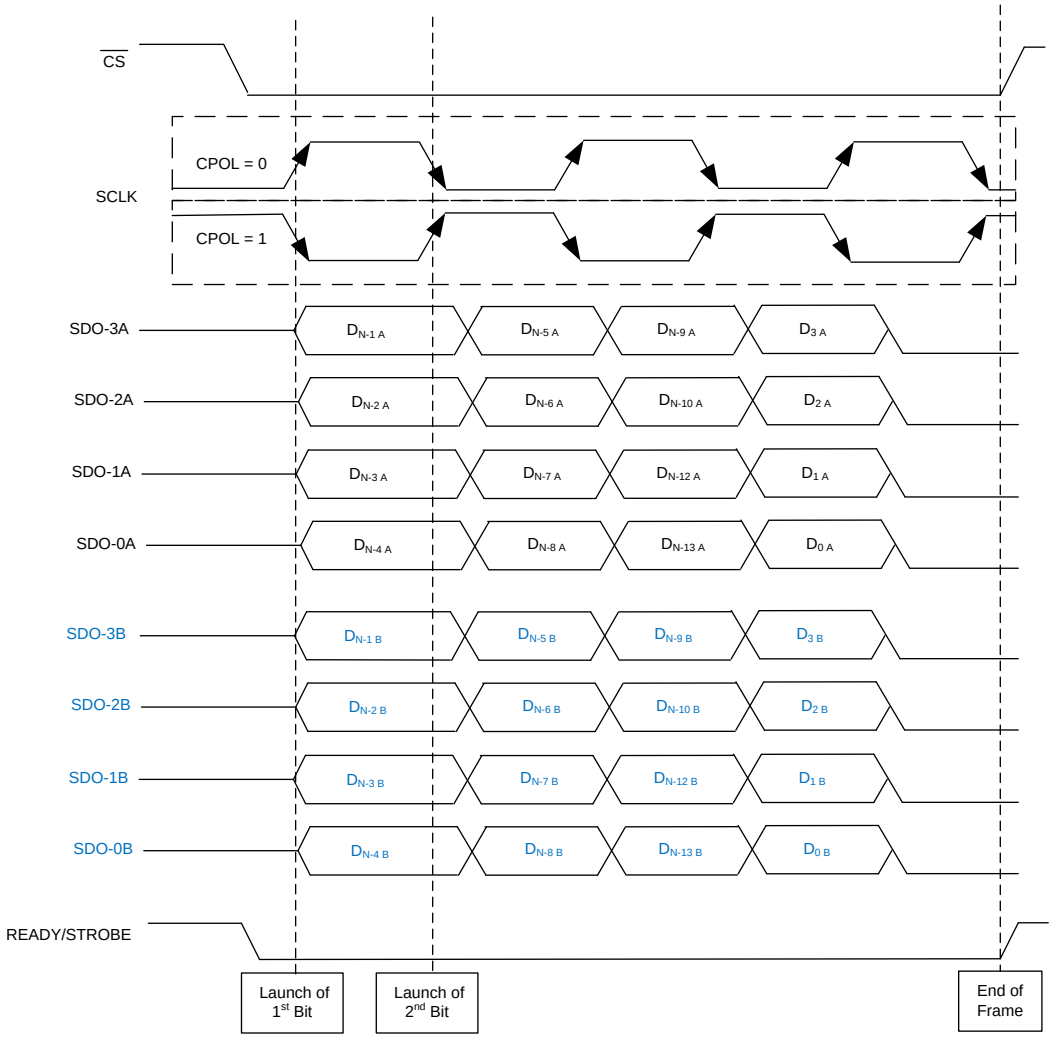

Figure 27. SPI-01-Q-DDR and SPI-11-Q-DDR Protocols

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7.6.2.1.4 Clock Re-Timer (CRT) Protocols (CRT-S-SDR, CRT-D-SDR, CRT-Q-SDR, CRT-S-DDR, CRT-D-DDR, CRT-Q-DDR)

In clock re-timer (CRT) protocols, the device sends out data on the SDO lines with a synchronized clock on the STROBE line. The data are synchronized to the rising edges of the STROBE pulses. For CRT protocols with a single data rate, the host can capture data on the falling edges of the STROBE pulses. For double data rate, the host must capture data on both edges of STROBE. The clock source for the STROBE output can be selected as an external clock (SCLK) or an internal clock by configuring the CRT_CLK_SELECT bits in the CRT_CFG register. For reading data from the device, SCLK is only required when the STROBE output is selected as an external clock. The SDOs that are not enabled by the BUS_WIDTH register are set to tri-state. Table 6 provides the details of different CRT protocols to read data from the device.

Table 6. CRT-S-SDR, CRT-D-SDR, CRT-Q-SDR, CRT-S-DDR, CRT-D-DDR, and CRT-Q-DDR Protocols for Reading From Device

PROTOCOL (1)	SCLK POLARITY (2)	CAPTURE EDGE	MSB LAUNCH EDGE	BUS WIDTH (3)	t_{READ} (4)	TIMING DIAGRAM
CRT-S-SDR	Low (CPOL = 0)	STROBE falling	1st STROBE rising	1	[15.5 × t_{STROBE} + m]	Figure 28
CRT-D-SDR	Low (CPOL = 0)	STROBE falling	1st STROBE rising	2	[7.5 × t_{STROBE} + m]	Figure 30
CRT-Q-SDR	Low (CPOL = 0)	STROBE falling	1st STROBE rising	4	[3.5 × t_{STROBE} + m]	Figure 32
CRT-S-DDR	Low (CPOL = 0)	STROBE rising and falling	1st STROBE rising	1	[7.5 × t_{STROBE} + m]	Figure 29
CRT-D-DDR	Low (CPOL = 0)	STROBE rising and falling	1st STROBE rising	2	[3.5× t_{STROBE} + m]	Figure 31
CRT-Q-DDR	Low (CPOL = 0)	STROBE rising and falling	1st STROBE rising	4	[1.5 × t_{STROBE} + m]	Figure 33

(1) For CRT protocols with SDR, set the SDO_PROTOCOL bits in the PROTOCOL_CFG register to 010b. For CRT protocols with DDR, set the SDO_PROTOCOL bits to 011b in the PROTOCOL_CFG register.
(2) The device only supports CPOL = 0 for CRT protocols with an external clock.
(3) For configuring the bus width, configure the BUS_WIDTH register.
(4) t_{READ} is the read time for reading the 16-bit output data word. For an external clock m = (t_{SU_CSCK} + t_{HT_CKCS}), and for an internal clock m = $t_{D\_CS\_STROBE}$.

Figure 28 through Figure 33 illustrate timing diagrams for the CRT-S-SDR, CRT-S-DDR, CRT-D-SDR, CRT-D-DDR, CRT-Q-SDR, and CRT-Q-DDR protocols, respectively.

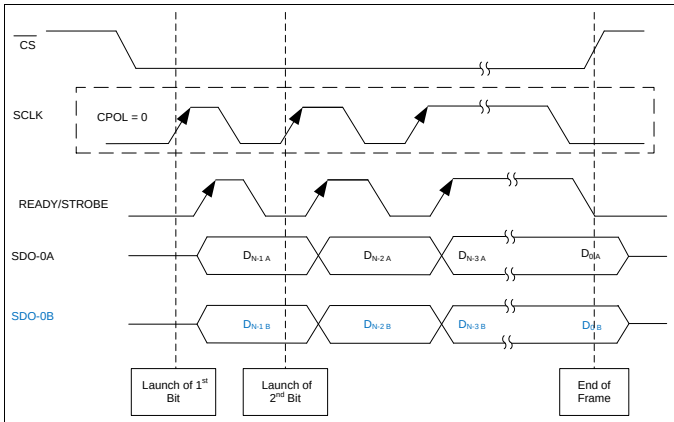

Figure 28. CRT-S-SDR Protocol

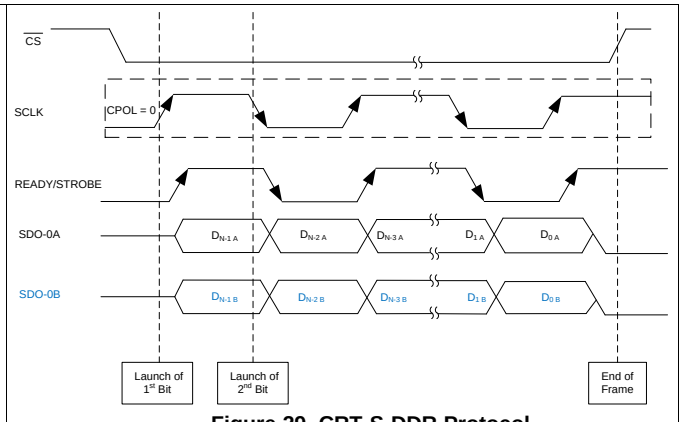

Figure 29. CRT-S-DDR Protocol

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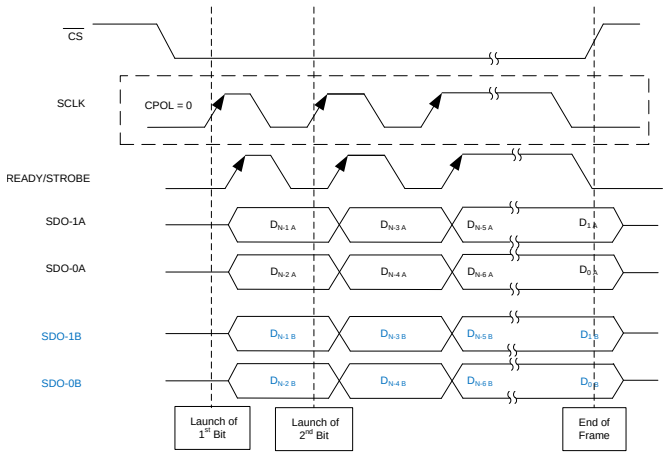

Figure 30. CRT-D-SDR Protocol

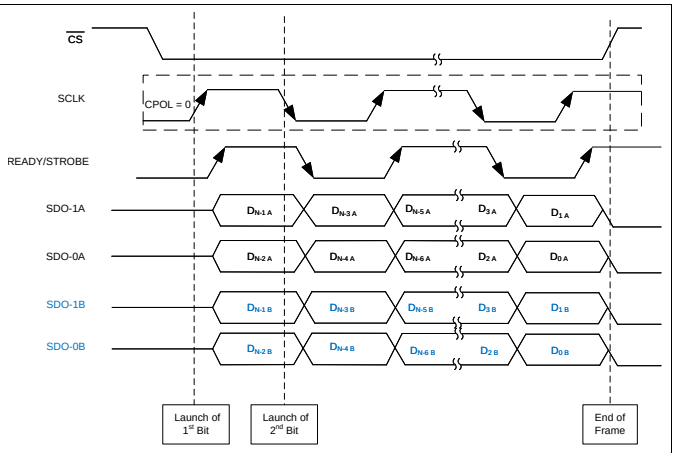

Figure 31. CRT-D-DDR Protocol

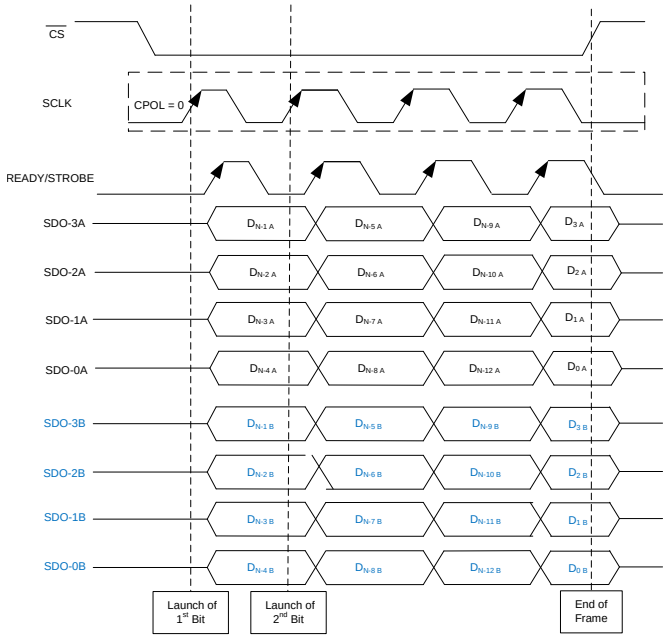

Figure 32. CRT-Q-SDR Protocol

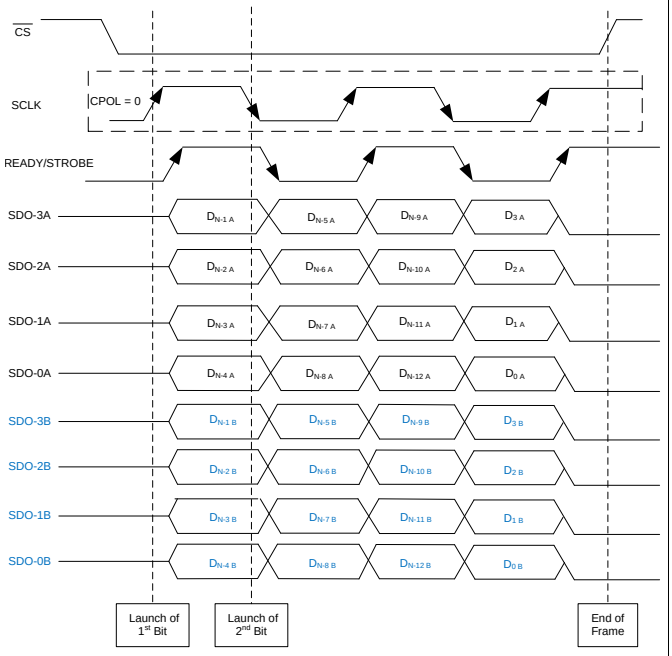

Figure 33. CRT-Q-DDR Protocol

For reading data, SCLK is only required when the STROBE output is selected as SCLK (external clock) in the CRT_CFG register. However, for configuring registers, SCLK is always required.

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7.6.2.1.5 Parallel Byte Protocols (PB-xy-AB-SDR, PB-xy-AA-SDR

In these protocols, the device sends out data from each ADC on all SDO lines in a byte format. The device supports all combinations of CPOL and CPHA in these protocols. The format of the data byte for these protocols can be set by the PARALLEL_MODE_DATA_FORMAT bits in the OUTPUT_DATA_WORD_CFG register. The device only supports a single data rate (SDR) in parallel byte protocols. Table 7 provides the details of different parallel byte protocols to read data from the device.

Table 7. PB-xy-AB-SDR, PB-xy-AA-SDR Protocols for Reading Data

PROTOCOL (1)	SCLK POLARITY (CPOL) (2)	SCLK PHASE (CPHA)	MSB LAUNCH EDGE	DATA FORMAT (3)	t_{READ} (4)	TIMING DIAGRAM
PB-00-AB-SDR	Low (CPOL = 0)	Rising (CPHA = 0)	$\overline{CS}$ falling	AB	[3.5 × t_{CLK} + k]	Figure 34
PB-01-AB-SDR	Low (CPOL = 0)	Falling (CPHA = 1)	1st SCLK rising	AB	[3.5 × t_{CLK} + k]	Figure 35
PB-10-AB-SDR	High (CPOL = 1)	Falling (CPHA = 1)	$\overline{CS}$ falling	AB	[3.5 × t_{CLK} + k]	Figure 34
PB-11-AB-SDR	High (CPOL = 1)	Rising (CPHA = 0)	1st SCLK falling	AB	[3.5 × t_{CLK} + k]	Figure 35
PB-00-AA-SDR	Low (CPOL = 0)	Rising (CPHA = 0)	$\overline{CS}$ falling	AA	[3.5 × t_{CLK} + k]	Figure 36
PB-01-AA-SDR	Low (CPOL = 0)	Falling (CPHA = 1)	1st SCLK rising	AA	[3.5 × t_{CLK} + k]	Figure 37
PB-10-AA-SDR	High (CPOL = 1)	Falling (CPHA = 1)	$\overline{CS}$ falling	AA	[3.5 × t_{CLK} + k]	Figure 36
PB-11-AA-SDR	High (CPOL = 1)	Rising (CPHA = 0)	1st SCLK falling	AA	[3.5 × t_{CLK} + k]	Figure 37

(1) For parallel byte protocols, set the SDO_PROTOCOL bits in the PROTOCOL_CFG register to 1xxb.
(2) Configure the SPI_CPOL and SPI_CPHA bits in the PROTOCOL_CFG register for the desired CPOL and CPHA.
(3) For selecting the data format for parallel byte protocols, configure the PARALLEL_MODE_DATA_FORMAT bits in the OUTPUT_DATA_WORD_CFG register.
(4) t_{READ} is the read time for reading the 16-bit output data word. k = (t_{SU_CSCK} + t_{HT_CKCS}).

Figure 34, Figure 35, Figure 36, and Figure 37 illustrate timing diagrams for the PB-00-AB-SDR and PB-10-AB-SDR, protocols, PB-01-AB-SDR and PB-11-AB-SDR, PB-00-AA-SDR and PB-10-AA-SDR, and PB-01-AA-SDR and PB-11-AA-SDR, respectively.

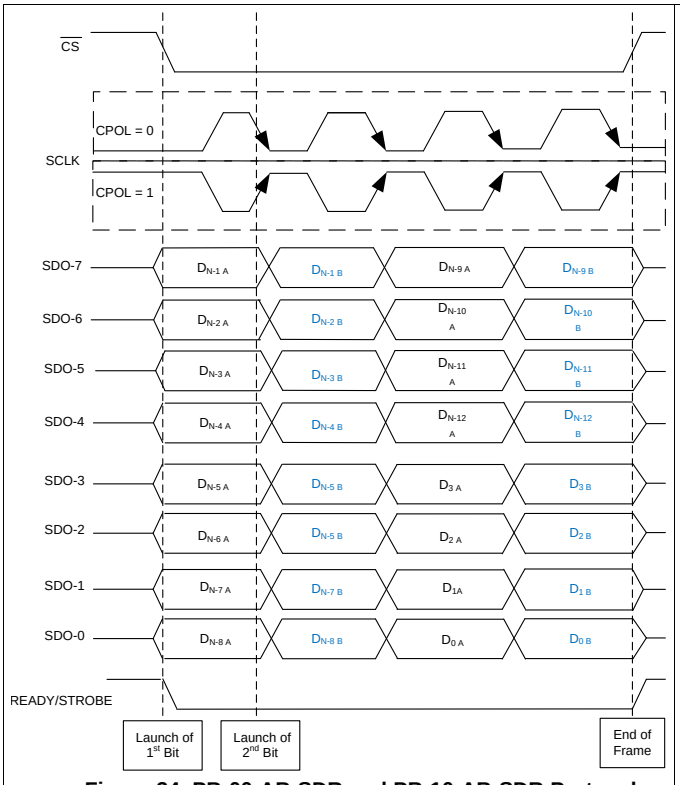

Figure 34. PB-00-AB-SDR and PB-10-AB-SDR Protocols

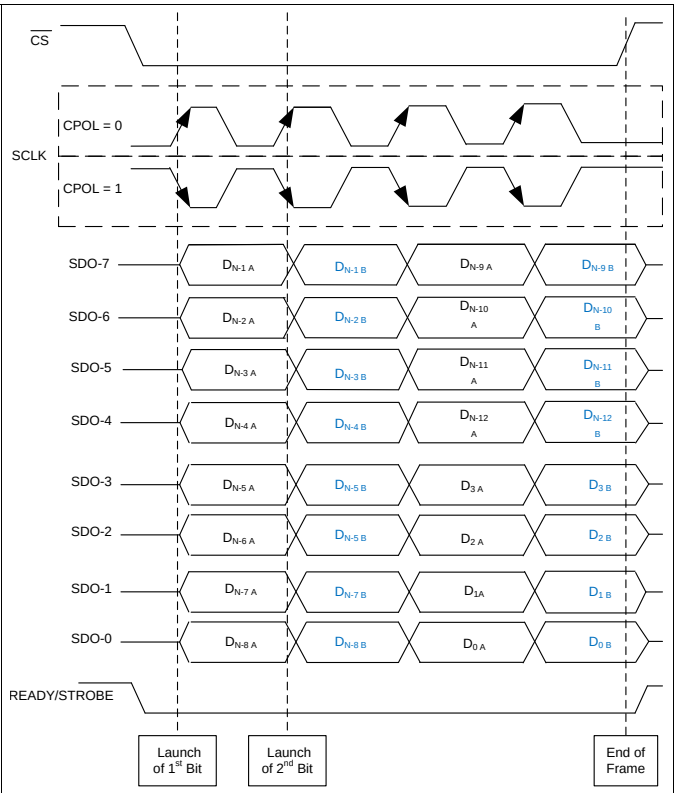

Figure 35. PB-01-AB-SDR and PB-11-AB-SDR Protocols

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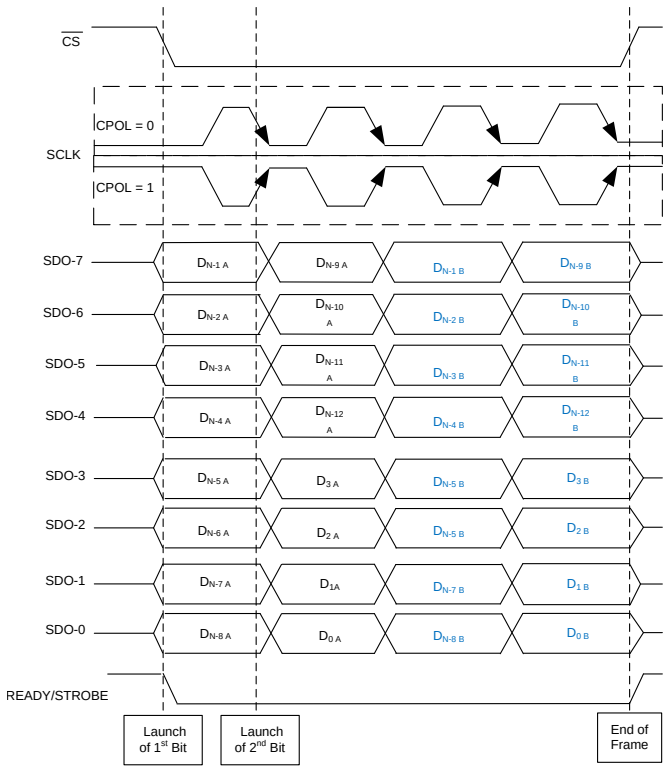

Figure 36. PB-00-AA-SDR and PB-10-AA-SDR Protocols

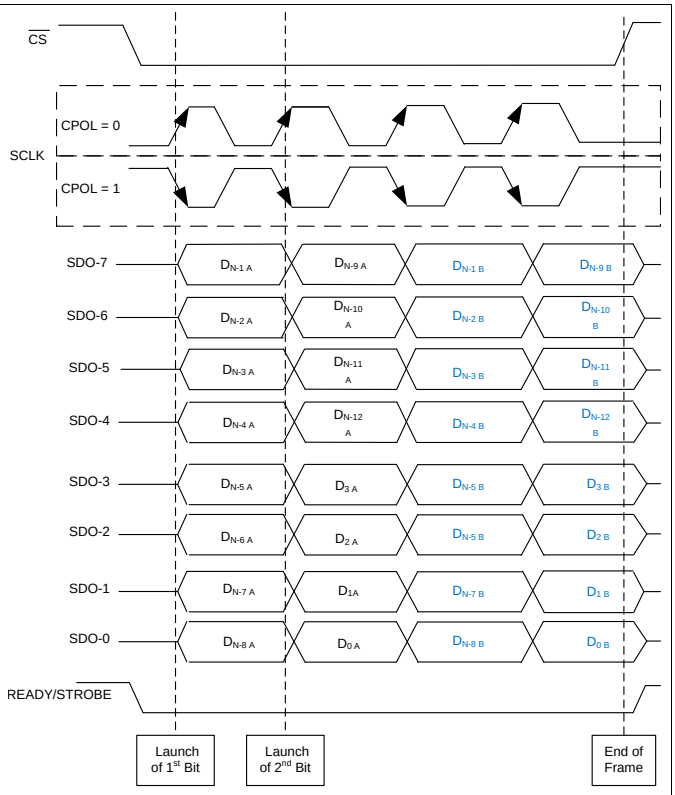

Figure 37. PB-01-AA-SDR and PB-11-AA-SDR Protocols

7.6.2.2 *Protocols for Configuring the Device*

The device supports an SPI protocol for writing into the device with all combinations of clock polarity and phase. On power-up or after reset, the device supports the SPI-00-S protocol for configuring the device. of As shown in Table 8, the host controller can use any of the four legacy, SPI-compatible protocols (SPI-00-S, SPI- 01-S, SPI-10-S, or SPI-11-S) to write data to the device.

Table 8. SPI Protocols for Configuring the Device

PROTOCOL	SCLK POLARITY (CPOL)(1)	SCLK PHASE (CPHA)(1)	MSB CAPTURE EDGE	t_{WRITE}(2)	TIMING DIAGRAM
SPI-00-S	Low (CPOL= 0)	Rising (CPHA = 0)	1st SCLK rising	[15.5 × t_{CLK} + k]	Figure 38
SPI-01-S	Low (CPOL= 0)	Falling (CPHA = 1)	1st SCLK falling	[15.5 × t_{CLK} + k]	Figure 39
SPI-10-S	High (CPOL= 1)	Falling (CPHA = 1)	1st SCLK falling	[15.5 × t_{CLK} + k]	Figure 38
SPI-11-S	High (CPOL= 1)	Rising (CPHA = 0)	1st SCLK rising	[15.5 × t_{CLK} + k]	Figure 39

(1) Configure the SPI_CPOL and SPI_CPHA bits in the PROTOCOL_CFG register for the desired CPOL and CPHA.
(2) t_{WRITE} is the write time for writing the 16-bit data word. k = (t_{SU_CSCK} + t_{HT_CKCS}).

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Figure 38 and Figure 39 show timing diagrams for the SPI-00-S, SPI-10-S and SPI-01-S, SPI-11-S protocols, respectively, for configuring the device.

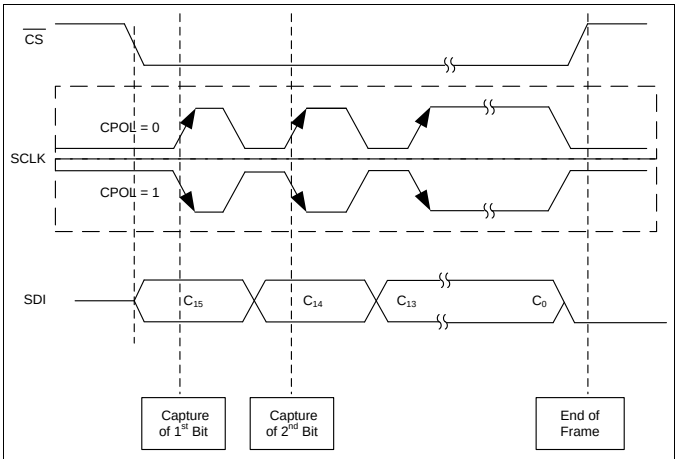

Figure 38. SPI-00-S and SPI-10-S Protocols for Configuring the Device

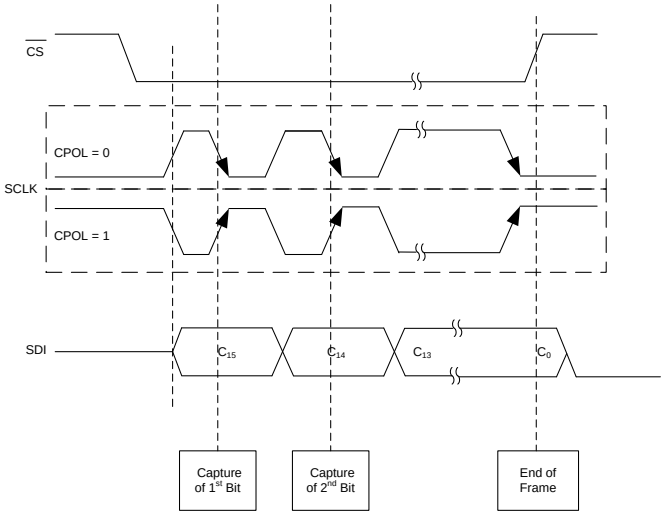

Figure 39. SPI-01-S and SPI-11-S Protocols for Configuring the Device

ADVANCE INFORMATION

7.6.3 Reading and Writing Registers

To read a register or write into a register, the host must provide a 16-bit command frame C[15:0] on SDI. A command frame consists of an OPCODE[3:0], ADDRESS[3:0], and DATA[7:0]. The host must keep the CONVST signal high for reading and writing the registers. Figure 40 shows the command frame. Table 9 provides the details of commands for reading and writing registers.

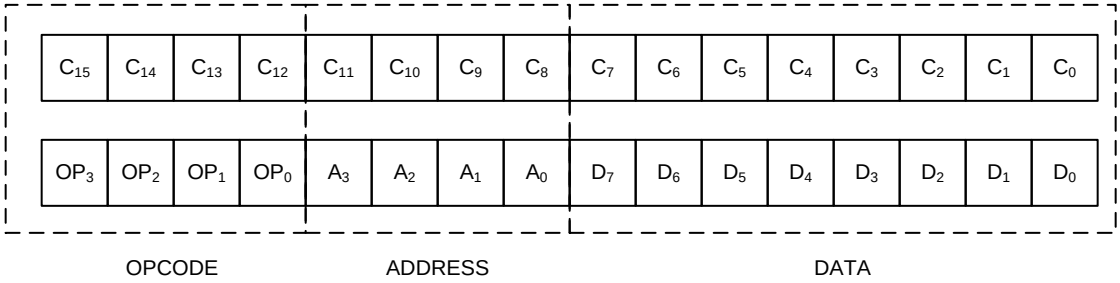

Figure 40. Command Frame C[15:0]

Table 9. Commands for Reading and Writing Registers

OPCODE[3:0]		DESCRIPTION	ADDRESS[3:0]	DATA[7:0]
0000	NOP0	Command for conversion control and reading conversion results	N/A	N/A
0001	WRITE	Command for writing registers	4-bit register address	8-bit register data
0010	READ(1)	Command for reading registers	4-bit register address	00h or FFh
0101	Set bit	Command for setting specific bits in a register without changing the other bits	4-bit register address	Bits with values of 1 in DATA are set and bits with values of 0 in register data are not changed.
0110	Clear bit	Command for clearing specific bits in a register without changing the other bits	4-bit register address	Bits with values of 1 in DATA are cleared and bits with values of 0 in register data are not changed.
1111	NOP1	Command for conversion control and reading conversion results	N/A	N/A

(1) Register data for READ command is provided by device in the next frame.

7.7 Register Maps

Table 10 lists the access codes for the ADS9224R, ADS9234R registers.

Table 10. ADS9224R, ADS9234R Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-W	R/W	Read or write
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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7.7.1 DEVICE_STATUS Register (address = 0h) [reset = 00h]

This register provides the error status of averaging mode and the status of zone 2 data transfer mode.

Figure 41. DEVICE_STATUS

7	6	5	4	3	2	1	0
0	0	0	0	0	ZONE2_ TRANSFER	AVG_ERROR	0
R-0b	R-0b	R-0b	R-0b	R-0b	R/W-0b	R/W-0b	R-0b

Table 11. DEVICE_STATUS Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	00000b	Reserved bits. Do not write. Reads return 00000b.
2	ZONE2_TRANSFER	R/W	0b	This bit is set when the device operates in zone 2 transfer mode with a wide read cycle. This bit is a sticky bit. Write 1 to this bit to clear.
1	AVG_ERROR	R/W	0b	This bit is set when the device receives a falling edge of $\overline{CS}$ before the current averaging operation is complete. This bit is a sticky bit. Write 1 to this bit to clear.
0	RESERVED	R	00000b	Reserved bits. Do not write. Reads return 00000b.

7.7.2 POWER_DOWN_CFG Register (address = 1h) [reset = 00h]

This register powers down different blocks in the device.

Figure 42. POWER_DOWN_CFG

7	6	5	4	3	2	1	0
0	0	PD_REFby2	0	PD_ADCB	0	PD_ADCA	PD_REF
R-0b	R-0b	R/W-0b	R-0b	R/W-0b	R-0b	R/W-0b	R/W-0b

Table 12. POWER_DOWN_CFG Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved bits. Do not write. Reads return 00b.
5	PD_REFby2	R/W	0b	This bit powers down the REFby2 output. 0: REFby2 is not powered down 1: REFby2 is powered down
4	RESERVED	R	0b	Reserved bits. Do not write. Reads return 00b.
3	PD_ADCB	R/W	0b	This bit powers down the ADC_B and REFBUF_B. 0: ADC_B and REFBUF_B are not powered down 1: ADC_B and REFBUF_B are powered down
2	RESERVED	R	0b	Reserved bits. Do not write. Reads return 00b.
1	PD_ADCA	R/W	0b	This bit powers down the ADC_A and REFBUF_A. 0: ADC_A and REFBUF_A are not powered down 1: ADC_A and REFBUF_A are powered down
0	PD_REF	R/W	0b	This bit powers down the internal reference voltage. 0: Internal reference voltage is not powered down 1: Internal reference voltage is powered down

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7.7.3 PROTOCOL_CFG Register (address = 2h) [reset = 00h]

This register configures the clock polarity (CPOL), clock phase (CPHA) for data transfer, and sets the protocol for reading data from the device.

Figure 43. PROTOCOL_CFG

7	6	5	4	3	2	1	0
0	SDO_PROTOCOL			0	0	SPI_CPOL	SPI_CPHA
R-0b	R/W-0b			R-0b	R-0b	R/W-0b	R/W-0b

Table 13. PROTOCOL_CFG Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0b	Reserved bits. Do not write. Reads return 0b.
6-4	SDO_PROTOCOL	R/W	000b	These bits set the protocol for reading data from the device. 000: Legacy, SPI-compatible protocols (SPI-xy-S-SDR); SPI-compatible protocols with bus width options and SDR (SPI-xy-D-SDR and SPI-xy-Q-SDR) protocols 001: SPI-compatible protocols with bus width options and DDR (SPI-x1-S-DDR, SPI-x1-D-DDR,SPI-x1-Q-DDR) protocols 010: Clock re-timer (CRT) protocols with SDR (CRT-S-SDR, CRT-D-SDR, CRT-Q-SDR) 011: CRT protocols with DDR (CRT-S-DDR, CRT-D-DDR, CRT-Q-DDR) 1xx: Parallel byte protocols.
3-2	RESERVED	R	00b	Reserved bits. Do not write. Reads return 00b.
1	SPI_CPOL	R/W	0b	This bit sets the clock polarity for reading data from the device and writing data into the device. 0: CPOL = 0 1: CPOL = 1
0	SPI_CPHA	R/W	0b	This bit sets the clock phase for reading data from the device and writing data into the device. 0: CPHA = 0 1: CPHA = 1

7.7.4 BUS_WIDTH Register (address = 3h) [reset = 00h]

This register configures the bus width (number of SDO Lines) for reading data from the device.

Figure 44. BUS_WIDTH

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SDO_WIDTH	
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-00b	

Table 14. BUS_WIDTH Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved bits. Do not write. Reads return 000000b.
1-0	SDO_WIDTH	R/W	00b	These bits set the number of SDO lines for reading data from the device. 0x: One SDO per ADC 10: Dual SDO per ADC 11: Quad SDO per ADC If the device is configured for parallel byte protocol, then SDO_WIDTH is ignored and the device sends data over all eight SDO lines as per the parallel byte protocol.

7.7.5 CRT_CFG Register (address = 4h) [reset = 00h]

This register selects the clock source for the strobe output for clock re-timer (CRT) protocols.

Figure 45. CRT_CFG

7	6	5	4	3	2	1	0
0	0	0	0	0	0	CRT_CLK_SELECT	
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-00b	

Table 15. CRT_CFG Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved bits. Do not write. Reads return 000000b.
1-0	CRT_CLK_SELECT	R/W	00b	These bits select the clock source for the strobe output for CRT protocols. 00: SCLK is used for the STROBE output 01: INTCLK is used for the STROBE output 10: INTCLK/2 is used for the STROBE output 11: INTCLK/4 is used for the STROBE output INTCLK is generated from the internal oscillator of the device.

7.7.6 OUTPUT_DATA_WORD_CFG Register (address = 5h) [reset = 00h]

This register configures the alignment of output data word, sets the output data word to a fixed pattern, and selects the format for the output data word in the parallel byte protocol.

Figure 46. OUTPUT_DATA_WORD_CFG

7	6	5	4	3	2	1	0
0	0	READY_MASK	PARALLEL_MODE_DATA_FORMAT	0	0	FIXED_PATTERN_DATA	DATA_RIGHT_ALIGNED
R-0b	R-0b	R/W-0b	R-0b	R-0b	R-0b	R/W-0b	R/W-0b

Table 16. OUTPUT_DATA_WORD_CFG Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved bits. Do not write. Reads return 00b.
5	READY_MASK	R/W	0b	This bit masks the READY output. 0: Does not mask the READY output 1: Masks the READY output, READY is set to 0 The STROBE output is provided in CRT protocols even if READY_MASK is set to 1. TI recommends masking the READY output for the *Conversion Control and Data Transfer Frame With Wide Read Cycle (Zone 2 Transfer)* section.
4	PARALLEL_MODE_DATA_FORMAT	R/W	0b	This bit selects the format for the output data word in the parallel byte protocol. 0: Data format AA: byte from ADC_A followed by byte from ADC_A (PB-xy-AA-zDR protocols) 1: Data format AB: byte from ADC_A followed by byte from ADC_B (PB-xy-AB-zDR protocols)
3-2	RESERVED	R	00b	Reserved bits. Do not write. Reads return 00b.
1	FIXED_PATTERN_DATA	R/W	0b	This bit enables a fixed pattern in the output data word. 0: Device provides the conversion results from the register data in the output data word 1: Device provides a fixed pattern (A55AA55Ah) in the output data word
0	DATA_RIGHT_ALIGNED	R/W	0b	This bit enables the right alignment in the output data word for ADS9234R devices. 0: Data are left-aligned in the output data word 1: Data are right-aligned in the output data word

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7.7.7 DATA_AVG_CFG Register (address = 6h) [reset = 00h]

This register configures the averaging of conversion results.

Figure 47. DATA_AVG_CFG

7	6	5	4	3	2	1	0
0	0	0	0	0	0	EN_DATA_AVG	
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-00b	

Table 17. DATA_AVG_CFG Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved bits. Do not write. Reads return 000000b.
1-0	EN_DATA_AVG	R/W	00b	These bits enable averaging of conversion results. 0x: No averaging 10: Enables averaging of two conversion results 11: Enables averaging of four conversion results

7.7.8 REFby2_OFFSET (address = 7h) [reset = 00h]

This register enables the offset for the REFby2 output.

Figure 48. REFby2_OFFSET

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	EN_REFby2_OFFSET
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-00b

Table 18. REFby2_OFFSET Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0000000b	Reserved bits. Do not write. Reads return 000000b.
0	EN_REFby2_OFFSET	R/W	0b	This bit enables the offset for the REFby2 output. 0: Offset for the REFby2 output is disabled 1: Offset for the REFby2 output is enabled and the REFby2 output increases by 100 mV

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR) analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section presents general principles for designing these circuits, followed by an application circuit designed using the ADS92x4R.

8.1.1 ADC Input Driver

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a charge kickback filter. The amplifier is used for signal conditioning of the input signal and the low output impedance of the amplifier provides a buffer between the signal source and the switched capacitor inputs of the ADC. The charge kickback filter helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC, and band-limits the wideband noise contributed by the front-end circuit. Careful design of the front-end circuit is critical to meet the linearity and noise performance of the ADS92x4R.

8.1.1.1 Charge-Kickback Filter

The charge-kickback filter is an RC filter at the input pins of the ADC that filters the broadband noise from the front-end drive circuitry, and attenuates the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor, C_{FLT} (as shown in Figure 49), is connected from each input pin of the ADC to the ground. This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. Generally, the value of this capacitor must be at least 20 times the specified value of the ADC sampling capacitance. For the ADS92x4R, the input sampling capacitance is equal to 16 pF; therefore, for optimal performance, keep C_{FLT} greater than 320 pF. This capacitor must be a COG- or NPO-type. The type of dielectric used in COG or NPO ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

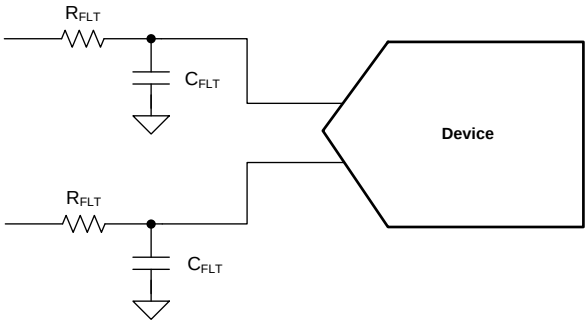

Figure 49. Charge Kickback Filter

Driving capacitive loads can degrade the phase margin of the input amplifier, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} helps with amplifier stability, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability of the driver amplifier and distortion performance of the design. Always verify the stability and settling behavior of the driving amplifier and charge-kickback filter by TINA-TI™ SPICE simulation. Keep the tolerance of the selected resistors less than 1% to keep the inputs balanced.

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Application Information (continued)

8.1.2 Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type, as well as the performance goals, of the data acquisition system. Some key amplifier specifications to consider when selecting an appropriate amplifier to drive the inputs of the ADC are:

- Small-signal bandwidth. Select the small-signal bandwidth of the input amplifiers to be as high as possible after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the ADC sample-and-hold capacitor and the RC filter (the charge-kickback filter) at the inputs of the ADC. Higher bandwidth amplifiers offer faster settling times when driving the capacitive load of the charge-kickback filter, thus reducing harmonic distortion at higher input frequencies. Equation 4 describes the unity gain bandwidth (UGB) of the amplifier to be selected in order to maintain the overall stability of the input driver circuit:

$$UGB \geq 4 \times \left(\frac{1}{2\pi \times R_{FLT} \times C_{FLT}} \right) \quad (4)$$

- Distortion. Both the ADC and the input driver introduce distortion in a data acquisition block. Equation 5 shows that to make sure that the distortion performance of the data acquisition system is not limited by the front-end circuit, the distortion of the input driver must be at least 10 dB less than the distortion of the ADC:

$$THD_{AMP} \leq THD_{ADC} - 10\,(dB) \quad (5)$$

- Noise. Noise contribution of the front-end amplifiers must be as low as possible to prevent any degradation in SNR performance of the system. Generally, to make sure that the noise performance of the data acquisition system is not limited by the front-end circuit, the total noise contribution from the front-end circuit must be kept below 20% of the input-referred noise of the ADC. Equation 6 explains that noise from the input driver circuit is band-limited by designing a low cutoff frequency, charge-kickback filte:

$$N_G \times \sqrt{2} \times \sqrt{\left(\frac{V_{1/f\_AMP\_PP}}{6.6} \right)^2 + e_{n\_RMS}^2 \times \frac{\pi}{2} \times f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{-\left(\frac{SNR(dB)}{20} \right)}$$

where

- V_{1/f_AMP_PP} is the peak-to-peak flicker noise in μV
- e_{n_RMS} is the amplifier broadband noise density in nV/√Hz
- f_{-3dB} is the 3-dB bandwidth of the charge-kickback filter
- N_G is the noise gain of the front-end circuit that is equal to 1 in a buffer configuration (6)

- Settling Time. For DC signals with fast transients that are common in a multiplexed application, the input signal must settle within an 16-bit accuracy at the device inputs during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired 16-bit accuracy. Therefore, always verify the settling behavior of the input driver by TINA-TI SPICE simulations before selecting the amplifier.

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8.2 Typical Application

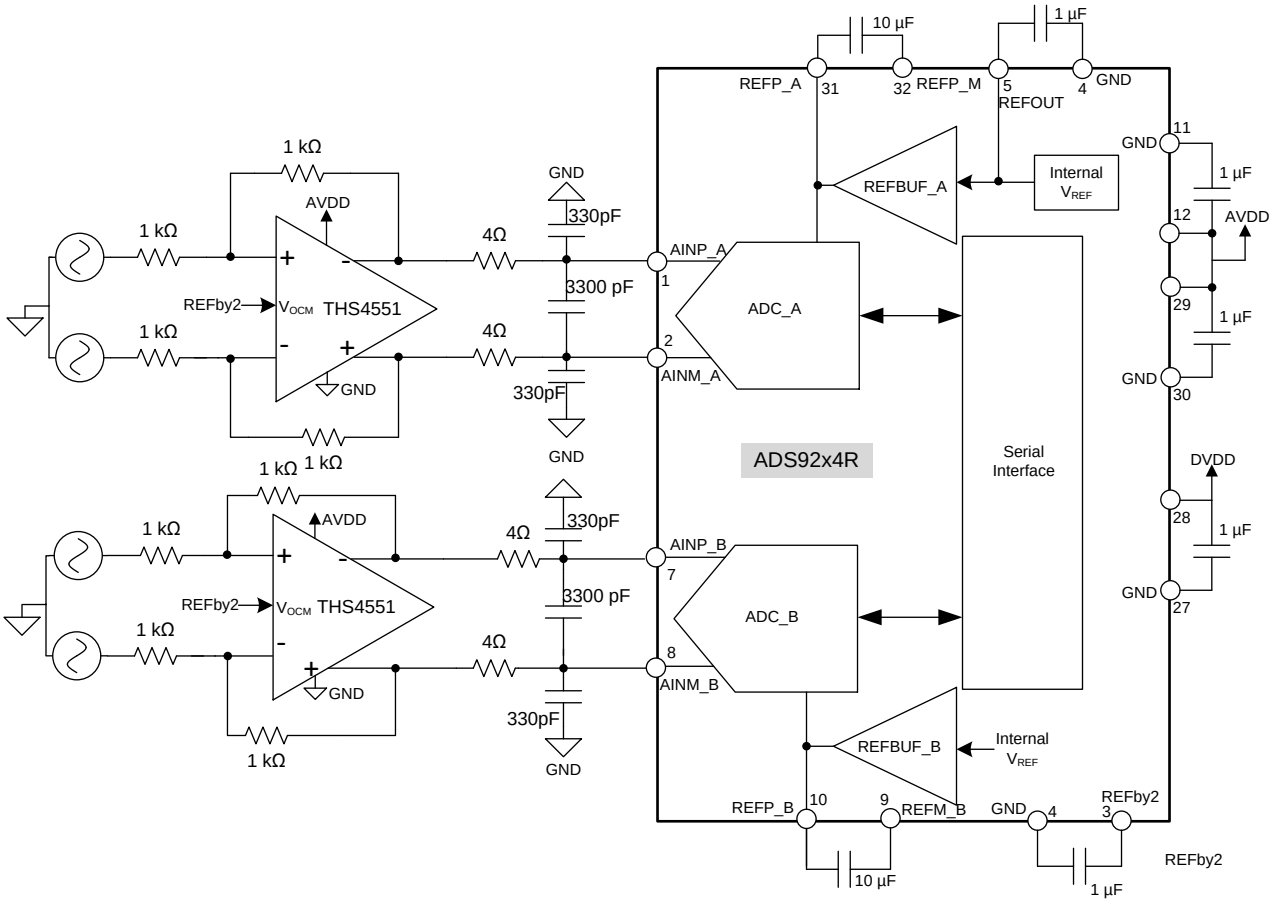

Figure 50. DAQ Circuit for Lowest Distortion and Noise With the ADS92x4R for a 100-kHz Input Signal

8.2.1 Design Requirements

The design parameters are listed in Table 19 for this example.

Table 19. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
ADC sample rate	3 MSPS
Analog input signal	100 kHz, 8.192 V_{PP}, fully differential
SNR	> 92 dB
THD	< –105dB
INL	< ±1 LSB
Power supply	5-V analog, 3.3-V digital

8.2.2 Detailed Design Procedure

Figure 50 shows an application circuit for this example. The device incorporates an internal 2.5-V reference voltage and independent matched reference buffers for each ADC. The internal reference output (REFOUT) is decoupled with a 1-µF capacitor. The matched reference buffers provide a gain of 1.6384 V/V and generate a high-precision, 4.096-V reference voltage for each ADC channel. Decouple the reference buffer outputs (the REFP_A and REFP_B pins) with the REFM_A and REFM_B pins, respectively, with 10-µF decoupling capacitors. The circuit in Figure 50 shows a fully-differential data acquisition (DAQ) block optimized for low distortion and noise using the THS4551 and the ADS92x4R. Both differential ADC inputs are driven using a high-bandwidth, low-distortion, fully differential amplifier (FDA) designed in a gain of 1 V/V and an optimal RC charge-

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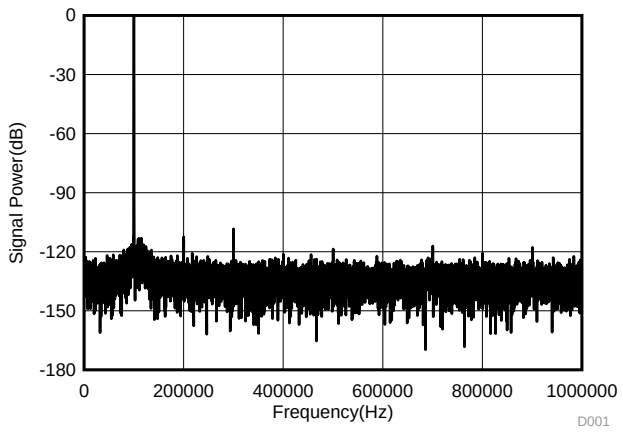
kickback filter before going to the ADC. Generally, the distortion from the input driver must be at least 10 dB less than the ADC distortion. Therefore, these circuits use the low-power THS4551 as an input driver that provides exceptional AC performance because of its extremely low-distortion and high bandwidth specifications. In addition, the components of the charge kickback filter are selected to keep the noise from the front-end circuit low without adding distortion. This front-end circuit configuration requires a differential signal at the input of the FDA and provides a differential output to drive the ADC inputs. The FDA establishes a fixed common-mode voltage at the ADC inputs using the VOCM input pin from the FDA. The ADS92x4R incorporates a REFby2 buffer output for setting the common-mode voltage. The ADS92x4R REFby2 output is decoupled using a 1-µF capacitor and connected to each FDA VOCM input pin. Each VOCM pin is decoupled using a 0.1-µF capacitor. For a complete schematic, see the ADS9224REVM-PDK user's guide located in the ADS9224R SAR analog to digital converter evaluation module tool folder.

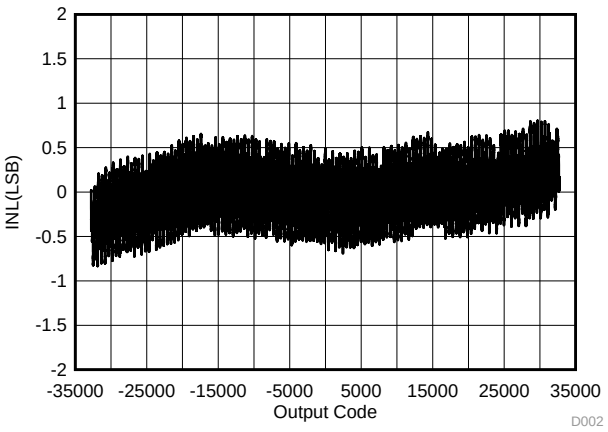
8.2.3 Application Curves

Figure 51 provides the typical FFT for the circuit in Figure 50 and Figure 52 provides the typical INL for the circuit in Figure 50.



SNR = 92.8 dB, THD = –105 dB, ENOB = 14.9 bits

Figure 51. Typical FFT With 100-kHz Signal



INL = ±0.8 LSB, DNL = ±0.2 LSB

Figure 52. Typical INL

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9 Power Supply Recommendations

The devices have two separate power supplies: AVDD and DVDD. The reference buffers, internal reference voltage, and converter modules (ADC_A and ADC_B) operate on AVDD. The serial interface operates on DVDD. AVDD and DVDD can be independently set to any value within their permissible ranges.

To operate the device with SCLK more than 20-MHz, TI recommends to set the DVDD voltage as: 2.35 V ≤ DVDD ≤ 5.5 V.

As shown in Figure 53, connect pins 12 and 29 together and place 1-µF decoupling capacitors between pin 12 (AVDD) and pin11 (GND), and between pin 29 (AVDD) and pin 30 (GND). To decouple the DVDD supply, place a 1-µF decoupling capacitor between pin 28 (DVDD) and pin 27 (GND).

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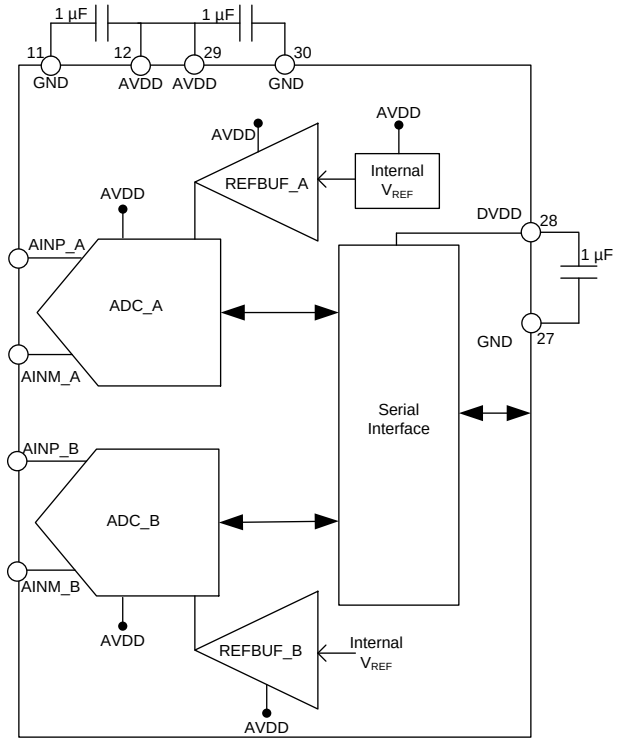

Figure 53. Power-Supply Decoupling

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10 Layout

10.1 Layout Guidelines

This section provides some layout guidelines for achieving optimum performance with the ADS92x4R.

10.1.1 Signal Path

As illustrated in Figure 54, the analog input signals are routed in opposite directions to the digital connections. The reference decoupling components are kept away from the switching digital signals. This arrangement prevents noise generated by digital switching activity from coupling to sensitive analog signals.

10.1.2 Grounding and PCB Stack-Up

Low inductance grounding is critical for achieving optimum performance. Grounding inductance is kept below 1 nH with 15-mil grounding vias and a printed circuit board (PCB) layout design that has at least four layers. Place all critical components of the signal chain on the top layer with a solid analog ground from subsequent inner layers to minimize via length to ground.

10.1.3 Decoupling of Power Supplies

Place the decoupling capacitors on AVDD and DVDD within 20 mil from the respective pins, and use a 15-mil via to ground from each capacitor. Avoid placing vias between any supply pin and the respective decoupling capacitor.

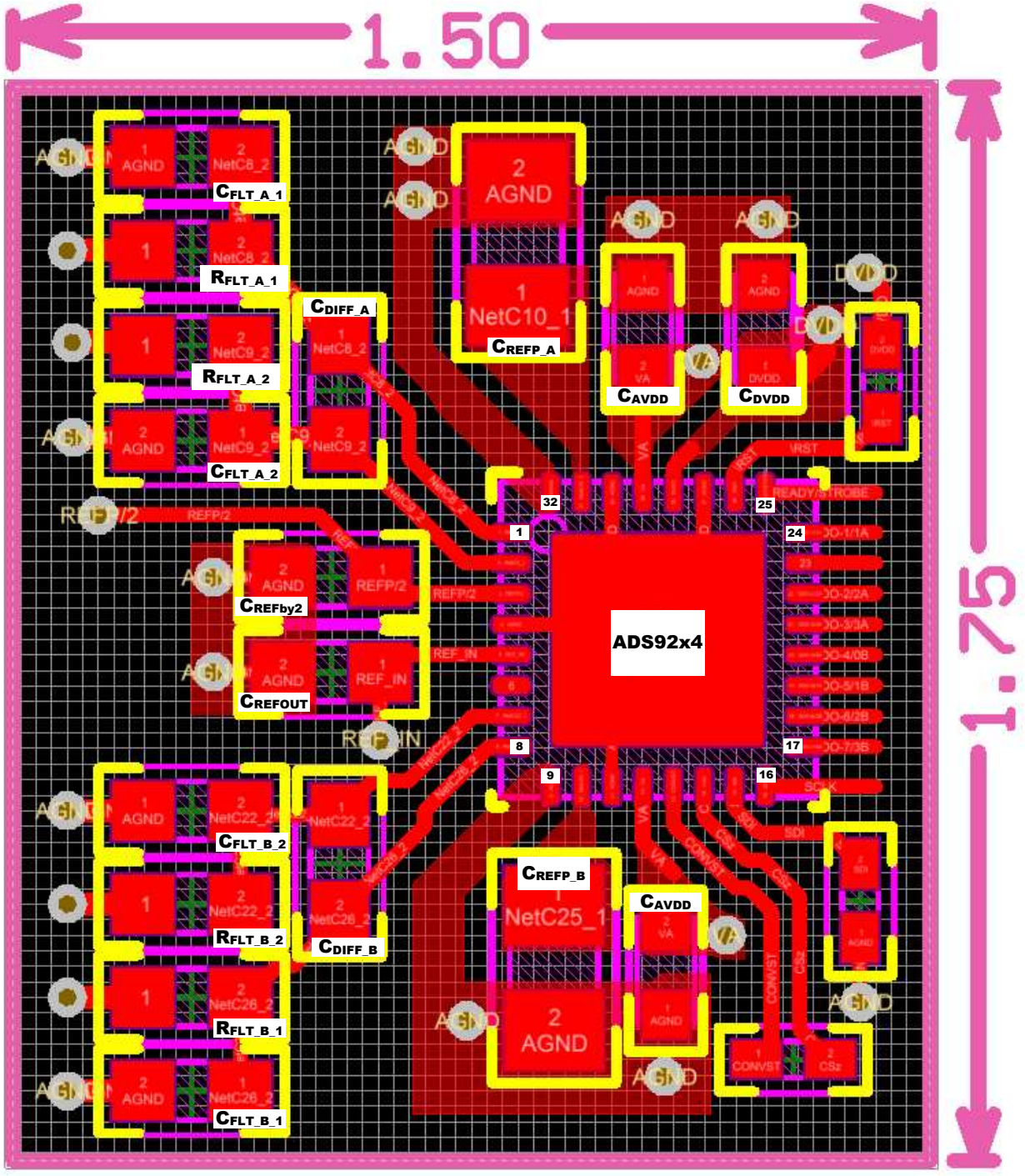
10.1.4 Reference Decoupling

Dynamic currents are present at the REFP_x and REFM_x pins during the conversion phase, and excellent decoupling is required to achieve optimum performance. Place a 10-µF, X7R-grade, ceramic capacitor with at least a 10-V rating, as illustrated in Figure 54. Select 0603- or 0805-size capacitors to keep equivalent series inductance (ESL) low. Connect the REFM_x pins to the decoupling capacitor before a ground via. Also place decoupling capacitors on the REFOUT and REFby2 pins.

10.1.5 Differential Input Decoupling

Dynamic currents are also present at the differential analog inputs of the ADS92x4R. Use C0G- or NPO-type capacitors to decouple these inputs because with these type of capacitors, capacitance stays almost constant over the full input voltage range. Lower-quality capacitors (such as X5R and X7R) have large capacitance changes over the full input-voltage range that may cause degradation in the performance of the device.

10.2 Layout Example



NOTE: Dimensions are in cm.

Figure 54. Example Layout for the ADS92x4R

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11 Device and Documentation Support

11.1 Related Documentation

For related documentation see the following:

- *THS4551 Low-Noise, Precision, 150-MHz, Fully Differential Amplifier*
- *TI Precision Designs: Verified Design 12 Bit 1 MSPS Single Supply Dual Channel Data Acquisition System for Optical Encoders in Motor Control Application*
- *REF50xx Low-Noise, Very Low Drift, Precision Voltage Reference*
- *OPAx350 High-Speed, Single-Supply, Rail-to-Rail Operational Amplifiers MicroAmplifier Series*
- *THS452x Very Low Power, Negative Rail Input, Rail-To-Rail Output, Fully Differential Amplifier*
- ADS9224REVM-PDK User's Guide

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

TINA-TI, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS9224RIRHBR	PREVIEW	VQFN	RHB	32	3000	TBD	Call TI	Call TI	-40 to 125		
XDS9224RIRHBR	ACTIVE	VQFN	RHB	32	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XDS9234RIRHBR	ACTIVE	VQFN	RHB	32	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

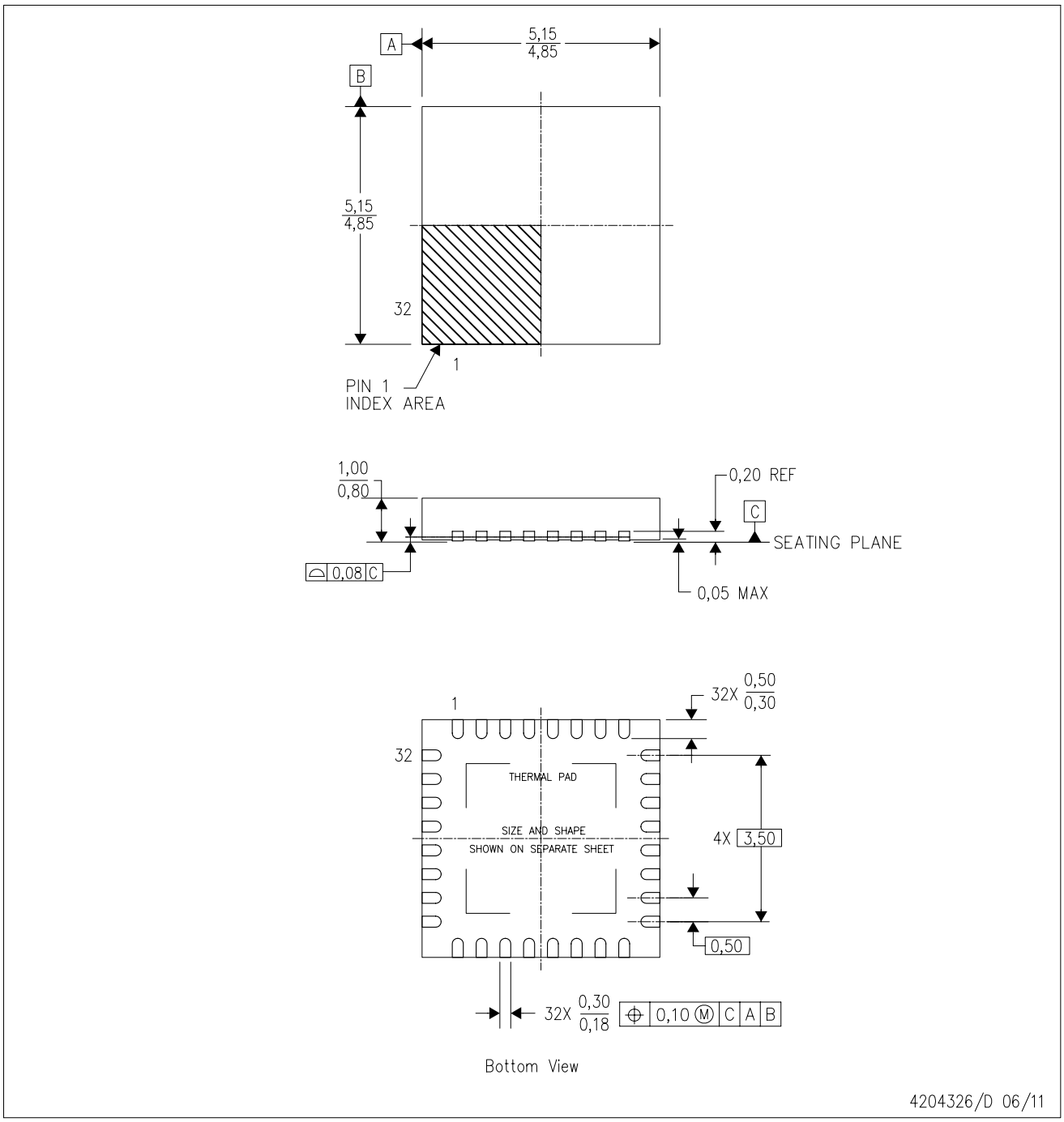
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

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