1.5V Drive Nch+Pch MOSFET

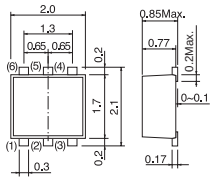
US6M11

●Structure
Silicon N-channel MOSFET /
Silicon P-channel MOSFET

●Features
1) Nch MOSFET and Pch MOSFET are put in TUMT6 package.
2) Low on-resistance.
3) Low voltage drive (1.5V drive).
4) Built-in G-S Protection Diode.

●Dimensions (Unit : mm)

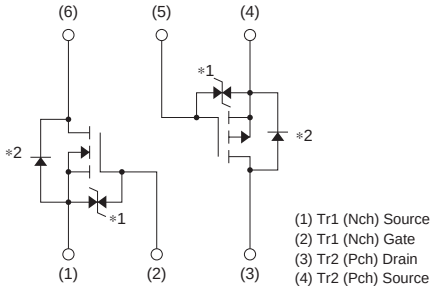
TUMT6



Abbreviated symbol : M11

●Applications
Switching

●Inner circuit



∗1 ESD PROTECTION DIODE
∗2 BODY DIODE

●Packaging specifications

Type	Package	Taping
	Code	TR
	Basic ordering unit (pieces)	3000
US6M11		◯

●Absolute maximum ratings (Ta=25°C)

Parameter		Symbol	Limits		Unit
			Tr1 : Nchannel	Tr2 : Pchannel	
Drain-source voltage		V_{DSS}	20	−12	V
Gate-source voltage		V_{GSS}	±10	±10	V
Drain current	Continuous	I_D	±1.5	±1.3	A
	Pulsed	I_{DP} ∗1	±6	±5.2	A
Source current (Body diode)	Continuous	I_S	0.5	−0.5	A
	Pulsed	I_{SP} ∗1	6	−5.2	A
Power dissipation		P_D ∗2	1.0		W / TOTAL
			0.7		W / ELEMENT
Channel temperature		Tch	150		°C
Range of storage temperature		Tstg	−55 to +150		°C

∗1 Pw≤10µs, Duty cycle≤1%
∗2 Mounted on a ceramic board.

●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	Rth(ch-a) ∗	125	°C/W / TOTAL
		179	°C/W / ELEMENT

∗ Mounted on a ceramic board

<N-ch>

●**Electrical characteristics** (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	±10	μA	V_{GS}= ±10V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	20	–	–	V	I_D= 1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	1	μA	V_{DS}= 20V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	0.3	–	1.0	V	V_{DS}= 10V, I_D= 1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$*	–	130	180	mΩ	I_D= 1.5A, V_{GS}= 4.5V
		–	170	240	mΩ	I_D= 1.5A, V_{GS}= 2.5V
		–	220	310	mΩ	I_D= 0.8A, V_{GS}= 1.8V
		–	300	600	mΩ	I_D= 0.3A, V_{GS}= 1.5V
Forward transfer admittance	$\|Y_{fs}\|$ *	1.6	–	–	S	V_{DS}= 10V, I_D= 1.5A
Input capacitance	C_{iss}	–	110	–	pF	V_{DS}= 10V
Output capacitance	C_{oss}	–	18	–	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	–	15	–	pF	f=1MHz
Turn-on delay time	$t_{d\ (on)}$ *	–	5	–	ns	V_{DD}≒ 10V I_D= 1A V_{GS}= 4.5V R_L≒ 10Ω R_G=10Ω
Rise time	t_r *	–	5	–	ns	
Turn-off delay time	$t_{d\ (off)}$ *	–	20	–	ns	
Fall time	t_f *	–	3	–	ns	
Total gate charge	Q_g *	–	1.8	–	nC	V_{DD}≒10V, V_{GS}= 4.5V
Gate-source charge	Q_{gs} *	–	0.3	–	nC	I_D= 1.5A
Gate-drain charge	Q_{gd} *	–	0.3	–	nC	R_L≒ 6.7Ω, R_G= 10Ω

*Pulsed

●**Body diode characteristics** (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	–	–	1.2	V	I_S= 1.5A, V_{GS}=0V

*Pulsed

<P-ch>

●**Electrical characteristics** (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	–	–	±10	μA	V_{GS}= ±10V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)\ DSS}$	–12	–	–	V	I_D= –1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	–1	μA	V_{DS}= –12V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	–0.3	–	–1.0	V	V_{DS}= –6V, I_D= –1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$*	–	190	260	mΩ	I_D= –1.3A, V_{GS}= –4.5V
		–	280	390	mΩ	I_D= –0.6A, V_{GS}= –2.5V
		–	400	600	mΩ	I_D= –0.6A, V_{GS}= –1.8V
		–	530	1060	mΩ	I_D= –0.2A, V_{GS}= –1.5V
Forward transfer admittance	$\|Y_{fs}\|$ *	1.4	–	–	S	V_{DS}= –6V, I_D= –1.3A
Input capacitance	C_{iss}	–	290	–	pF	V_{DS}= –6V
Output capacitance	C_{oss}	–	28	–	pF	V_{GS}= 0V
Reverse transfer capacitance	C_{rss}	–	21	–	pF	f=1MHz
Turn-on delay time	$t_{d\ (on)}$ *	–	8	–	ns	V_{DD}≒ –6V I_D= –0.6A V_{GS}= –4.5V R_L≒ 10Ω R_G= 10Ω
Rise time	t_r *	–	10	–	ns	
Turn-off delay time	$t_{d\ (off)}$ *	–	30	–	ns	
Fall time	t_f *	–	9	–	ns	
Total gate charge	Q_g *	–	2.4	–	nC	V_{DD}≒ –6V, V_{GS}= –4.5V
Gate-source charge	Q_{gs} *	–	0.6	–	nC	I_D= –1.3A
Gate-drain charge	Q_{gd} *	–	0.4	–	nC	R_L≒ 4.6Ω, R_G= 10Ω

*Pulsed

●**Body diode characteristics** (Source-drain) (Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward voltage	V_{SD} *	–	–	–1.2	V	I_S= –1.3A, V_{GS}=0V

*Pulsed

●Electrical characteristic curves

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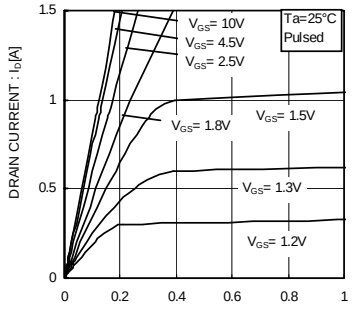


Fig.1 Typical Output Characteristics(Ⅰ)

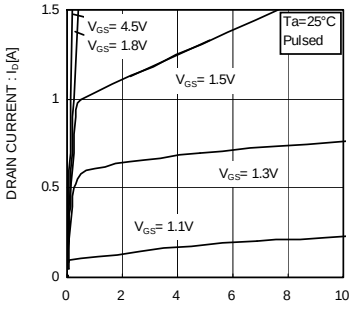


Fig.2 Typical Output Characteristics(Ⅱ)

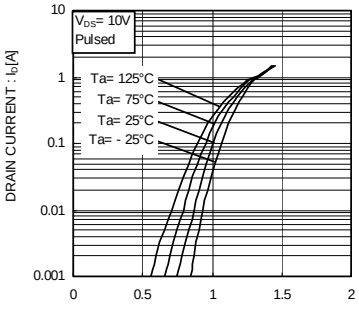


Fig.3 Typical Transfer Characteristics

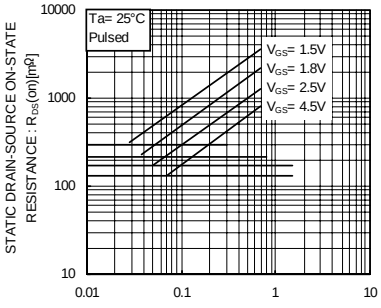


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(Ⅰ)

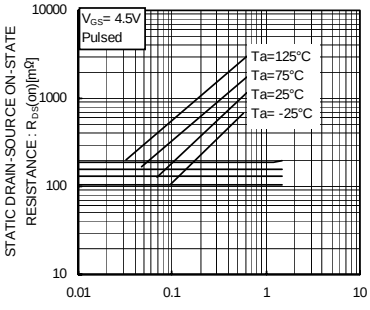


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(Ⅱ)

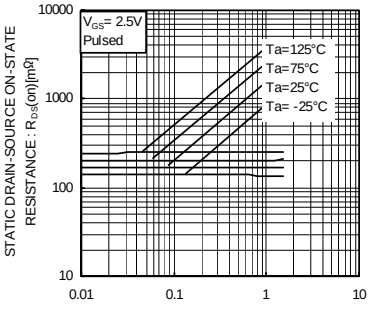


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(Ⅲ)

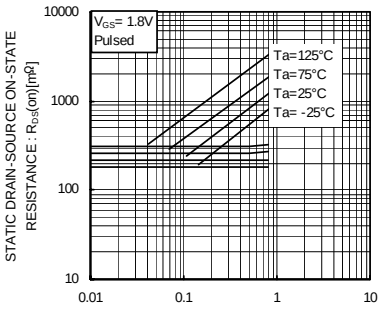


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(Ⅳ)

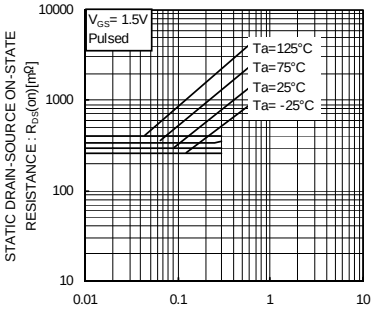


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(Ⅴ)

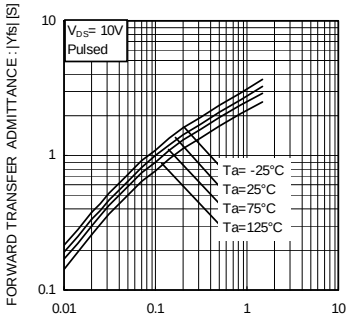
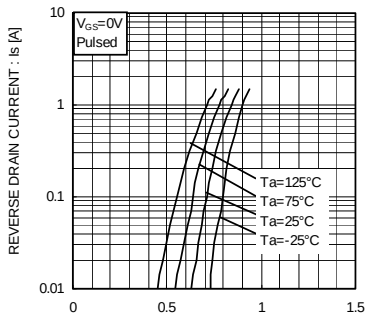
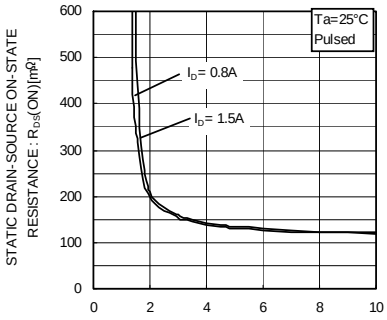


Fig.9 Forward Transfer Admittance vs. Drain Current



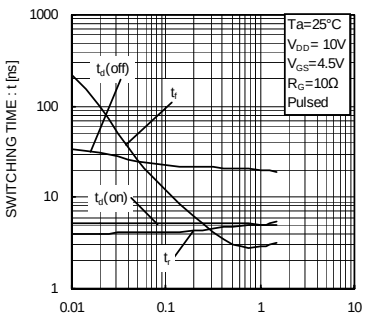
SOURCE-DRAIN VOLTAGE : V_{SD} [V]

Fig.10 Reverse Drain Current vs. Sourse-Drain Voltage



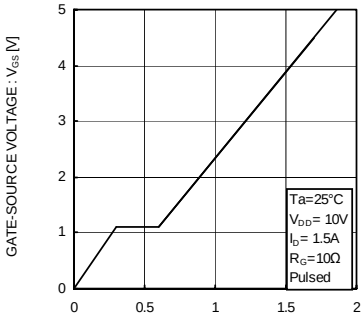
GATE-SOURCE VOLTAGE : V_{GS}[V]

Fig.11 Static Drain-Source On-State Resistance vs. Gate Source Voltage



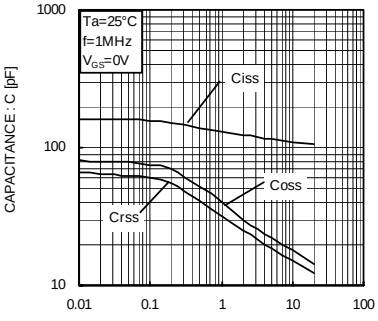
DRAIN-CURRENT : I_D[A]

Fig.12 Switching Characteristics



TOTAL GATE CHARGE : Qg [nC]

Fig.13 Dynamic Input Characteristics



DRAIN-SOURCE VOLTAGE : V_{DS}[V]

Fig.14 Typical Capacitance vs. Drain-Source Voltage

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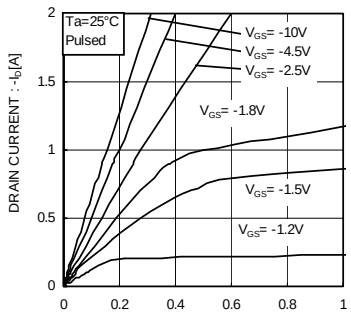

Fig.1 Typical output characteristics(Ⅰ)

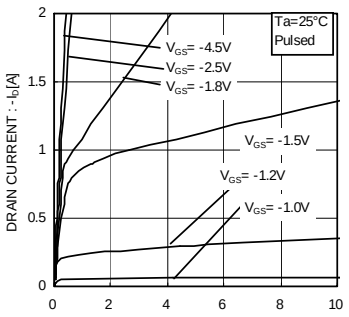

Fig.2 Typical output characteristics(Ⅱ)

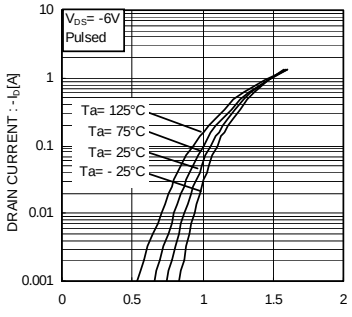

Fig.3 Typical Transfer Characteristics

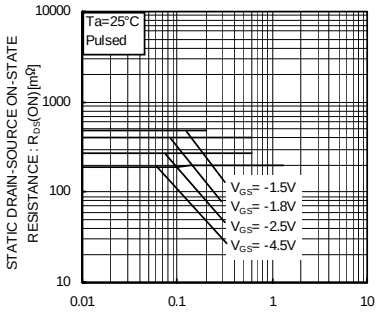

Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(Ⅰ)

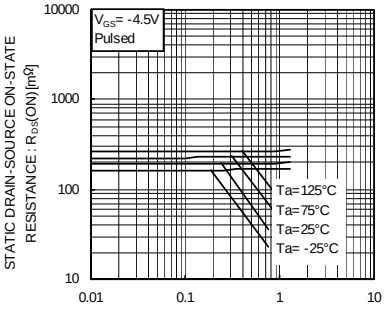

Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(Ⅱ)

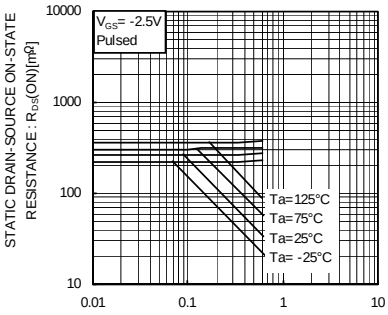

Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(Ⅲ)

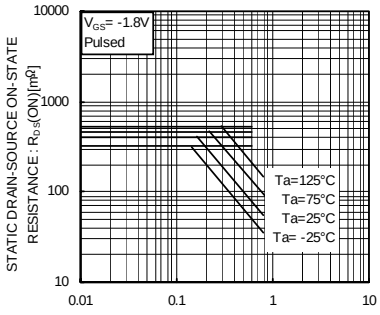

Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(Ⅳ)

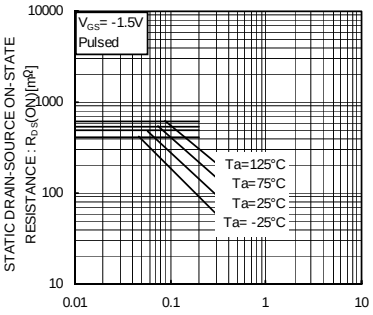

Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(Ⅳ)

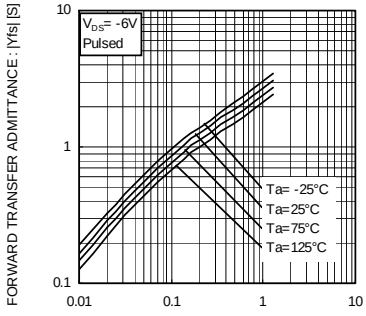

Fig.9 Forward Transfer Admittance vs. Drain Current

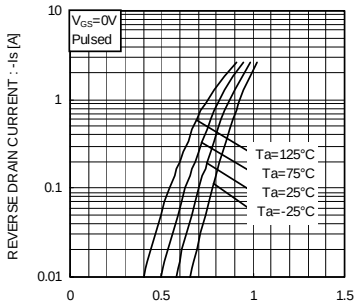

Fig.10 Reverse Drain Current vs. Sourse-Drain Voltage

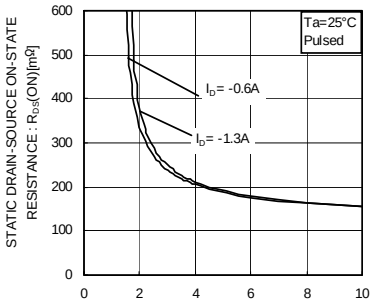

Fig.11 Static Drain-Source On-State Resistance vs. Gate Source Voltage

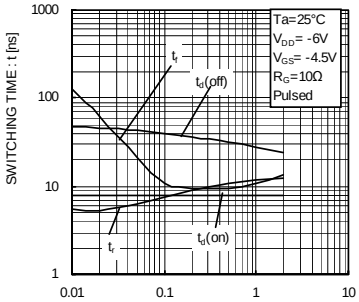

Fig.12 Switching Characteristics

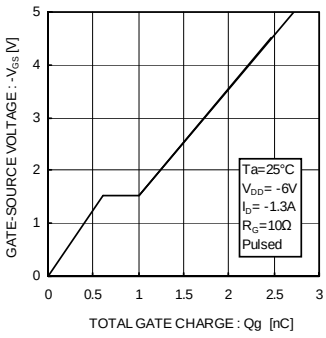

Fig.13 Dynamic Input Characteristics

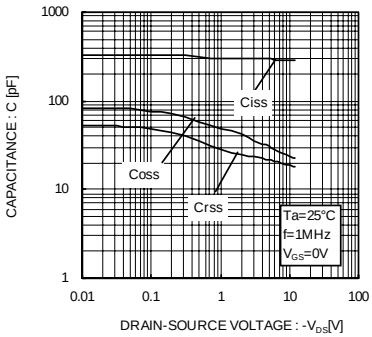

Fig.14 Typical Capacitance vs. Drain-Source Voltage

●Measurement circuit

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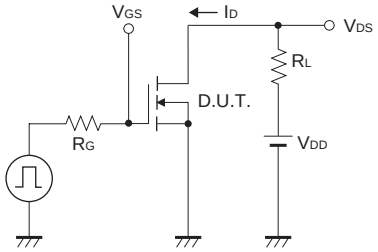

Fig.1-1 Switching Time Measurement Circuit

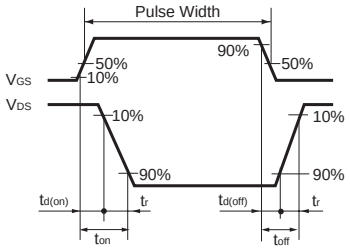

Fig.1-2 Switching Waveforms

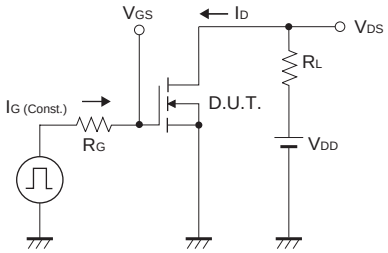

Fig.2-1 Gate Charge Measurement Circuit

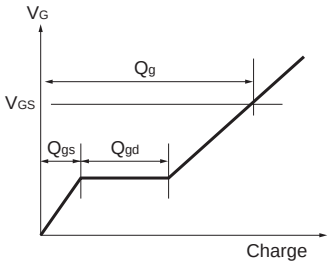

Fig.2-2 Gate Charge Waveform

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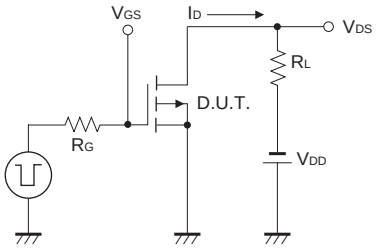

Fig.3-1 Switching Time Measurement Circuit

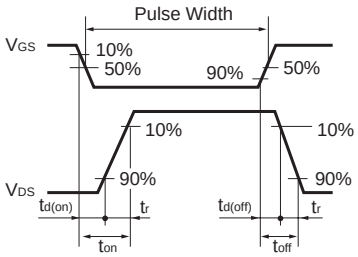

Fig.3-2 Switching Waveforms

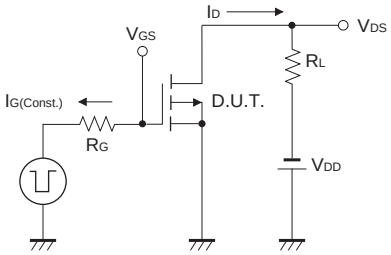

Fig.4-1 Gate Charge Measurement Circuit

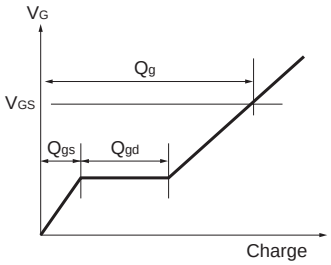

Fig.4-2 Gate Charge Waveform

●Notice

This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.

Notes

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Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. ROHM shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). ROHM shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.

ROHM SEMICONDUCTOR

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