

SGM708 Low-Cost, Microprocessor Supervisory Circuit

GENERAL DESCRIPTION

The SGM708 microprocessor supervisory circuit reduces the complexity and number of components required to monitor power supply and monitor microprocessor activity. It significantly improves system reliability and accuracy compared to separate ICs or discrete components.

The SGM708 provides power supply monitoring circuitry that generates a reset output during power-up, power-down and brownout conditions. The reset output remains operational with V_{CC} as low as 1V.

In addition, there is a 1.25V threshold detector for power-fail warning, low-battery detection, or monitoring an additional power supply. An active-low manual-reset input ($\overline{\text{MR}}$) is also included.

The SGM708 is available in Green SOIC-8 package. It operates over an ambient temperature range of -40°C to +85°C.

FEATURES

- Precision Supply-Voltage Monitor
 - 4.65V for SGM708-L
 - 4.40V for SGM708-M
 - 4.0V for SGM708-J
 - 3.08V for SGM708-T
 - 2.93V for SGM708-S
 - 2.63V for SGM708-R
- Guaranteed RESET Valid at V_{CC} = 1V
- 200ms Reset Pulse Width
- Debounced TTL/CMOS-Compatible Manual-Reset Input
- Voltage Monitor for Power-Fail or Low-Battery Warning
- Dual Reset Outputs: (Active-Low and Active-High)
- -40°C to +85°C Operating Temperature Range
- Available in Green SOIC-8 Package

APPLICATIONS

Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical µP Power Monitoring

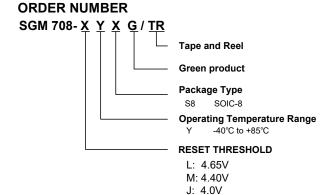


PACKAGE/ORDERING INFORMATION

MODEL	RESET THRESHOLD (V)	PACKAGE DESCRIPTION	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
	4.65	SOIC-8	SGM708-LYS8G/TR	SGM708-LYS8	Tape and Reel, 2500
	4.40	SOIC-8	SGM708-MYS8G/TR	SGM708-MYS8	Tape and Reel, 2500
SGM708	4.0	SOIC-8	SGM708-JYS8G/TR	SGM708-JYS8	Tape and Reel, 2500
3GW1700	3.08	SOIC-8	SGM708-TYS8G/TR	SGM708-TYS8	Tape and Reel, 2500
	2.93	SOIC-8	SGM708-SYS8G/TR	SGM708-SYS8	Tape and Reel, 2500
	2.63	SOIC-8	SGM708-RYS8G/TR	SGM708-RYS8	Tape and Reel, 2500

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

NOTE: Order number is defined as the follow:



ABSOLUTE MAXIMUM RATINGS

(Typical values are at T_A = +25°C, unless otherwise noted.) Terminal Voltage (with respect to GND)

T: 3.08V S: 2.93V

R: 2.63V

reminar vertage (with respect to entry)	
V _{CC}	0.3V to 6.0V
All Other Inputs	$-0.3V$ to $(V_{CC} + 0.3V)$
Input Current, V _{CC}	20mA
GND	20mA
Output Current, (all outputs)	20mA
Operating Temperature Range	40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	65°C to +150°C
Lead Temperature (Soldering, 10s)	+260°C
ESD Susceptibility	
HBM	4000V
MM	300V

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

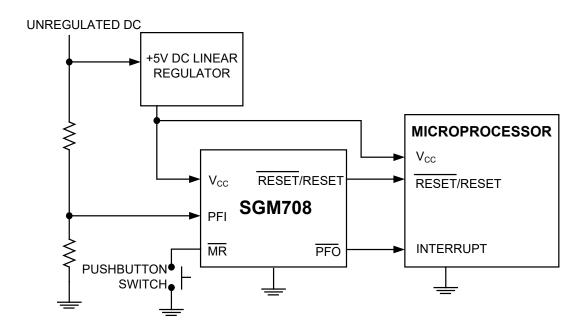
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

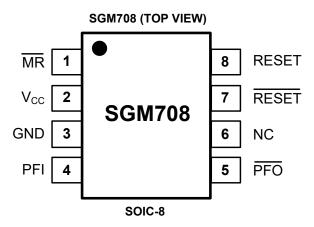
DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

TYPICAL APPLICATION CIRCUIT



PIN CONFIGURATION



PIN DESCRIPTION

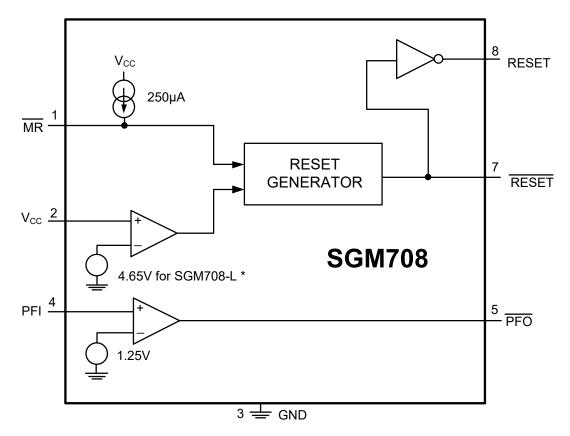
PIN	NAME	FUNCTION
1	MR	Manual-Reset Input triggers a reset pulse when pulled below 0.8V. This active-low input has an internal $250\mu A$ (V_{CC} = +5V) pull-up current. It can be driven from a TTL or CMOS logic line as well as shorted to ground with a switch.
2 V _{CC}		Power Supply Voltage that is monitored.
3	GND	0V Ground Reference for all signals.
4	PFI	Power-Fail Voltage Monitor Input. When PFI is less than 1.25V, $\overline{\text{PFO}}$ goes low. Connect PFI to GND or V_{CC} when not used.
5	PFO	Power-Fail Output goes low and sinks current when PFI is less than 1.25V; otherwise $\overline{\text{PFO}}$ stays high.
6	NC	No Connect.
7	RESET	Active-Low Reset Output pulses low for 200ms when triggered, and stays low whenever V_{CC} is below the reset threshold (4.65V for SGM708-L, 4.40V for SGM708-M, 4.0V for SGM708-J, 3.08V for SGM708-T, 2.93V for SGM708-S and 2.63V for SGM708-R). It remains low for 200ms after V_{CC} rises above the reset threshold or \overline{MR} goes from low to high.
8	RESET	Active-High Reset Output is the inverse of $\overline{\text{RESET}}$. Whenever $\overline{\text{RESET}}$ is high, RESET is low, and vice versa.

ELECTRICAL CHARACTERISTICS

 $(V_{CC} = 4.75V \text{ to } 5.5V \text{ for SGM708-L}; V_{CC} = 4.5V \text{ to } 5.5V \text{ for SGM708-M}; V_{CC} = 4.07V \text{ to } 5.5V \text{ for SGM708-J}; V_{CC} = 3.14V \text{ to } 5.5V \text{ for SGM708-R}; V_{CC} = 2.68V \text{ to } 5.5V \text{ for SGM708-R}; T_A = -40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}, \text{ unless otherwise noted.})$

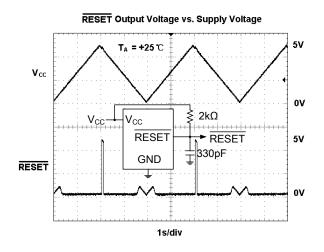
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS	
Operating Voltage Range (V _{CC})			1.0		5.5	V	
Supply Current (I _{SUPPLY})				20	60	μA	
		SGM708-L	4.5	4.65	4.75		
		SGM708-M	4.25	4.4	4.5		
Decet Threehold () ()		SGM708-J	SGM708-J 3.91 4		4.07	.,	
Reset Threshold (V _{RT)}		SGM708-T	3.02	3.08	3.14	V	
		SGM708-S	2.85	2.93	2.95	1	
		SGM708-R	2.56	2.63	2.68		
		SGM708-T, SGM708-S, SGM708-R		25			
RESET Output Voltage RESET Output Voltage MR Pull-Up Current MR Pulse Width (t _{MR}) Low	SGM708-J		35		mV		
		SGM708-L, SGM708-M		20 4.65 4.4 4.0 3.08 2.93 2.63 25			
Reset Pulse Width (t _{RS})			120	200	290	ms	
		I _{SOURCE} = 800μA	0.7 × V _{CC}				
RESET Output Voltage		I _{SINK} = 3.2mA			0.4	V	
		V _{CC} = 1V, I _{SINK} = 50μA			0.3		
DECET Output Valtage		I _{SOURCE} = 800μA	0.7 × V _{CC}			V	
RESET Output Voltage		I _{SINK} = 1.2mA			0.4	V	
MR Pull-Up Current		MR = 0V	100	250	600	μA	
MR Pulse Width (t _{MR})			250			ns	
· · · · · · · · · · · · · · · · · ·	Low	T			0.8		
MR Input Inreshold	High	T _A = +25°C	2			_ V	
MR to Reset Out Delay (t _{MD})				100	350	ns	
PFI Input Threshold		V _{CC} = 5V	1.17	1.25	1.3	V	
PFI Input Current				0.2		nA	
DEG Contract Valle in		I _{SOURCE} = 800µA	0.7 × V _{CC}			V	
PFO Output Voltage		I _{SINK} = 3.2mA			0.4		

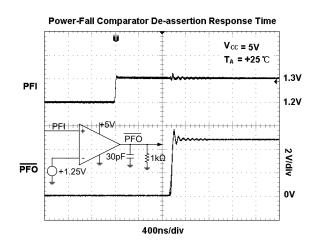
FUNCTIONAL BLOCK DIAGRAM

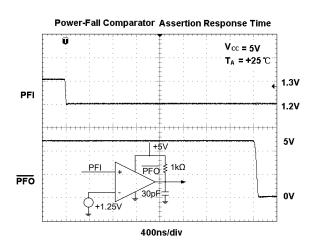


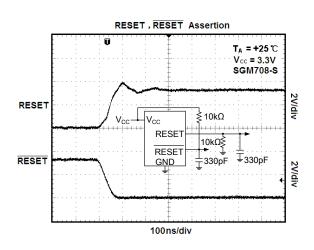
- * 4.65V for SGM708-L
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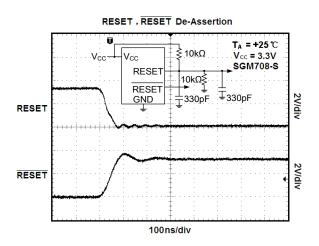
TYPICAL PERFORMANCE CHARACTERISTICS

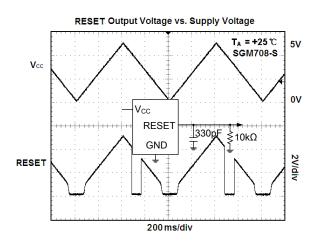




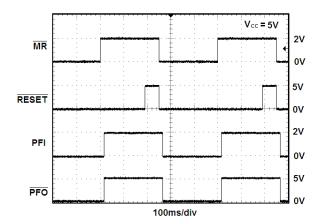


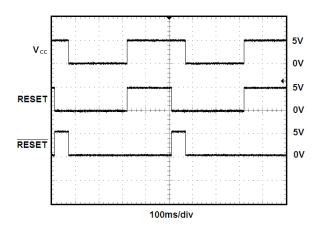


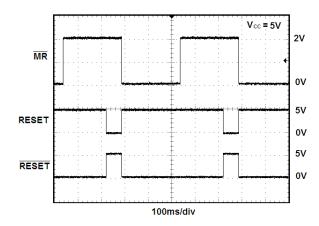




TYPICAL PERFORMANCE CHARACTERISTICS (continued)







APPLICATION INFORMATION

Ensuring a Valid $\overline{\text{RESET}}$ Output Down to $V_{CC} = 0V$

When V_{CC} falls below 1V, the SGM708 RESET output no longer sinks current-it becomes an open circuit. High-impedance CMOS logic inputs can drift to undetermined voltages if left undriven. If a pull-down resistor is added to the RESET pin as shown in Figure 1, any stray charge or leakage currents will be drained to ground, holding RESET low. Resistor value (R1) is not critical. It should be about $100k\Omega$, large enough not to load RESET and small enough to pull RESET to ground.

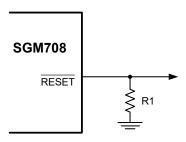


Figure 1. RESET Valid to Ground Circuit

Monitoring Voltages Other Than the Unregulated DC Input

Monitor voltages other than the unregulated DC by connecting a voltage divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10 times the sum of the two resistors in the potential divider network) between PFI and $\overline{\text{PFO}}$. A capacitor between PFI and GND will reduce the power-fail circuit's sensitivity to high-frequency noise on the line being monitored. $\overline{\text{RESET}}$ can be asserted on other voltages in addition to the +5V V_{CC} line. Connect $\overline{\text{PFO}}$ to $\overline{\text{MR}}$ to initiate a $\overline{\text{RESET}}$ pulse when PFI drops below 1.25V. Figure 2 shows the SGM708 configured to assert $\overline{\text{RESET}}$ when the +5V supply falls below the reset threshold, or when the +12V supply falls below approximately 11V.

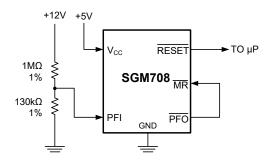


Figure 2. Monitoring Both +5V and +12V

Monitoring a Negative Voltage

The power-fail comparator can also monitor a negative supply rail (Figure 3). When the negative rail is good (a negative voltage of large magnitude), $\overline{\text{PFO}}$ is low, and when the negative rail is degraded (a negative voltage of lesser magnitude), $\overline{\text{PFO}}$ is high. By adding the resistors and transistor as shown, a high $\overline{\text{PFO}}$ triggers reset. As long as $\overline{\text{PFO}}$ remains high, the SGM708 will keep reset asserted ($\overline{\text{RESET}}$ = low, RESET = high). Note that this circuit's accuracy depends on the PFI threshold tolerance, the V_{CC} line, and the resistors.

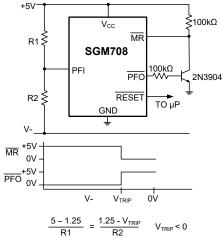


Figure 3. Monitoring a Negative Voltage

Interfacing to µPs with Bidirectional Reset Pins

μPs with bidirectional reset pins, such as the Motorola 68HC11 series, can contend with the SGM708 $\overline{\text{RESET}}$ output. If, for example, the $\overline{\text{RESET}}$ output is driven high and the Microprocessor wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7kΩ resistor between the $\overline{\text{RESET}}$ output and the μP reset I/O, as in Figure 4. Buffer the $\overline{\text{RESET}}$ output to other system components.

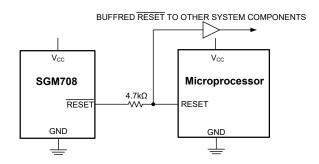


Figure 4. Interfacing to Microprocessors with Bidirectional Reset I/O

SGM708

REVISION HISTORY

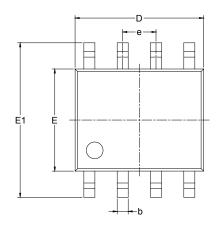
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

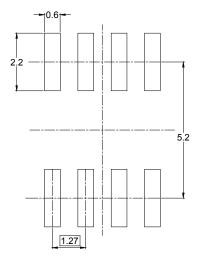
DECEMBER 2017 - REV.A.3 to REV.A.4

DESCRIBER 2017 - REV.A.G to REV.A.G
Changed Electrical Characteristics section
JANUARY 2013 – REV.A.2 to REV.A.3
Added Recommended Land Pattern Information
Added Tape and Reel Information
MARCH 2011 – REV.A.1 to REV.A.2
Updated Package Description
MAY 2010 – REV.A to REV.A.1
Added Reset Threshold
Changes from Original (APRIL 2010) to REV.A
Changed from product preview to production data

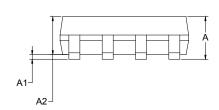


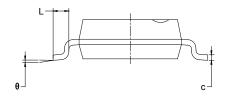
PACKAGE OUTLINE DIMENSIONS SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)

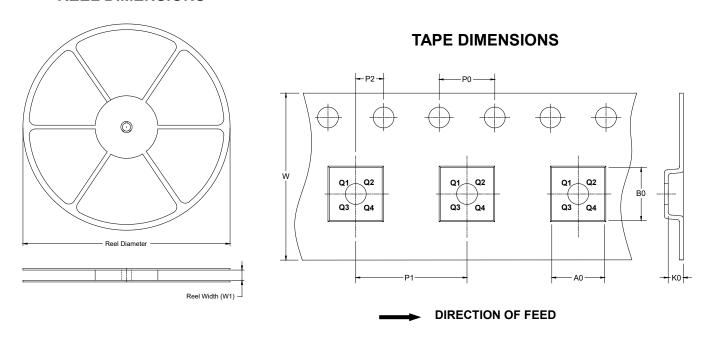




Symbol		nsions meters	Dimensions In Inches		
,	MIN	MAX	MIN	MAX	
А	1.350	1.750	0.053	0.069	
A1	0.100	0.250	0.004	0.010	
A2	1.350	1.550	0.053	0.061	
b	0.330	0.510	0.013	0.020	
С	0.170	0.250	0.006	0.010	
D	4.700	5.100	0.185	0.200	
E	3.800	4.000	0.150	0.157	
E1	5.800	6.200	0.228	0.244	
е	1.27 BSC		0.050	BSC	
L	0.400	1.270	0.016	0.050	
θ	0°	8°	0°	8°	

TAPE AND REEL INFORMATION

REEL DIMENSIONS

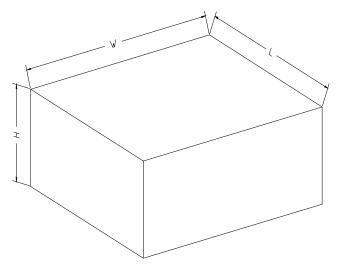


NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SOIC-8	13"	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	e Length Width (mm)		Height (mm)	Pizza/Carton	
13"	386	280	370	5	