DRV110A-Q1 120- and 230-V AC, 6- to 48-V DC Current Controller for Solenoids, Relays, and Valves

1 Features

- AEC-Q100 Qualified for Automotive Applications:
  - Device Temperature Grade 1: –40°C to +125°C, T_A
- Internal Zener Diode on Supply Pin for High-Voltage Operation
  - 120- and 230-V AC Supply Through Rectifier and R_S Resistor
  - 24-V, 48-V, and Higher DC Supply Through R_S Resistor
- Drives an External MOSFET With PWM to Control Solenoid Current
  - External Sense Resistor for Regulating Solenoid Current
- Fast Ramp-Up of Solenoid Current to Ensure Activation
- Solenoid Current is Reduced in Hold Mode for Lower Power and Thermal Dissipation
- Ramp Peak Current, Keep Time at Peak Current, Hold Current, and PWM Clock Frequency Can Be Set Externally. They Can Also Be Operated at Nominal Values Without External Components.
- Protection
  - Thermal Shutdown
  - Undervoltage Lockout (UVLO)
- Optional STATUS Output
- 14-Pin TSSOP Package

2 Applications

- Electromechanical Drivers: Solenoids, Valves, Relays, Contactors, Switchgear, Pneumatics
- EV Charging Station Power Modules, On-Board Chargers, Battery Management Systems

3 Description

The DRV110A-Q1 device is a PWM current controller for solenoids. The device is designed to regulate the current with a well-controlled waveform to reduce power dissipation. The solenoid current is ramped up fast to ensure opening of the valve or relay. After initial ramping, the solenoid current is kept at a peak value to ensure correct operation, after which the current is reduced to a lower hold level to avoid thermal problems and reduce power dissipation.

The peak current duration is set with an external capacitor. The peak and hold levels of the current ramp, as well as the PWM frequency, can independently be set with external resistors. External setting resistors can also be omitted if the default values for the corresponding parameters are suitable for the application.

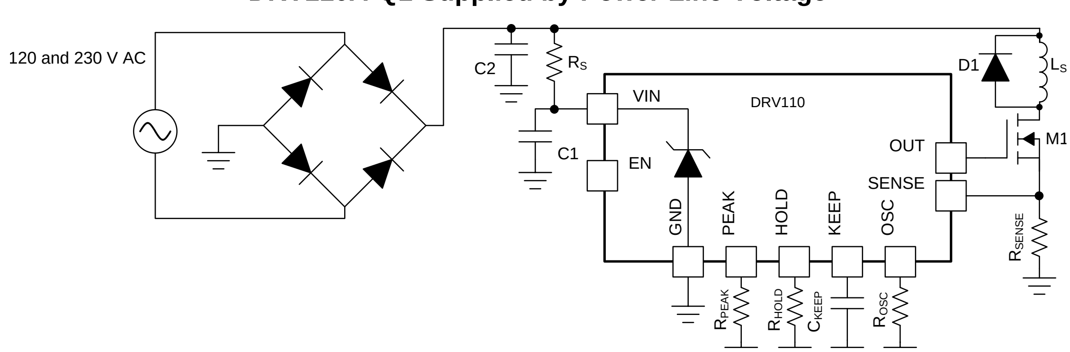
The DRV110A-Q1 device has an internal Zener diode that limits the supply at VIN to V_{ZENER} for applications that require a higher supply voltage. Using the internal Zener, the DRV110A-Q1 can be powered from 120-V and 230-V AC supplies through a rectifier and current-limiting resistor. High DC voltages such as 48-V can also be accommodated this way.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV110A-Q1	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

DRV110A-Q1 Supplied by Power Line Voltage



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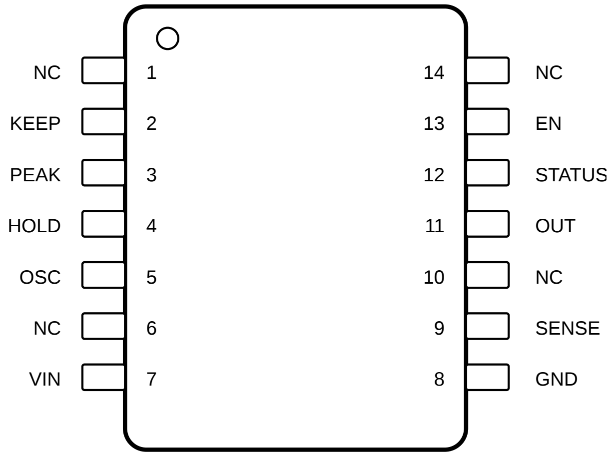
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2018	*	Initial release.

5 Pin Configuration and Functions

PW Package
14-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	**NO.**		
EN	13	I	Enable
GND	8	—	Ground
HOLD	4	I	Hold current set
KEEP	2	I	Keep time set
NC	1	—	No connect[1]
NC	6	—	No connect[1]
NC	10	—	No connect[1]
NC	14	—	No connect[1]
OSC	5	I	PWM frequency set
OUT	11	O	Solenoid switch gate drive
PEAK	3	I	Peak current set
SENSE	9	I	Solenoid current sense
STATUS	12	O	Open drain status indicator
VIN	7	I	6-V to 15-V supply

(1) Keep NC pins floating. Do not connect NC pins to GND or any other node.

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6 Specifications

6.1 Absolute Maximum Ratings

See (1) and (2)

		MIN	MAX	UNIT
VIN	Input voltage	–0.3	20	V
	Voltage on EN, STATUS, PEAK, HOLD, OSC, SENSE, KEEP	–0.3	7	V
	Voltage on OUT	–0.3	20	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1] HBM ESD Classification Level 2		±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	All pins	±500	
			Corner pins (1, 7, 8, and 14)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

–40°C ≤ T_A ≤ 125°C (unless otherwise noted)

		MIN	NOM	MAX	UNIT
I_Q	Supply current (the device sinks additional current when $V_{IN} > V_{ZENER}$[1])	1	1.5	3	mA
V_{IN}	Voltage at the VIN pin[2][3] (see *Detailed Description*)	6			V
V_S	Voltage directly from the supply before clamped by the Zener diode	6		330	V
C_{IN}	Input capacitor between VIN and GND[4]	1	4.7		µF
T_A	Operating ambient temperature	–40		125	°C

(1) The device regulates the supply with an internal Zener diode. The device sinks up to 3 mA with the added supply current. See Equation 5 to find appropriate value for the R_S resistor.
(2) The maximum input voltage of the device depends on the clamping voltage of the internal Zener diode, which changes over temperature. A current-limiting resistor is required to limit current to the Zener diode if the input voltage (V_{IN}) is greater than V_{ZENER}. For more information on resistor sizing see the *Detailed Description* section and *Application and Implementation* section.
(3) For V_S voltages less than V_{ZENER}, $V_{IN} = V_S$. For V_S voltages greater than V_{ZENER}, $V_{IN} = V_{ZENER}$.
(4) 4.7-µF input capacitor and full wave rectified 230-Vrms AC supply results in approximately 500-mV supply ripple.

6.4 Thermal Information

THERMAL METRIC[1]		DRV110A-Q1 PW (TSSOP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance ψ	51.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_{IN} = 14 V, –40°C ≤ T_A ≤ 125°C, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Standby current	EN = 0, V_{IN} = 14 V, bypass deactivated		200	250	µA
	Quiescent current	EN = 1, V_{IN} = 14 V, bypass deactivated		360	570	µA
	Internally regulated supply	EN = 0, I_{VIN} = 2 mA, bypass activated	10.5	15	19	V
		EN = 1, I_{VIN} = 2 mA, bypass activated	14.5	15	15.5	V
GATE DRIVER						
V_{DRV}	Gate drive voltage	Supply voltage in regulation		V_{IN}		V
I_{DRV_SINK}	Gate drive sink current	V_{OUT} = 15 V; V_{IN} = 15 V	8	15		mA
I_{DRV_SOURCE}	Gate drive source current	V_{OUT} = GND; V_{IN} = 15 V		–15	–10	mA
f_{PWM}	PWM clock frequency	OSC = GND	15	20	27	kHz
D_{MAX}	Maximum PWM duty cycle			100%		
D_{MIN}	Minimum PWM duty cycle			7.5%		
t_D	Start-up delay	Delay between EN going high until gate driver starts switching, f_{PWM} = 20 kHz			50	µs
CURRENT CONTROLLER, INTERNAL SETTINGS						
I_{PEAK}	Peak current	R_{SENSE} = 1 Ω, PEAK = GND	270	300	330	mA
I_{HOLD}	Hold current	R_{SENSE} = 1 Ω, HOLD = GND	40	50	65	mA
CURRENT CONTROLLER, EXTERNAL SETTINGS						
t_{KEEP}	Externally set keep time at peak current	C_{KEEP} = 1 µF		100		ms
V_{PEAK}	Voltage of internal reference to which the SENSE pin voltage is compared to for I_{PEAK}	R_{PEAK} = 50 kΩ		900		mV
		R_{PEAK} = 200 kΩ		300		mV
V_{HOLD}	Voltage of internal reference to which the SENSE pin voltage is compared for I_{HOLD}	R_{HOLD} = 50 kΩ		150		mV
		R_{HOLD} = 200 kΩ		50		mV
f_{PWM}	Externally set PWM clock frequency	R_{OSC} = 160 kΩ		25		kHz
		R_{OSC} = 200 kΩ		20		kHz
LOGIC INPUT LEVELS (EN)						
V_{IL}	Input low level				1.3	V
V_{IH}	Input high level		1.65			V
R_{EN}	Input pullup resistance		350	500		kΩ
	Input pulldown resistance			250		kΩ
LOGIC OUTPUT LEVELS (STATUS)						
V_{OL}	Output low level	Pulldown activated, I_{STATUS} = 2 mA			0.3	V
I_{IL}	Output leakage current	Pulldown deactivated, V(STATUS) = 5 V			2	µA
UNDERVOLTAGE LOCKOUT						
V_{UVLO}	Undervoltage lockout threshold			4.6		V
THERMAL SHUTDOWN						
T_{TSU}	Junction temperature start-up threshold			140		°C
T_{TSD}	Junction temperature shutdown threshold			160		°C

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6.6 Typical Characteristics

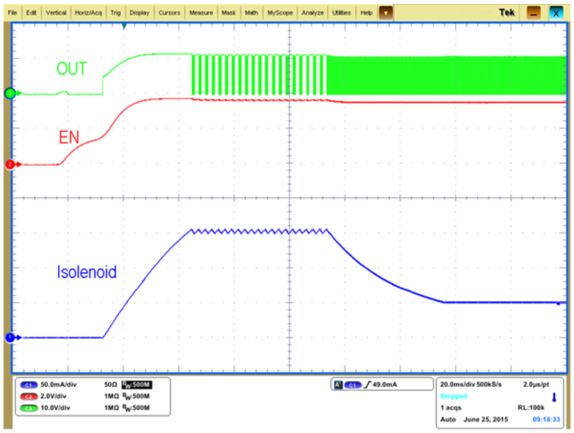


Figure 1. Solenoid Current, EN, and PWM vs Time

7 Detailed Description

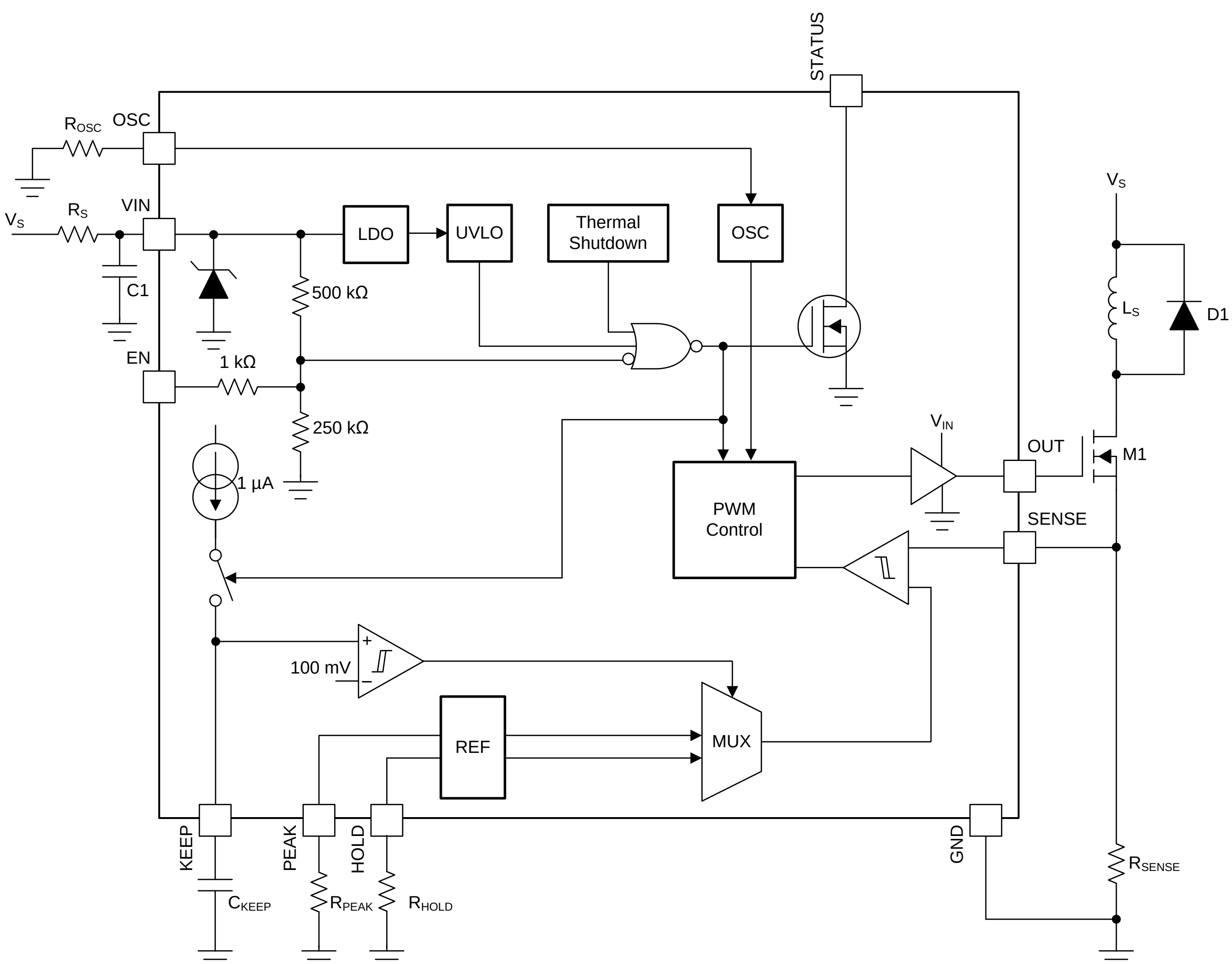
7.1 Overview

The DRV110A-Q1 device provides a PWM current controller for use with solenoids. The device provides a quick ramp to a high peak current value in order to ensure opening of the valve or relay. The current is held for a programmable time and then lowered to the hold current value to maintain the open state of the valve or relay while reducing the total current consumption. Peak current duration, peak current amount, hold current amount, and PWM frequency can all be controlled by external components or used at default levels by omitting these components (except peak current duration).

Enable and disable of the switch is controlled by the EN pin. The EN pin contains an internal resistor network to set the pin to logic HIGH when the EN pin is floating. This feature can be used for situations where a control signal is not required and the solenoid is only energized when a supply voltage is present. Such applications could be valves or contactors.

The DRV110A-Q1 also features a wide VIN range with an internal bypass regulator to maintain VIN at an acceptable level. Finally, the device features an open-drain pull-down path on the STATUS pin which is enabled as long as undervoltage lockout or thermal shutdown has not triggered.

7.2 Functional Block Diagram



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7.3 Feature Description

The DRV110A-Q1 controls the current through the solenoid as shown in Figure 2. Activation starts when EN pin voltage is pulled high either by an external driver or internal pullup. In the beginning of activation, DRV110A-Q1 allows the solenoid current to ramp up to the peak value I_{PEAK} and it regulates it at the peak value for the time, t_{KEEP}, before reducing it to I_{HOLD}. The solenoid current is regulated at the hold value as long as the EN pin is kept high. The initial current ramp-up time depends on the inductance and resistance of the solenoid. Once EN pin is driven to GND, DRV110A-Q1 allows the solenoid current to decay to zero.

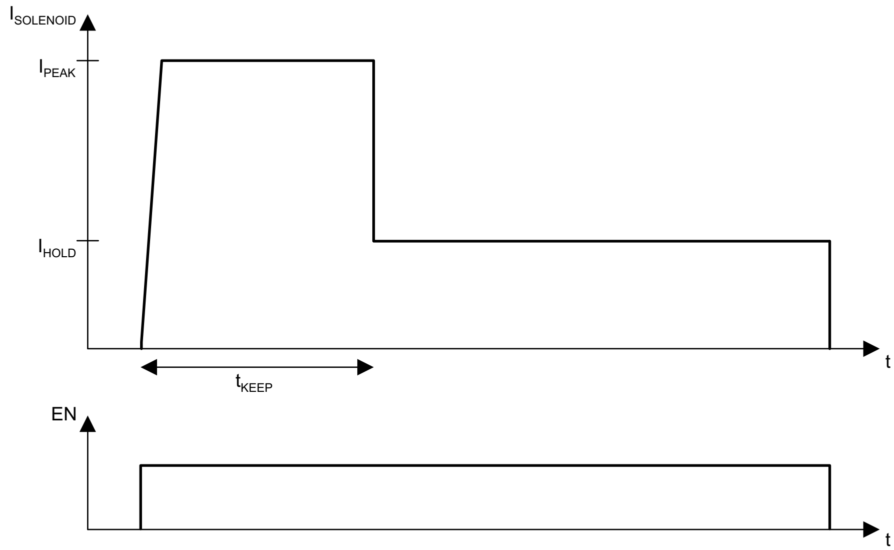

Figure 2. Typical Current Waveform Through the Solenoid

7.3.1 Keep Time

The keep time, t_{KEEP}, is set externally by connecting a capacitor to the KEEP pin. A constant current is sourced from the KEEP pin that is driven into an external capacitor resulting in a linear voltage ramp. When the KEEP pin voltage reaches 100 mV, the current regulation reference voltage, V_{REF}, is switched from V_{PEAK} to V_{HOLD}. The internal current source is switched off, and the capacitor is grounded for discharge. The dependency of t_{KEEP} from the external capacitor size can be calculated with Equation 1.

$$t_{KEEP}\left[s\right] = C_{KEEP}\left[F\right] \cdot 10^5 \left[\frac{s}{F}\right] \tag{1}$$

7.3.2 PWM Current Control

The current control loop regulates, cycle-by-cycle, the solenoid current by sensing voltage at the SENSE pin and controlling the external switching device gate through the OUT pin. During the ON-cycle, the OUT pin voltage is driven and kept high (equal to VIN voltage) allowing current to flow through the external switch as long as the voltage at the SENSE pin is less than V_{REF}. As soon as the voltage at the SENSE pin is above V_{REF}, the OUT pin voltage is immediately driven low and kept low until the next ON-cycle is triggered by the internal PWM clock signal. In the beginning of each ON-cycle, the OUT pin voltage is driven high and kept high for at least the time determined by the minimum PWM signal duty cycle, D_{MIN}.

Because the current sense is done by comparing the voltage at the SENSE pin to a reference voltage, the DRV110A-Q1 device acts like a hysteresis controller. When the device acts like a hysteresis controller, it can make the PWM frequency and duty cycle appear uneven for some solenoids (see Figure 3).

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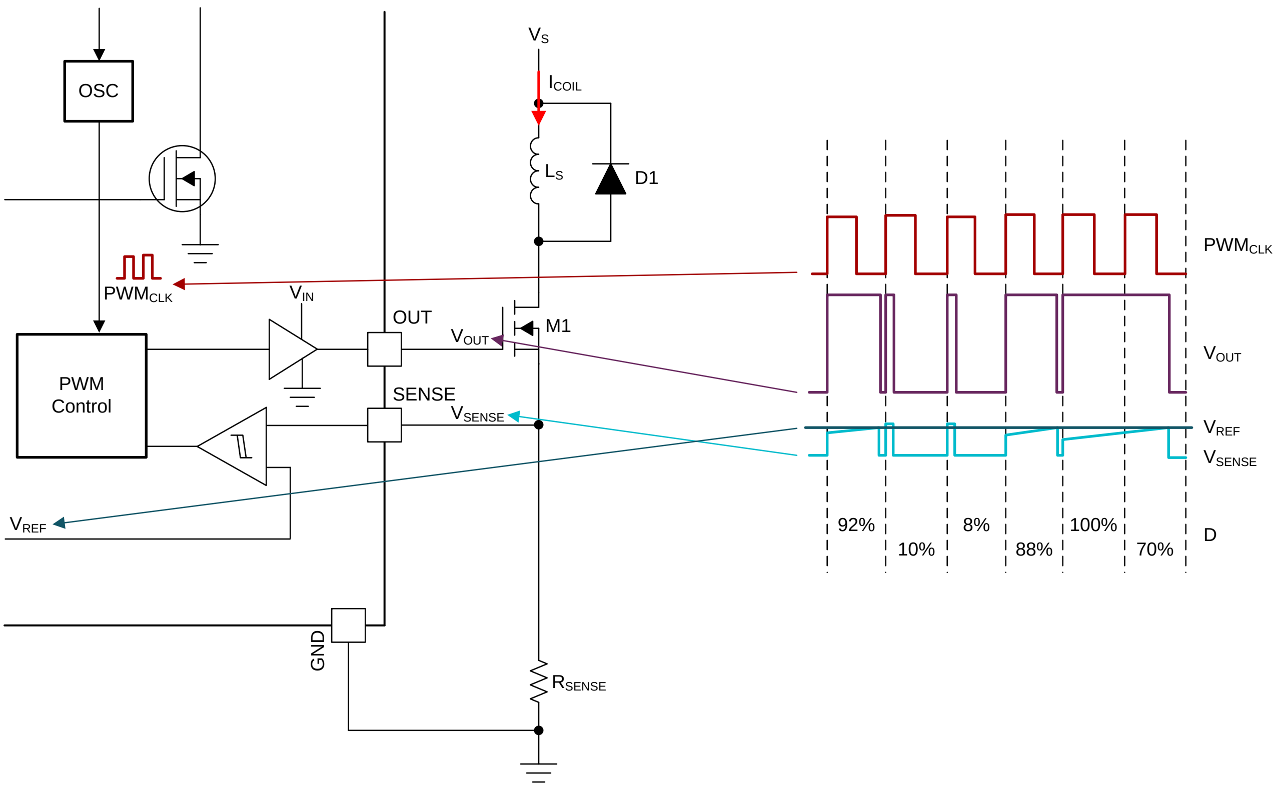
Feature Description (continued)



(1) The DRV110A-Q1 device measures the voltage at the SENSE node (V_{SENSE}). This voltage is compared against the reference voltage (V_{REF}) each clock cycle. The voltage at the output node (V_{OUT}) becomes low when $V_{SENSE} \geq V_{REF}$. The duty cycle (D) of the output voltage varies from 8% to 100%. In summary, the SENSE voltage is sampled after each rising edge of the PWM CLK signal (PWM_{CLK}) and goes low when $V_{SENSE} \geq V_{REF}$ at a minimum duty cycle of 8%.

Figure 3. DRV110A-Q1 Current Control with Varying OUT Duty Cycle

7.3.3 Configuring Peak and Hold Currents

I_{PEAK} and I_{HOLD} depend on fixed resistance values R_{PEAK} and R_{HOLD} as shown in Figure 4. If the PEAK pin or HOLD pin is connected to ground or R_{PEAK} or R_{HOLD} is less than 43.33 kΩ (typical), then I_{PEAK} is at its default value of 300 mA for I_{PEAK} and 50 mA for I_{HOLD}.

The I_{PEAK} value can alternatively be set by connecting an external resistor to ground from the PEAK pin. For example, if a 60-kΩ (= R_{PEAK}) resistor is connected between PEAK and GND, and R_{SENSE} = 1 Ω, then the externally set I_{PEAK} level will be 900 mA. If R_{PEAK} = 200 kΩ and R_{SENSE} = 1 Ω, then the externally set I_{PEAK} level will be 300 mA. TI does not recommend using a resistor from 30 kΩ and 55 kΩ to avoid the I_{PEAK} or I_{HOLD} current slipping from the maximum current setting to the default setting.

In case R_{SENSE} = 2 Ω instead of 1 Ω, then I_{PEAK} = 450 mA (when R_{PEAK} = 55 kΩ) and I_{PEAK} = 150 mA (when R_{PEAK} = 200 kΩ). The external setting of the HOLD current, I_{HOLD}, works in the same way as the external setting for I_{PEAK} but the current levels are 1/6 of the I_{PEAK} levels for the same resistor setting.

External settings for I_{PEAK} and I_{HOLD} are independent of each other. If R_{PEAK} or R_{HOLD} is decreased below 33.33 kΩ (typical value), then the reference is clamped to the internal setting of 300 mV for PEAK and 50 mV for HOLD. Use Equation 2 and Equation 3 to calculate the values for I_{PEAK} and I_{HOLD} respectively.

The currents and resistor values should be chosen such that the voltage across the sense resistor is more than 30 mV.

$$I_{PEAK} = \frac{V_{REF}}{R_{SENSE}} = \frac{1\,\Omega \times 900\text{ mA} \times 66.67\text{ k}\Omega}{R_{PEAK}} \times \frac{1}{R_{SENSE}}; 66.67\text{ k}\Omega < R_{PEAK} < 2\text{ M}\Omega \tag{2}$$

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Feature Description (continued)

$$I_{HOLD} = \frac{V_{REF}}{R_{SENSE}} = \frac{1\,\Omega \times 150\text{ mA} \times 66.67\text{ k}\Omega}{R_{HOLD}} \times \frac{1}{R_{SENSE}}; 66.67\text{ k}\Omega < R_{HOLD} < 333\text{ k}\Omega \quad (3)$$

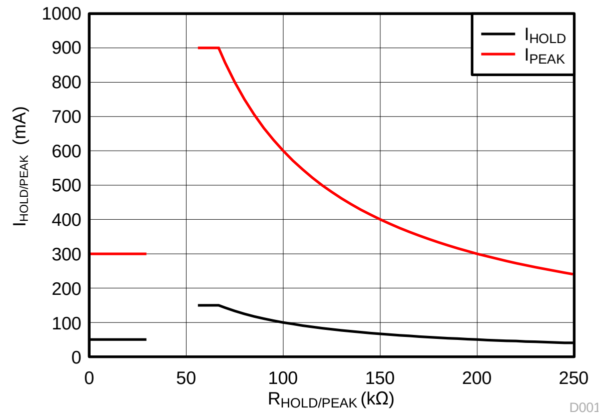

Figure 4. I_{PEAK} and I_{HOLD} settings for R_{SENSE} = 1 Ω

7.3.4 Configuring the PWM Frequency

Frequency of the internal PWM clock signal, PWM_{CLK}, that triggers each OUT pin ON-cycle can be adjusted by external resistor, R_{OSC}, connected between OSC and GND. Frequency as a function of resistor value is shown in Figure 5. Default frequency is used when OSC is connected to GND directly. Use Equation 4 to calculate the PWM frequency as a function of the external fixed adjustment resistor value (greater than 160 kΩ).

$$f_{PWM} = \frac{60\text{ kHz}}{R_{OSC}} \times 66.67\text{ k}\Omega;\ 160\text{ k}\Omega < R_{OSC} < 2\text{ M}\Omega \quad (4)$$

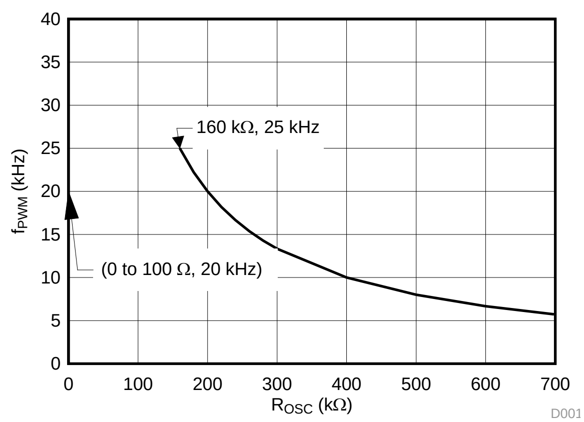

Figure 5. PWM Clock Frequency Setting

7.3.5 Voltage Supply and Integrated Zener Diode

Voltage at the OUT pin, that is the gate voltage of an external switching device, is equal to VIN voltage during the ON-cycle. The voltage is driven to ground during the OFF-cycle. VIN voltages below V_{ZENER} can be supplied directly from an external voltage source. Supply voltages of at least 6 V are supported.

The DRV110A-Q1 is able to regulate VIN voltage from a higher external supply voltage, V_S, by an internal bypass regulator that replicates the function of an ideal Zener diode. This requires that the supply current is sufficiently limited by an external resistor between V_S and the VIN pin. An external capacitor connected to the VIN pin is used to store enough energy to charge the external switch gate capacitance at the OUT pin. A range of current limiting resistor sizes ($R_{S,min}$ and $R_{S,max}$) can be calculated with Equation 5 and Equation 6. This range keeps the VIN current within the recommended operating conditions.

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Feature Description (continued)

$$R_{S,max} = \frac{V_{S,minDC} - V_{ZENER}}{1\,mA + I_{Gate,AVE}}$$

where

- $I_{Gate,AVE}$ is the current flowing to the external switch. For a MOSFET, $I_{Gate,AVE}$ is equal to the external FET gate charge multiplied by f_{PWM}. (5)

$$R_{S,min} = \frac{V_{S,maxDC} - V_{ZENER}}{3\,mA + I_{Gate,AVE}} \quad (6)$$

Ideally, the DRV110A-Q1 device clamps the input voltage to 15 V. For configurations that do not use the EN pin (force the pin high or leave it floating), the DRV110A-Q1 device clamps at 15 V (V_{ZENER} = 15 V) across the temperature range of the device. If the EN pin is set to 0, then refer to the values in Table 1 to find the V_{ZENER} used when calculating the value of R_S, based on the temperature range of the application. Because the V_{ZENER} changes when the EN state changes, select a value for R_S that meets the current requirements at both V_{ZENER} voltages.

Table 1. V_{ZENER} Value

TEMPERATURE RANGE	ENABLE STATE	V_{ZENER}
–40°C ≤ T_A ≤ 125°C	1	15 V
–40°C ≤ T_A ≤ 35°C	0	15 V
–40°C ≤ T_A ≤ 45°C	0	14.2 V
–40°C ≤ T_A ≤ 55°C	0	13.9 V
–40°C ≤ T_A ≤ 65°C	0	13.5 V
–40°C ≤ T_A ≤ 75°C	0	13.1 V
–40°C ≤ T_A ≤ 85°C	0	12.7 V
–40°C ≤ T_A ≤ 95°C	0	12.3 V
–40°C ≤ T_A ≤ 105°C	0	12 V
–40°C ≤ T_A ≤ 115°C	0	11.4 V
–40°C ≤ T_A ≤ 125°C	0	11 V

The open-drain pulldown path at the STATUS pin is deactivated if the undervoltage lockout or thermal shutdown blocks have triggered or if the EN pin is low.

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7.4 Device Functional Modes

7.4.1 Normal Mode

The DRV110A-Q1 transitions through three different states in normal mode:

OFF state In the OFF state, the EN pin is low and the PWM output is off.

PEAK state The PEAK state begins when the EN pin is set high, and ends when the t_{KEEP} time has been reached. During this state, the PWM operates to reach the I_{PEAK} current set by the R_{PEAK} resistor.

HOLD state In the HOLD state, the t_{KEEP} time has been reached, and the PWM continues to operate but at the I_{HOLD} level. This continues until the EN pin is set low again and the PWM turns off.

7.4.2 Shutdown

The DRV110A-Q1 turns off the gate driver in undervoltage lockout (VIN < 4.6 V) or thermal shutdown (T_J > 160°C). If temperature shutdown is activated, the DRV110A-Q1 resumes operation when the junction temperature is below 140°C. The shutdown conditions are expressed by the STATUS pin going to the high-impedance state. A pullup resistor can be connected to the STATUS pin so these conditions may be observed by a microcontroller. Table 2 provides an explanation of this operation.

Table 2. Shutdown Operation

CONDITIONS			OUTPUT PINS	
EN	UVLO	TSD	STATUS	OUT
0	X	X	Hi-Z	LOW
1	0	0	Pulled down	HIGH or PWM
1	X	1	Hi-Z	LOW
1	1	X	Hi-Z	LOW

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV110A-Q1 device is designed to operate a solenoid valve or relay. For detailed information on using the DRV110A-Q1 with 230 V AC solenoids. A typical DC input design will be outlined in *Typical Application*. Approximate resistor and capacitor values for the peak current, hold current, sense, and keep time will be derived for a sample application.

8.2 Typical Application

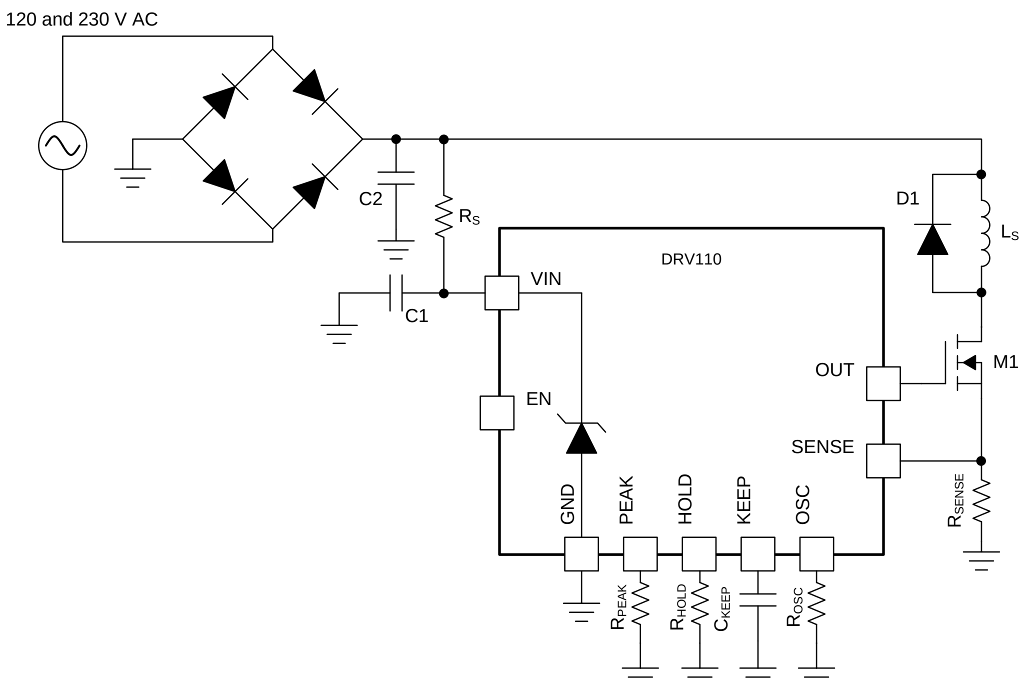

Figure 6. DRV110A-Q1 Powered by a Rectified AC Power Source

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Typical Application (continued)

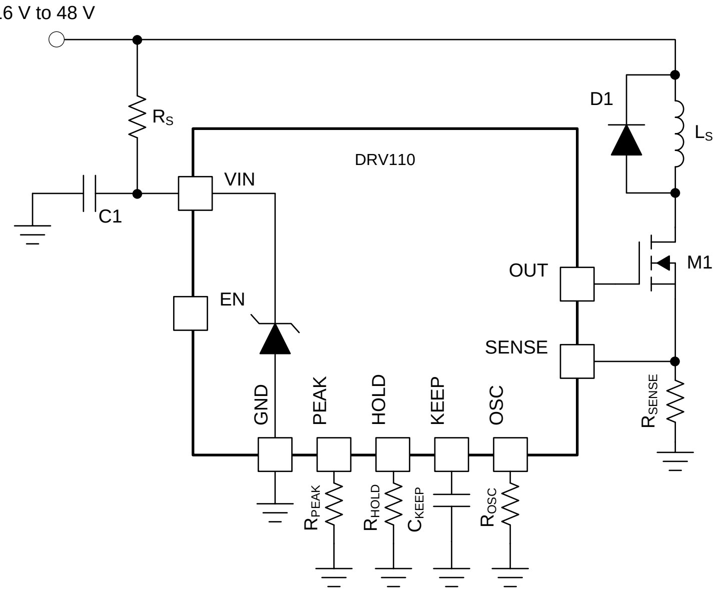

Figure 7. DRV110A-Q1 Powered by a DC Power Source Greater than 15 V

8.2.1 Design Requirements

The key elements to identify here are the system input voltage, peak current, hold current, and peak keep time values required for the solenoid or relay being used. With these values, approximate R_S, R_{PEAK}, R_{HOLD}, C_{KEEP}, and R_{SENSE} values can be determined and the proper FET and diode can be identified. R_{OSC} can be varied in order to tune the circuit to the chosen solenoid or relay.

8.2.2 Detailed Design Procedure

8.2.2.1 Current Limiting Resistor Selection

The temperature range, input voltage, and enable state must be considered when selecting the current limiting resistor. These values must be considered because the Zener clamping voltage of the DRV110A-Q1 device starts dropping from its ideal 15 V at temperatures greater than 45°C when the EN pin is pulled low. Applications that leave the EN pin floating or pulled high at all times only require a current-limiting resistor when the input voltage is greater than 15 V across all temperature.

While using a current-limiting resistor is not required when the supply voltage (V_S) is less than the Zener clamping voltage, V_{ZENER}, TI recommends populating a small resistor in case of possible input voltage transients during operation. At the very least, TI recommends placing a resistor footprint jumped by a 0-Ω resistor. Table 3 lists recommended resistor values for voltages close to V_{ZENER} and common voltages greater than V_{ZENER} for different enable states.

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Table 3. Recommended Resistor Values
–40°C ≤ T_A ≤ 125°C

SUPPLY VOLTAGE	RECOMMENDED CURRENT-LIMITING RESISTOR
EN Pulled High or Floating	
< 15 V	500 Ω
24 V	9 kΩ
48 V	33 kΩ
110 V to 120 V	100 kΩ
220 V to 240 V	200 kΩ
EN Toggled Between 0 and 1	
10 V	510 Ω
11 V	510 Ω
12 V	1 kΩ
13 V	2 kΩ
14 V	3 kΩ
15 V	3.9 kΩ
24 V	13 kΩ
48 V	36 kΩ
110 V to 120 V	100 kΩ
220 V to 240 V	200 kΩ

8.2.2.2 Passive Component Selection

With the selected peak current, hold current, and peak keep time values, the values of R_{PEAK}, R_{HOLD}, C_{KEEP}, and R_{SENSE} can be determined. Table 4 lists the example values and results from calculation.

Table 4. Example Application Values When R_{SENSE} = 1 Ω

VARIABLE	VALUE	DEVICE VALUES	CALCULATED FROM
Peak current	150 mA	R_{PEAK} = 400 kΩ	Equation 2
Hold current	50 mA	R_{HOLD} = 200 kΩ or connect HOLD to ground	Equation 3
Keep time	100 ms	C_{KEEP} = 1 µF	Equation 1
PWM frequency	20 kHz	R_{OSC} = Shorted to ground	Equation 4

Use Equation 2 and Equation 3 to calculate the values of the R_{PEAK} resistor and R_{HOLD} (if applicable) resistor. For the sample values, the R_{PEAK} resistor is set to 400 kΩ and the R_{HOLD} resistor is shorted to GND. TI recommends using a 0-Ω resistor for prototyping in case changes to this value are desired.

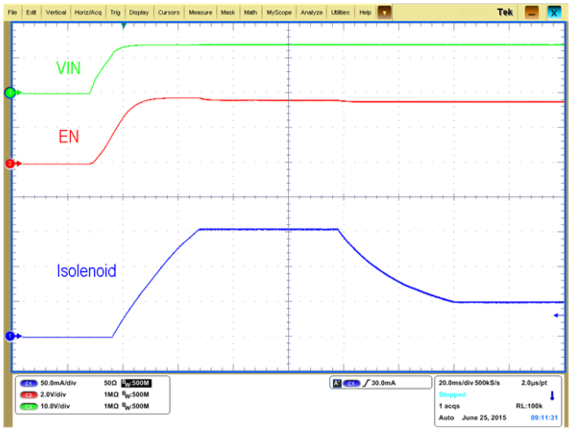
Next, select the value of the C_{KEEP} capacitor based on Equation 1. For the sample value, the C_{KEEP} capacitor is set to 1 µF. The R_{OSC} resistor is initially be shorted to GND, but a 0-Ω resistor is also recommended for prototyping. Additionally, a low-pass filter on the SENSE line can be added in a high-noise environment and is recommended for prototyping. The typical value for the low pass filter resistor is 1 kΩ and the typical value for the filter capacitor is 100 pF.

The value of sense resistor can be selected based on the preference of the designer. The only restriction is that the voltage across the sense resistor (found by the R_{SENSE} resistance times the I_{HOLD} current) must be greater than 30 mV for reliable operation.

The external FET and current recirculation diode must be selected based on the current values defined in and the supply voltage. The current recirculation diode should be a fast recovery diode.

ADVANCE INFORMATION

8.2.3 Application Curve



R_{OSC} = 0 Ω	R_{PEAK} = 400 kΩ	R_{HOLD} = 0 Ω
R_{SENSE} = 1 Ω	C_{KEEP} = 1 µF	L_{ind} = 1 H
R_{ind} = 50 Ω	Measured on the EVM	

Figure 8. $I_{SOLENOID}$, EN, and V_{IN} vs Time

9 Power Supply Recommendations

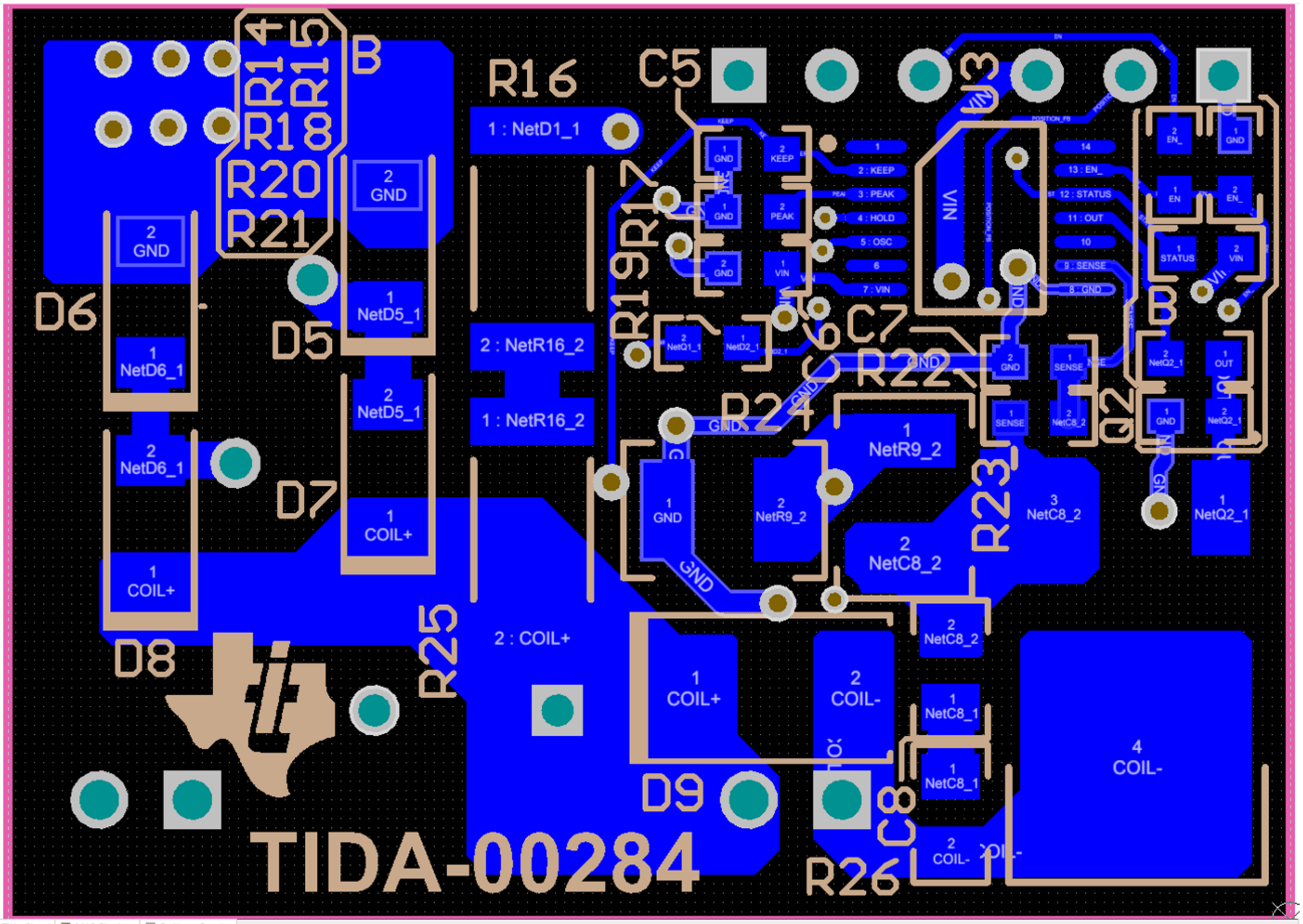
The input supply range must be at least 6 V, and needs a current-limiting resistor above V_{ZENER}. An input capacitor of 4.7 µF (typical) is required as well. I_Q max is 3 mA, but additional current will be required to operate the solenoid or relay.

10 Layout

10.1 Layout Guidelines

Routing for the SENSE pin should be careful to avoid noise sources. Routing for the output node and sense node should be minimized. The trace for the solenoid or relay current should be wide in order to prevent any unexpected voltage drop. Make sure that no connect (NC) pins are kept floating and are not connected to GND or any other node.

10.2 Layout Example



The TIDA-00284 TI Design is shown as an example of good layout practices with the DRV110A-Q1. The TIDA-00284 design is not intended for automotive applications.

Figure 9. Layout Schematic

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *DRV110 and DRV120 Evaluation Modules (EVM)* user's guide

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PDRV110AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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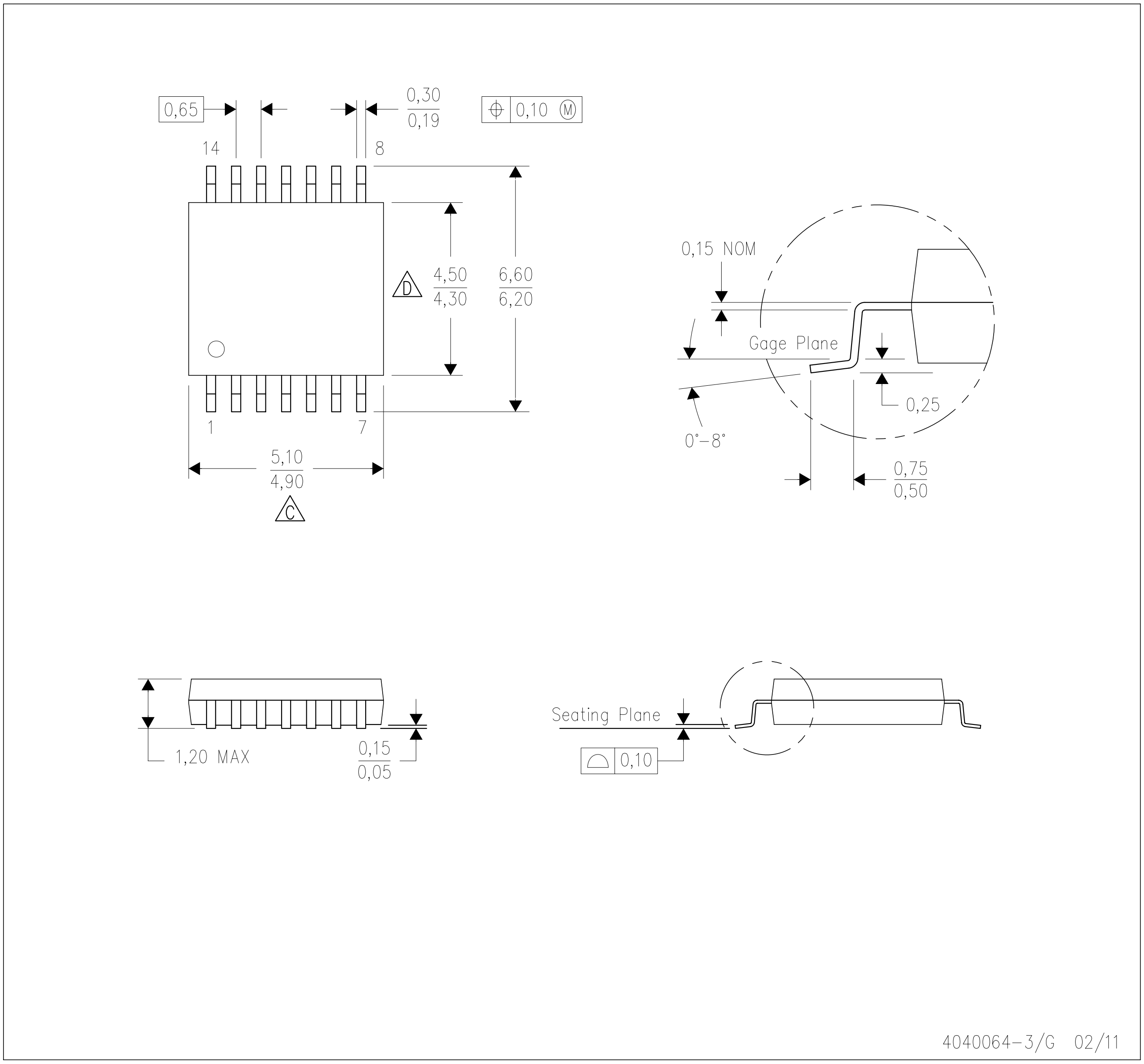
PW (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

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